Status of the DHCAL DIF

Detector InterFace Board

Sébastien Cap, Julie Prast,

Guillaume Vouters

Guillaume Vouters, DHCAL Europe
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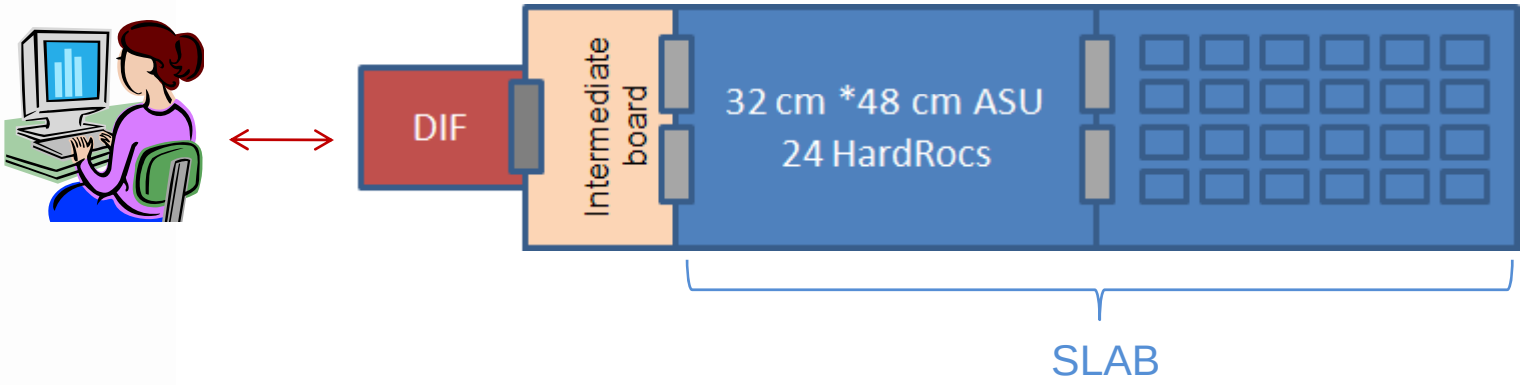
The DHCAL Architecture

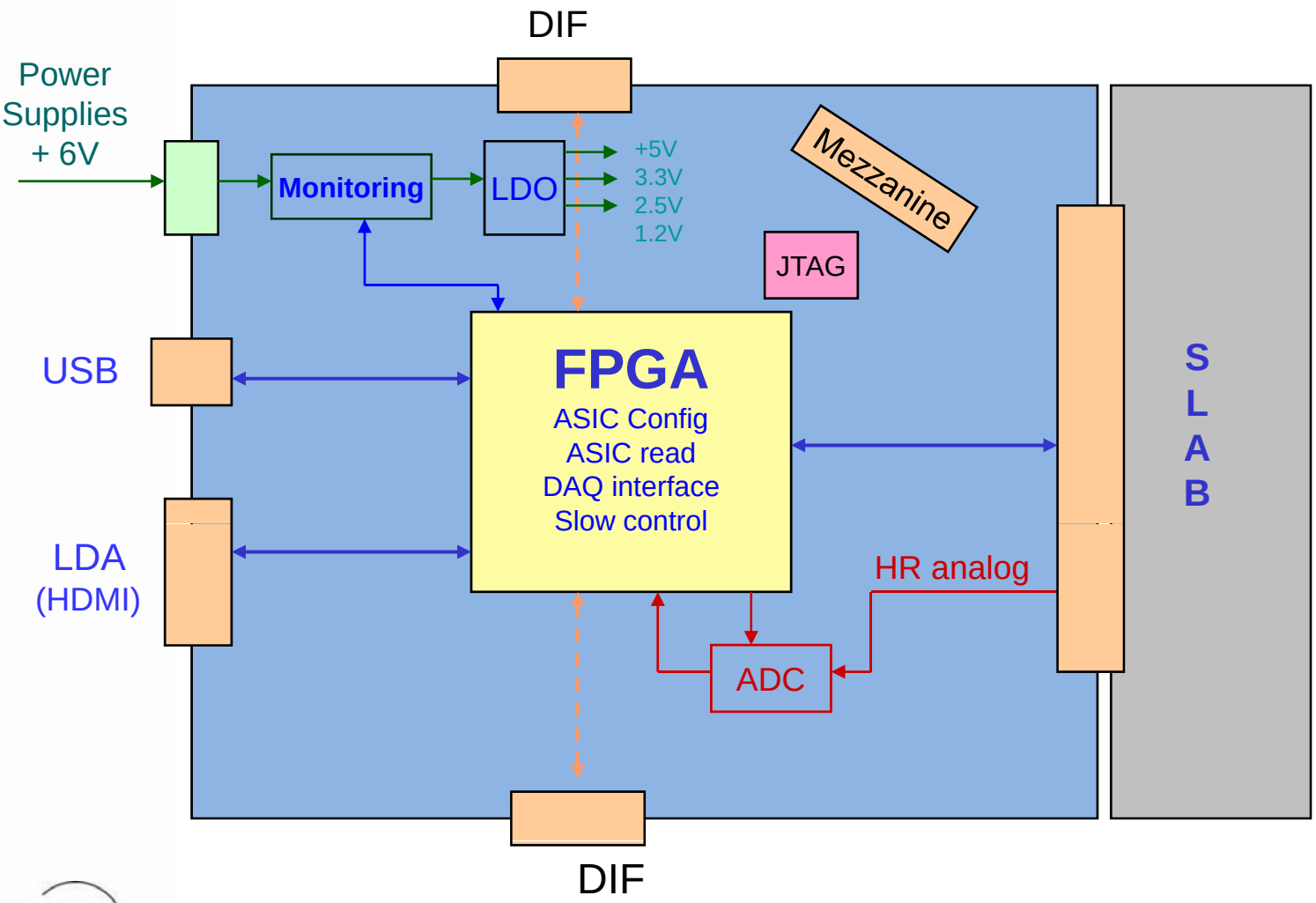


Main aims of the DIF:

- The DIF has to be able to communicate with PCs and HardRocs on the SLAB through the intermediate board.

- The DIF has to be able to configure ASICs and to perform analog and digital readout.

Architecture of the DIF Board



The DHCAL DIF Board

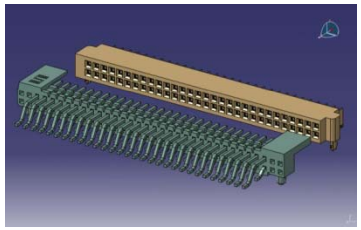
- Based on a Cyclone 3 Altera FPGA (EP3C6F484).
- Separated from the slab for more flexibility.
  - Can handle slab what ever the nb of HardRoc on it.
  - DIF task force interface compliant.
  - MicroMegas and RPC detector compatible.
  - HardRoc, Lyon's asics and also Spiroc and Skyroc compatible.
- On the DAQ side, interface with :
  - The LDA (final DAQ).
  - PC through USB for standalone tests and debugs.
  - DIF neighbors.
  - Interface with the analog DAQ removed.

GND	1		2	GND
MUX3_CSn	3		4	Analog_0
MUX2_CSn	5		6	GND
MUX1_CSn	7		8	Analog_1
spare1	9		10	GND
MUX_ENN	11		12	C_test
MUX_WRN	13		14	GND
spare2	15		16	MUX_A4
en_otaq	17		18	MUX_A3
GND	19		20	MUX_A2
SR_reset	21		22	MUX_A1
hold	23		24	MUX_A0
spare3	25		26	Ramfullext
SR_IN	27		28	Reset_BCID
spare4	29		30	GND
SR_OUT	31		32	Resetn
spare5	33		34	Start_Conv_daqb
SR_clk	35		36	End_Readout
GND	37		38	Start_acq
TransmitOn_3	39		40	RamFull
Pwr_analog	41		42	Dout_3
TransmitOn_2	43		44	GND
Pwr_dac	45		46	Dout_2
Pwr_ss/Pwr_sca	47		48	Start_Readout
GND	49		50	Trig_ext
TransmitOn_1	51		52	Start_Readout_Bypass
Pwr_digital	53		54	Dout_1
TransmitOn_0	55		56	GND
Pwr_adc	57		58	Dout_0
SC_SROUT	59		60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61		62	SC_SRIN
SC_select	63		64	SC_reset
SC_clk	65		66	SC_load
User_LVDS_P	67		68	User_LVDS_N
Trig_Ext_P	69		70	Trig_Ext_N
DVDD	71		72	AVDD
Clk_5MHz_0_P	73		74	Clk_5MHz_0_N
Clk_5MHz_1_P	75		76	Clk_5MHz_1_N
GND	77		78	GND
Clk_40MHz_0_P	79		80	Clk_40MHz_0_N
Clk_40MHz_1_P	81		82	Clk_40MHz_1_N
DVDD	83		84	AVDD
Raz_Chn_P	85		86	Raz_Chn_N
Val_Evt_P	87		88	Val_Evt_N
AVDD	89		90	AVDD

SLAB Interface

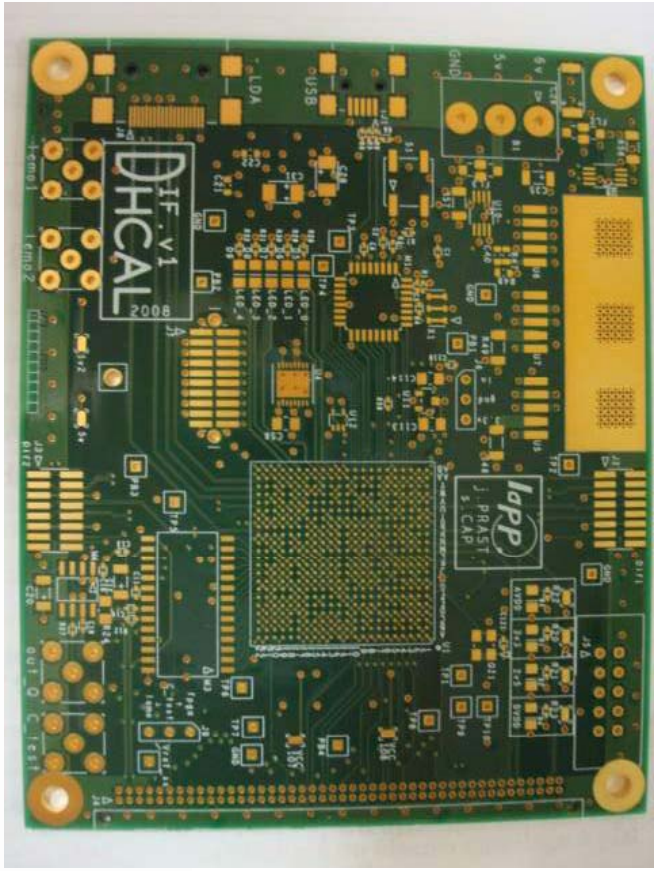
The connector has been designed for DHCAL but also ECAL or AHCAL

So the DHCAL DIF can also be used for ECAL or AHCAL !



Samtec FSH/ SFMH 90 pin connector

Status of the DHCAL prototype

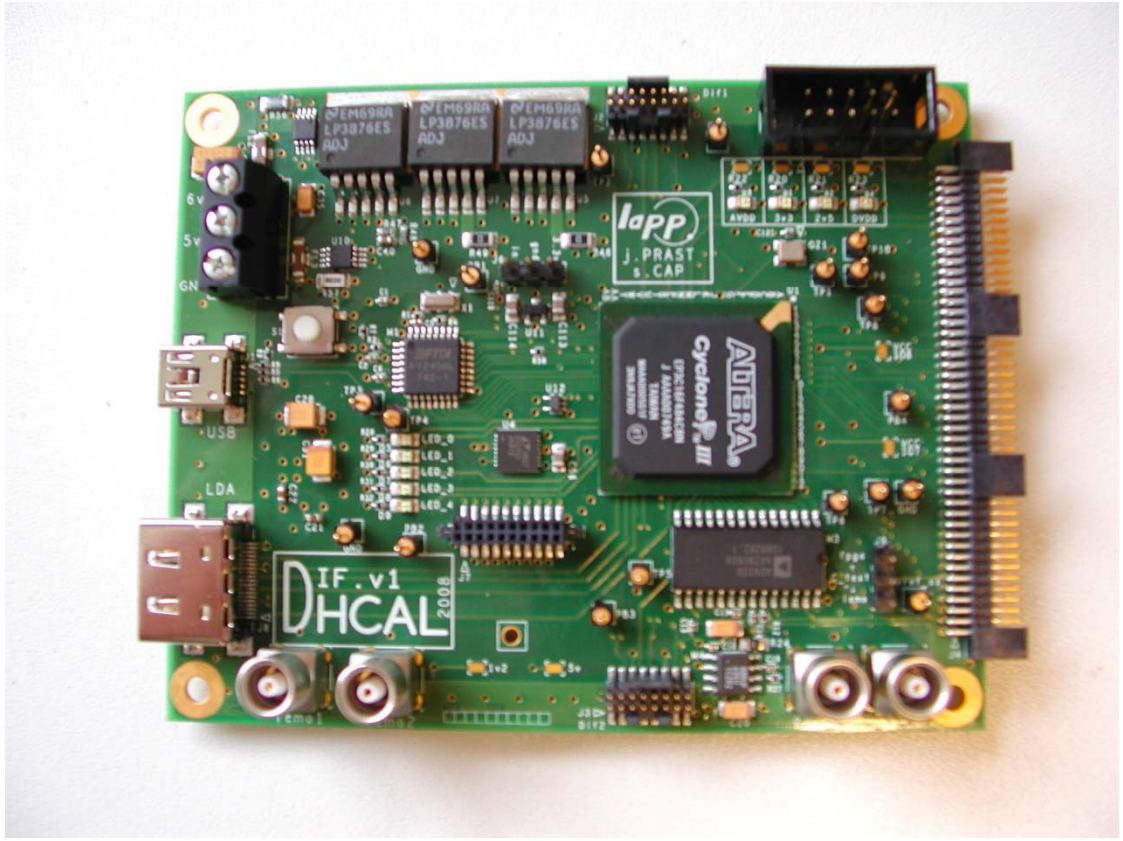


- Sent to production on April 29 th.
- 10 PCB are manufactured.

DIF Board without cabling

The DIF Board !!

We received it 2 days ago !!

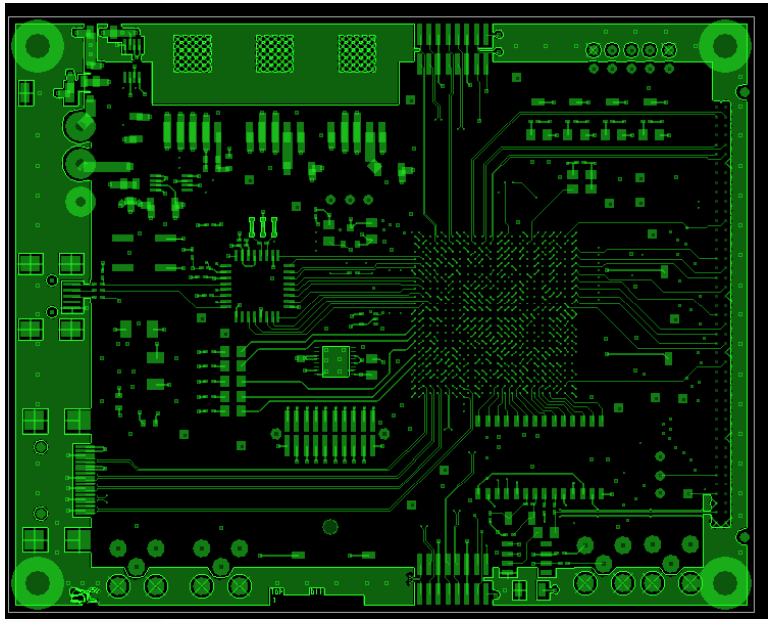


Tests of the DIF Board

We have done some tests:

- Electrical tests: OK
- JTAG test: OK

Mechanical and Electrical Characteristics

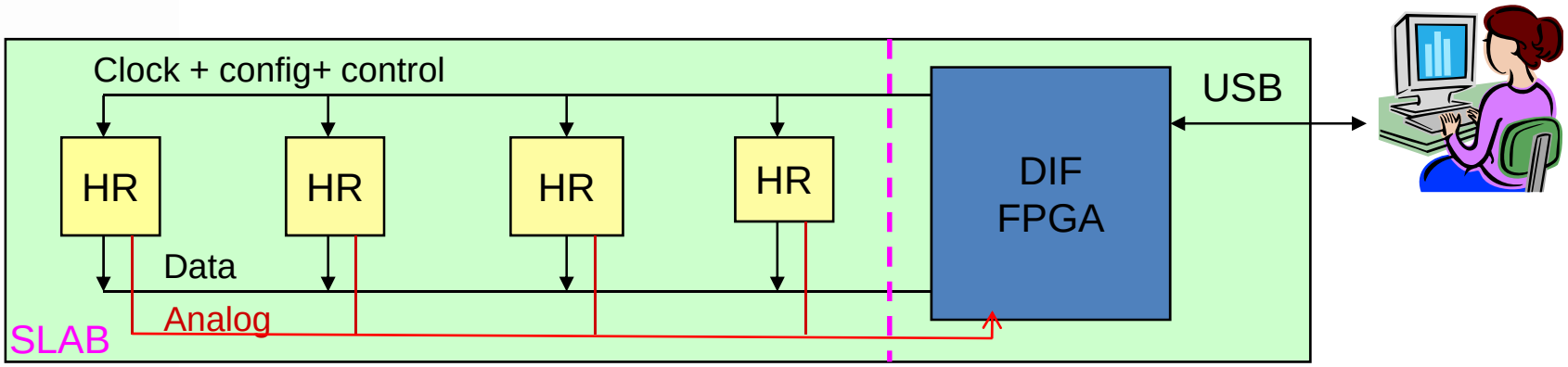


DIF Top View

- 8 cm *10 cm *1.6 mm
- 10 layers
  - 4 signal layers
  - Controlled impedance
  - Classe 6 (0.12 mm wire)

Many thanks to Sébastien Cap for the CAD.

Firmware Status (1)



Main performances of the FPGA:

- After receiving Slow Control data from PC, it has to configure ASICs correctly

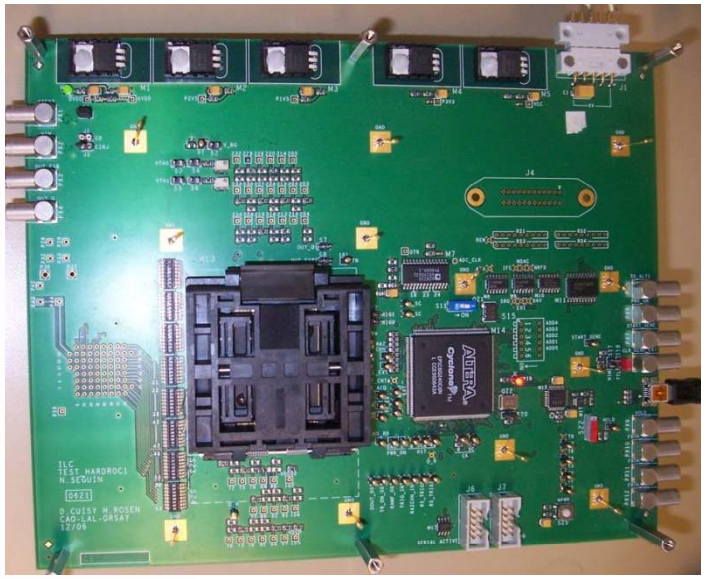
- It has to be able to launch acquisition and analog/digital readout and to send data it will receive from ASICs to a PC.

Firmware Status (2)

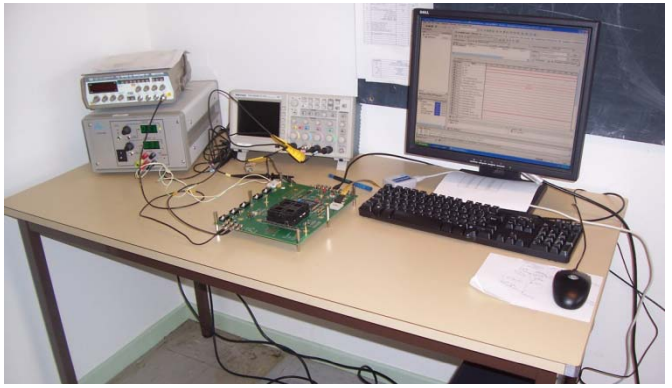
- USB interface : OK
  - R/W registers, commands, …
- Slow control : OK
  - HardRoc configuration
  - Checking : DAC output (V) = f(SC DAC value), Return signal (SC_q)
- Acquisition and Digital Readout : OK
  - Reception of data after doing acquisition and readout.
- Analog readout : to be tested
- Monitoring : to be tested
- LDA interface : to be developed

Software is developed by Christophe Combaret (IPN Lyon).
See his talk

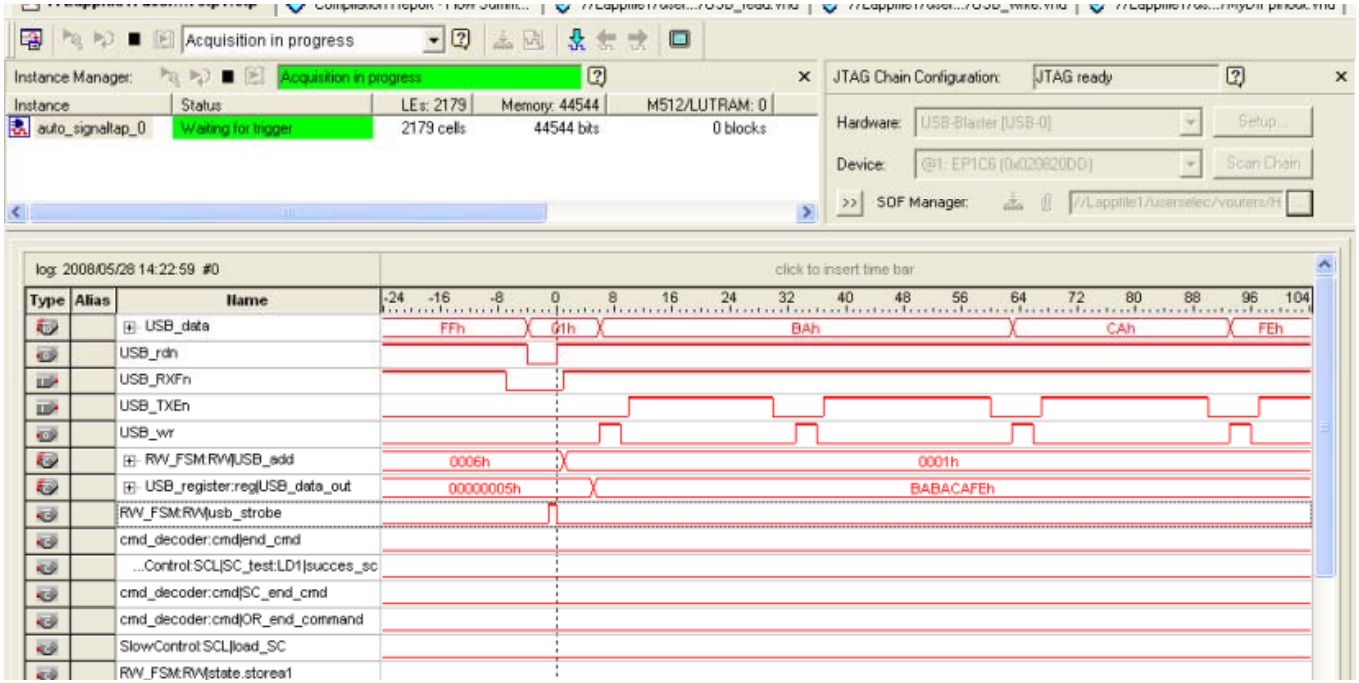
FW validation on the HR test board



- LAL HardRoc test board
  - 1 HR + Cyclone FPGA.
  - 12 bits ADC for the analog RO.
  - Possibility of charge injection.
  - USB interface.



Firmware debug

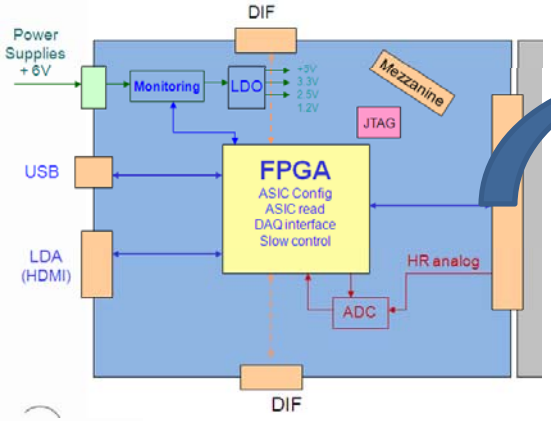


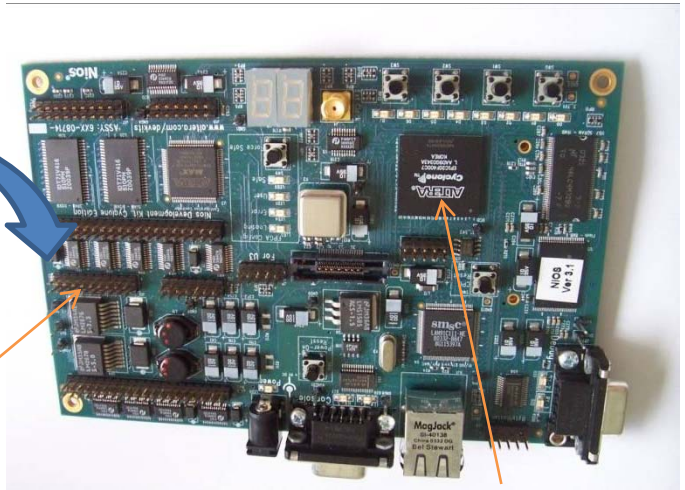
We use a very useful tool to debug the Firmware : Signal Tap
It allow to see signals in FPGA at when we want it during experimentations !

Validation of the DHCAL DIF

- ASU are not available yet to test the DIF.
- Emulation of HardRocs using an Altera evaluation kit.
  - Fit the HR VHDL (digital part) in the FPGA.
  - User defined IO connector to interface with the DIF.

=> Will allow validation of the DIF and FW for N HR





User defined connector

FPGA to emulate HardRocs

Conclusion

- DHCAL DIF boards are back from production, Firmware and corresponding software (Lyon) are in progress.
- Before ASU reception, the DIF will be tested using an Altera evaluation kit to emulate HardRocs.

=> Necessity to have a validated and reliable DIF for the November test beam.