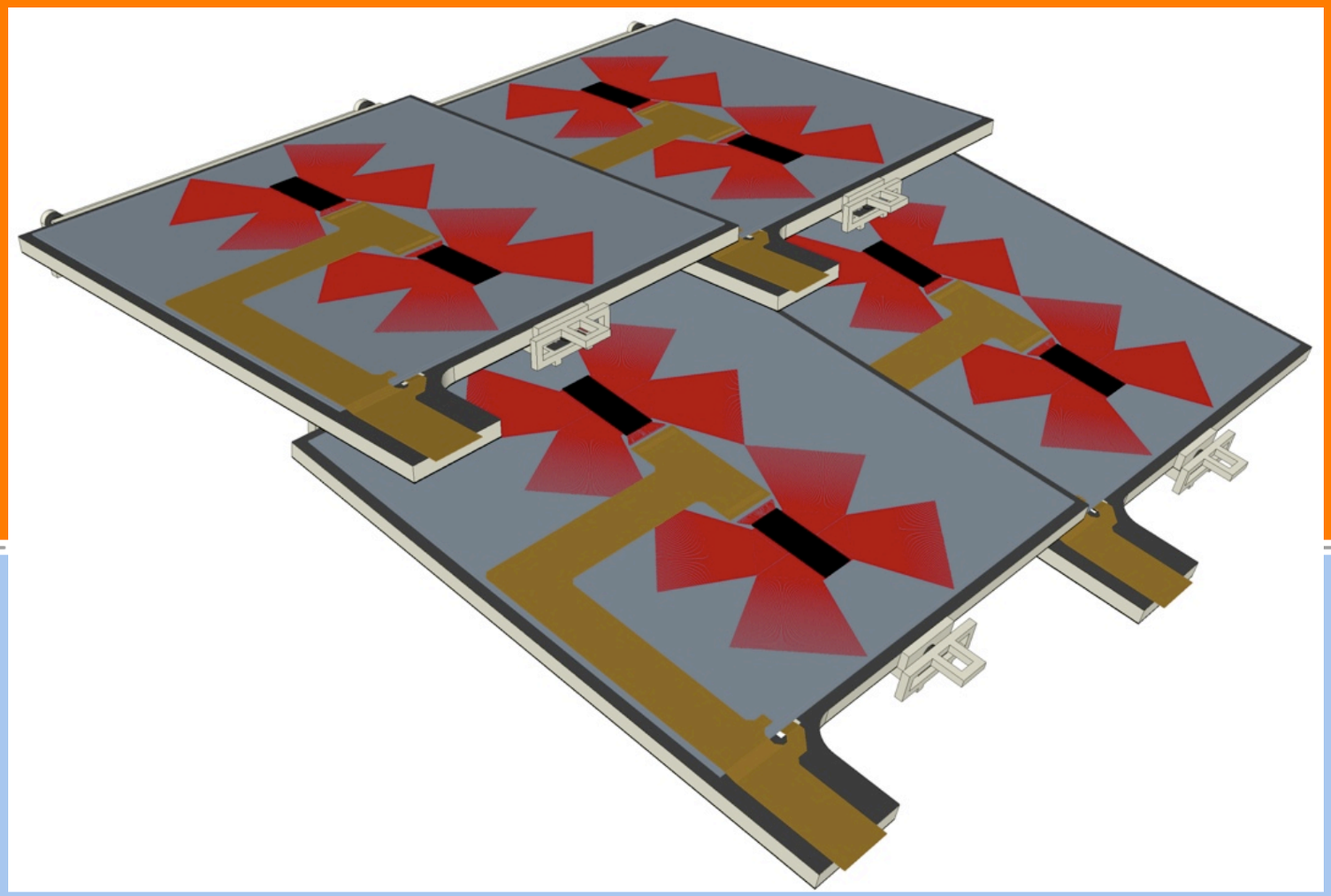
*Si*D Tracker Design: Status and Plans



Tim Nelson

SLAC

VLCW - 7/20/2006

Tracking Requirements

Superior P_T resolution:

- $e^+e^- \rightarrow Z^0 H^0 \rightarrow \mu^+\mu^- + X$

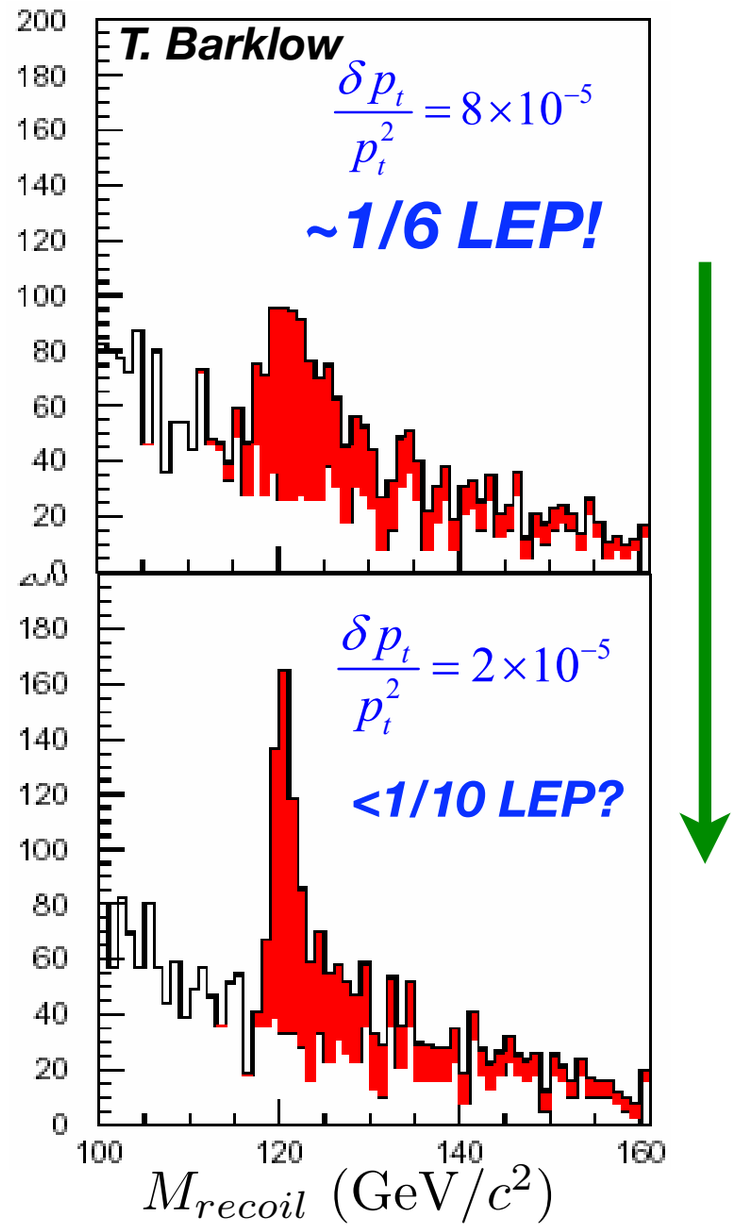
$$\text{Given } \sqrt{s}, M_Z, M_{\mu\mu} \Longrightarrow M_H$$

Low mass:

- Production of secondaries in tracking will threaten jet reconstruction in calorimeter
- Goal: average <1% X_0/layer

Mass producible / low cost:

- Roughly same scale as LHC trackers
- Production of components must be simple



Solutions: *Si*D Philosophy

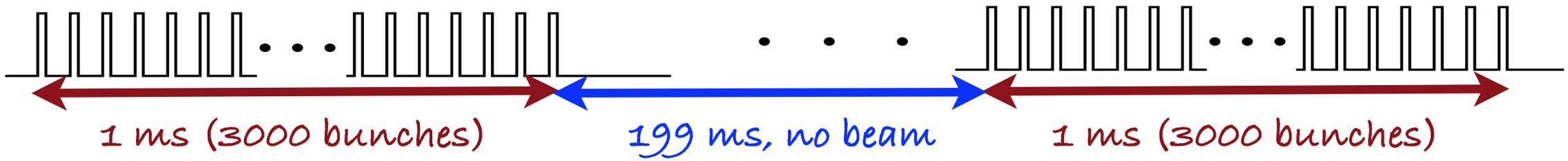
Superior P_T resolution:

- Large radial span
  ⇒ SiW ECAL gets large, expensive
- Large magnetic field
  ⇒ CMS-type solenoid of maximal field
- Smallest single-hit resolution
  ⇒ Silicon, optimized for precision

Low mass vs. Mass producible Si:

- BaBar (and others) have done low mass but NOT mass producible
- LHC did mass producible but NOT low mass
  ⇒ Need a design that shatters this dilemma

Use ILC Machine Attributes



During collisions (0.5%):

- **Most noise-generating digital functions of chip can be turned off**
  - **Need readout chip that buffers signals during train**
  - **Simplifies isolation/filtering generally requiring a hybrid**

    ⇒ **Mass reduction AND assembly simplification**

Between collisions (99.5%):

- **Power-consuming front-end can be powered down**
  - **Need readout chip that can be “power pulsed”**
  - **Eliminates need for active cooling**

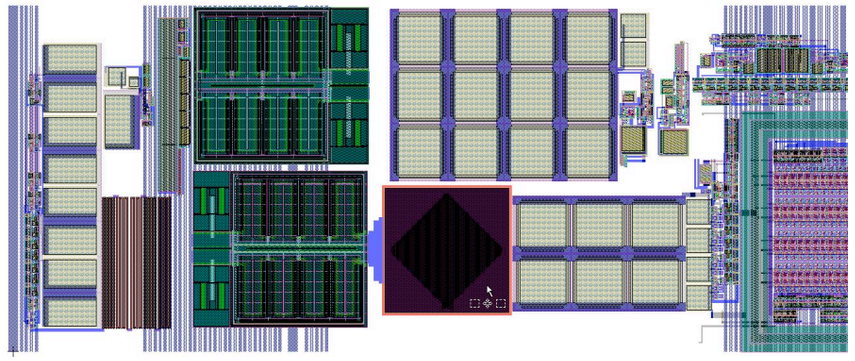
    ⇒ **Mass reduction AND assembly simplification**

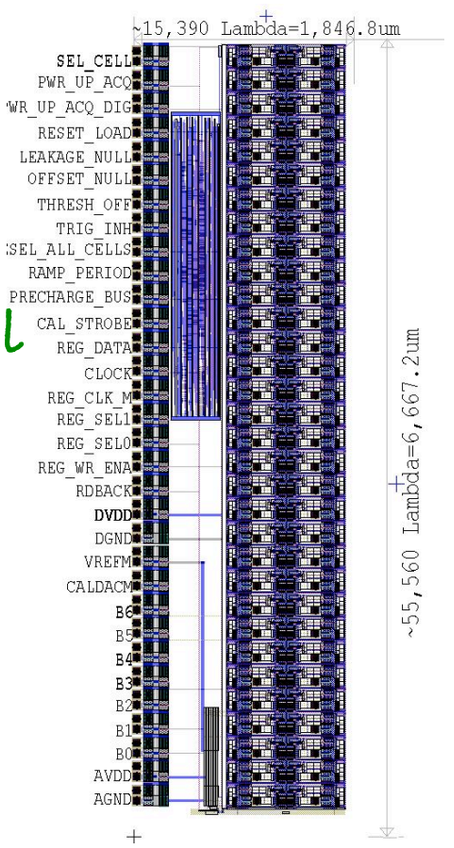
KPiX Readout Chip

Already under development at SLAC for *SiD* ECAL!

- 1024 Channels
- Power-pulsed, average power ~20mW
- 4 time-stamped analog buffers for readout between trains
- Designed for bump-bonding directly to silicon - no hybrid
- Dual-range logic for ECAL is only extraneous component

All the basic attributes we require



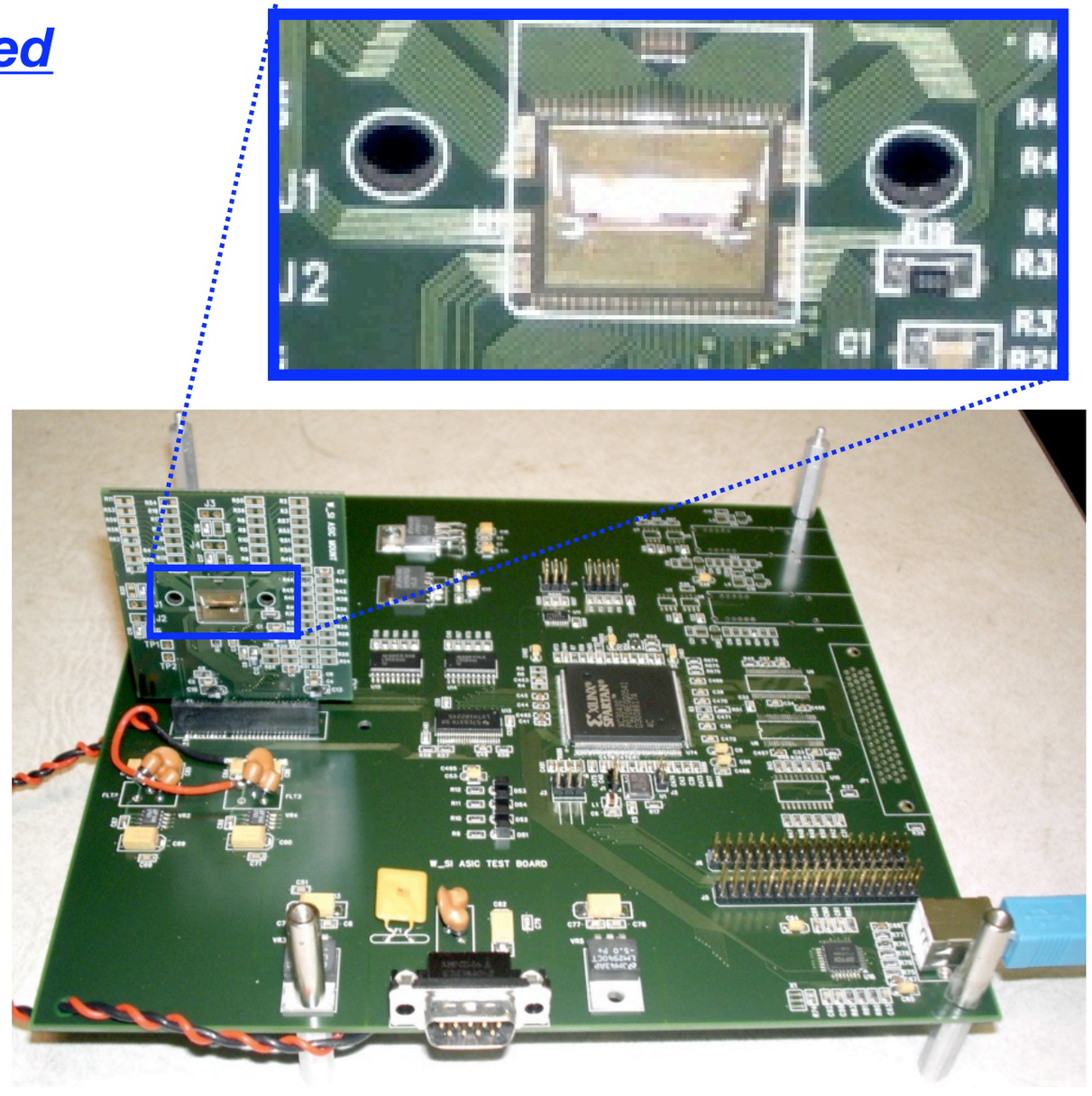


64-channel prototype: KPiX64

KPiX64-2

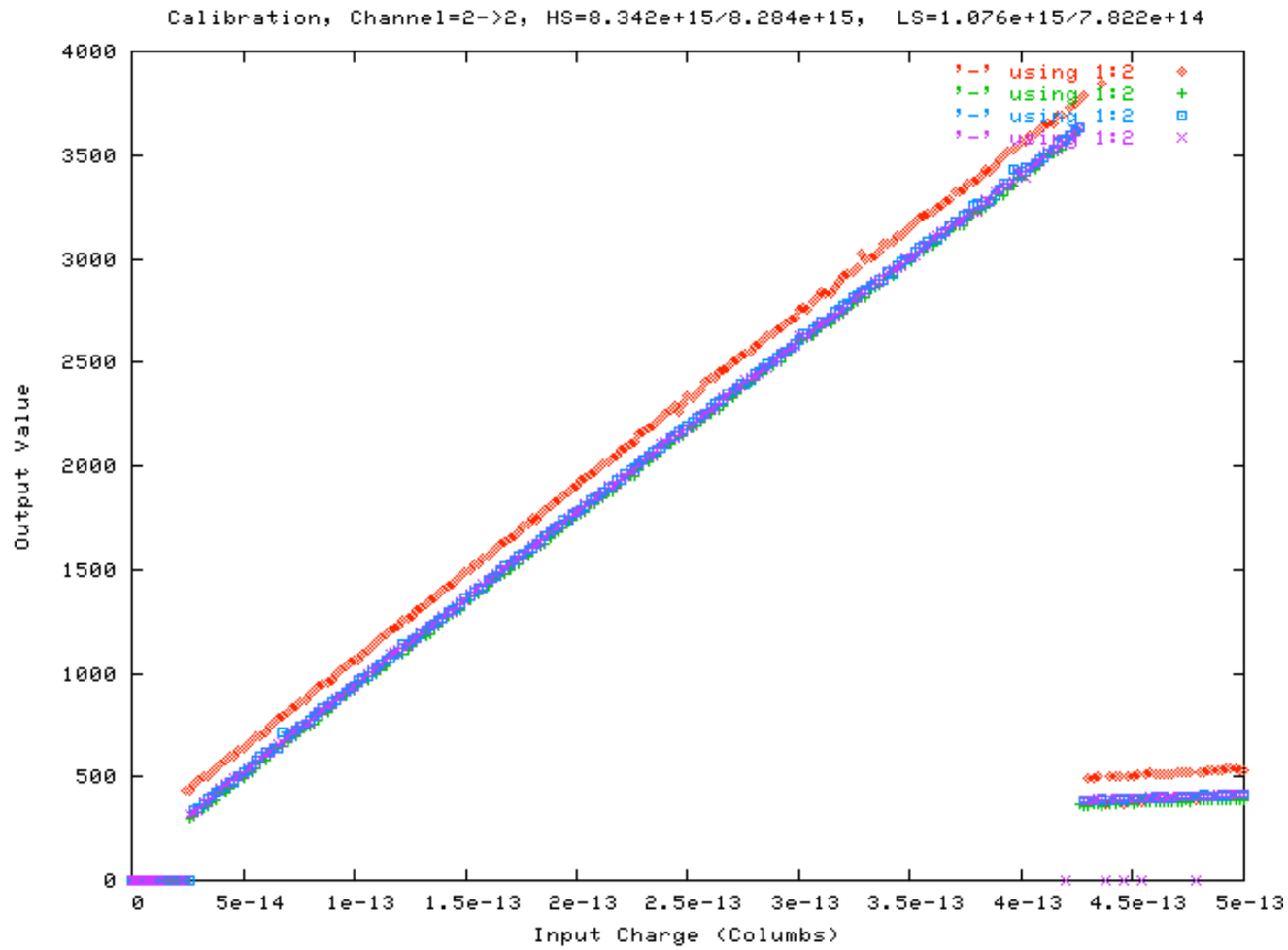
Second submission of 2×32 chip received

- **0.25 μm TSMC**
- **Currently undergoing testing: some mysteries, but chip appears to be functional**
- **Third 2×32 submission July 27th**
  - **Cleaner cell layout**
  - **External trigger for test beam**
  - **Input polarity option for GEM HCAL readout**
- **Fourth submission to include nearest-neighbor logic for tracker**



KPiX64-2

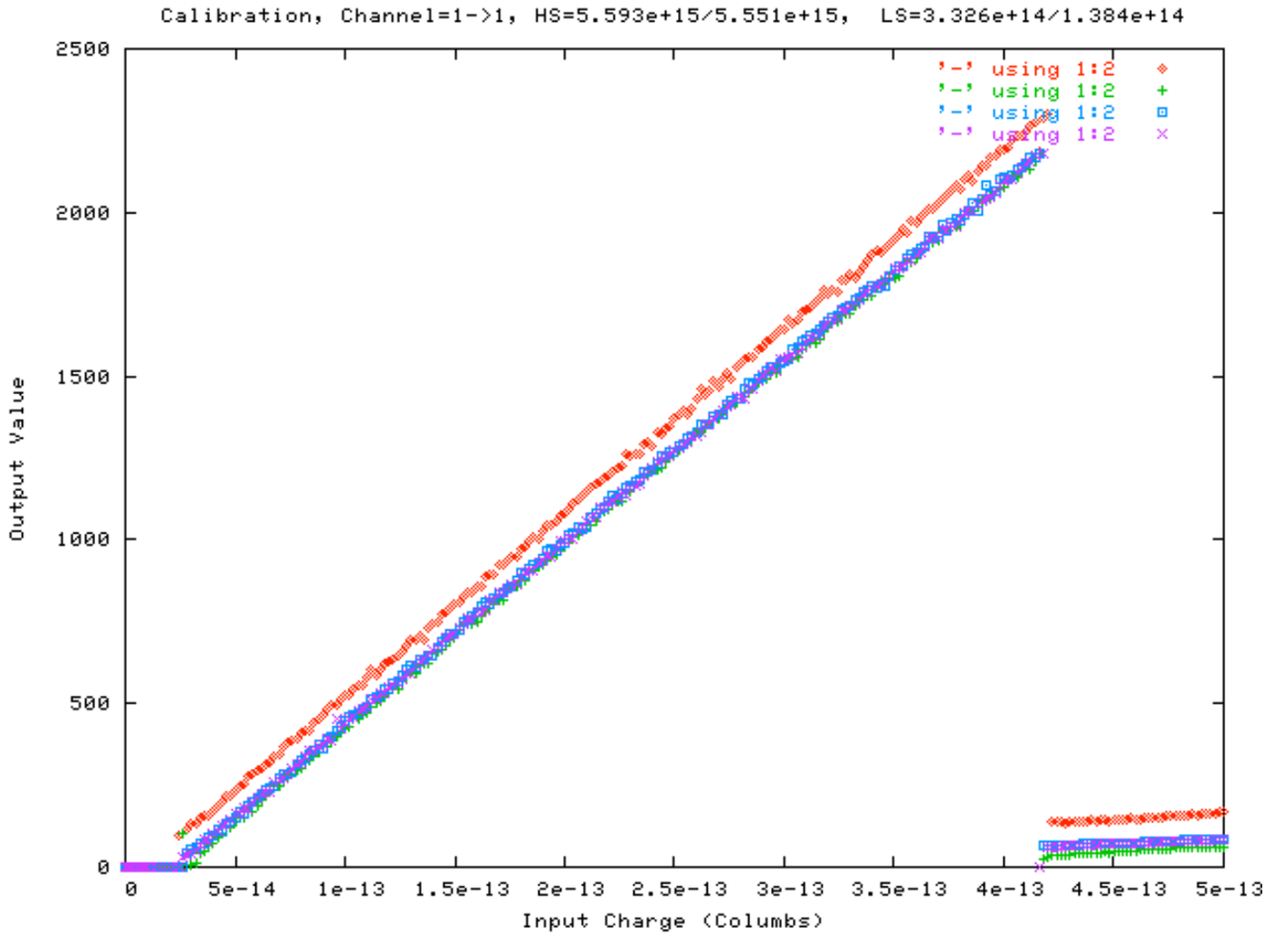
- Linearity appears good
- Dual range logic operates



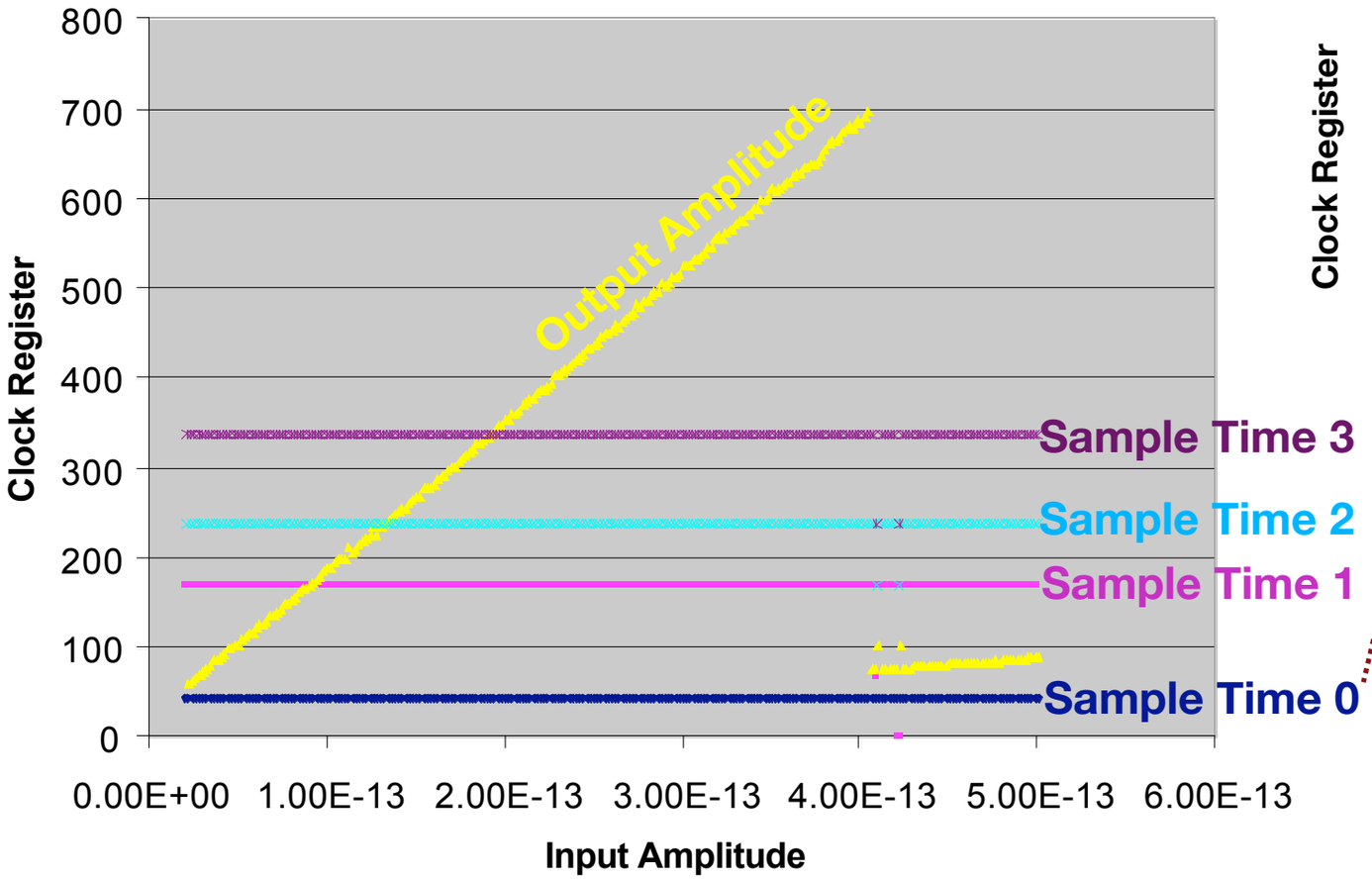
KPiX64-2

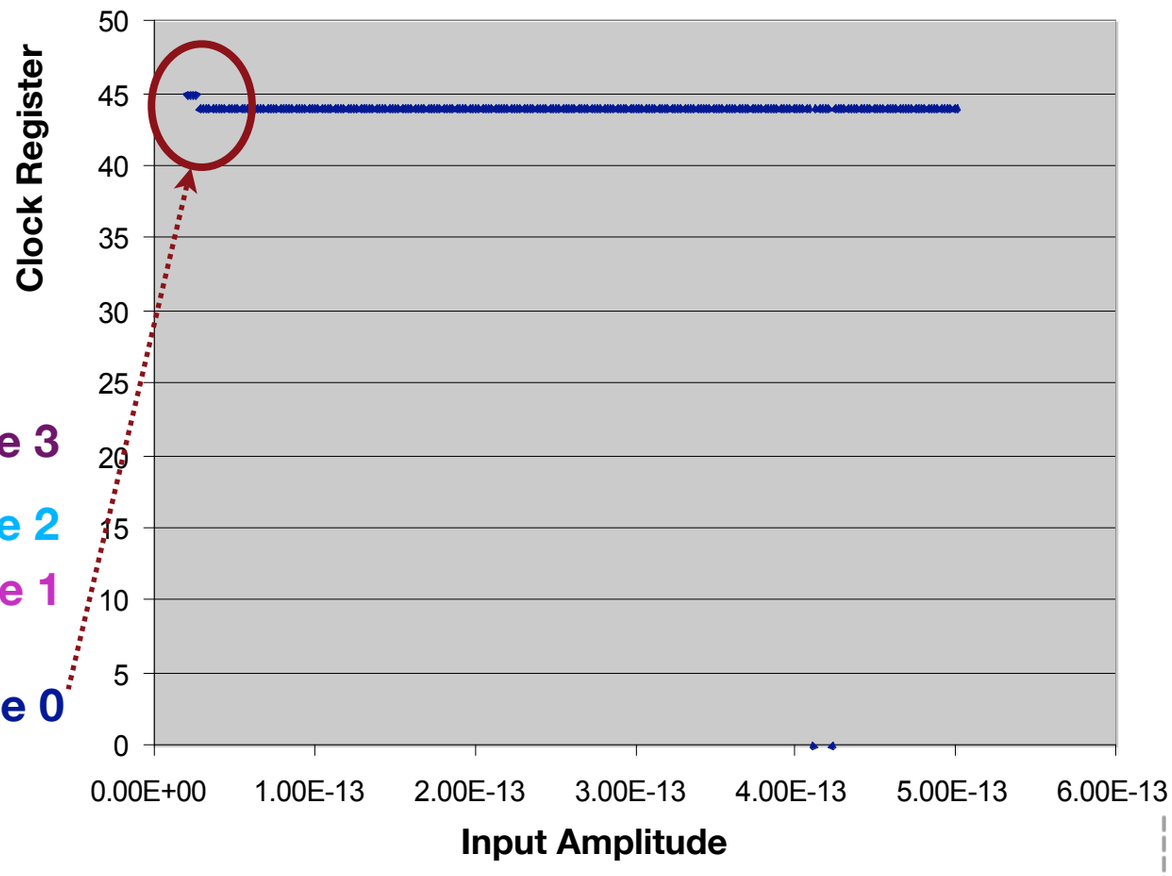
- Linearity appears good
- Dual range logic operates
- Channel-to-channel gain variations not understood

Noise studies are ongoing



KPiX64-2





- **Time-stamping circuitry works**
- **Minor mystery with wrong bucket on very low input charge**

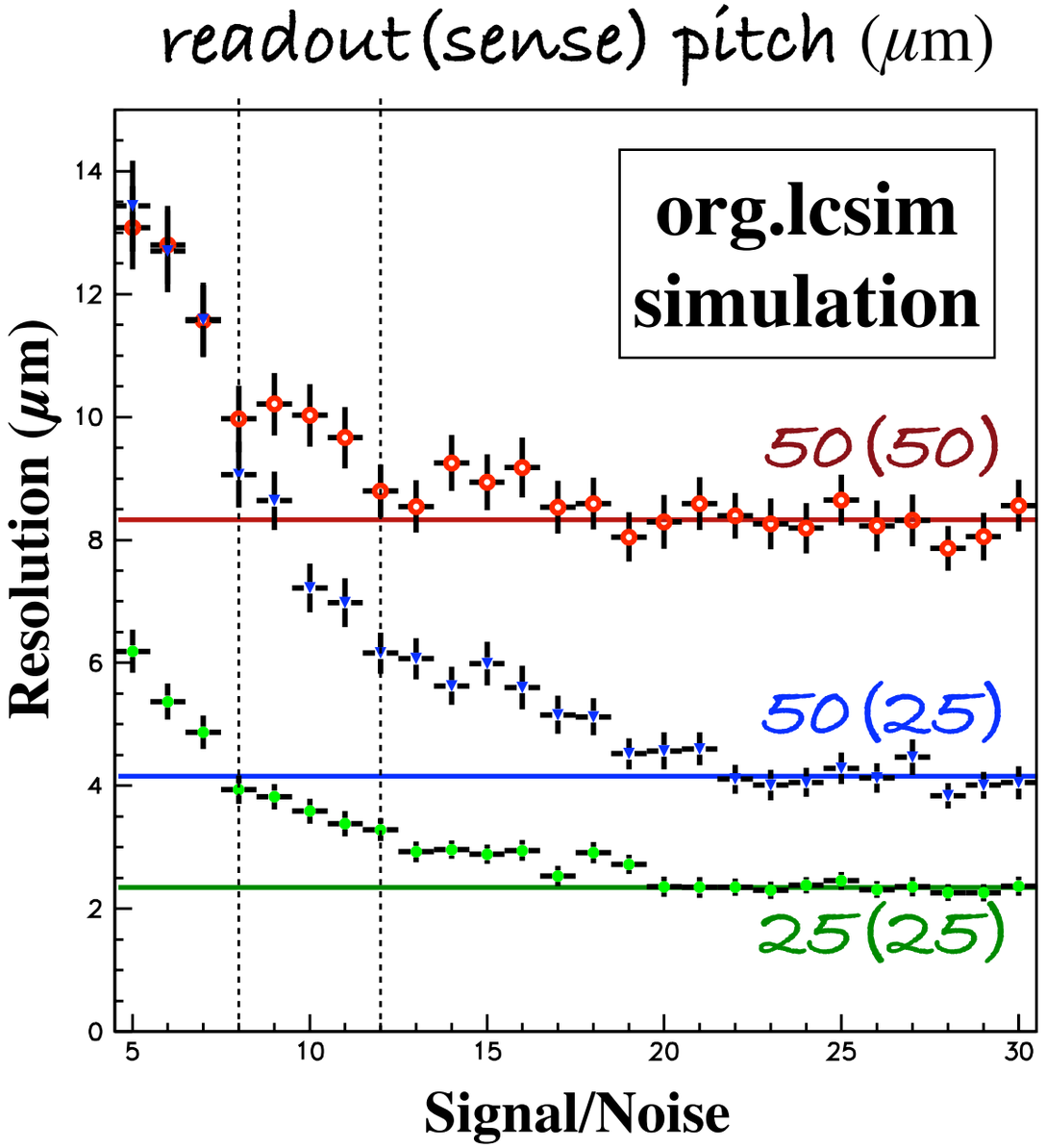
More details: M. Breidenbach's talk in ECAL session

Short Module Philosophy 101: Optimizing Single-hit Resolution

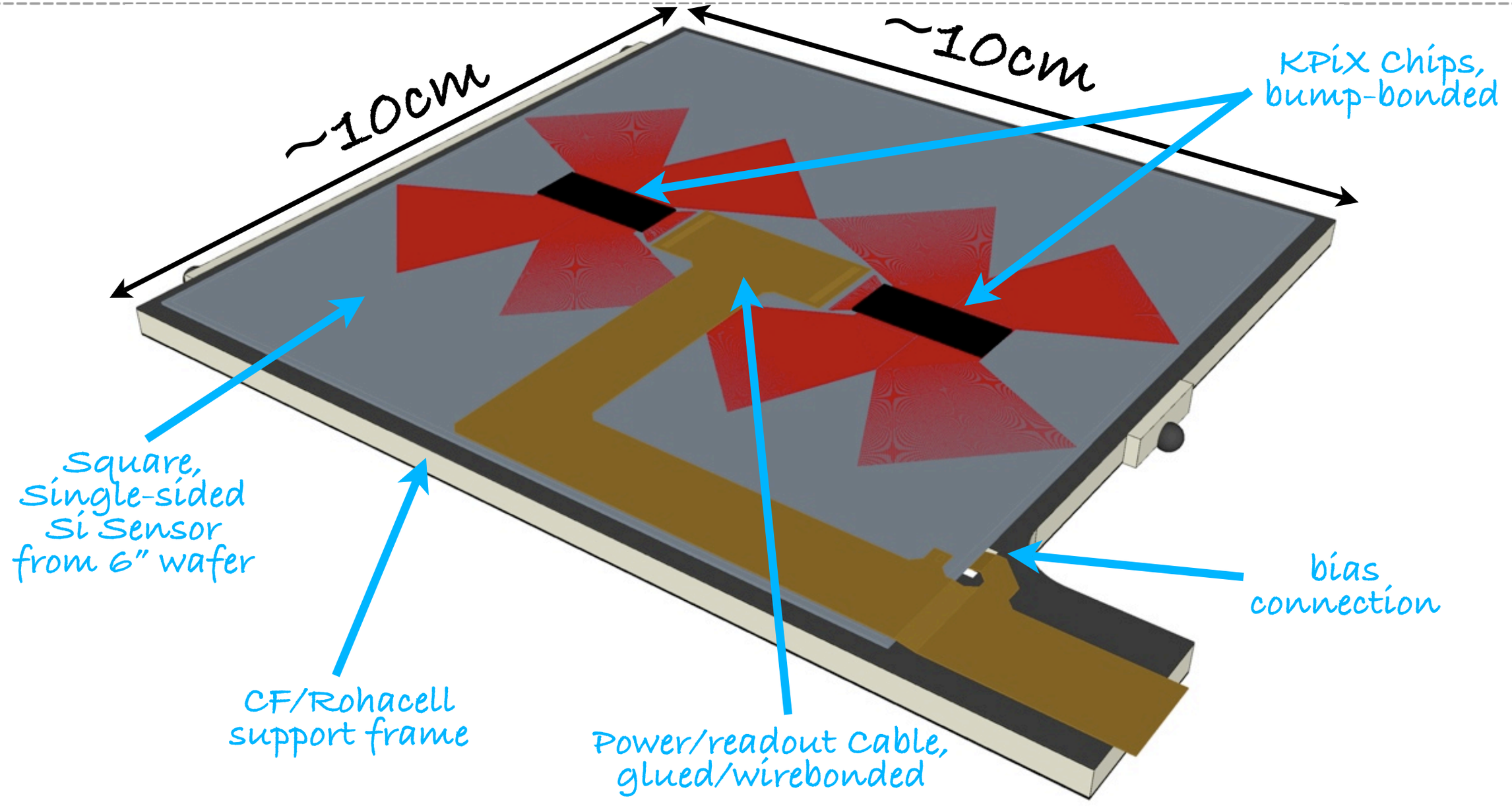
Reduce sense pitch (~25 μm)

- **Huge channel count/density: readout becomes difficult**
  ⇒ Read out every-other channel
- **Delivers resolution that approaches full 25 micron readout for high S/N**
- **Requires high S/N to deliver best performance**

⇒ Short strips for small input capacitance on amplifier



Short Module Design

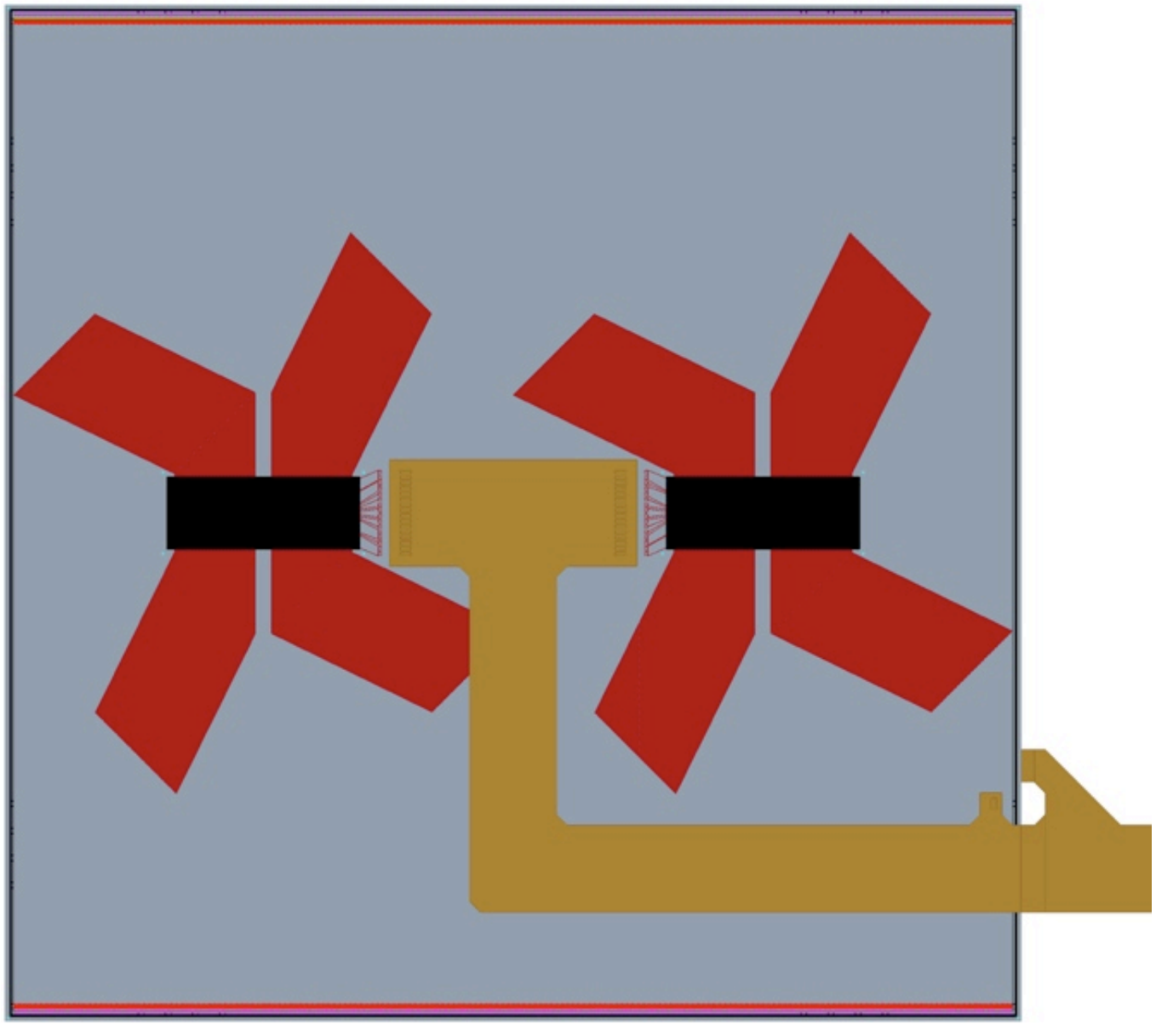


Sensor Design

- Single-sided p^+/n silicon
- AC-coupled, poly-biased
- 50(25) μm readout(sense) pitch
- 93.531mm × 93.531mm
- 1840 readout channels (3680 sense strips)

➡ Preparing detailed design and specs for HPK

➡ Submit this fall for delivery in early 2007

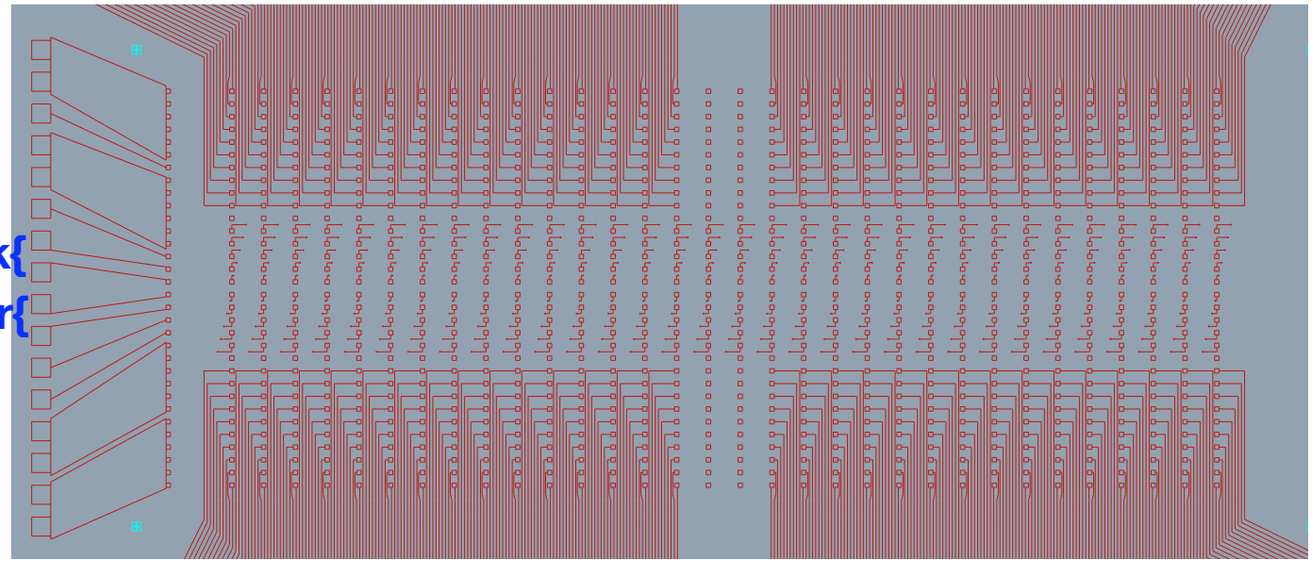


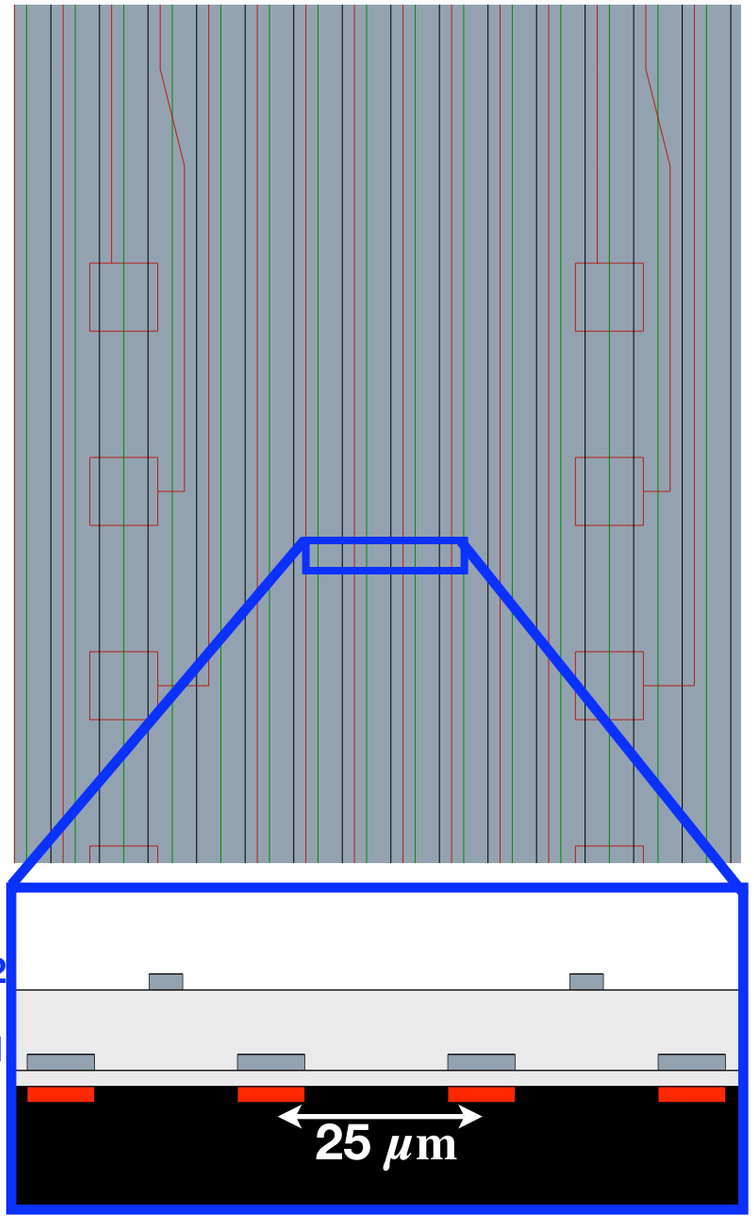
Sensor Design - Chip Station

critical LVDS lines:

clock{

ext trigger{





Double-metal layout:

- Carries digital signals and power between cable and *KPiX:* layout minimizes exposure to noise from LVDS clock lines
- Carries signals to *KPiX* bonding array: layout minimizes and equalizes capacitance among channels
  - Shortest trace: est. 15pf, 150 ohms
  - Longest trace: est. 21pf, 400 ohms

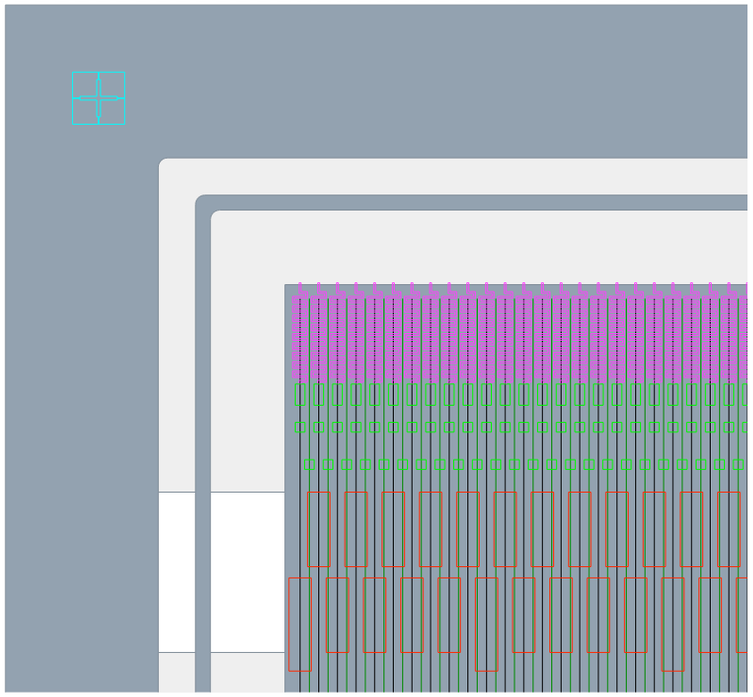
⇒Should achieve S/N ≥ 25 with *KPiX*

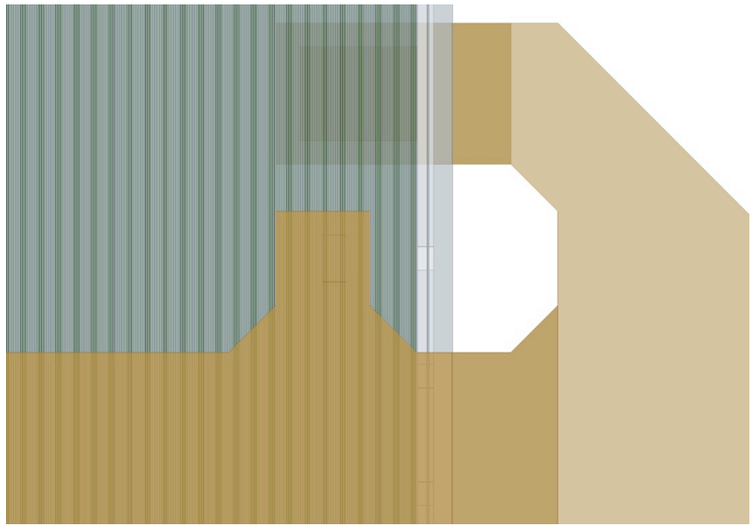
- Channel mapping facilitates nearest-neighbor readout

Sensor Design

- **Traditional wirebonding arrays at both ends**
  - Facilitates broad array of testing options
  - Leaves open possibility of longer modules without additional mask design
- **Unpassivated regions on bias/guard ring leave many options for detector biasing**

➡ **Design of short “pigtail” cable getting underway**





Short Module Philosophy 102: Support

Short modules require much less material than long ones to be self-supporting

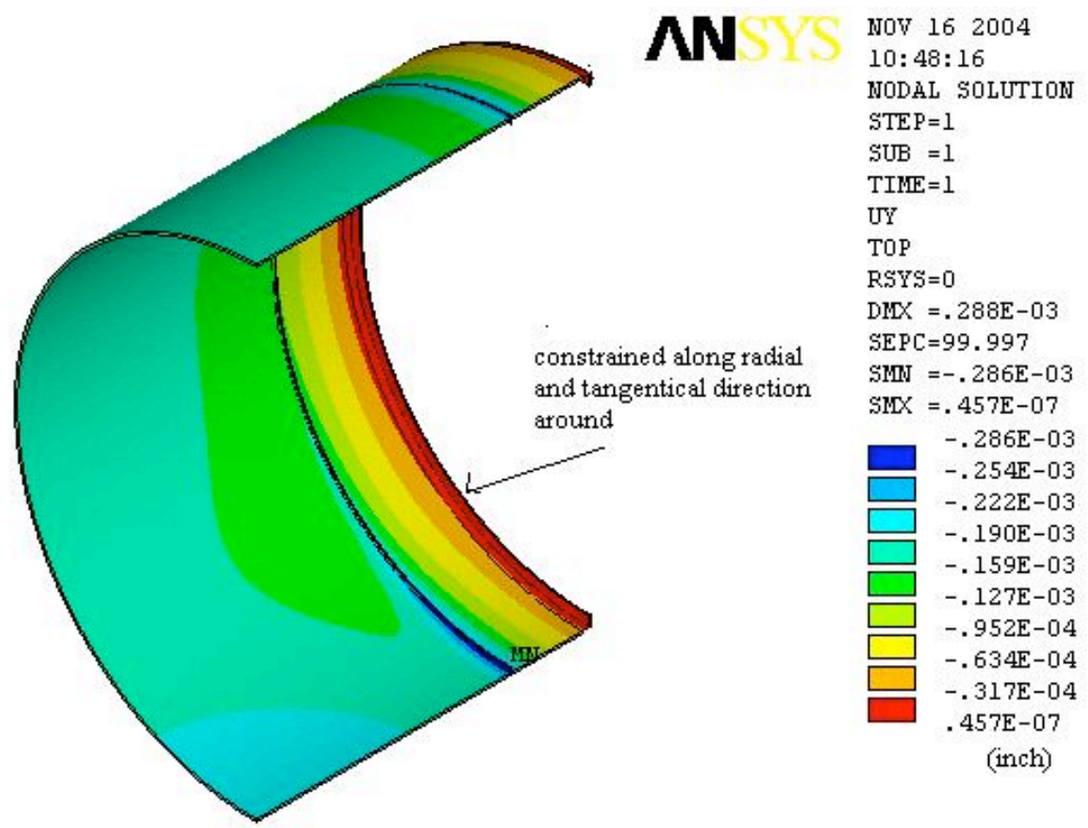
- **Redistributing material from module to underlying support allows it to be tied together into monolithic structure for maximum rigidity**

- **A continuous cylinder is the ultimate expression of this philosophy**

CF/Rohacell/CF sandwich with 0.3% X_0

7μm maximum deflection when fully loaded

W. Cooper, K. Krempetz - FNAL



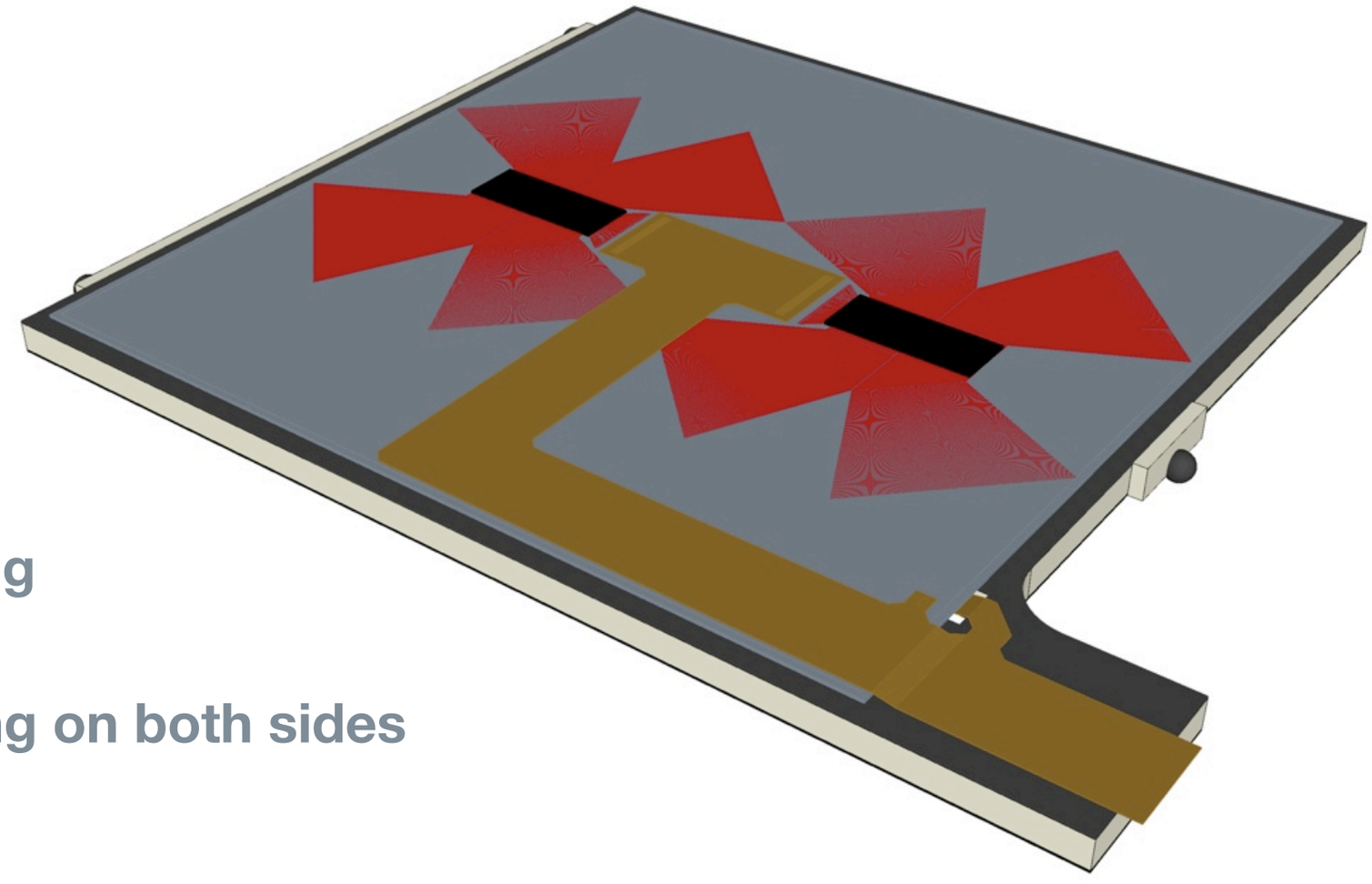
Vertical deflection with a 16mm x 7.5 mm carbon ring and 48 mm x 7.5 mm endring radial and tangencial direction has been constrained around the endring to simulate a very rigid endring.

Probably overkill!

Module Support

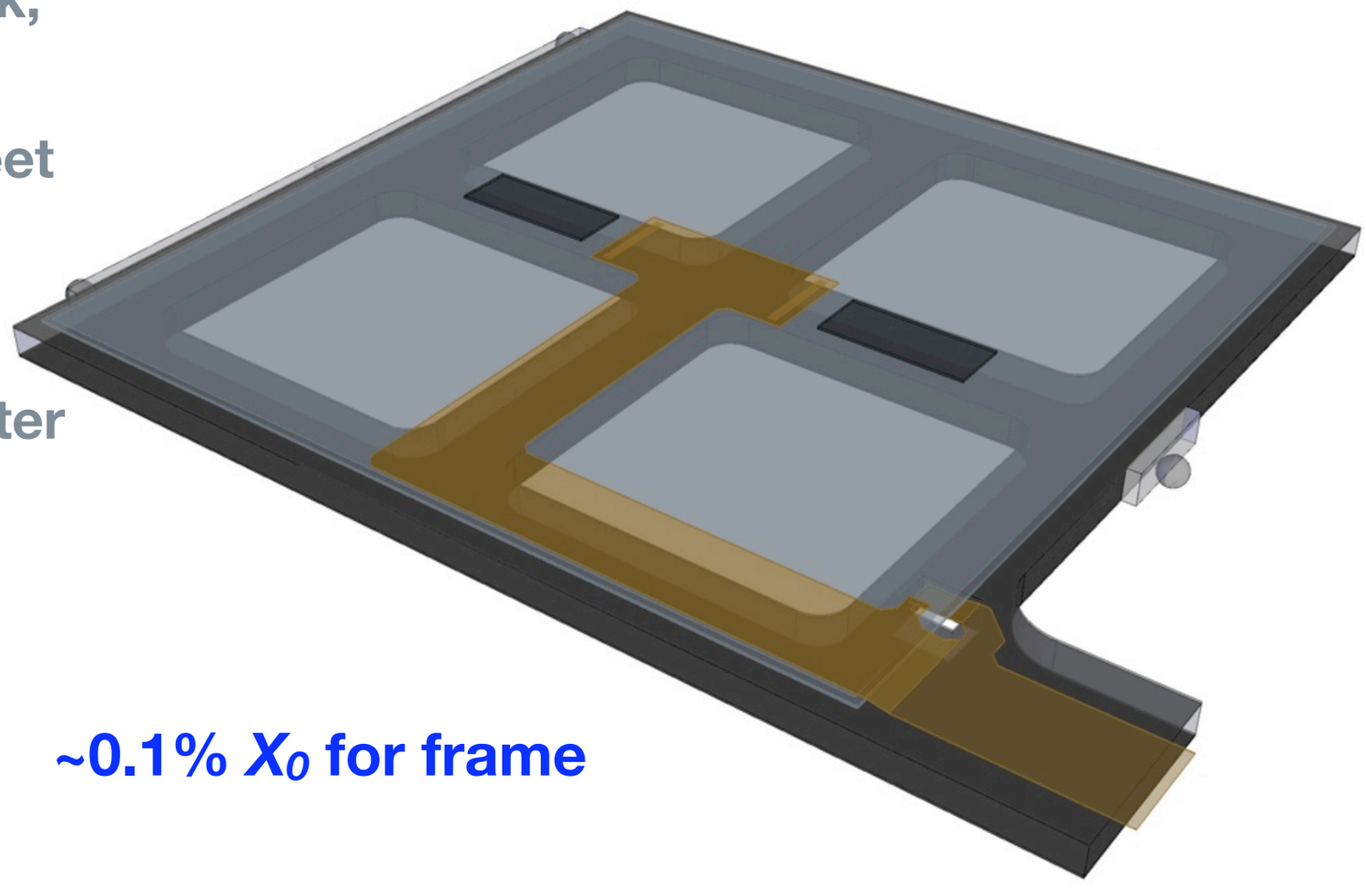
Can be minimal

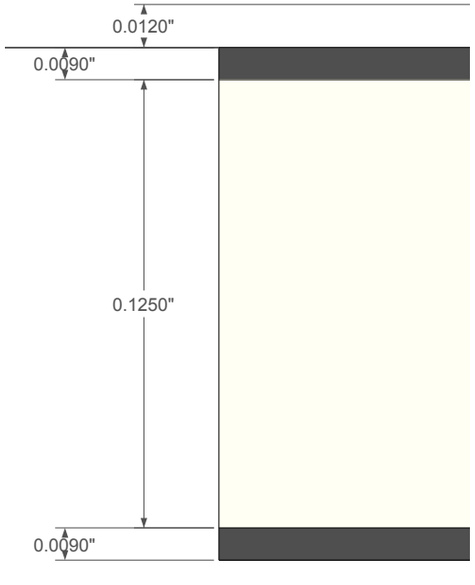
- Hold silicon flat
- Facilitate handling
- Provide stable positioning
- Allow for silicon mounting on both sides



Silicon Support Frame

- Two 60-60-60, 0.009” thick, high-modulus CF sheets
- 0.125” Rohacell foam sheet
- 50% void - CF under chip
- Tab for handling, cable strain relief, bias filter





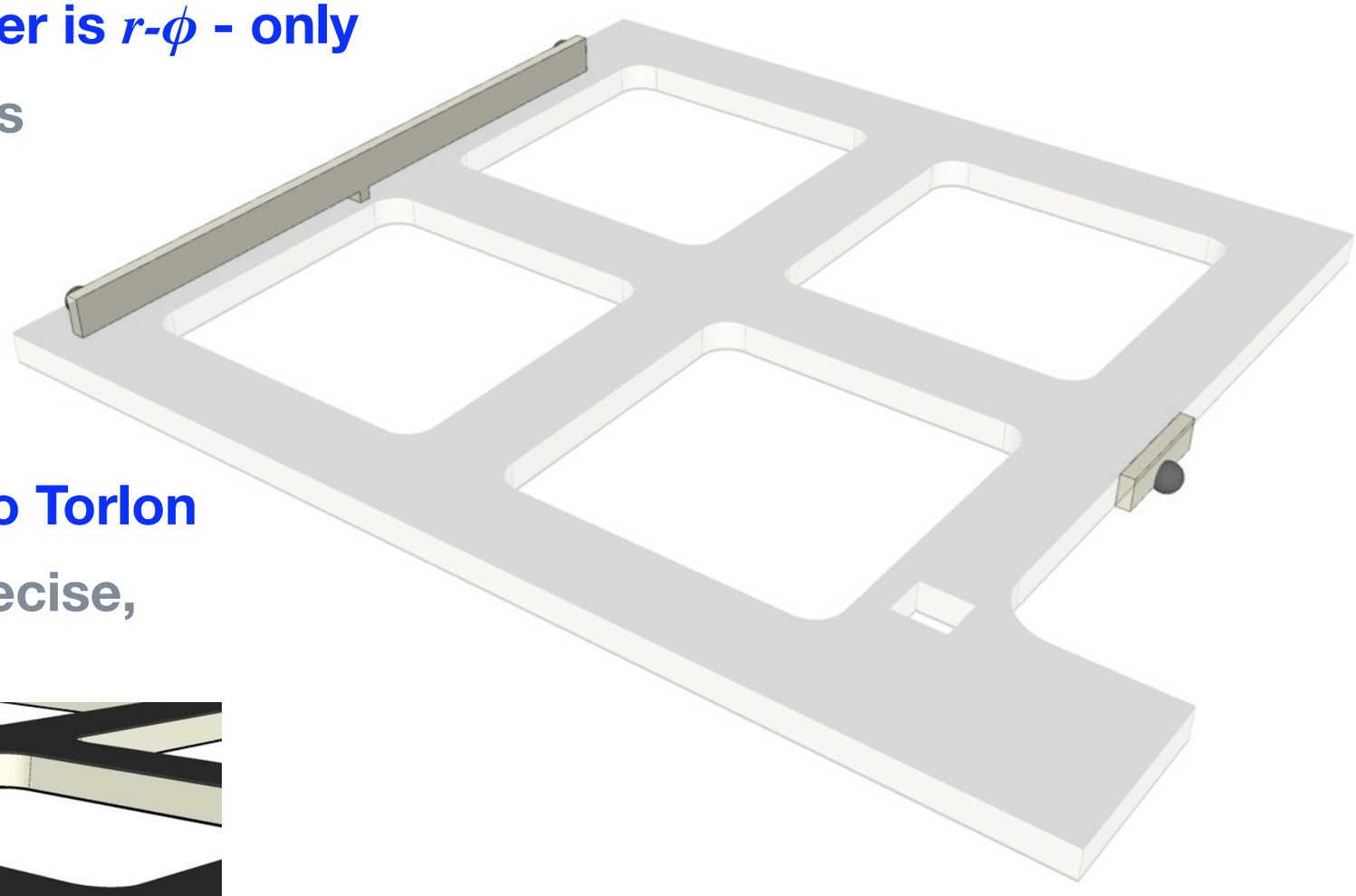
~0.1% X_0 for frame

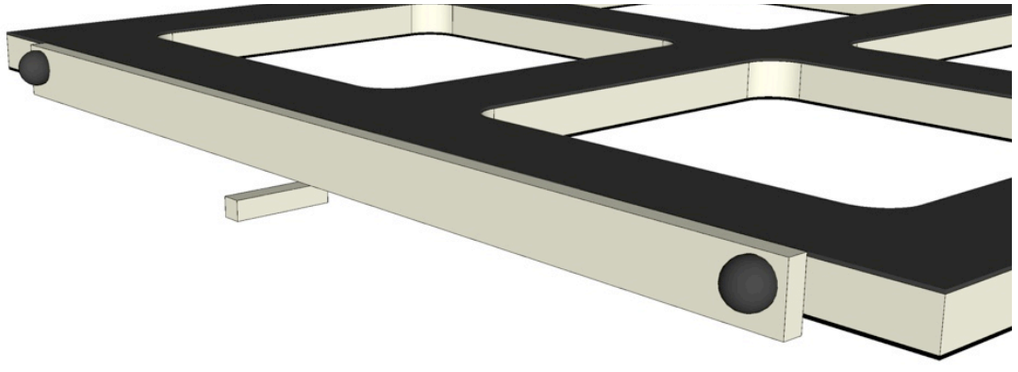
Next: FEA to test/refine frame design

Mounting Precision

Stringent requirement on strip parallelism for standalone tracking if tracker is r-ϕ - only

- 30% CF-filled Torlon strips
  - Modulus = 1/3 7075 Al
  - CTE = Si + 3×10^{-6} /°K
- **Mounting points: 0.125” Si_3N_4 balls, insert-molded directly into Torlon**
  - extremely hard and precise, light, inexpensive



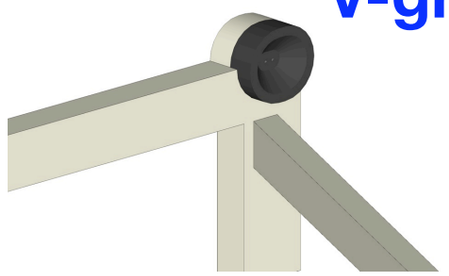


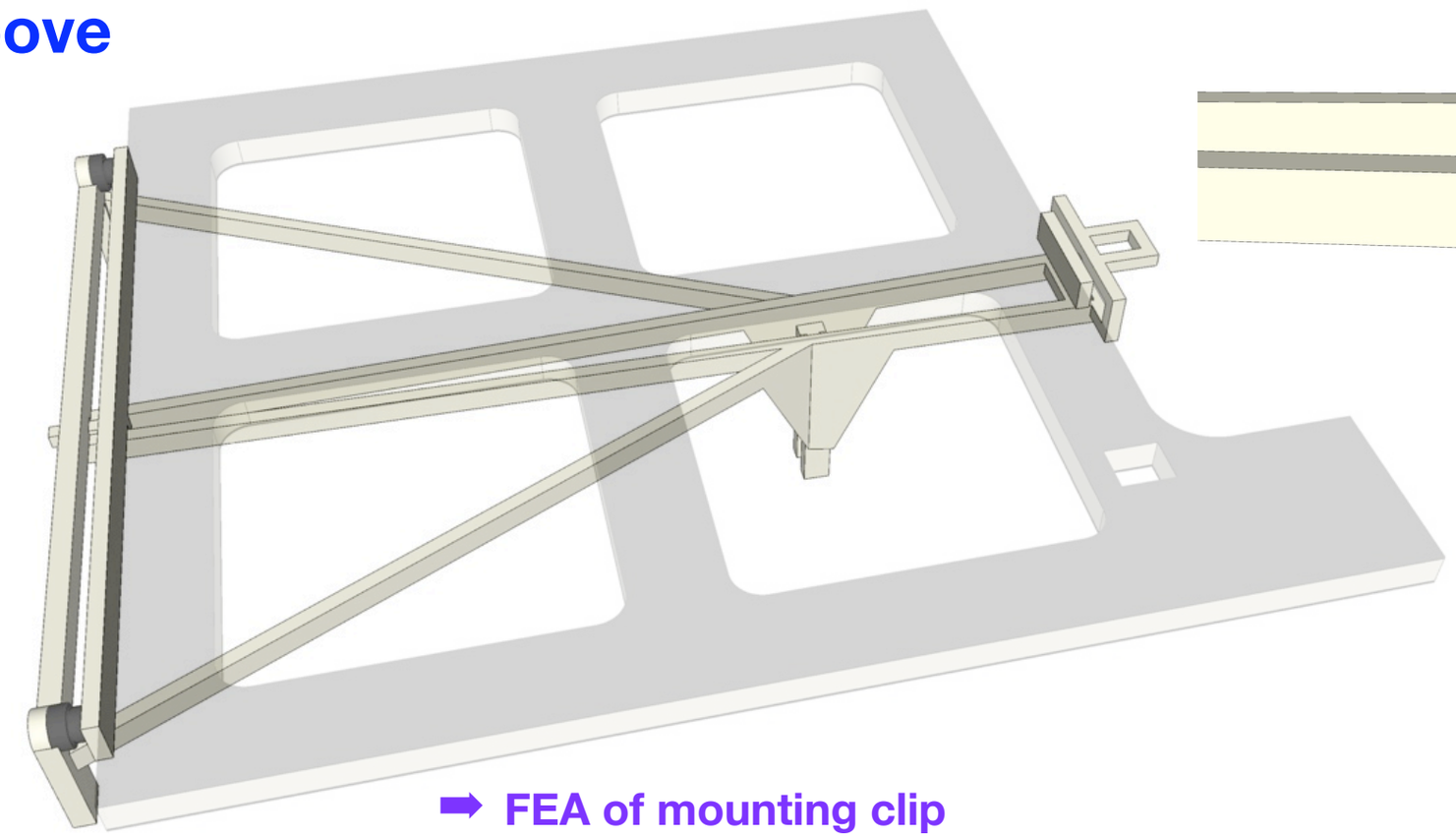
Simulation must tell us how serious this is

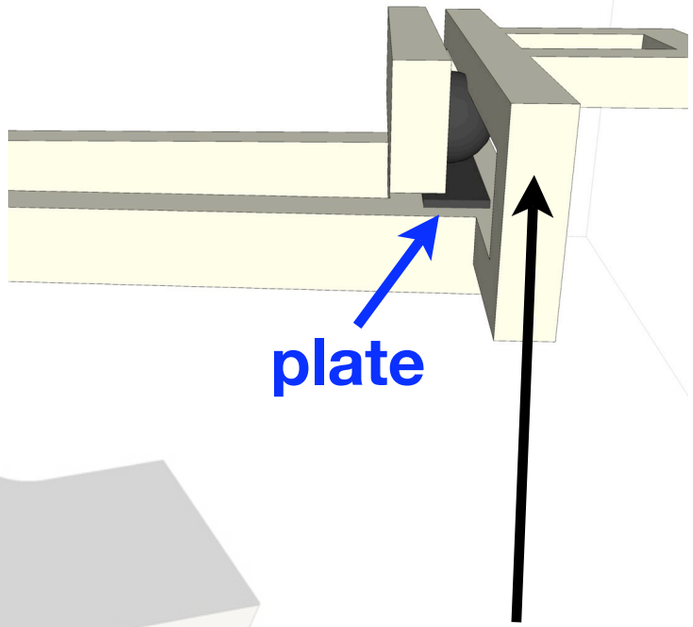
Mounting Clip

CF-filled Torlon with custom Si_3N_4 inserts

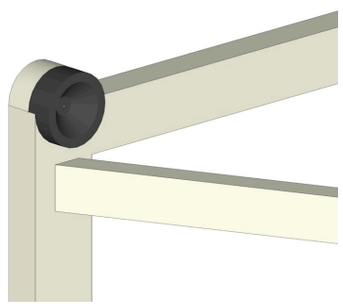
v-groove







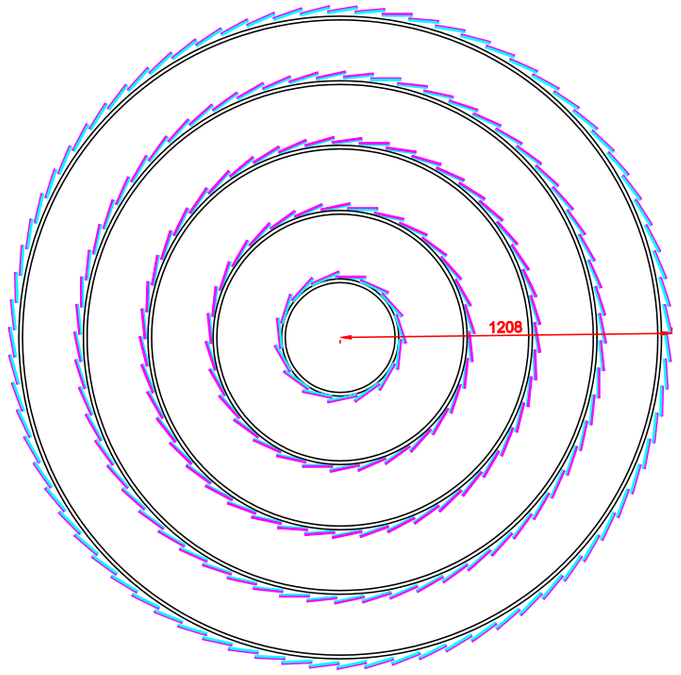
cone



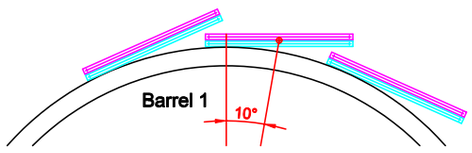
- ➡ FEA of mounting clip
- ➡ Rapid prototyping: are Si_3N_4 mating parts even necessary to achieve repeatable orientation of strips for r-ϕ - only standalone?

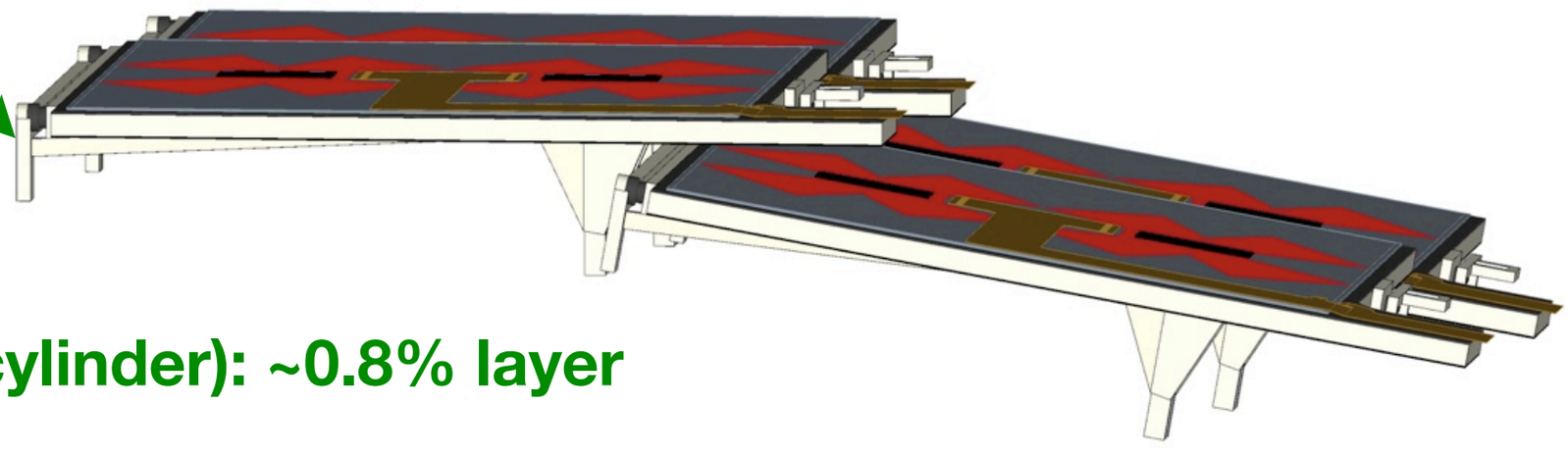
Module Tiling

- *Design provides necessary overlap*
- **Feet of mounting clips glued into holes machined in cylinders**
- **Very short path from support cylinder to critical ball-and-cup joints**



Sensors:
Cut dim's: 104.44 W x 84 L
Active dim's: 102.4 W x 81.96 L
Boxes:
Outer dim's: 107.44 W x 87 L x 4 H
Support cylinders:
OR: 213.5, 462.5, 700, 935, 1170
Number of phi: 15, 30, 45, 60, 75
Central tilt angle: 10 degrees
Sensor phi overlap (mm):
Barrel 1: 5.3
Barrel 2: 0.57
Barrel 3: 0.40
Barrel 4: 0.55
Barrel 5: 0.63
Cyan and magenta sensors and boxes are assumed to be at different Z's and to overlap in Z.
Within a given barrel, cyan sensors overlap in phi as do magneta sensors.



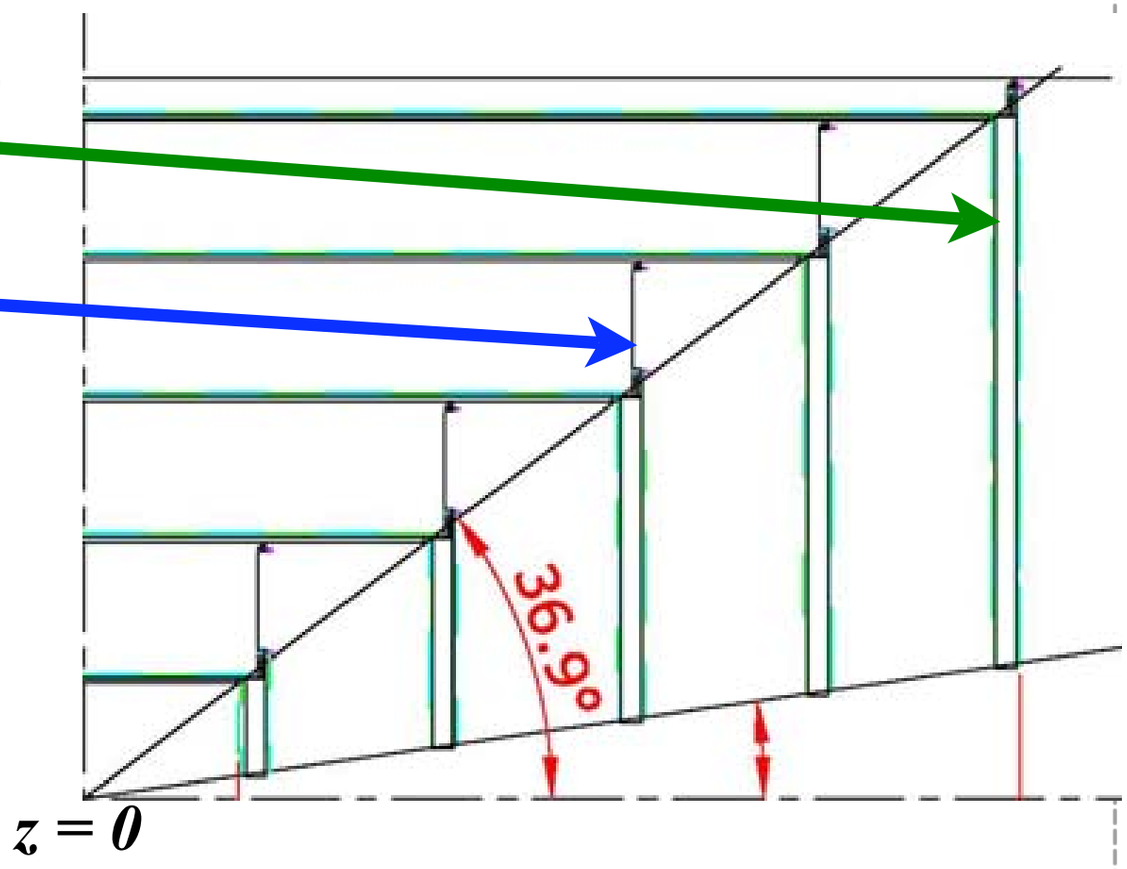


Total barrel material (incl. cylinder): ~0.8% layer

Endcaps?

- Close ends of cylinders with annular disks of similar composition
- Annular CF rings connect nesting barrels, host power/readout distribution boards
- Power distribution via DC/DC conversion minimizes copper into tracking volume
- Same module concept, probably double-sided
  - Also squares (90-degree stereo)?
  - Wedges?
  - Hexagons?

Simulation must answer this question: should be possible soon



1/4 r-z view

SiD Tracker R&D Roadmap

2006

- Produce working *KPiX64*, test fully
- Design/order prototype silicon from HPK
- Design prototype pigtail cables
- Produce fully engineered module design
- Produce fully engineered mounting scheme: test with rapid prototypes

2007

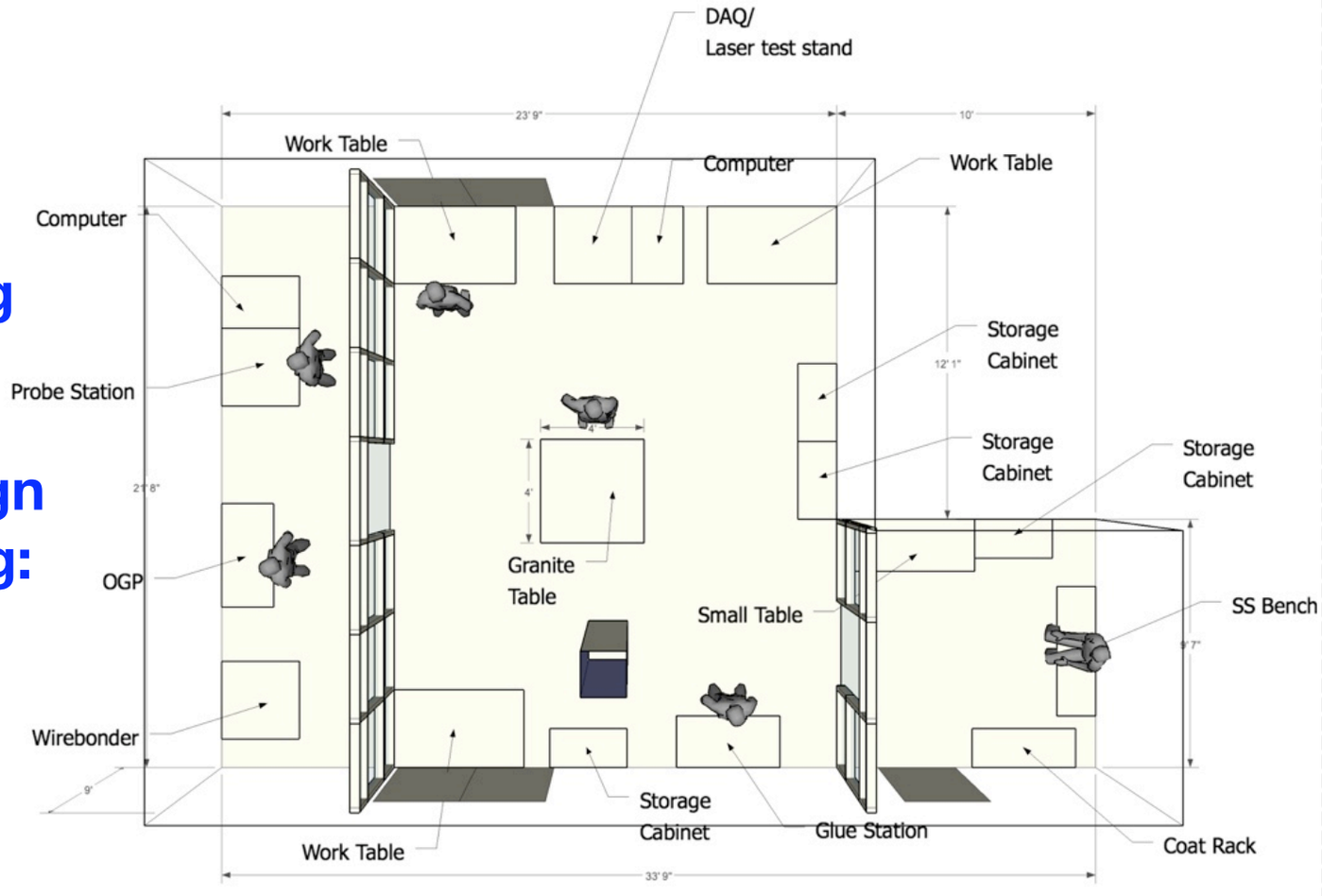
- Produce and test first 1024-channel KPiX
- Obtain prototype sensors and pigtails, testing/assembly/wirebonding with sensors
- Fabricate prototype module supports, mechanical testing
- Create module assembly fixtures and assemble first prototype module
- Produce design for endcap modules
- Design power distribution system

2008

- Assemble telescope of ~10 barrel modules for beam test
- Obtain parts for and assemble prototype of endcap module

Summary

- ***Si*D tracker continues to develop around *KPiX* readout chip: *KPiX* progressing well**
- **Barrel silicon design approaching submission to HPK**
- **Fully developed conceptual design for module support and mounting: ready for rapid prototyping**
- **On track to build complete prototype module in 2007**



Assembling a small silicon lab at SLAC to support SiD there