DAQ Status & Developments

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ILD WS 2010
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Overview

- Many recent activities
  - Letter of Intend
  - Test Beam WS in LAL in november
  - EUDET meeting in december
  - AIDA call for FP7
- Near future
  - *Preparation of ILD DBD → Plans until 2012*
  - What is needed for TB (stand alone & combined)
    - *could also be seen for ILD as a " small scale repetition"*
    - Mutualisation : HW, SW, protocols, experience
    - Test of technologies

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DAQ for ILD in the LOI

- 10^9 channels & 5 Hz * ms bunch trains
  ⇒ triggerless operation (globally) with local auto-storage & SW filters
- Data, Computing < LHC
- Rates estimations
  - Beam-Beam Bgd dominated
    - ee pairs
  - Baseline SiW ECAL + AHCAL
  - For nominal parameters
    - HCAL 8000 Hits/BX
    - ECAL: 150 Hits/BX
    - TPC: 400 Hits/BX
    - VTX: 3 Hits/cm²
    - × 10 for Low P option on some det
      - if kept redo for SB2009
  - Missing: “pure beam” background

Subdetector	Channels [10^6]	Occupancy [%]	Data volume [MB]
VTX	800	1.0	50
TPC	2	< 0.1	12
FTD	1	9	2
SIT	1	30	6
SET	5	1	1
ETD	4	10	7
ECAL	100	< 0.1	3
HCAL	8	1	(DHCAL: 20) 130
MUON	0.1	< 0.1	≤ 1
LCAL	0.2	70	4
BEAMCAL	0.04	100	126
TOTAL	≈920		≈340

TABLE 5.1-1
Data Volume in MB per bunch train for the major ILD detector components

max thoughput of 20 GB/s with margins
(✔ : ~ follows Moore's law)

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DAQ After the LoI

- Improved estimation of BDG
  - What security margin should be kept wrt bgd estimation ?
    - vs. additional cost for full det (FCAL, VTX, SIT), or small part of CALOs
    - beam-beam predicted bdg (Pair prod)
    - beam “unpredicted” beam bdg (check progress of BDSIM).
- Estimation of rates based on more detailed set-up
  - ASICs occupancy
  - **ASIC Pipeline length ← ⚠ Loss of ℒ or acceptance**
  - Topology (Data concentration & redundancy)
  - Noise & Calibration data
- **Power-Pulsing in 4T field**
- Cost estimate
- Develop Commons:
  → Combined TB programs

1. Continue **R&Ds on critical components** to demonstrate proof of principle.
2. Define a **feasible baseline design** (options may also be considered).
4. Develop a realistic simulation model of the baseline design, including faults and limitations.
…
8. Simulate and analyse some reactions at 1 TeV, including realistic higher energy backgrounds demonstrating the detector performance.
9. ***Develop an improved cost estimate.***

- ASIC communication ? Daisy chain vs I2C vs …
- FE communication ←→ DAQ
- DAQ code, data formats, synchronsation procedures, …

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AIDA for TB and DAQ

- Successor of EUDET (→ end 2010) and DEVDET († 2009)
  - *AIDA targets user communities preparing experiments at a number of key potential future accelerators*
  - submitted in December;
    selection: April/May → funding in december
  - 9 Work packages ⊃ joint research activities (RTD)
    - WP3, task 2 & 3: 3D Interconnection & Shareable IP Blocks for HEP
    - WP8 (Improvement and equipment of irradiation and beam lines): Coord. T. Behnke
      - Task 6.1: “common DAQ infrastructure”: coord. V. Boudry & D. Haas (UniGe)
        → toward combined TB (Pixel + Tracking + SiTr + Calos)
        Synchronisation of systems (HW [Clk & signals], SW)
        - *Experience from EUDET Telescope + MANY*
        - *Implicated: CNRS-LLR-LAPP, RHUL (CALO), UniGe, Bristol(Pixel), Lund, ULB (TPC) IFJPAN, TAU (FCAL), CNRS-LPNHE (SiTr)*
    - Critical for many groups: CH, UK
      - esp. EUDET telescope / EUDAQ

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LCTW09: LC TB WS in LAL (3-5 nov 09)

http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=3735

- Plans summarized for all LC R&D
- Talks on DAQ integration: VTX, TPC, Calo + summary
  D. Decotigny, M. Killenberg, D. Haas, M. Wing
  - 1st attempt in AIDA call
    - 1st task = evaluate the situation and needs.
    - 1st meeting yesterday in ILD WS pre-meeting
- *→ Convergence on HW & SW, data formats for combined TB*
  - *Synchronisation Units (TLU), Beam InterFace card*
  - *EUDAQ, Calice (XDAQ + DOOCS + Tango),*
    Slow Control (⊃ DB for management of ½ MCh]
  - *All data storage in LCIO (⊃ RAW) ?*
  - *Philosophy = "BE LAZY" scenario aka follow "minimal action" path*
- *Interface to the TB facility → standard API for recording of beam conditions*

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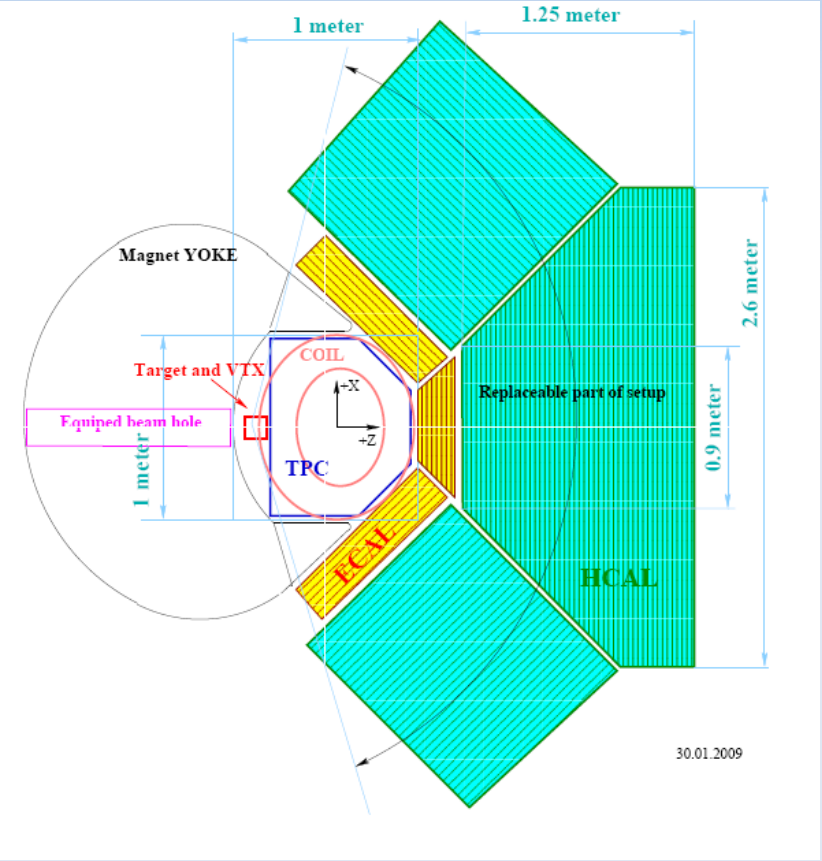
EUDET meeting

http://ilcagenda.linearcollider.org/conferenceOtherViews.py?view=standard&confId=4127

- Goal for combined TB
  - PFA testing:
    - far from obvious without very extended setup
    - Requires improved GEANT4 Hadronic models & thin target data
  - Test of key techniques
    - VTX scales
    - Reconstructions techniques
      - Separation in pseudo-jets
    - Improvement of Simulation
  - Mutualisation & cooperation
  - Better demonstration of performances



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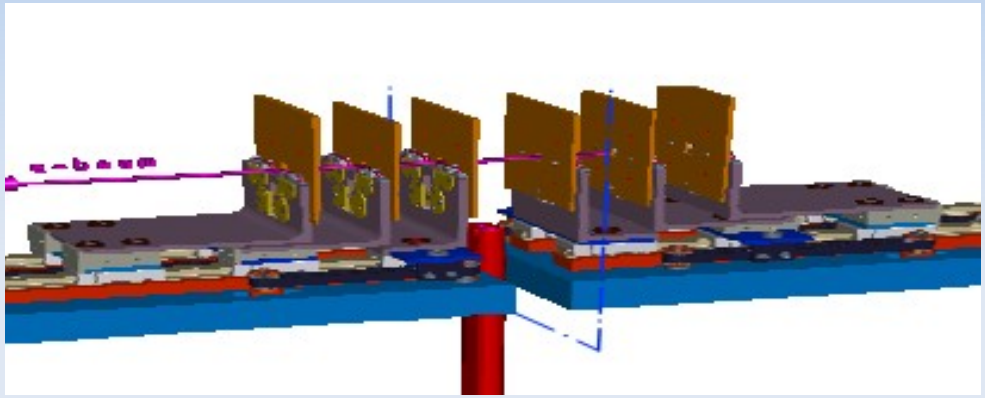
Status of Pixel / EUDET telescope

- *Pixel Sensors tests done practically in the EUDET telescope*
  - ***EUDAQ** complete ACQ framework*
  - ***TLU**: generic Synchronization Unit*
- *Man power critical*
  - *1 person on DAQ (UniGe)*
    now future depending on AIDA
    - *→ future of EUDAQ ?*
    - *Long and successful experience in combining devices*



- *Sensor: Mimosa26*
  - *10.6 × 21.2 mm², 576 × 1152 pixels, ∫dt = 115 µs*
    100 MB/s chip → ~ 10 kHz in TB in spill ?
  - *Next version: Ultimate Chip*
    - *200 MB/s / chip × 20 sensors → test for concentration scheme and high BW.*
    - *Work started on fast acquisition in Plume collaboration*

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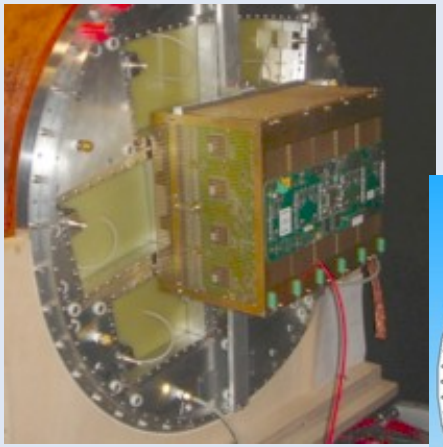
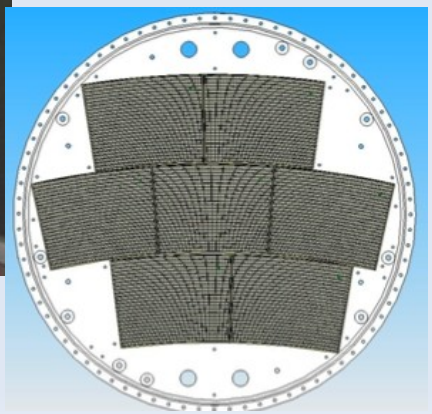
TPC Readout

- Now 2 advanced DAQ for TB, 3 readout electronics
  - (ALICE) ALTRO for double GEMs
    - (8×16ch → FE Card) × 80 → 3 RCU ←opt→ DAQ PC
    - Ad-hoc DAQ (C code on Alice) + Slow Control
    - RAW data online writing → LCIO writing
  - (T2K) AFTER for µMegas
    - (4×72ch → FE Card) ×6 → FE Mezzanine ←opt→ DCC ←Eth→ DAQ PC
    - T2K DAQ writing to LCIO on the GRID
  - Manpower: 3 persons (part time) (Brussels, Lund, Saclay)
- Important effort on the miniaturisation (even for TB!) ongoing
- Plan to test µTCA, test EUDAQ
- For ILD
  - 10 cm for RO electronics
  - Clock precision ?





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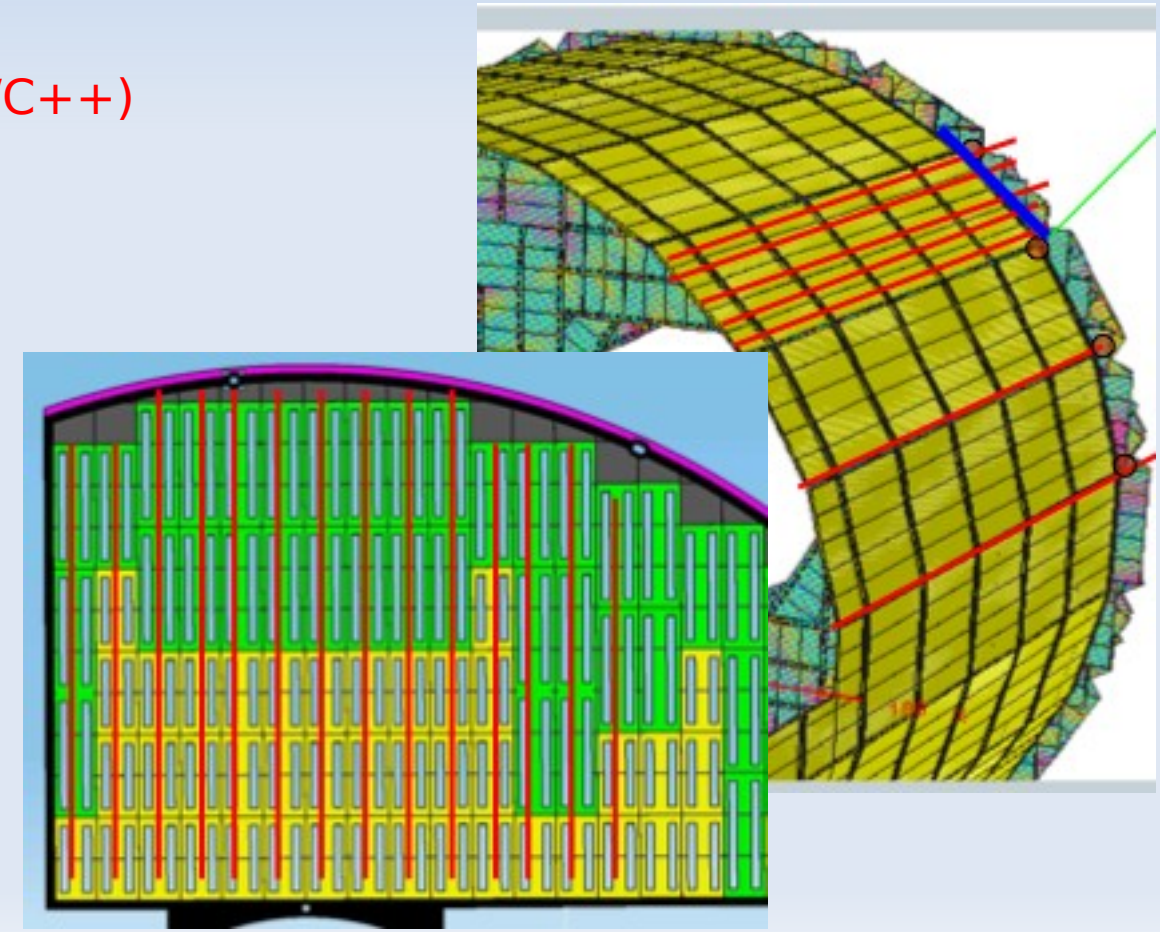
Si Tracking

- 4 ≠ types of sensors → RO chip
  - Va1 chip → SiTr130_128
- 2560 ch (today) → 15kch (mid 2010) → much more in 2011-12
- DAQ
  - NARVAL Framework (ADA/C/C++)
    - support in LAL
  - Slow Control by ENX
  - Custom HW toolkit box
    - Sync and more...
  - Manpower: 1 person (LPNHE)
- Reflexion on ILD ∫ started
  - Chaining of chips
  - ⚠ Power pulsing in 4T



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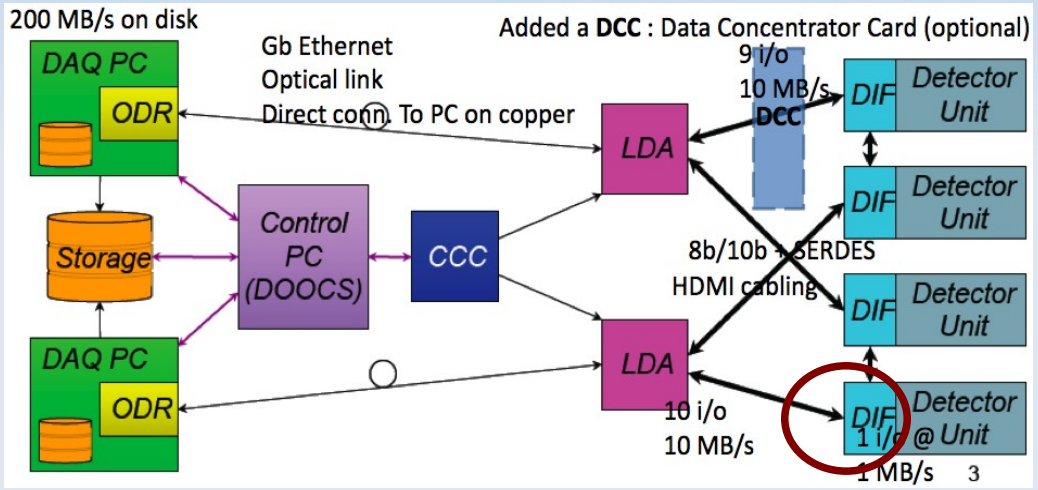
Calorimeter

- Calice DAQ
  - Vers1 used in TB (ECAL, AHCAL, Muons)
  - DAQ2 being developed for more modular & embedded ASICs readout
    - "ROC" ASIC familly & DIRAC chip
    - As prototype for ILD DAQ
      - all on 1 cable
    - To be fully ready end 2010
      - Reduced vers in June
      - DHCAL then ECAL, AHCAL
    - Working modes:
      - Triggered or ILC-like
      - test of Power Pulsing
    - General SW undecided yet but
      - Pieces of DOOCS, Event building & data format, performances test & simulation
      - **Large working environment in XDAQ** (⊃ with support from expert)



Specific Detector Interface

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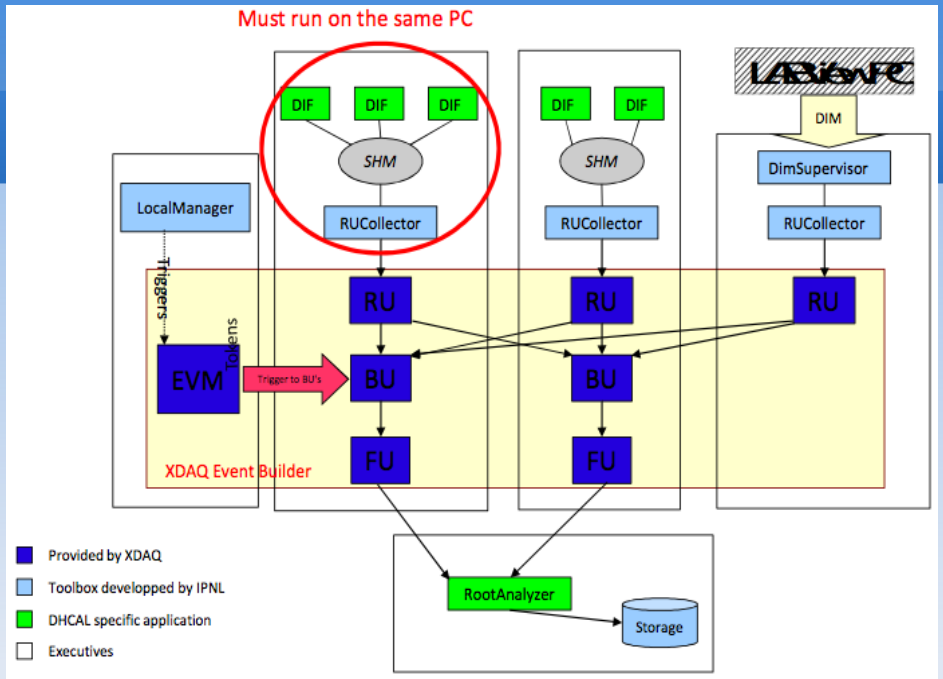
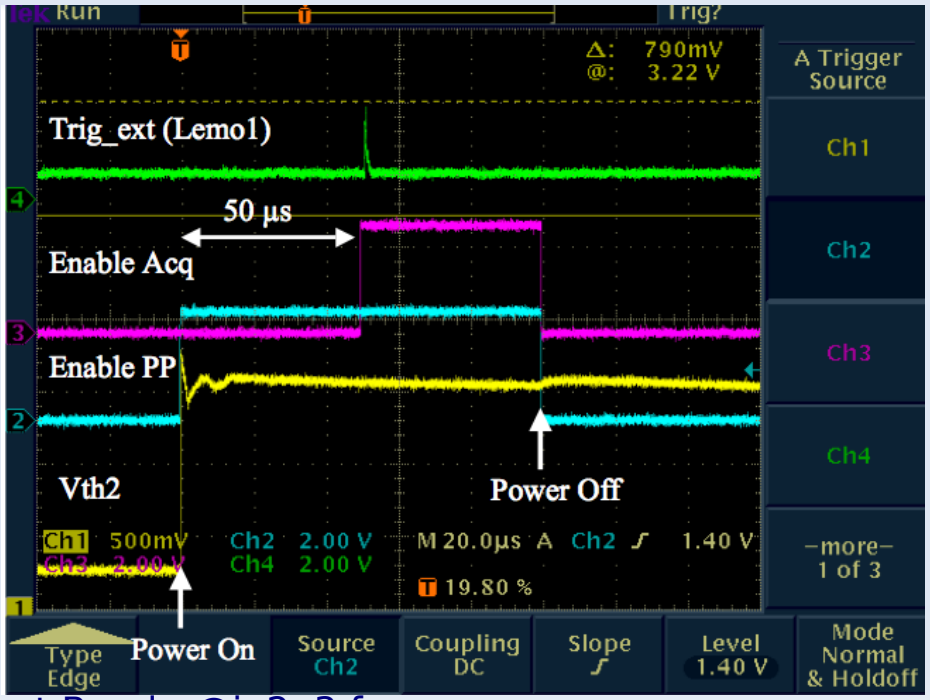
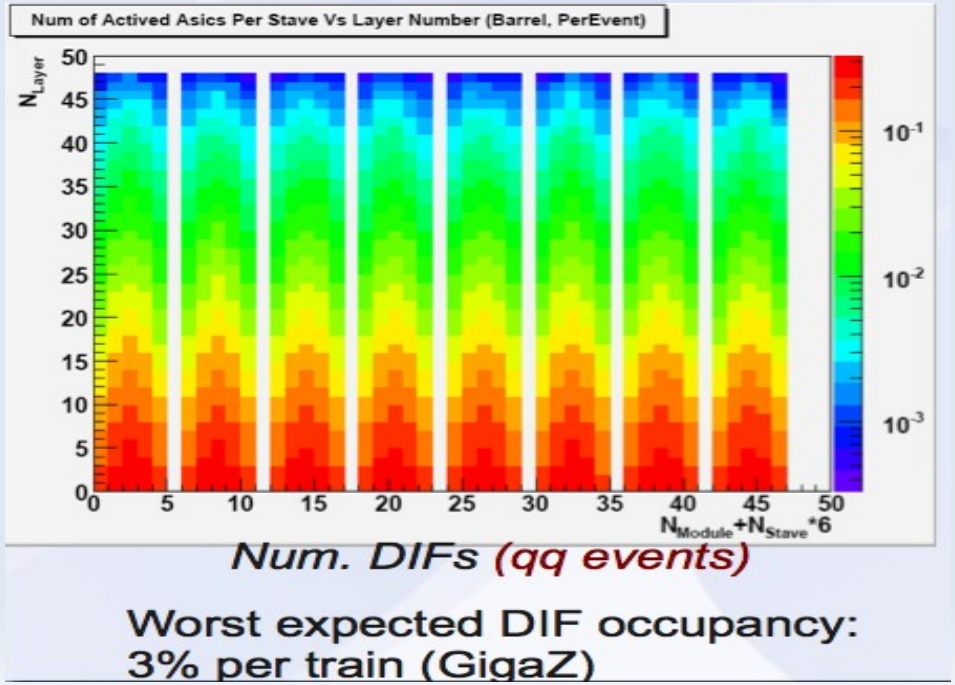
Calorimeter (2)

- XDAQ running for different DHCAL Card format & protocols
  → solution for global integration
- First preliminary results on Power Pulsed readout
  - to be tested in 3T soon





- Simulation of occupancy per ASIC/SLAB



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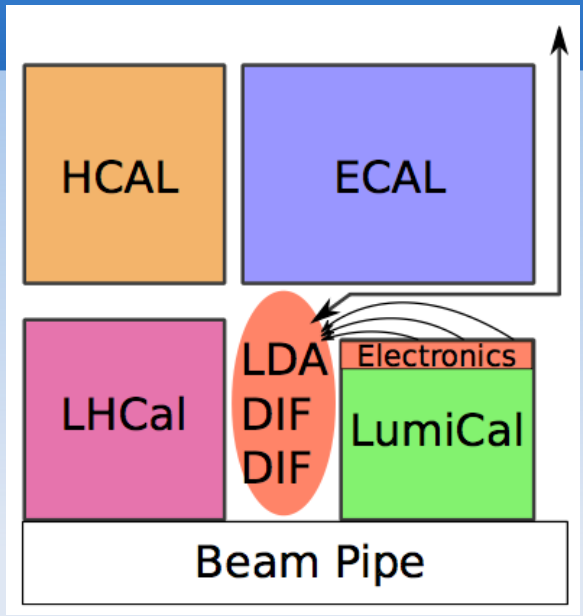
FCALs

- Not foreseen in combined TB
- ≠ detectors, sensors, expected rates (occupancy 1% in LCAL, 100% in BeamCal)
  - FE & ADC ASIC readout by FPGA
    - radiation hardness
  - Recent dev^{t} → benefit from other systems
  - Could be identical to calorimeters
    - DIF + LDA + opt link
    - Higher performances
    - Dedicated fast path for machine tuning
- Studies for ILD
  - Bandwith
    - topology & lowest Power dissipation
  - Placement



- what about radiation resistance of DIF and LDA? Can they tolerate radiation loads in this location?

- data volumes and rates are known
  - in LumiCal: 4 MB/train and 160 Mbit/s or 16 Gbit/s
  - in BeamCal: 130 MB/train and 5 Gbit/s
  - BeamCal fast feedback: 80 B/bx and 1.6 Gbit/s
  - in Pair Monitor: 3.2 MB/train and 128 Mbit/s

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Path on TB combined DAQ

- Work on comparison of various system in view of combined TB has started
  - Sharing of experience will lead to avoid duplicated work and re-use of material / code
  - Manpower is scarse
  - Follow the least effort path
    - keep slow controls SW pieces
    - Exchange of basic SW signals + merging of data fluxes (most based on LCIO)
    - Trigger, Clock & Busy distribution/collect HW exist, must be interfaced
- Possible in 2012 ?

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Some ILD DAQ open questions

- Technological choices & constraints
  - Time precision needed (clock distribution) per detector
  - Data Concentration topology & technology
    - Redundancy of data/config paths ?
    - Ethernet / fibre / custom ?
    - Power distribution & local power storage
    - Power pulsing constraints in a 4T Field
      - Specifications for cables & power route on PCBs
  - Grounding & EMC (ILD & TB)
  - Fault tolerance
    - Local storage of HW configurations → PROM
      - Checking of loaded config auto recovery in case of default ?
    - Busy handling (e.g. memory full)
  - Use of FPGA or ASICs in FE ?
    - Rad Hardness / Power dissipation / price

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More open questions

- Central DAQ
  - Reconstruction etc: not yet critical but not to be forgotten
  - Price of Farm & storage
  - Load balance: Switches → UDP as a data packet format ?
- Central DB
  - Geometry mapping vs. HW configuration Database(s)
  - Automatic handling of noisy channels almost necessary
    - *Noise is our absolute ennemy*
    - Central / Local / Semi-local ? If local → more complex FE
- RAW data format storage :
  - Per bunch train
    - TPC integration time / recalibration
    - Possibility of analysis for long living particle decay

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