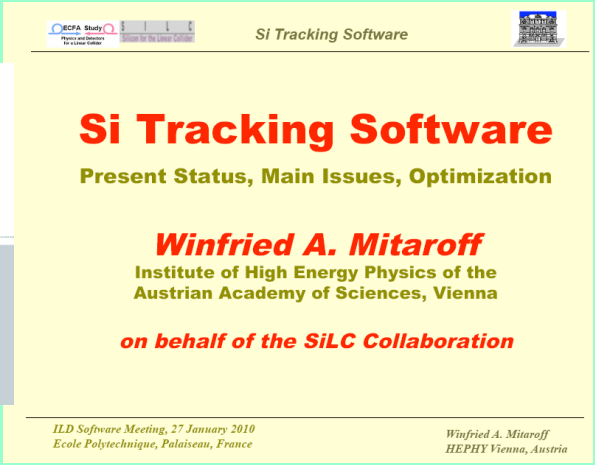
ILD Silicon Tracking system

A. Savoy-Navarro, Université Pierre et Marie Curie/CNRS-IN2P3

Based on the ongoing R&D work by the SiLC Collaboration.
Also to be included as contributions to this Workshop:

Preparatory Meeting for ILD Workshop

Contribution to the DAQ pre-Meeting (A. Charpy)



Contribution on behalf of SiLC to the Simu pre-Meeting (W.Mitaroff)

IVth ILD Worshop, January 29, 2010

Les Cordeliers, Université Pierre et Marie Curie, Paris

Main topics on the 2012 roadmap for the ILD Si tracking system

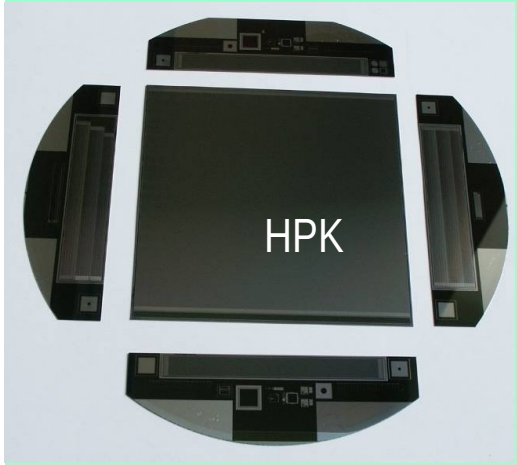
- Sensors
- FE Electronics
- FEE/ sensor direct connection

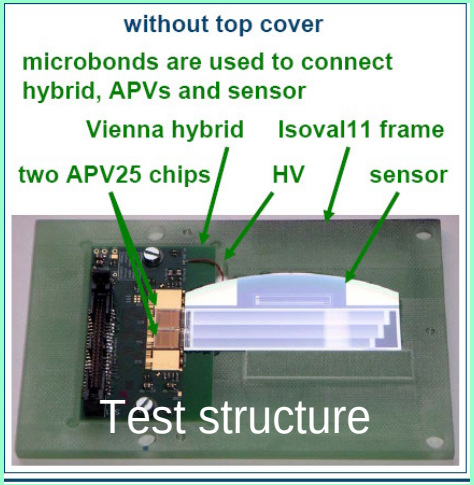
- Associated DAQ chain -> global DAQ system
- Mechanics & Detector Integration issues
- Test bench and test beam inputs
- Detailed simulation developments
- Work plan for 2010-2012

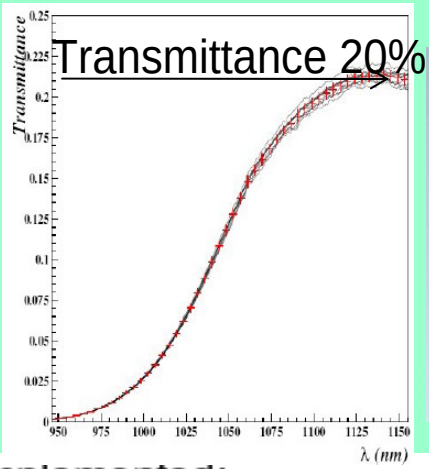
  also Keeping an eye on longer term future => Beyond Baseline

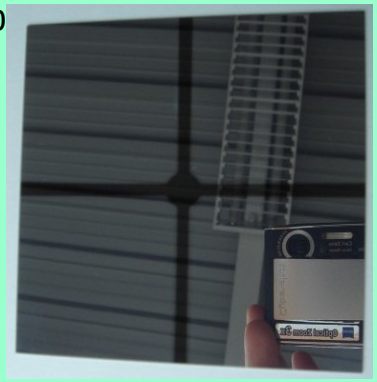
Silicon Sensors

- **Baseline**: strip sensors, 8'', 200 µm thick, 50 µm pitch, alignment friendly (a.f.) with 70% transmittance & active edge options.
- **Present status**: 6'', 320 m thick, 9.15x9.15 cm^2, 50 pitch (HPK) and very preliminary A.F. option (20% measured transmittance)









Fully characterized at Lab and test beam with detailed Test Structure studies

Implemented:

- ∅~10 mm window where Al back-metalization has been removed

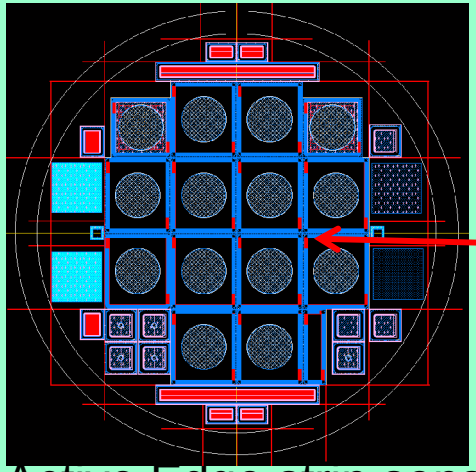
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)

Si sensors: how to reach 2012 baseline

R&D based on developed Lab test infrastructure, expert Labs, Industry, transfer to Industry

1) Next step on standard strips with HPK: 200μ m thick and 6''(8'') *(feasible)*
2) Developing more performing A.F. strips: R&D IMB-CNM and IFCA-CSIC

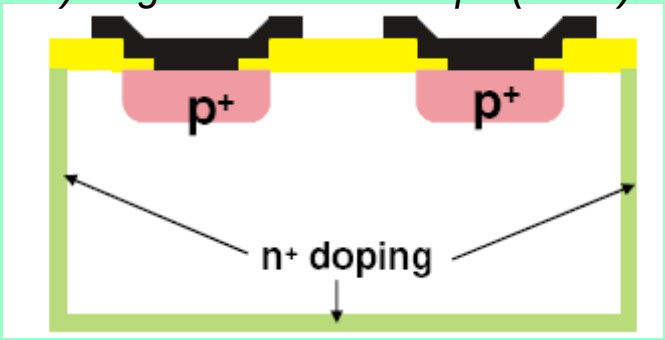


Very detailed simulation studies
Design and production of baby-sensor prototypes with optimised transmittance: 70%
First batch produced by CNM, under test by IFCA:
Promising first results. R&D pursued at least 2 more years.
Once technology is fully proven, transfer to Industry

Looks in good shape and feasible by 2012

3) Active Edge strip sensors: two research lines under investigation

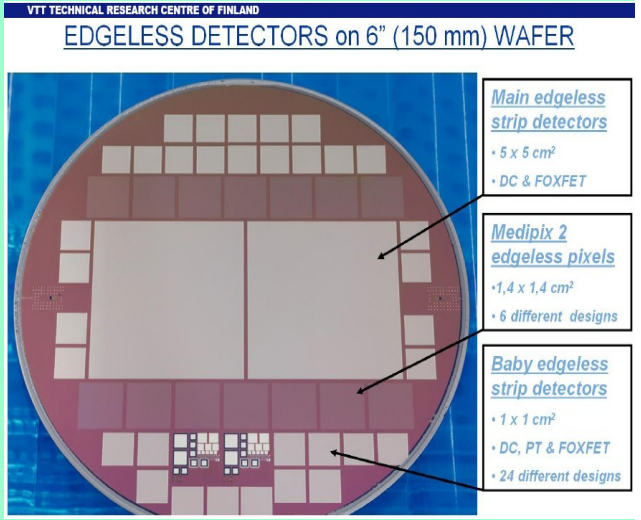
i) Edgeless Planar strips (IRST)



2.5x5 cm2 proto sensors by Spring 2010

ii) Edgeless SOI strips (VTT)

Full electrical tests
5x5cm^2 sensors
Look very promising

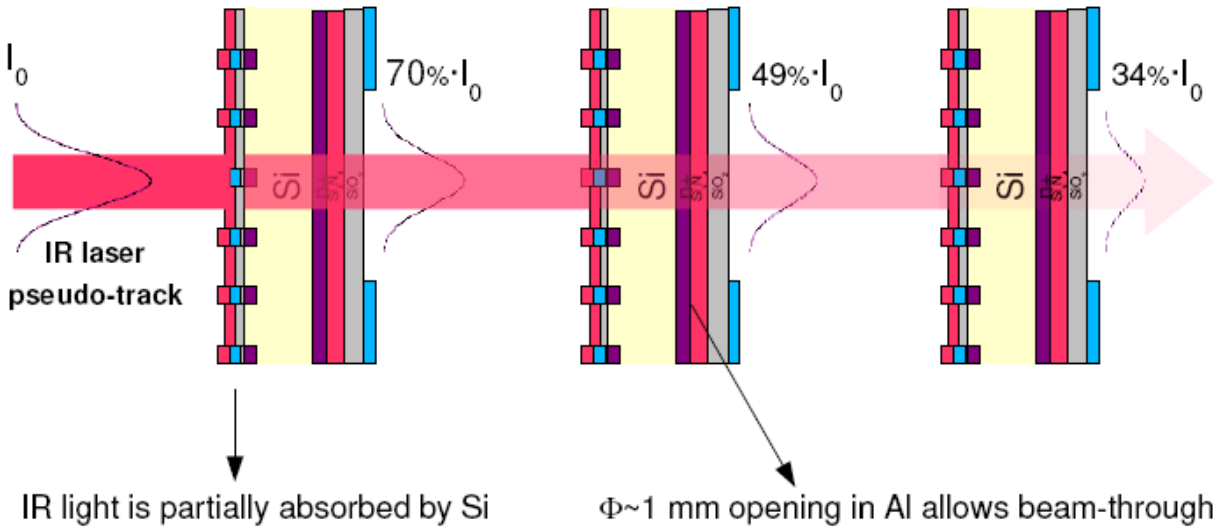


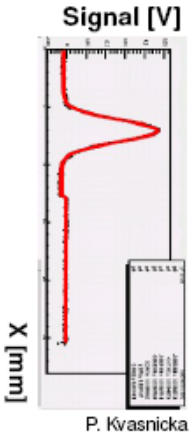
Once R&D is achieved and techno proven: transfer to Industry

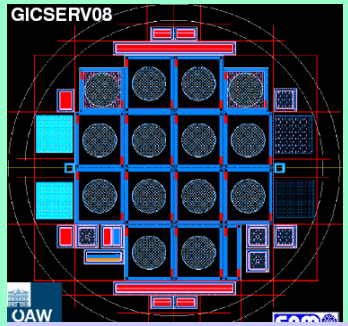
Latest on A.F. sensors developments

report by M. Fernandez at IXth SiLC meeting-Paris

• Aim: align Si microstrip sensors using IR laser tracks







- 5+1 wafers
- 12 µstrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50 µm RO pitch (25 µm interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3,5,10,15 µm)

• Higher %T ⇒ simpler implementation of the system:

Transmittance	90%	80%	70%	60%	50%	40%	20%
Traversed	30	15	10	7	5	4	2

SiLC HPK

• System features:

– Laser intensity~200 MiPS ⇒ **sharing same DAQ as Si detector**

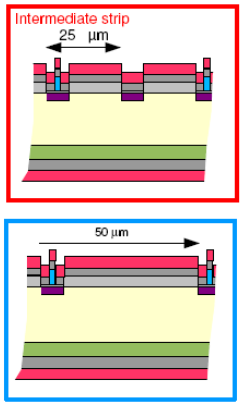
– Silicon modules are directly monitored, **no external fiducial marks**

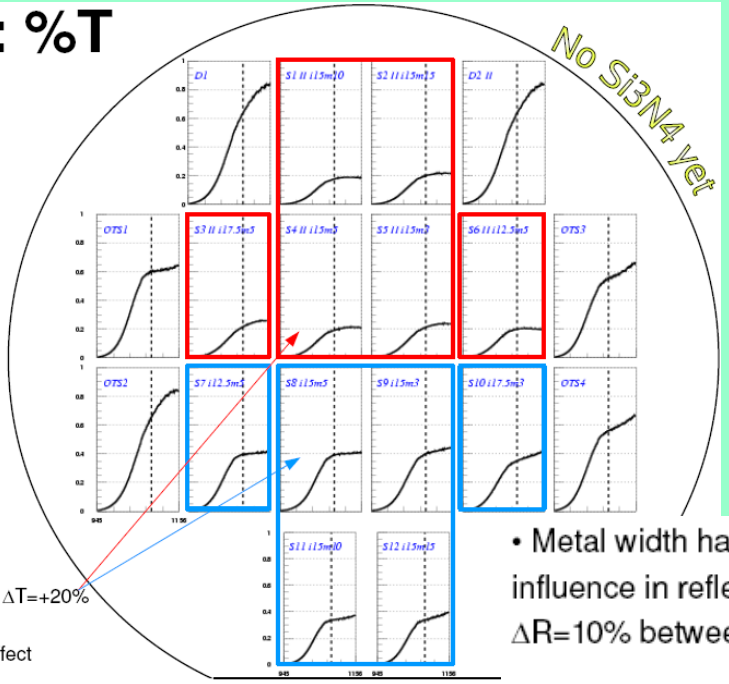
Latest on A.F. sensors developments

report by M. Fernandez at IXth SiLC meeting-Paris

Wafer 1:: %T

measured



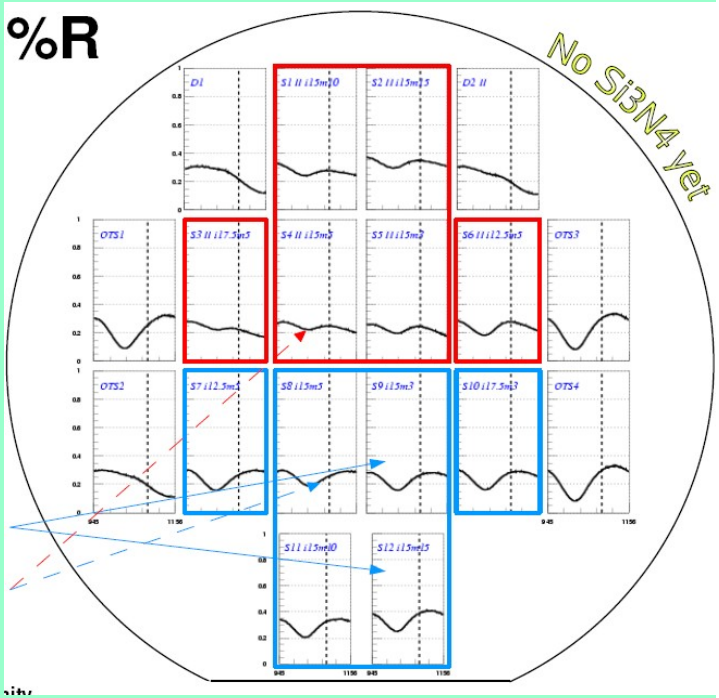


- T~70-80% test structures
- No intermediate implant ⇒ ΔT=+20%
- Metal width:
  [3-5] µm: second order effect
  >10 µm: ΔT≤-5%

- Metal width has higher influence in reflectance: ΔR=10% between [3-15] µm

- Removal of intermediate implant does not double %R (as it did in the %T case)
- **⇒ %R linked to Al width while %T related to uniformity**

%R



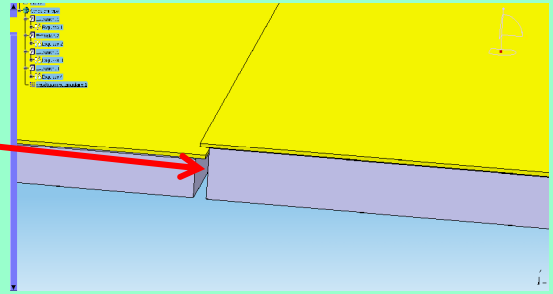
Promising results: R&D foreseen until end 2011, then transfer to Industry

Edgeless strips sensors: Why?

Edgeless sensors decrease the non active edge regions of sensors (usually of a few hundreds of microns) down to about 10 to 20 µm.

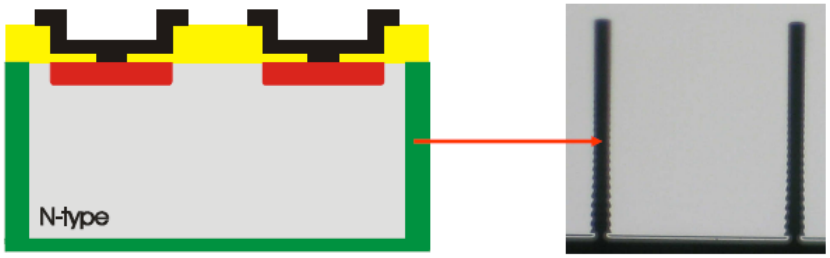
Our interest in edgeless or active edge sensors is motivated by:

- ✓ allow building large area Silicon trackers seamlessly tiled detector matrices,
- ✓ thus no need for sensor overlap
- ✓ easier to build
- ✓ decrease of the material budget
- ✓ improvement of the tracking performances both in momentum and spatial resolution.



Two solutions based on the edgeless strip based on Edgeless planar and Edgeless SOI technologies are pursued.

Next steps (2): Planar detectors with active edge



- Trench etching steps investigated on test wafers
- TCAD simulations for breakdown prediction
- Layout complete (p-on-n, mainly strips)

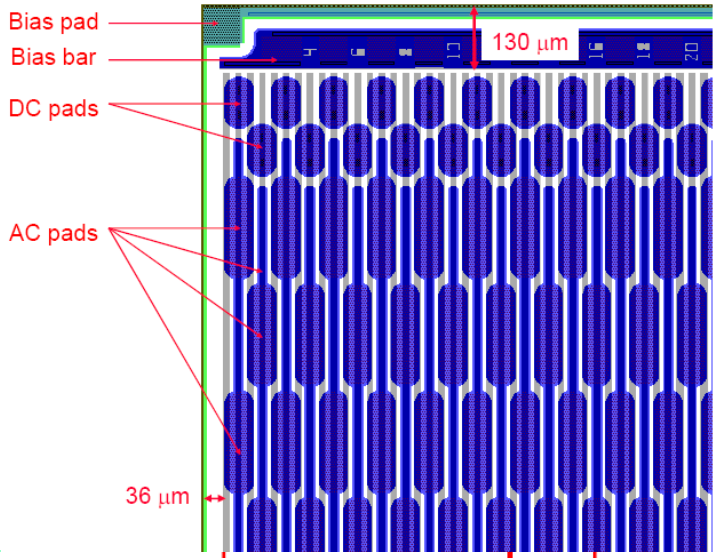
From Gian Franco's slides to IXth SiLC meeting

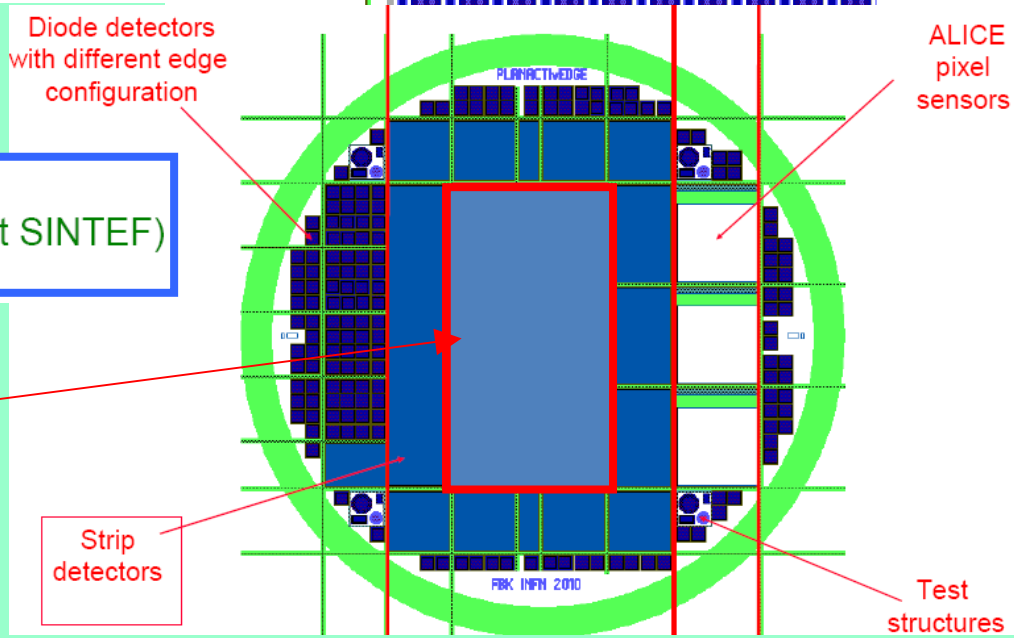
Planar – active edge.
Started, 18 wafers with bonded support (made at SINTEF)
to be completed by March 2010

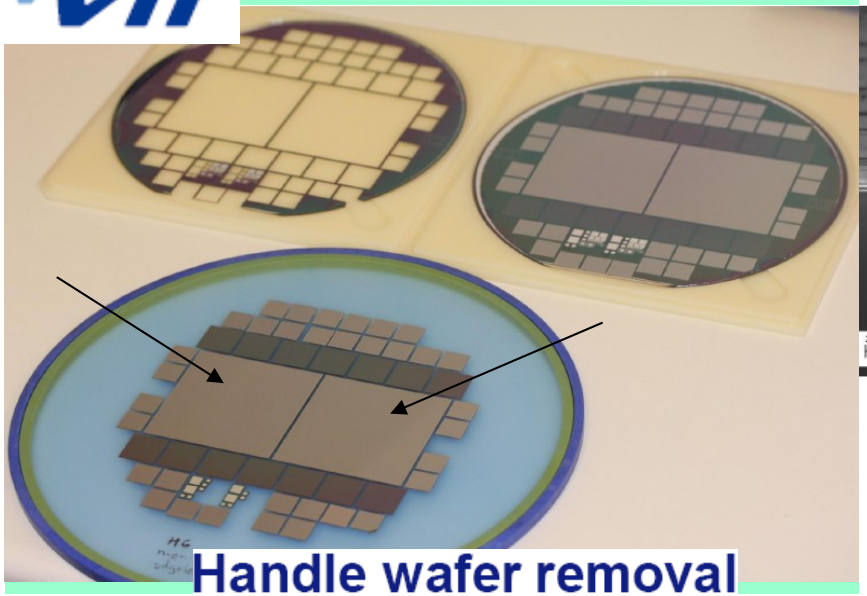
A test module will be built by LPNHE with these new sensors (2x[2.5x5]cm2) read out first with VA1 ref chips, foreseen to be ready for 2010 beam test

EDGELESS STRIP SENSORS

(2.5x5.0 cm^2, 498 read-out strips, pitch 50 μm, with floating strips)

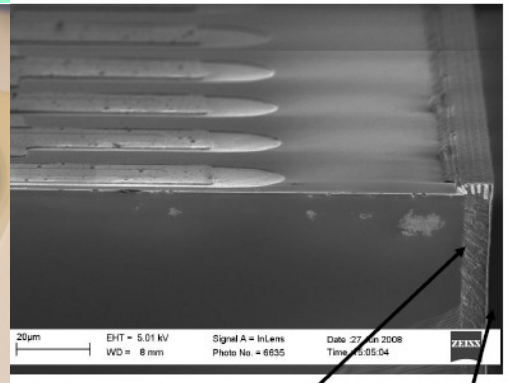


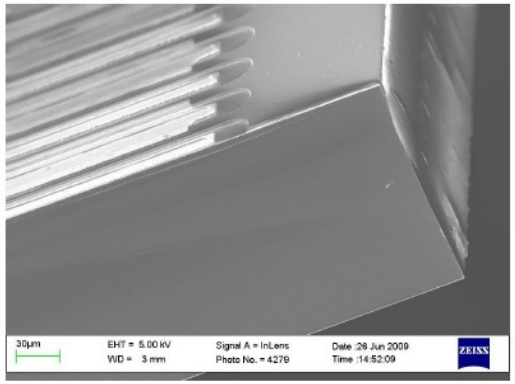


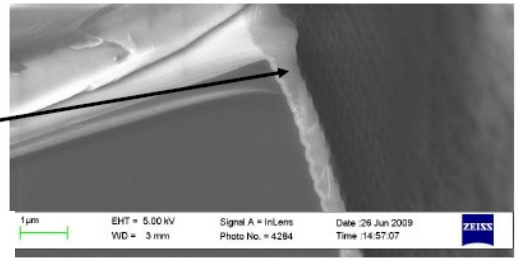


Poly process

Edge implantation







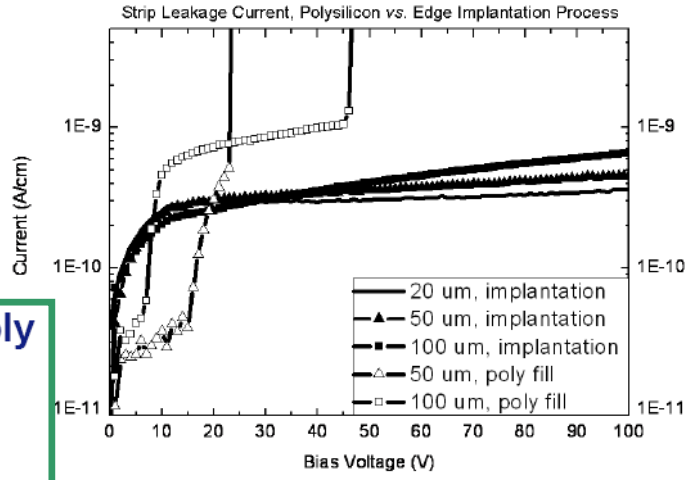
6 um inactive polysilicon

500 nm oxide

Handle wafer removal

3D PROCESSING WITH ALTERNATIVE PROCESS

- No need for polysilicon filling, planarization and separate ICP dicing
- Fast process and no bowing of the wafer
- Detector edges sustain handling – no edge cracking
- Physical inactive edge region <1 µm
- Requires non-planar lithography -> readiness available at VTT



Strip leakage current: p-on-n implantation vs. poly

- Low leakage currents for both process approaches
- Very early breakdown voltages for poly filling
- Leakage current depends on the active edge distance

Juha just brought with him the 2 first 5x5cm^2 sensors at LPNHE

From Juha's slides to IXth SiLC meeting

FE & R.O Electronics

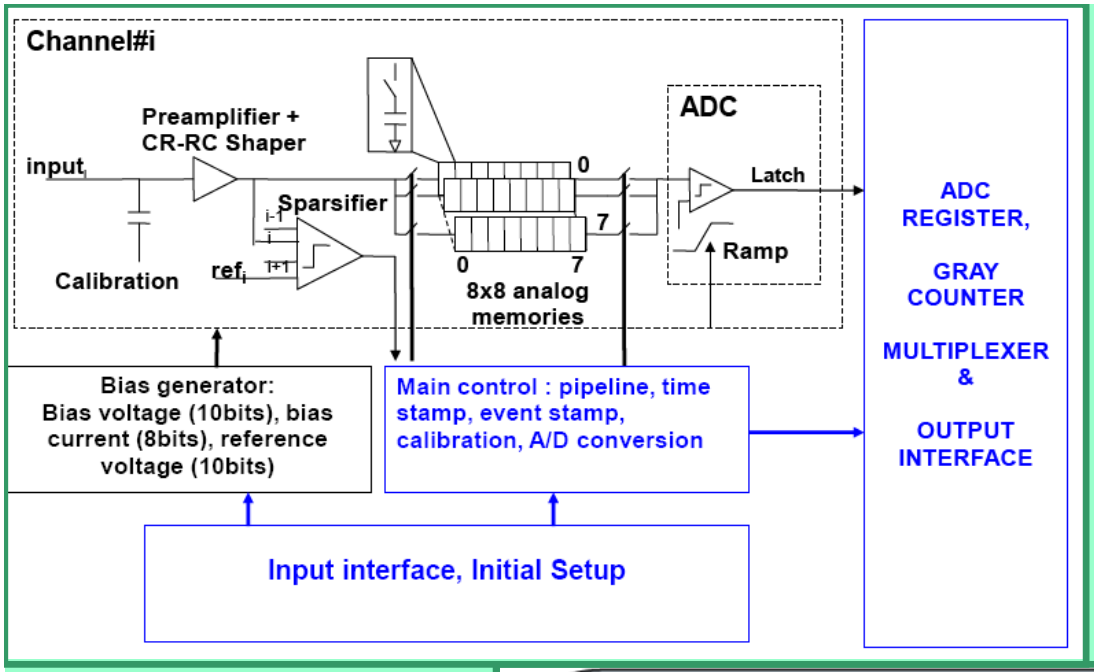
- **Baseline**: *mix-mode analogue & digital SiTR design, in 90 nm DSM technology, blocks of 256 channels, direct connection with strip sensors, connection to DAQ (cabling, signal transmission), time stamping.*

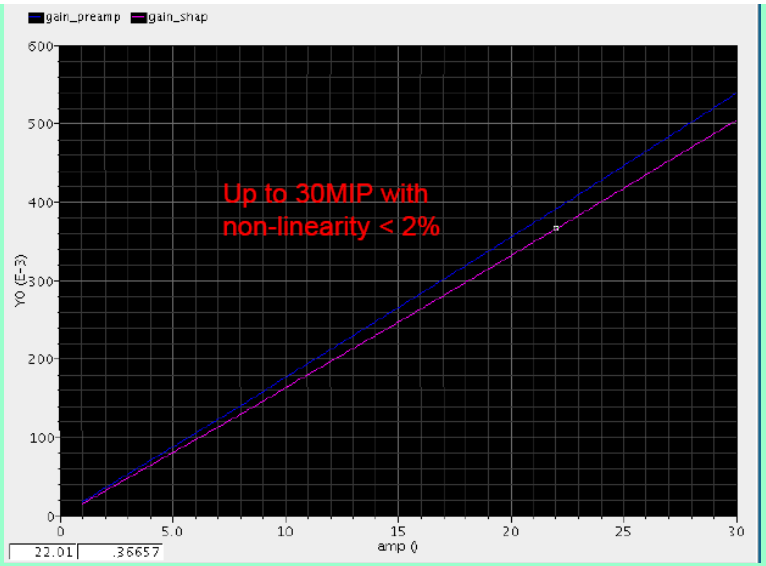
- **Current status:** in preparation, SiTR_IBM-128, 130nm IBM, to equip a large number of test beam prototypes.
  - Preliminary versions with various levels of design integration produced and tested:
  - SiTR_180 (VFE), SiTR_130-4 (all analogue+A/D), SiTR_130-88 (full mix-mode design)
  - SiTR_130-128: *available end 2010 for equipping Si tracker prototypes for test beams.*

FE/ RO Electronics: how to reach 2012 baseline

ROADMAP ON ELECTRONICS

- Go to 256 channels => block of 8x256 in one
- Go to 90nm CMOS techno
- Thinning 50 μm
- **Direct connection FE-chip onto strip sensor**
- **Connection to the DAQ (serial/parallel)**
- Connectics and cabling

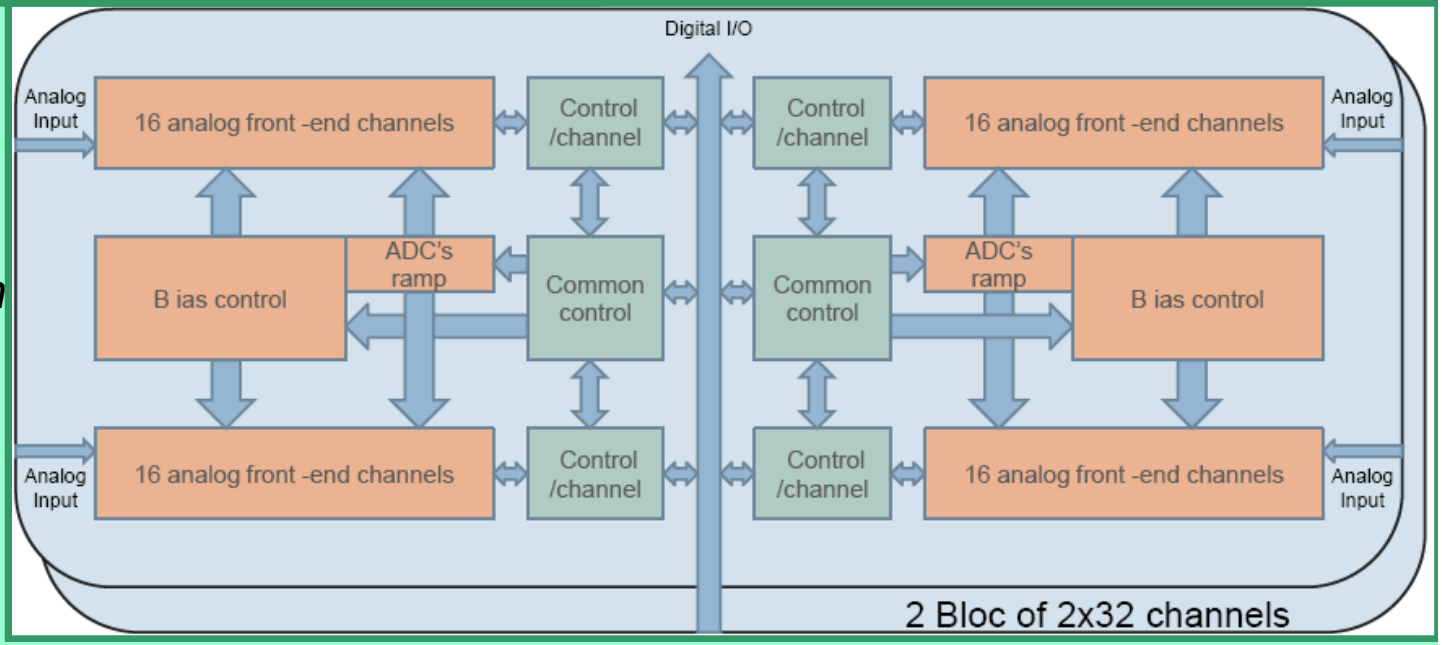




NEW SiTR_IBM130-128

Simulations => better performances than the previous ***SiTR_130-UMC*** *version already within specs*

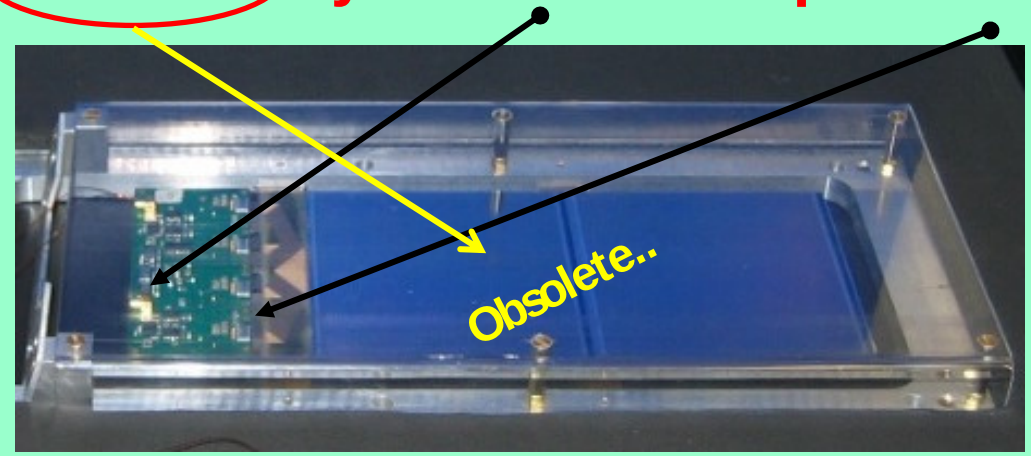
From Hung's slides to IXth SiLC meeting



Direct connection sensors-FEE

Major R&D objective: NO MORE Hybrid FEE board +pitch adapter

Presently:
Module with 2 HPK built for EUDET at LPNHE

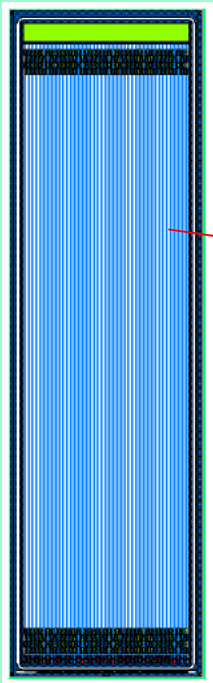


ALL in ONE SOLUTION => direct connection of FE chip onto the sensor

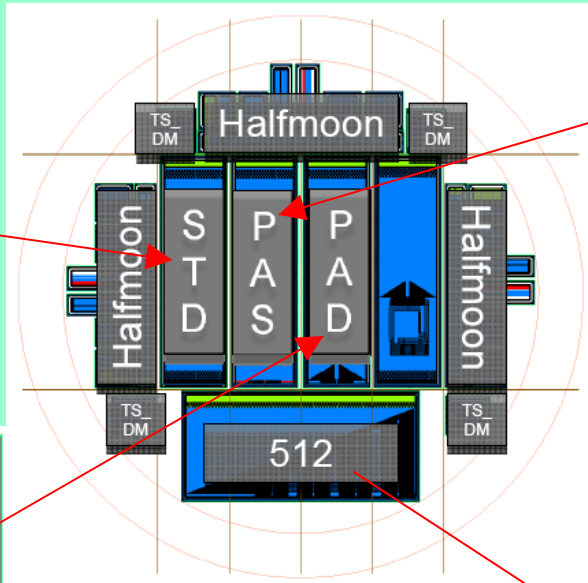
- material budget,
- simplification of elementary module (tile) and
- of overall detector construction (burden put on sensor and FEE chip),
- improvement in performances
- Use high tech advances (cost?)

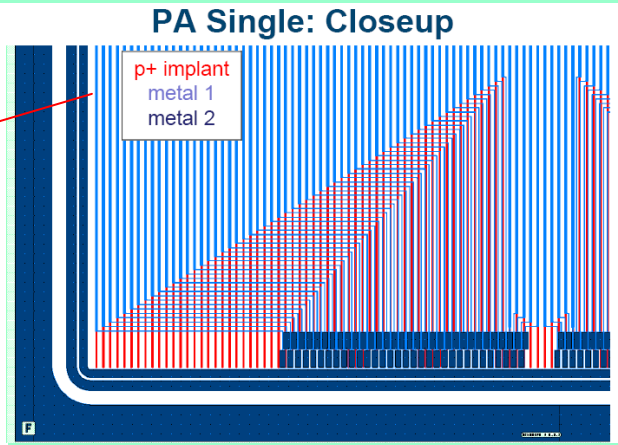
SiLC is pursuing in different steps: wiring onto the sensors: HEPHY + ITE-Warsaw (proto at CERN t.b'09-10); bump bonding in 10-11: HPK+LPNHE (with new FE chip), HEPHY+ITE (tests with APV25); investigating new ways in //: 3D vertical interconnect (part of the worldwide 3D interconnect effort) and **alternative solutions**.

Sensors with integrated pitch adapters

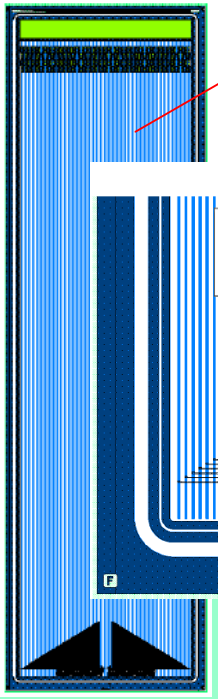


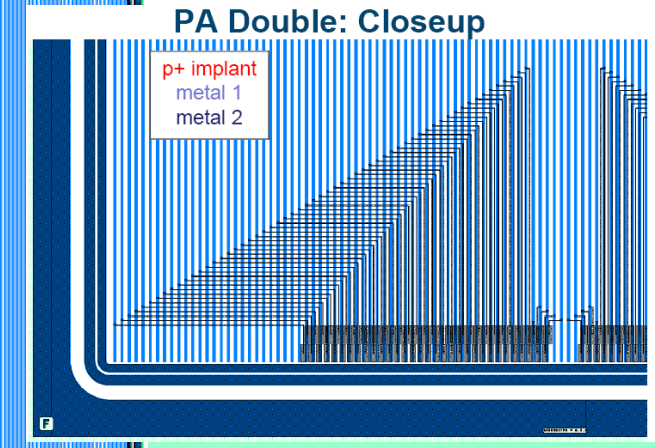
STA=standard





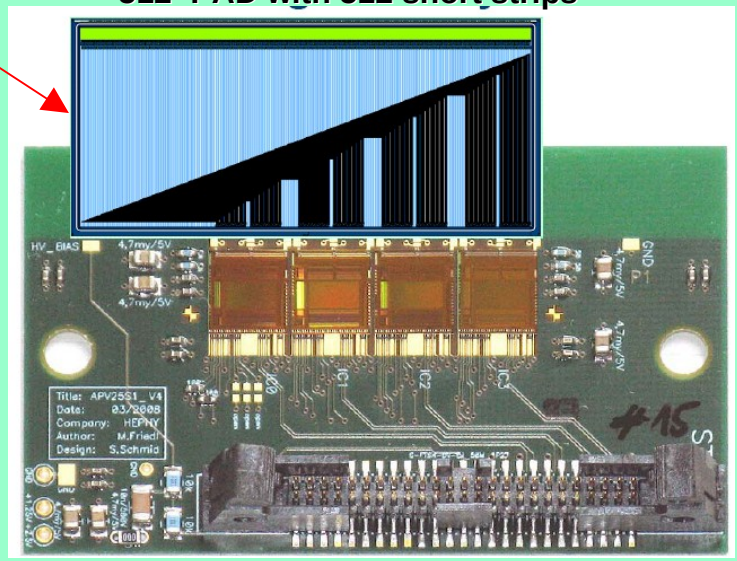
PAS=Pitch Adapter integrated with Single metal layer





PAD=Pitch Adapter integrated with Double metal layer

512=PAD with 512 short strips



From Thomas slides to IXth SiLC meeting

LPNHE
Laboratoire de Physique Nucléaire et des Hautes Energies

DAQ Silicon tracking architecture

A global schematic view of the Silicon DAQ architecture

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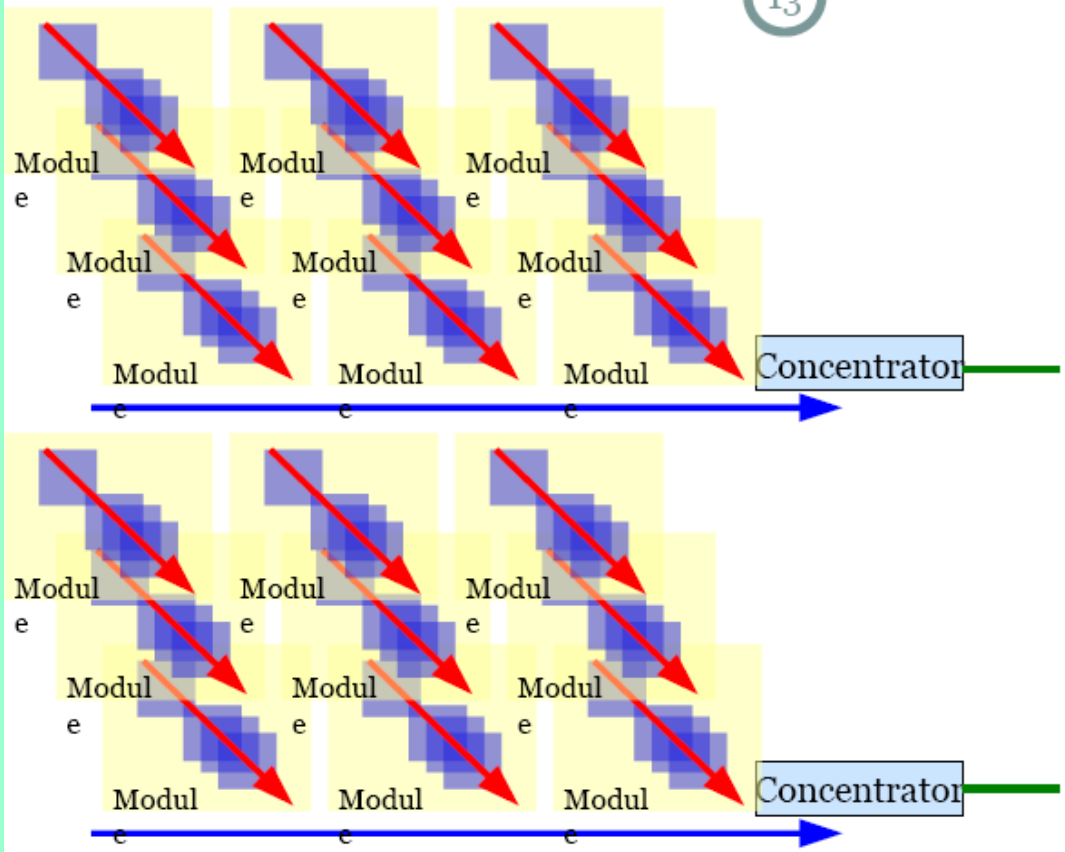


3 "floors":

F1: chip on sensor, full readout chain in a single chip (A/D, zero suppression, multiplex ...)

F2: on detector sides, daisy chains chips, data buffering, preprocessing ...

F3: processing, azimuthal sector, track reconstruction

Si Tracking DAQ – ILC workshop, Warsaw (june 08)

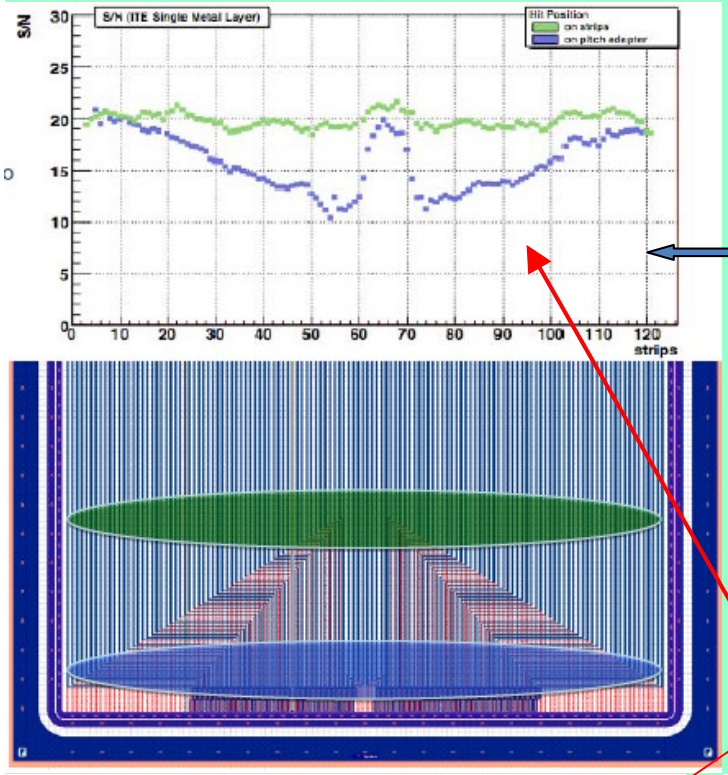
A. Charpy (DAQ pre-Meeting)

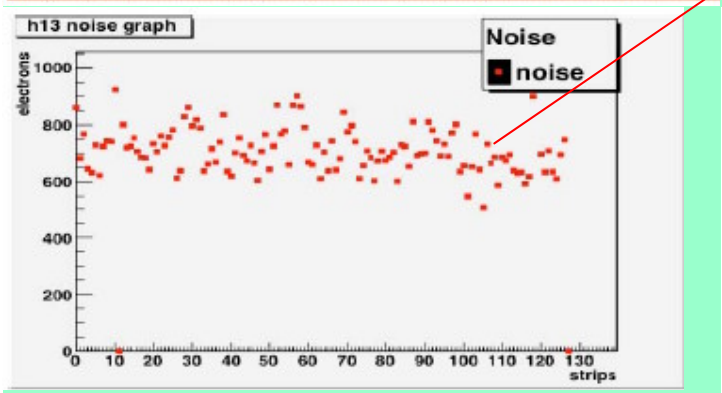
Total number of modules:
500 (SIT) + 2500 (SET) + 2000 (ETDs)
5000 modules of 1792 channels

Total number of channels:
10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)
10×10^6 channels
~5.12 Gbytes

Not taken into account:
FTD data
Zero suppression …

Just starting to work on this item: lot to be done!!





Results from 2009 test beam

Test beam at SPS-beam
2009 → 2010

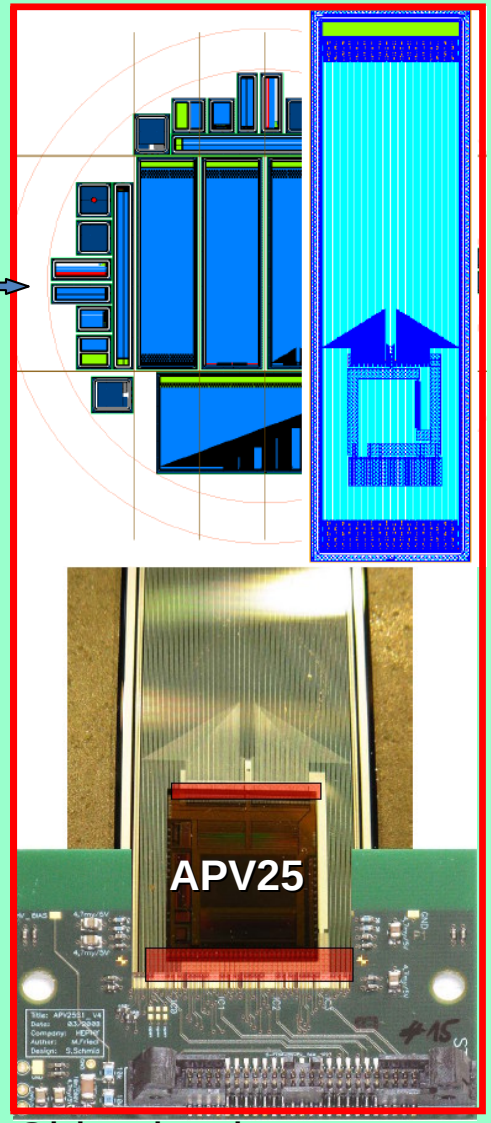
From Thomas slides to IXth SiLC meeting

Not due to noise increase but to signal loss

Reason:

- capacitance of integrated coupling capacitor gets extremely low when metal strip moves away from implant in routing region
- Remody: routing on dedicated, second, metal

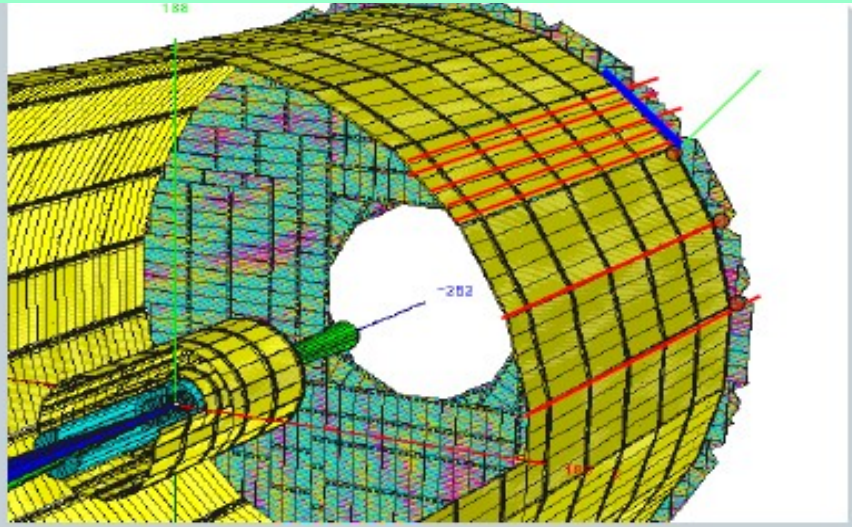
Next: to be tested in 2010



Chip glued on sensor:
wire or bump bonding

Chaining the DAQ sub-elements

A. Charpy DAQ Pre-meeting



- On the "module":
Chaining of 8 SiTR_130-256

- "Super Module":
Chaining the adjacent ladders toward a level 1 concentrator

- Half cylinder ("Detector Element"):
Level 1 concentrator (toward level 2 ?)

- Toward the global Silicon DAQ system by Optical fibers

- Send to Global DAQ system

Depending on the final requirements

Just starting to think about the topology design & how to build the DAQ chain:
***Just getting our nose out of the FEE chip*….LOT to DO: setting of a task force**

Mechanics and Detector Integration

Baseline includes:

- Modules made of planar strip sensors, FEE chip directly connected to strips , light structures and cabling/connectics, easy to build, based on a unique sensor size (but FTD).
- Light support structures
- Alignment systems & cooling included in the Si detector schema.

Optimization => simplified architecture, minimized %X0

Present status: experience & advances gained from:

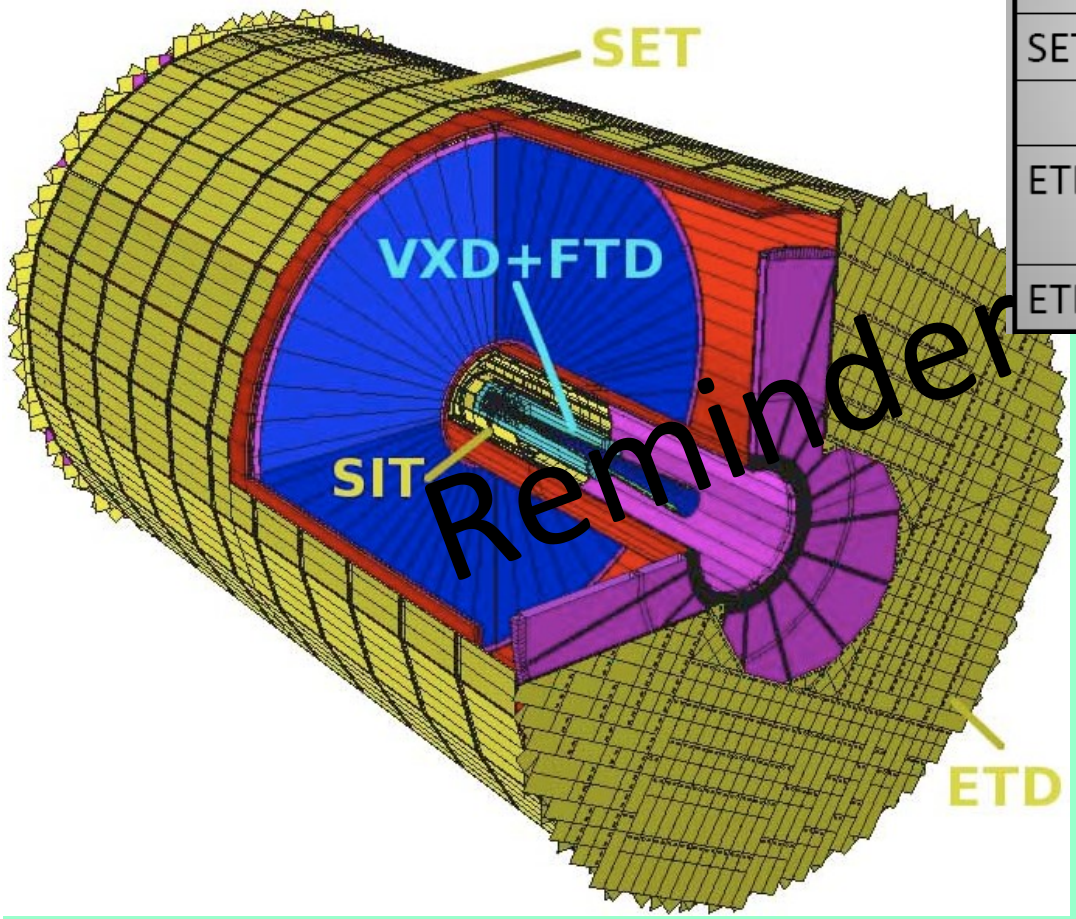
- expertise from LHC R&D and construction
- construction of prototypes for beam tests (SiLC)
- work on the ILD-LOI:
  - => preliminary design of each component
  - => their integration in the ILD detector design
  - => the answers to alignment issues
    - to push pull
    - to time stamping

But still lot of work to do for the 2012 baseline!

ILD Hybrid tracking: *The Silicon Envelope*

(in numbers as currently in the ILD LOI)

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30



Total number of channels:

10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)

= **$10 x10^6$ channels**

Total area:

7 (SIT)+110 (SET) +2x30(ETDs) = **180 m^2**

Total number of modules:

500 (SIT) + 2500 (SET) + 2000 (ETDs)=

5000 modules with same sensor unit.

Unique sensor type (except FTD) but variable length strips wrt module location

GEANT4 simulation **(here) & mechanical design** (CATIA) in progress

Mechanics & Integration: how to reach the 2012 baseline

The to-do-list:

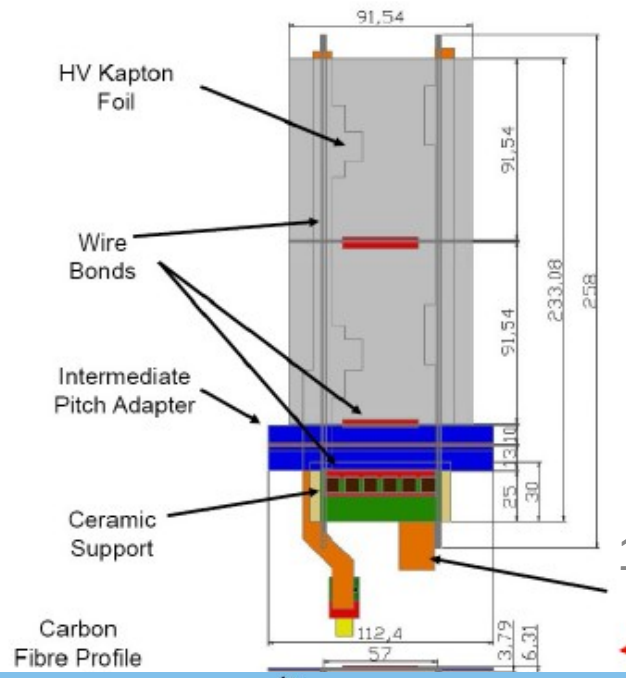
- **Elementary module sensor, FEE & connection/strip, cabling, support structure**
- **CAD design of each components**, including more and more details.
- **Support structure studies**: constraint studies, tests with mechanical prototype
- **Integration in the overall ILD detector**
- **Alignment systems**: laser based (A.F.) with AF sensors for FTD, SIT (SET, ETD?)
  Alignment system for Si components between them and with the other components.
- **Cooling**: to be further evaluated (power cycling real impact and eventual drawback?)
- **Construction lines**: design and development of tools for construction lines appropriate to the detector to be built, even in Labs already equipped for LHC, construction set-up have to be adapted.
- **Push pull** issues to be studied and solved (tests?) but first better defined!

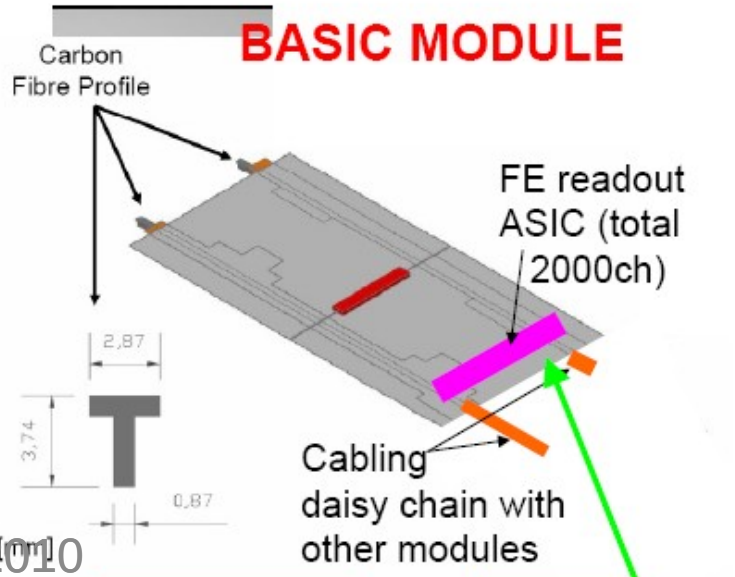
(In red the most critical issues)

➔ *CAD studies, detector prototyping for test beams, mechanical prototypes for dedicated studies, definition of the tools and setting up of the construction lines. Completed in parallel with detailed simulation studies and test beams.*

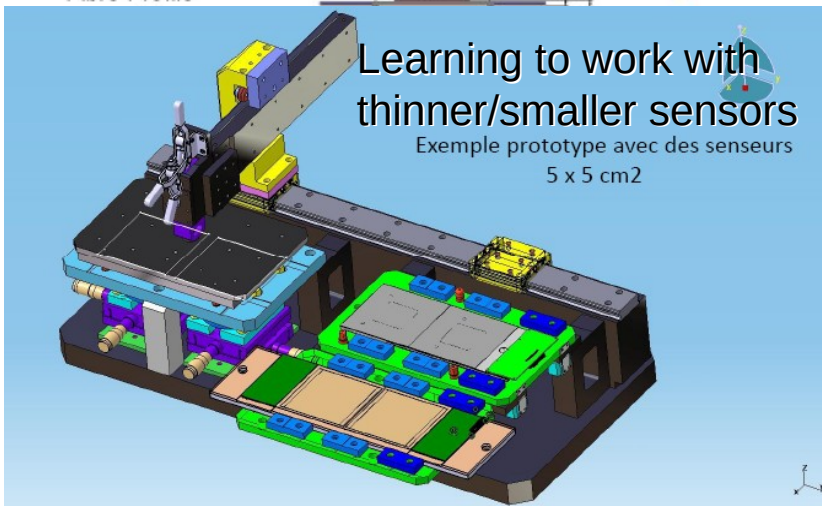
THE ELEMENTARY "TILE":

sensor x FEE chip x connect FE/strips x mechanics x cabling ≤ 0.8% total





1/29/2010



Present status (left) vs next step

DSM-FE readout into one single unit:
- 8-256ch chips

Total size: 8x0.5 cm2

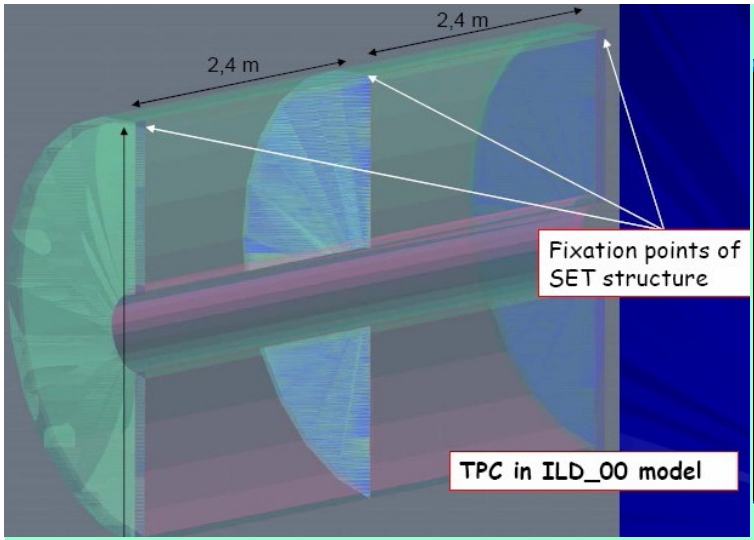
Thinned: 50μm

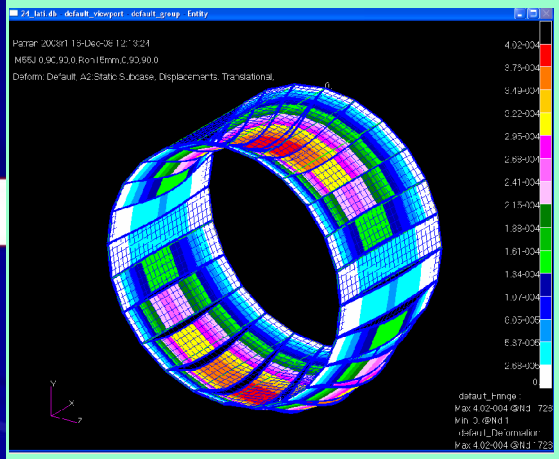
Directly connected onto the sensor

⇒No more pitch adapter,

⇒No more hybrid board

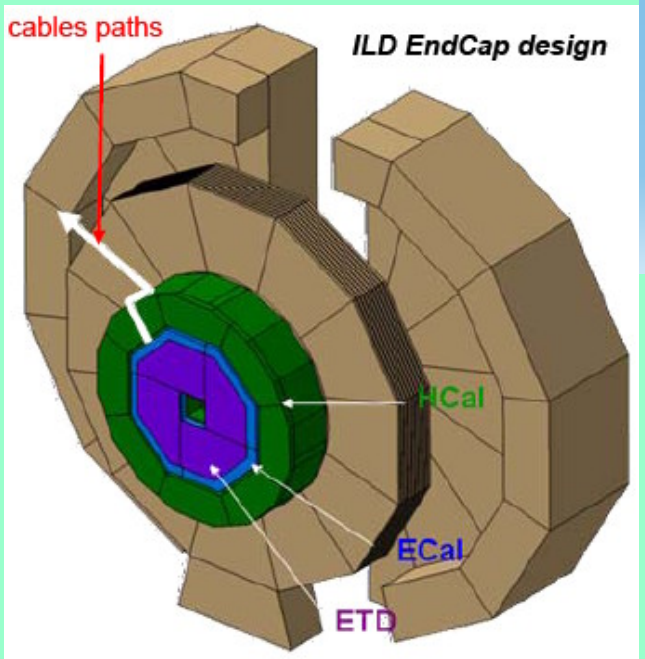
⇒Change in the cabling technology

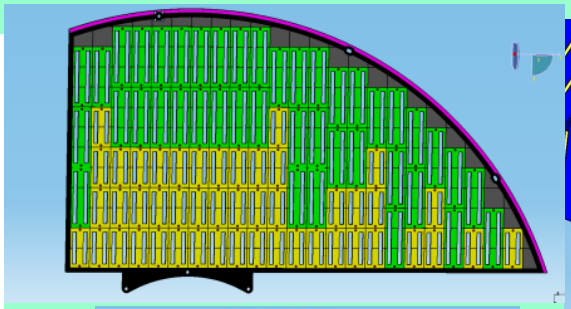


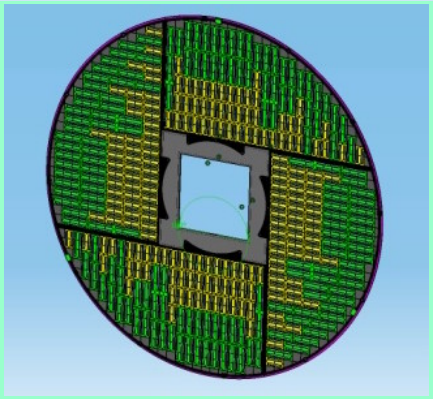


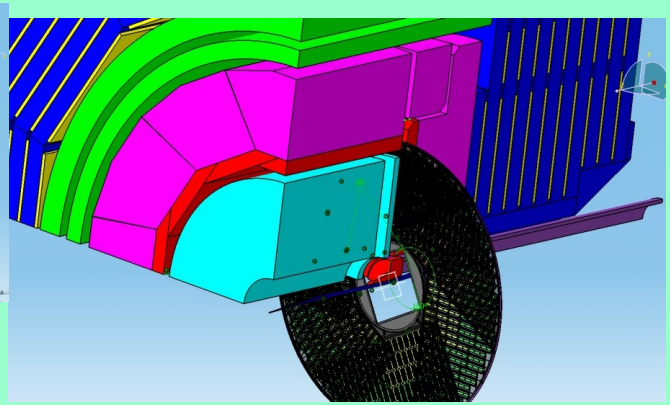
SET/ETD: CAD & INTEGRATION

Restarting work on CAD design of the SET and SIT/SET possible common support (Torino)









Progress made on detailed CAD for ETD (LPNHE)
=> to be pursued with calorimetry and full integration design

SIT/SET/ETD:

- Detector design: good design => to be detailed
- Detailed CAD of support structures, SIT/SET common structure
  (common support structure proposed by Torino)
- ETD: CAD design well advanced to be rediscussed with calo/Mathieu
- Detailed simulation studies to be performed in the barrel with realistic material budget
- Same and much more tricky in the EndCap: (TPC endcap?)
- Alignment: SIT can use the same system than FTD
  not the SET or the ETD (to be studied)
- Alignment between SET/SIT (strategy OK)

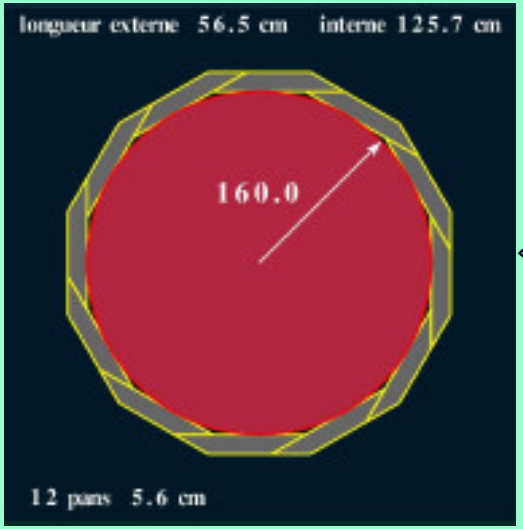
TPC to ECAL play: 10cm → 6 ? ETD layers, TPC cables and services?

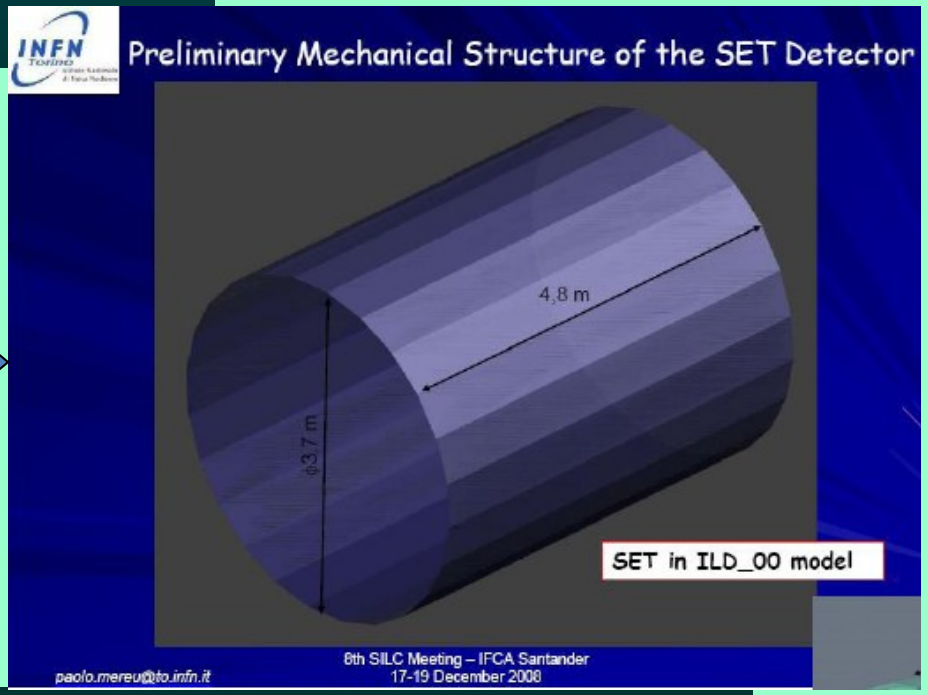
TPC end-plate thickness 10cm → 6? what does that contain?

TPC shape, what is going on in the corner? SET?

TPC outer field cage thickness 65mm → ?
connection between TPC, SET, ECAL

Henri's questions
⇐(see his talk yesterday):
quite relevant





With a precise SET how much can we play with the TPC radius?
What is the stronger constraint, TPC radius or ECAL radius?

Innermost Si tracking: SIT+FTD

- To be optimized: number and positioning of the disks
- To be decided: Si technology & 3+4 present scheme
- Alignment: OK for SIT and for FTD with A.F. sensors (include fibers)
- Estimate of material budget to be refined
- Support of SIT & FTD disks on TPC to be revisited

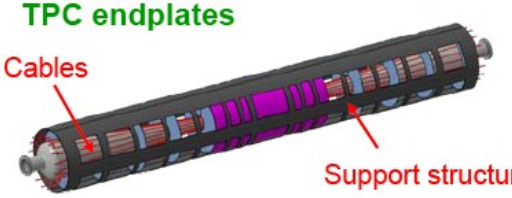
More on FTD (see J. Duarte's talk)

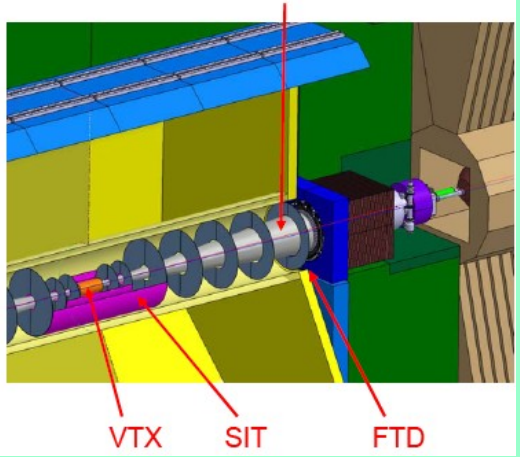
Integration status of SIT & FTD

M. Jore (Seoul'09)

- Modelised but not yet supported…
  - **Need to work with you on the integration**
- However, we've got some prelimary ideas :
  - **Put the cables along the conical beam tube (volume/type of cables?)**
  - **Supported with a structure which also hang :**
    - Beam pipe : via cables for alignment
    - Vertex : clamped on beam tube
- The support structure
  - **could be split in 2 shells for mounting and accessing to Vertex detector**
  - **Slit in TPC with rails or hang on each TPC endplates**

To be revisited

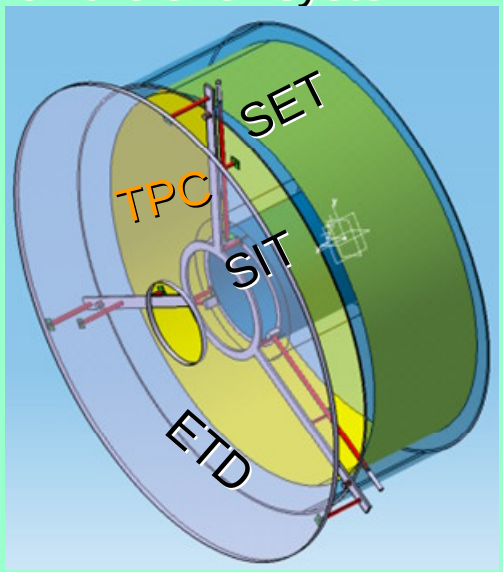




The spanish teams especially IFCA & IFIC have taken care of FTD simulations, detector design and alignment. Needs to be pushed further on.

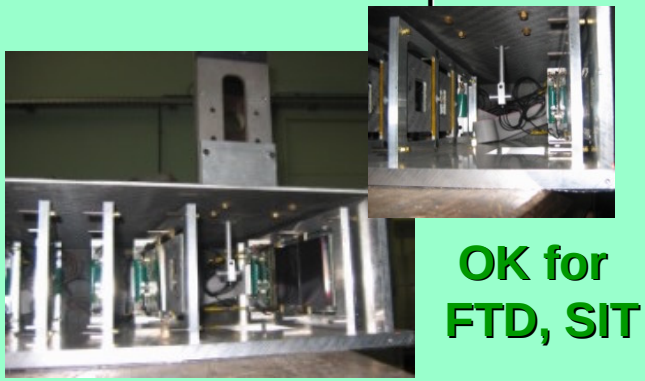
Alignment strategies:

Between components: IR Laser+fibers + pixels + FEE off the shell system



How to align SET & ETD?

Multilayer Si tracking system: A.F. sensors + IR laser + fibers read out as usual strip sensor



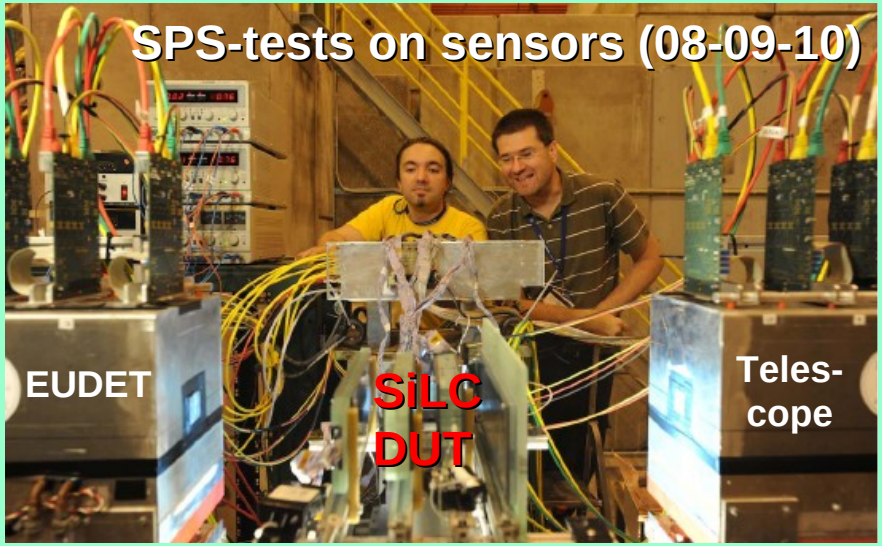
OK for FTD, SIT

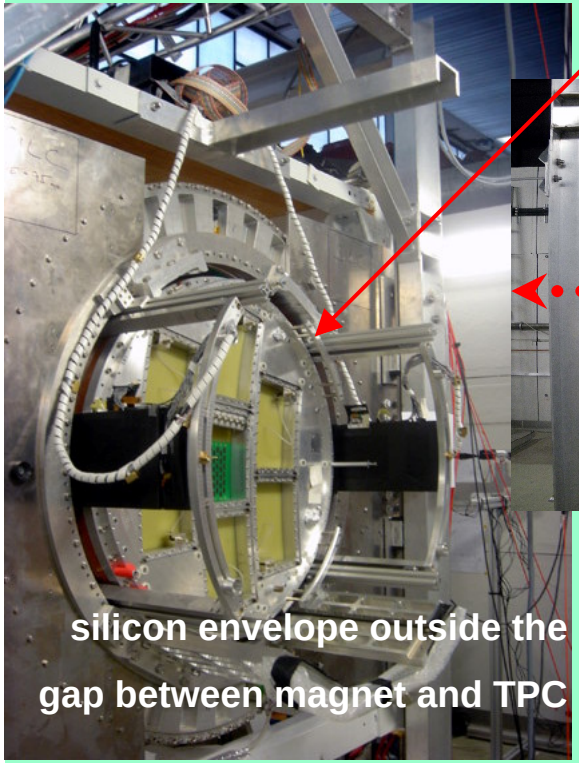
Passing from test bench to the reality of a large detector

System kit set-up to Experience the system in the Lab test bench.

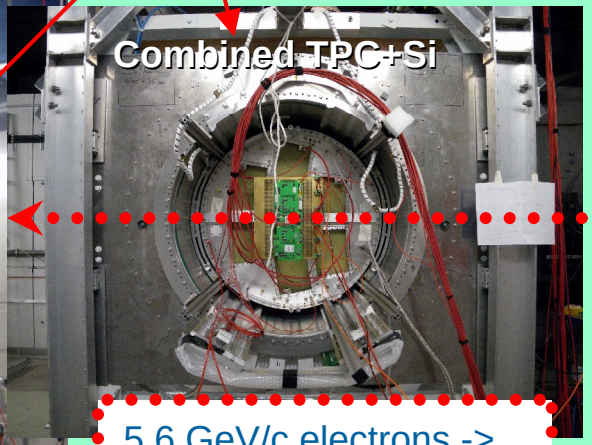
An Hybrid tracking system as ILD tracking system: TPC+Si
⇒Not only one system to align the whole Si tracker as in the case of an All-Si-Tracker

Useful also when push pull: system run outside data taking. Independent DAQ.



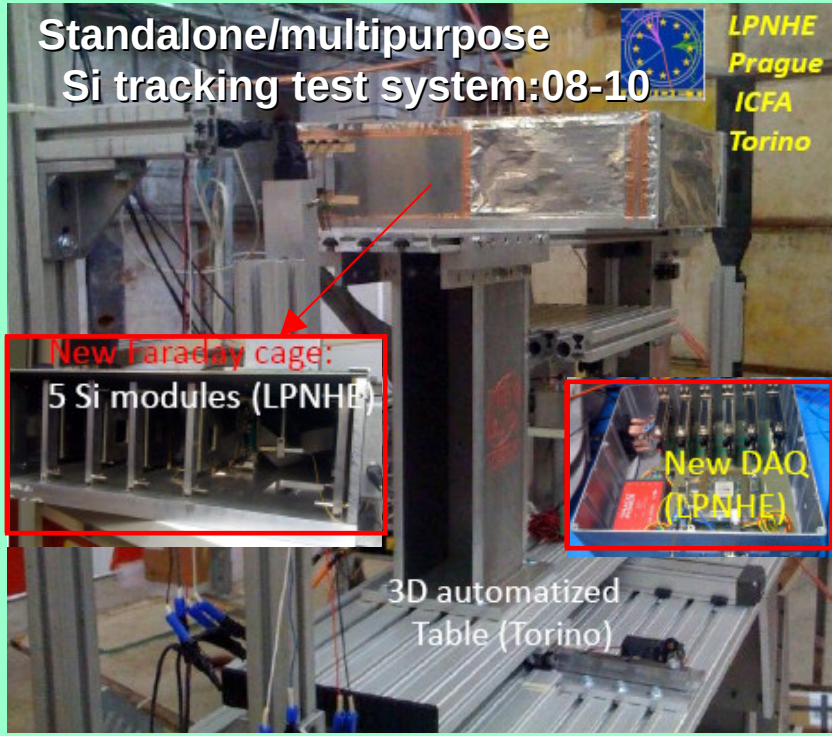


Oct-Nov'09 at DESY



5.6 GeV/c electrons ->
to minimize multiplicity

BEAM TESTS



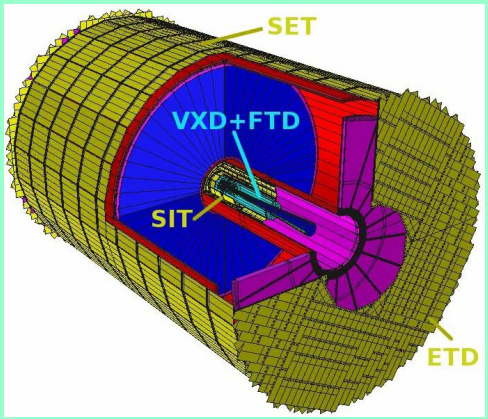
Simulations and performances studies

(W. Mitaroff presentation at simu pre-meeting)

LOI => DBD: from SGV/ LDT fast simus to detailed simulation

Si Tracker Detector Geometry

- Full Simulation Systems:
  - **Mokka** (*V. Saveliev*): not fully implemented ILD_00;
  - **ILCroot** (*A. Charpy*): full & detailed description.
- New Geometry System:
  - will replace present Mokka-GEAR database system;
  - commitment to the "full description" as in ILCroot.



Si Tracker Material Budget

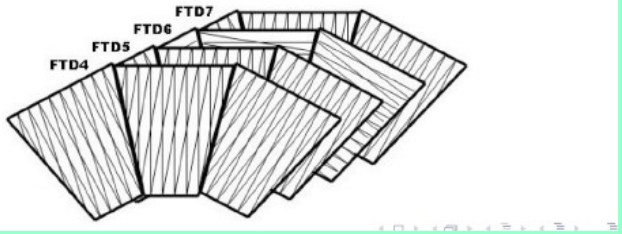
- Work on including realistic figures for
  - **Front/end electronics**;
  - **Cabling on detector;**
  - **"Cooling" of detector**.

Already a good approximation provided by the R&D activities; will be updated.

- Open questions: how important are
  - **Longitudinal resolution** (strip stereo angles – how) ?
  - **Time tagging** (relief bunch-train induced problems) ?
  - **ETD:** assess usefulness – for forward calorimetry ?
- Goal: optimization studies to be revisited
  - so far done mainly by LDT, to be redone by Full Sim.

■ Proposal for an optimized forward tracker (with minimal diversity of sensors):

Layer	R [mm]	|z| [mm]	RL [%]	σ [μm]	d_{strip} [μm]	α [°]	Type
FTD1	24.5-160	220	0.25	7	-	-	Pixels
FTD2	39.9-160	380	0.25	7	-	-	Pixels
FTD3	52.0-304	660	0.25	7	-	-	Pixels
FTD4	84.4-309	1070.6	0.65	-	25	6	Strips
FTD5	116.7-309	1481.2	0.65	-	25	6	Strips
FTD6	149-309	1891.8	0.65	-	25	6 (rot. by 90°)	Strips
FTD7	181.4-309	2302.5	0.65	-	25	6	Strips



Simulations and performances studies (cont'd)

(W. Mitaroff presentation at simu pre-meeting)

Si Tracker Software Tools

Track Reconstruction (1)

- Three main regions and three track reconstruction strategies (see Winfried's talk)
  - => very forward (FTD only)
  - => EndCap (VXD+FTD+piece of TPC+ETD)
  - => Central Barrel (TPC + SIT/SET)
- -> In parallel pursue the development of the track reconstruction ambitious plan as proposed by Winfried (provided we have the manpower...)
- **As first step**: work with the hits on **all** Si tracking components as done so far with SIT and FTD

Let's Keep an eye on longer term future

=> Beyond BaseLine: A Silicon Pixel Tracker *Ch. Damerell (RAL)*

- **The idea (first presented at Sendai LCWS 2008) is to develop a silicon pixel tracking system as a possible upgrade for ILD**
- **Main advantage would be reduced material budget (<10% X_0 over all polar angles for vertex detector plus tracking system)**
- **Guiding principle is a 'separated function' approach:**
  - **~5 tracking layers (barrel plus disks) with 50 μm pixels, integrating signals throughout the bunch train (~0.6% X_0 per layer)**
  - **A few timing layers (two as an envelope close to the ECAL, one as a barrel between vertex detector and first tracking layer) with 150 μm pixels (~2% X_0 per layer)**
- **So we provide precise timing for each track, but not for each point on the track**
- **This approach relies on the well-established robustness of pixel tracking systems wrt background – what is lost in timing can be compensated by fine granularity.**
  Timing consumes power (hence increases material budget) while granularity need not
- **One promising technology is charge-coupled CMOS pixels, already under development for ILD vertexing (the ISIS option)**

The SiLC collaboration is including this research line with 3 key points: detailed simulation studies, possible staging (?), pixel technology

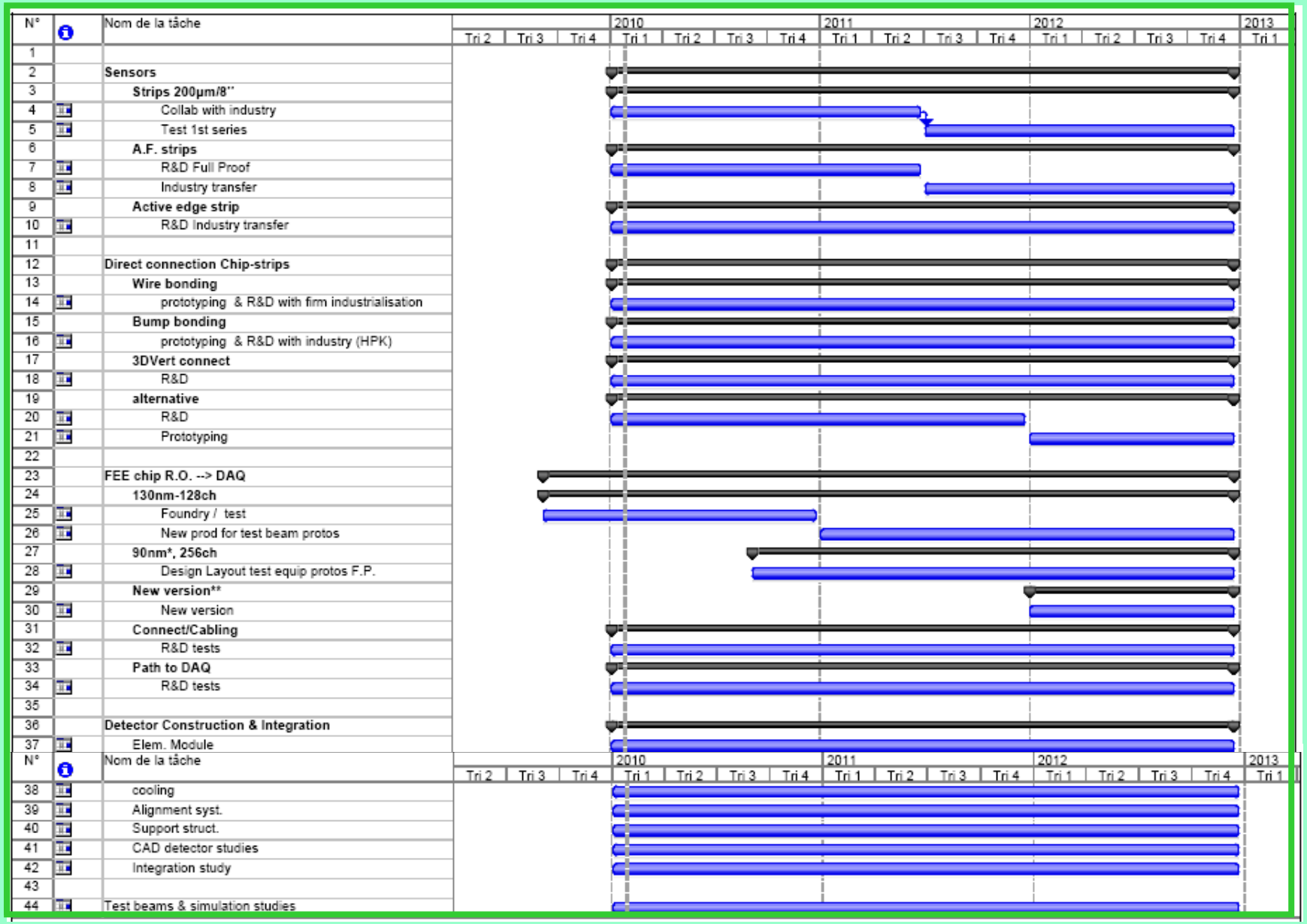
Plan & timeline (still tentative)

Legend: 90nm* =change in technology; New version** = 90nm+8x256 block+thinning

Workpackage	item	2010	2011	2012
1) **sensors**	Strips 200µm/8''	Collab with	Industry Test	1st series
	A.F. strips	R&D →	Full proof Ind	ustry transfer
	Active edge strip	R&D	R&D	Industry transfer
2) Direct	Wire bonding	Prototyping &	R&D with firm	industrialisation
connection	Bump bonding	Prototyping	& R&D with	Industry (HPK)
Chip-strips	3DVert connect	R&D	R&D	R&D
	alternative	R&D	R&D	prototyping
3) FEE chip	130nm-128ch	Foundry/test/	New prod for	Test beam protos
R.O.->DAQ	90nm*, 256ch	design	Layout test	Equip protos F.P.
	New version**			New version
	Connect/Cabling	R&D	R&D & tests	R&D & tests
	Path to DAQ	R&D	R&D & tests	

Si tracking-ILD: Plan & timeline (cont'd)

Workpackage	item	2010	2011	2012
4)Detector	Elem. Module	→	→	→
Construction	cooling	→	→	→
&integration	Alignment syst.	→	→	→
	Support struct.	→	→	→
	CAD detector studies	→	→	→
	Integration study	→	→	→
5) Test beams	Will accompany	& complete the	R&D studies &	developments
& simulation	Will accompany	& complete the	R&D studies &	developments
studies				


N°
Nom de la tâche
2010
2011
2012
2013
Tri 2
Tri 3
Tri 4
Tri 1
Tri 2
Tri 3
Tri 4
Tri 1
Tri 2
Tri 3
Tri 4
Tri 1
Tri 2
Tri 3
Tri 4
Tri 1
1
2 Sensors
3 Strips 200µm/8''
4 Collab with industry
5 Test 1st series
6 A.F. strips
7 R&D Full Proof
8 Industry transfer
9 Active edge strip
10 R&D Industry transfer
11
12 Direct connection Chip-strips
13 Wire bonding
14 prototyping & R&D with firm industrialisation
15 Bump bonding
16 prototyping & R&D with industry (HPK)
17 3DVert connect
18 R&D
19 alternative
20 R&D
21 Prototyping
22
23 FEE chip R.O. --> DAQ
24 130nm-128ch
25 Foundry / test
26 New prod for test beam protos
27 90nm*, 256ch
28 Design Layout test equip protos F.P.
29 New version**
30 New version
31 Connect/Cabling
32 R&D tests
33 Path to DAQ
34 R&D tests
35
36 Detector Construction & Integration
37 Elem. Module
38 cooling
39 Alignment syst.
40 Support struct.
41 CAD detector studies
42 Integration study
43
44 Test beams & simulation studies

Concluding remarks

- Reasonably good chances to reach the 2012 defined baseline on each of the crucial items,
- Provided (at least keeping) the FTE (avoid dispersion in too mmany other projects)
- And getting the needed funding
- ASSET: synergy with LHC upgrades