Plans of the VTX Group for the TDR

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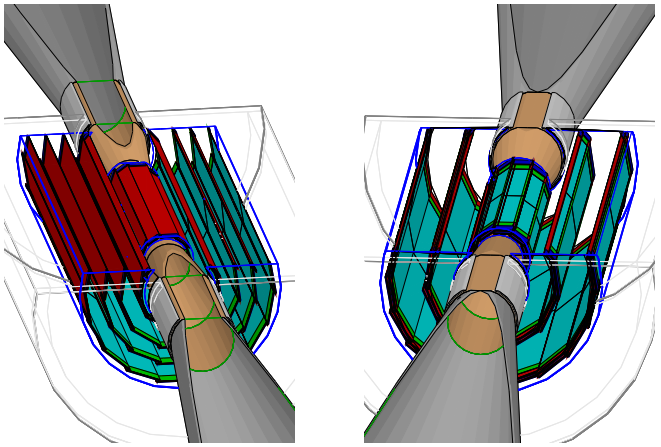
(on behalf of the VTX group)

OUTLINE

- Work plan on performance target values
- Foreseen pixel technology R&D
- Work plan on system integration
- Uncovered tasks
- Summary

Performance Target Values (1/2)



- **Improve justification of $\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta$**
  - $\Rightarrow$ guidance for pixel and ladder R&D

- **Studies based on realistic & detailed phys. simulations**

  (including beam background and $\gamma\gamma$ collisions)

  - ⁂ justify the constraint on a ($\leq$ 5 μm):
    - determine the necessary single point resolution
    - estimate necessary alignment accuracy and monitoring
  - ⁂ justify the constraint on b ($\leq$ 10 $\mu m \cdot GeV/c$):
    - estimate the acceptable (ladder) material budget (b $\propto \sqrt{X/X_0}$)
      - $\hookrightarrow$ estimate the impact of material at shallow angle (”end-plate” material budget)
    - estimate an acceptable value of the inner radius (b $\propto$ R$_{in}$)
    - special concern: low P & θ tracks and vertex charge

- **Quantify necessary performance improvements for running at $\sim$ 1 TeV**

Performance Target Values (2/2)

- **Improve justification of the time resolution** (continuous r.o.) **or pixel pitch** (delayed r.o.)

  ⇒ guidance for pixel and ladder R&D

geometry	radius [mm]		ladder length [mm]		read-out time [μs]	
	VXD-03	VXD-05	VXD-03	VXD-05	VXD-03	VXD-05
layer 1	*15.0*	*16.0/18.0*	*125.*	*125.*	*25–50*	*25–50*
layer 2	*26.0*	*37.0/39.0*	*250.*	*250.*	*50–100*	*100-200*
layer 3	*37.0*	*58.0/60.0*	*250.*	*250.*	*100-200*	*100-200*
layer 4	*48.0*		*250.*		*100-200*	
layer 5	*60.0*		*250.*		*100-200*	

FPCCDs integrate over the full train duration

- **Studies based on realistic & detailed phys. simulations**

  (based on critical beam background consideration)

  ⁂ evaluate degradation of physics performance as a function of increasing occupancy

  ⁂ compare continuous and delayed read-out

  ⁂ study impact of track matching with surrounding detectors (bunch tag)

Pixel Technologies (1/2)

- **Pursue pixel technology R&D inside & beside the ILD community**
  - **a)** inside ILD: MIMOSA, FPCCD, DEPFET, 3D (CAIRN), ISIS (?)
  - **b)** beside ILD: MIMOSA, DEPFET, APSEL, 3D (INFN), others ?

- **Achieve pixel technology specifications at various degrees (a, b, c, d)**
  - **a)** proof of principle
  - **b)** small prototype performance vs specifications:
    σ_{sp}, thinning, read-out speed, radiation tolerance, P_{diss}.
  - **c)** real scale (20–30 % of final sensor area) validation of a) $\oplus$ b)
  - **d)** including system integration aspects: mechanical support, servicing (cooling, power pulsing)

- **Aim at providing a status of each R&D (including its perspectives) at the time of the TDR**

Pixel Technologies (2/2)

- **Make sure that $\geq$ 1 technology (continuous or/and delayed read-out) is qualified at level c) or d)** $\Rightarrow$ nearly all prominent specs satisfied within a factor ≤ 2

- **Assess consequences of technology specific system integration issues:**
  - power pulsing
  - delayed read-out vs continuous read-out
  - material distribution inside/outside fiducial volume (e.g. read-out chips)
  - etc.

- **Clarify performance perspectives at 1 TeV:**
  - which technologies are best suited for running at 1 TeV ?
  - which specific R&D should be performed ?
  - etc.

System Integration : General Remarks

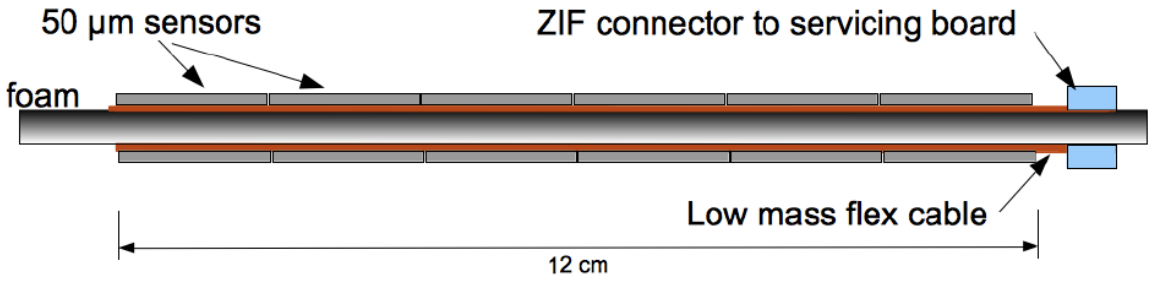
- **System Integration is a critical & prominent VTX topic for TDR:**
  - very challenging material budget (may be more critical with power cycling ?)
  - target specifications ($\leq$ 0.16 % X_0 / ladder) well beyond the state of the art
  - substantial amount of work remaining to be done
  - ladder concept is (partly) pixel technology dependent
  - ”end-plate” material assessment & consequences on fw tracking (added value of double-layers ?)
  - 2 ladder concepts: single-sided vs double-sided $\Rightarrow$ how do they compare ?
  - missalignment resulting from push-pull $\rightarrowtail$ how to get the required accuracy w.r.t. beam BG core ?

- **4 identified ladder developments under way :**
  - inside ILD: double-sided ladder by the PLUME collaboration
    and unsupported single-sided ladder (SERWIETE project)
  - beside ILD: single-sided ladders for BELLE-II by the DEPFET collaboration
    and for STAR at RHIC by the CMOS collaboration

- **Development of 0.16% X_0 double-layer may also start soon if funded** (FPCCD groups)

System Integration : PLUME Project

- **PLUME** $\equiv$ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding



- **Objectives :**
  - ⁂ achieve a low material, double-sided, ladder prototype for an ILC vertex detector by 2012
  - ⁂ use MIMOSA, ISIS (???), FPCCD (?), other (?) sensors
  - ⁂ evaluate benefits of 2-sided concept (mini-vectors) :
    σ_{sp}, alignment, shallow angle pointing, elongated ($\equiv$ fast r.o.) vs square ($\equiv$ precise pixels)

- **Collaboration:** Bristol - DESY - Oxford - Strasbourg (synergy with Vertex Detector of CBM/FAIR)

- **Working plan:**
  - ⁂ 2009: prototype Nr.0 (2 sensor on each side) tested at CERN-SPS
  - ⁂ 2010: prototype Nr.1 (6 MIMOSA-26 sensors on each side) featuring $\sim$ 0.6 % X_0 tot. mat. budget
  - ⁂ 2011: prototype Nr.2, like Nr.1 but with 0.4 - 0.5 % X_0 total material budget
  - ⁂ 2012: prototype Nr.3, like Nr.2 but with 0.3 - 0.4 % X_0 ttotal material budget
    (potentialy one side with $\sim$ 10 μs read-out time)

System Integration : SERWIETE Concept

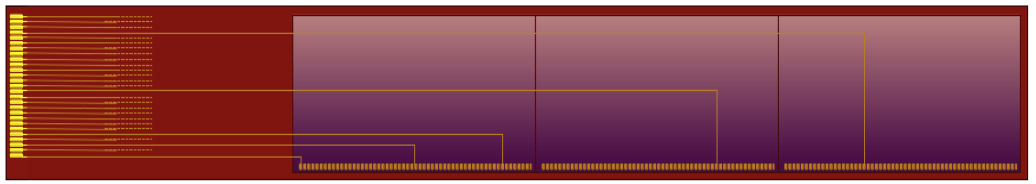
- **Unsupported ladder:** $\equiv$ **SE**nsor **R**ow **W**rapped **I**n an **E**xtra-**T**hin **E**nvelope **(SERWIETE)**

- **Objectives :**
  - achieve a sensor assembly mounted on flex and wrapped in polymerised film with $\lesssim$ 0.15 % X_0 in total
  - evaluate possibility of mounting unsupported ladder on cylindrical surface (serving as mechanical support)
  - proof of principle expected in 2012

Proto 1 ▷ Spring 2010

- **Working programme:**
  - prototype Nr. 1 (2010) made of 1 sensor : MIMOSA-18 (analog output, $\lesssim$ 4 ms)
  - prototype Nr. 2 (2011) made of 3 sensors : MIMOSA-26 (digital output, $\lesssim$ 110 μs)

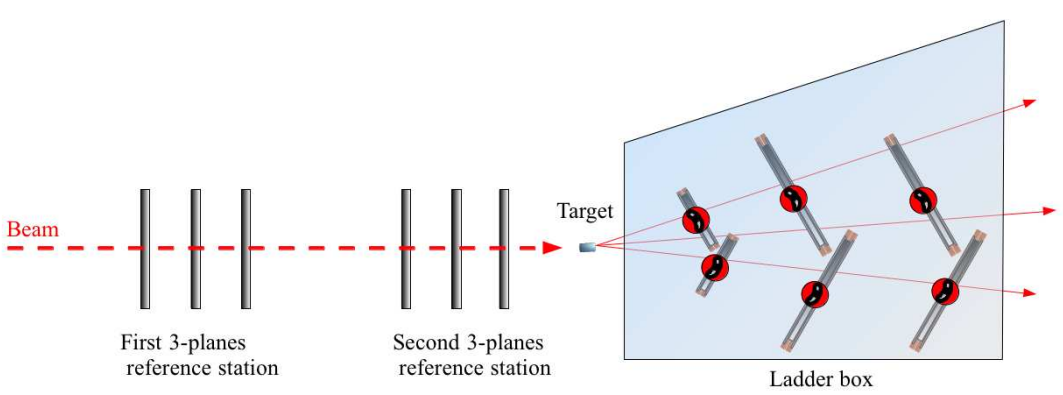
Proto 2 ▷ Summer 2011

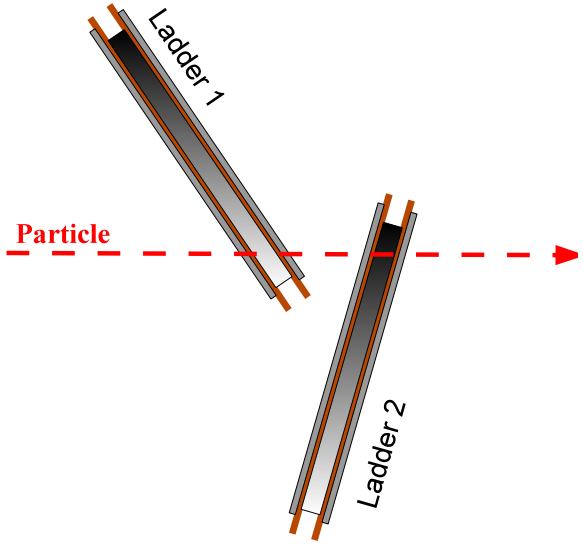


- **Context of development:**
  - E.U. project Hadron Physics 2 (FP-7)
  - collaboration between Frankfurt (CBM/FAIR) and IPHC/Strasbourg

Infrastructure to Study Integration Issues

- **On-beam test infrastructure:**
  - ⁜ Large Area beam Telescope (LAT)
  - ⁜ Alignment Investigation Devices (AID): mini-telescope and/or ladder box
  - ⁜ Very thin removable target





- **Off-beam test infrastructure:**
  - ⁜ thermo-mechanical studies, including effect of air-flow based power extracting system
  - ⁜ power cycling effect in strong magnetic field, e.g. Lorentz forces, on ultra-light ladders
- **Project part of AIDA–FP7 proposal (coll. of PLUME membres + Univ. Geneva + Univ. Warsaw) :**
  - ⟶ project likely to happen independently of AIDA approval

Uncovered Tasks

- **Development (engineering) of global design concept :**
  - design of ”cryostat” (ladder support, field cage, cabling, etc.)
    in case FPCCD project not (fully) funded
  - inner layer supports on beam pipe
  - powering and cabling
  - cooling
  - DAQ
- **Global inner tracker concept optimisation :**
  - track link with neighbouring sub-detectors
  - bunch tagging provided by these sub-detectors
  - special concern: shallow angle vertexing (effect of material versus limited nb of hits/track, ...)

Prominent Milestones

- **Summer 2011:** main parametres impacting physics should be frozen
  - Pixel technologies: basic param. of each technology (phys. and BG oriented)
  - Ladder design (technology dependent)
  - Cryostat and services design (technology dependent)
  - Clustering and tracking tools $\rightarrowtail$ flavour tagging, beam BG rejection
  - Main characteristics of surrounding tracking detectors
  - Main changes for 1 TeV running
- **Summer 2012:**
  - Viable sensor parametres supporting predicted VTX performances
  - Viable ladder parametres supporting predicted VTX performances
  - Residual missalignment $\sim$ quantified
  - $\sim$ complete engineering design
- **Towards end of 2012:**
  - Educated guess on extrapolating from achieved performances to final ones (with timeline)

Summary

- **Improved target values are requested for more precise guidance to VTX design :**
  - ⁕ based on complete simulations including beam BG (& 2γ collisions) $\Rrightarrow$ guidance for R&D
  - ⁕ improve understanding of double-sided versus single-sided ladder performance differences
- **Several pixel technologies will continue maturing :**
  - ⁕ CMOS sensors, FPCCD, DEPFET (for Belle-II), 3DIT, etc.
  - ⁕ $\geq$ 1 technology expected to be mature enough to give credit to predicted VTX performances
- **Substantial effort on system integration :**
  - ⁕ full scale 2-sided ladder & unsupported ladder (on pipe ?) prototypes will be fab. & tested
    $\hookrightarrow$ not clear whether material budget of $\sim$ 0.16% X_0 is reachable ($\sim$ 0.3% X_0 may be a limit)
  - ⁕ beside ILD: evolution of DEPFET-ladder for BELLE-II & CMOS-ladder for STAR
  - ⁕ extensive studies on alignment foreseen, as well as on power cycling
  - ⁕ design of cryostat and services may be carried through (depends on funding decisions)
- **Several major tasks (may) remain uncovered :**
  - ⁕ cryostat design, cooling and cable implementation, ...
  - ⁕ integration in inner tracking system and in IP environment (beam pipe)
- **Summer 2011: all decisive simulation parametres expected to be frozen for the TDR**

BACK UP SLIDES

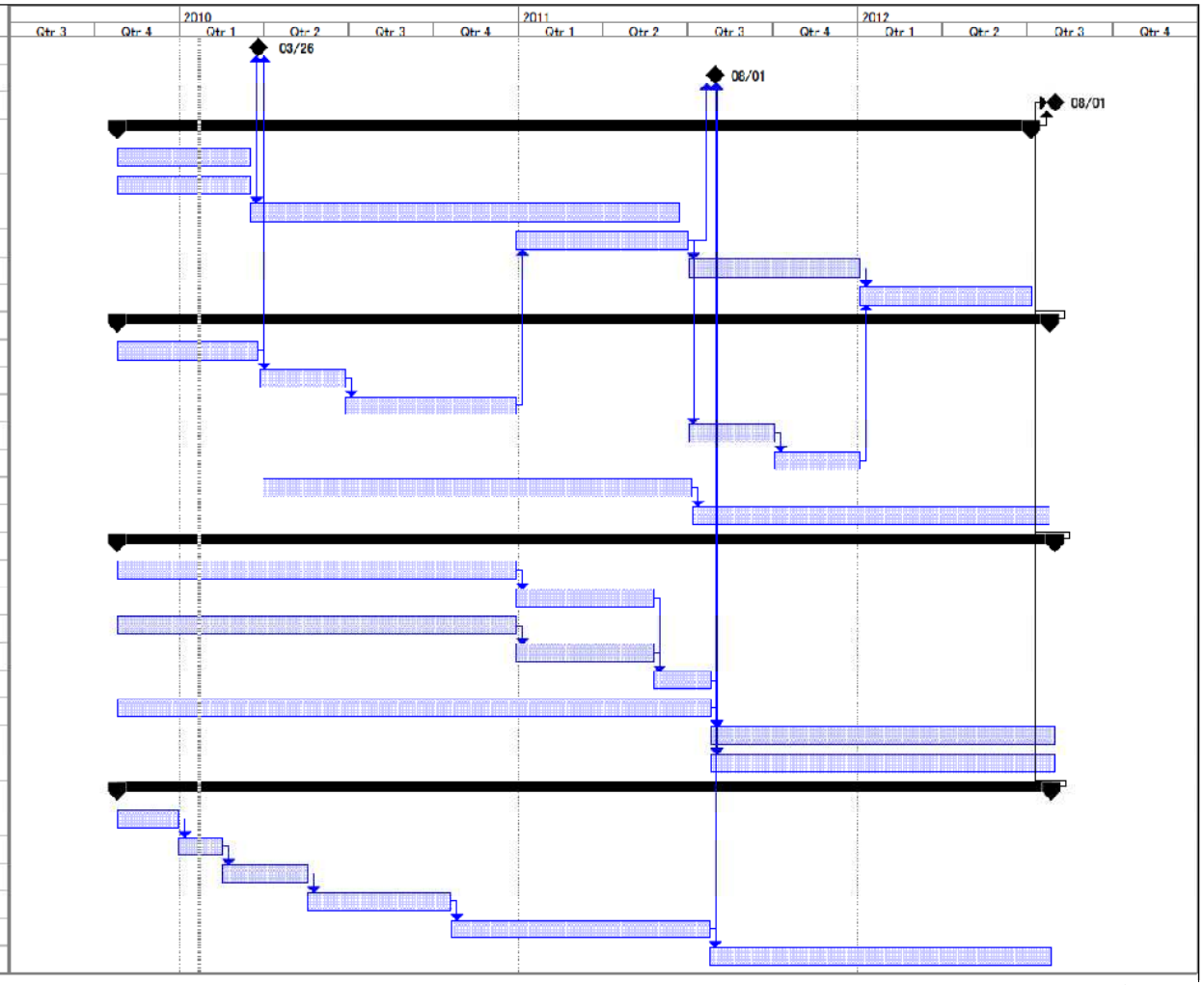
Plans of FPCCD Groups (1/2)

- **Sensor R&D:** extrapolate from existing small prototypes (FPCCD1/2) presently under test
  - FPCCD3 (6x6 mm^2) to be fabricated in 2010 (beam tests with r.o. ASIC-2 in 2010)
  - FPCCD4 (10x62.5 mm^2) to be fabricated by mid-2011 (tests in 2011/12) with ASIC-3
  - validation procedure includes radiation immunity (-40°C with CO2) and wafer thinning
- **Electronics R&D:** develop r.o. ASIC extrapolating from already existing & tested ASIC-1
  - ASIC-2 to be fab. in 2010 (tests in 2011, with FPCCD3 on beam)
  - ASIC-3 to be fabricated in 2011, tests with FPCCD4 in 2012
  - also: development of clock drivers, digital signal processor, etc.
- **System integration studies:**
  - develop double-sided ladders with 0.16% X_0 total material budget
  - develop cryostat
  - realise detailed engineering design
- **Software developments**
  - FPCCD digitiser, cluster reconstruction, BG rejection from cluster shape
  - track finder using double-layer structure
  - flavour-tagging capability despite intense beamstrahlung background

Plans of FPCCD groups (2/2)

Timeline

ID	Name
1	LCWS2010
2	Baseline decision
3	Detailed design
4	**Sensor R&D**
5	FPCCD1/2 test
6	Development of FPCCD3
7	FPCCD3 test
8	FPCCD3 beam test
9	Development of FPCCD4 (full size)
10	FPCCD4 test
11	**Electronics R&D**
12	FE-ASIC2 design
13	FE-ASIC2 fabrication
14	FE-ASIC2 test
15	FE-ASIC3 development
16	FE-ASIC3 test
17	Design of driver/peripheral
18	Fabrication/test driver/peripheral
19	**Engineering R&D**
20	Design of ladder
21	Fabrication of dummy ladder
22	Design of cryostat/cooling system
23	Fabrication of cryostat/cooling system
24	Test dummy ladder
25	Study of wafer thinning
26	Fabrication of prototype ladder
27	Detailed engineering design
28	**Software development**
29	FPCCD Digitizer
30	Digitizer implementation/test
31	Cluster reconstruction/BG rejection
32	Tracking with super-layer
33	Flavor Tag
34	Physics analysis



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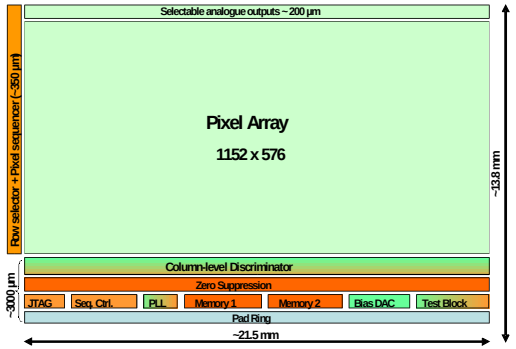
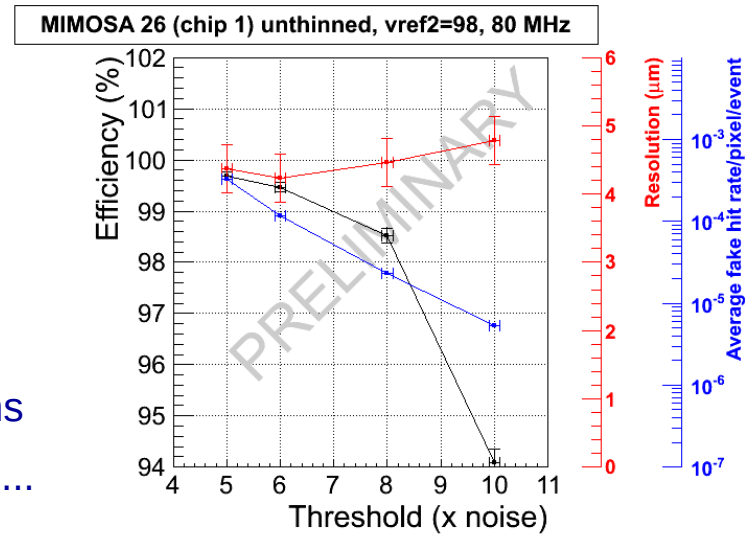
MIMOSA-26: Full Size CMOS Sensor with Integrated ∅

- **Full size sensor with integrated zero-suppression fab. in 2009:**
  - ⁂ Active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - ⁂ Pitch: 18.4 μm $\rightarrowtail$ $\sim$ 0.7 million pixels $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm
  - ⁂ T$_{r.o.}$ $\lesssim$ 110 μs $\Rrightarrow$ suited to $>$ 10^6 particles/cm^2/s
  - ⁂ P $\sim$ 300 mW/cm^2 (static) + 100 mW/cm^2 (dynamic with 1% occ.)
  - ⁂ Data transmission: 1 output at $\geq$ 160 Mbits/s
    or 2 outputs at $\geq$ 80 Mbits/s
  - ⁂ 6 sensors equip the final set-up of the EUDET beam telescope



- **$>$ 30 sensors tested in lab and $\sim$ 10 sensors at CERN-SPS:**
  - ⁂ $\gtrsim$ 99.5 % detection efficiency routinely observed
    over the whole sensitive area, with a fake rate $\lesssim$ O(10^{-4})
  - ⁂ $\sigma_{sp}^{M26} \sim$ 4–4.5 μm (preliminary) $\rightarrowtail$ expect $\sigma_{sp} \lesssim$ 4 μm

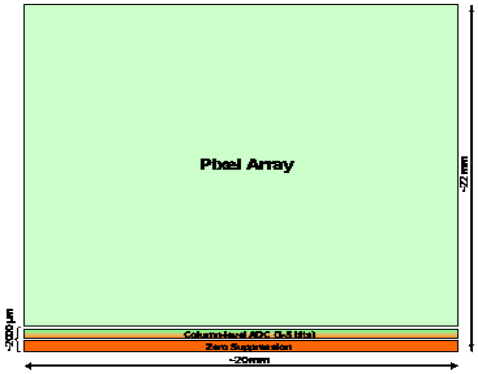


▷▷▷ MIMOSA-26 architecture validated for numerous applications
$\Rrightarrow$ currently being extended for STAR-PIXEL and CBM-MVD, ...
also investigated as an option for ALICE–ITS upgrade

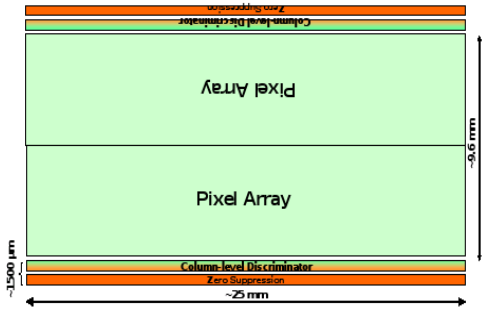
From MIMOSA-26 to the ILC Design

- **Ellaborate on MIMOSA-26 architecture and sensors going to equip STAR-HFT and CBM-MVD**

- **Outer layers ($t_{int} \sim$ 100 μs) :**
  - pitch $\lesssim$ 35 μm (need phys. studies)
  - 4-bit ADC $\Rightarrow$ $\sigma_{sp} \sim 3\ \mu m$
  - 576 col. of 576 pixels $\Rightarrow$ 2x2 cm^2



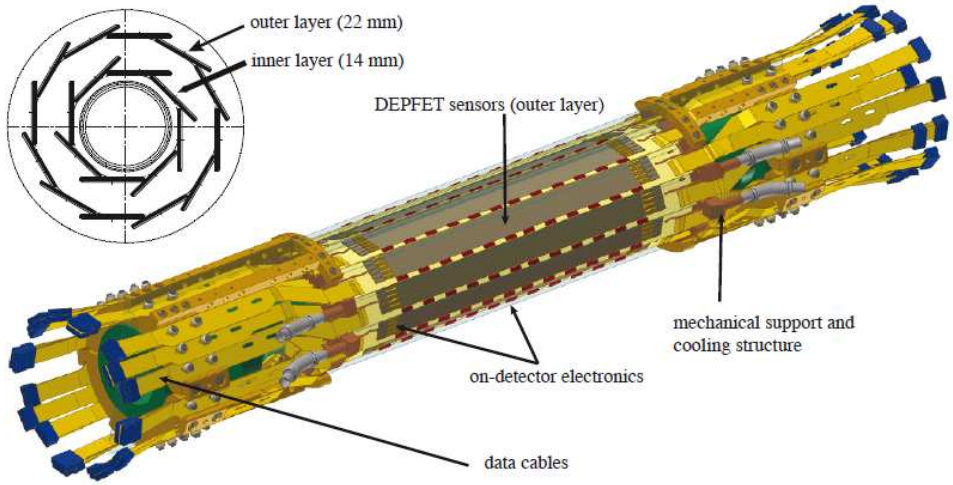
- **Inner layers ($t_{int} \sim$ 25 - 50 μs) :**
  - double-sided r.o. $\Rightarrow$ twice shorter (= faster) columns
  - pitch $\lesssim$ 15 μm
  - binary r.o. $\Rightarrow$ $\sigma_{sp} \lesssim 3\ \mu m$
  - 1600 columns of 320 pixels $\Rightarrow$ $\lesssim$ 24x0.95 mm^2

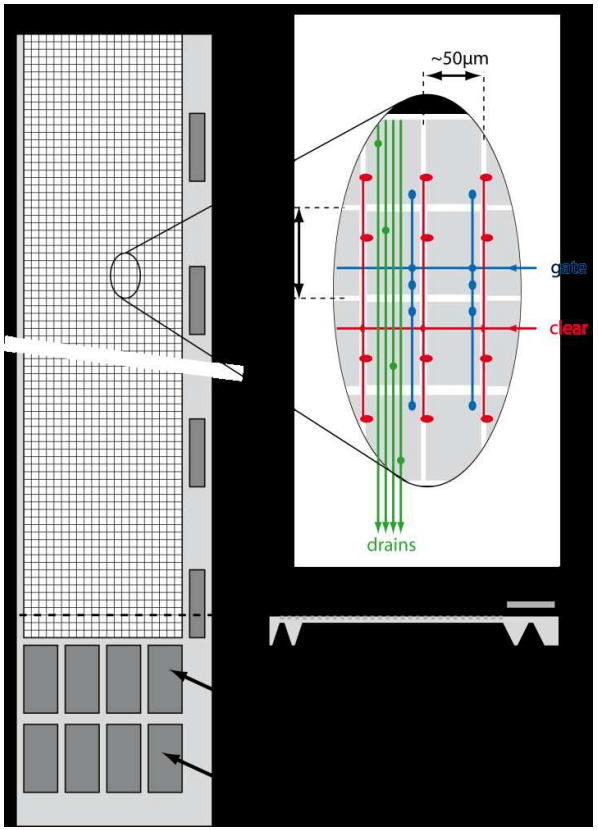


- **The path to $\lesssim$ 10–20 μs:**
  - exploit double layer concept to implement elongated pixels on one side of inner layer
  - reduced nb of pixels per column $\Rightarrow$ shorter read-out time $\Rightarrow$ goal: factor 4–6 w.r.t. square pixel side
  - depleted epitaxial layer $\Rightarrow$ wider sensing diode spacing $\Rightarrow$ $\lesssim$ 10 μs may be reachable

Contributions from the DEPFET Collaboration (1/2)

DEPFETs for Belle II, some numbers





- 2 layers of DEPFET APS ladders
- L1: 90x12.5 mm2, 8 ladders, 50x50µm2, 1600x250 pix/ladder
- L2: 126x12.5 mm2, 12 ladders, 50x75µm2, 1600x250 pix/ladder
- Thin (50µm) sensitive area, ladder concept like in ILD
- Framerate 100kHz (L1) and 50kHz(L2), continues read-out
- Linerate: 12.5 MHz, “rolling shutter” mode

Radiation damage: a few Mrad/year
- No requirements in forward region
  → relaxed end-of-ladder (EOL) specs for material and services
- no power pulsing possible, but aggressive (liquid) cooling on EOL allowed

DEPFET contribution for ILD and timeline

- ladder concept very similar to ILD → Belle II ladders as ILD demonstrator
- DEPFET technology optimization (rad. tolerant) during production for Belle II
- ILD prototypes with small pixel size with Belle II DEPFET production
- Development of rad-hard r/o ASICs and steering chips with 80 ns line rate, extendable to faster read-out
- Development of the interconnection technologies on-ladder (low mass bump bond) and off-ladder (flex cable), as well the necessary DAQ systems

In this sense, the DEPFET Collaboration will be able to push the DEPFET to the technology readiness level (c.), even beyond (d.) (engineered detector), but in the geometry of Belle II (smaller acceptance, smaller pixel size)

In parallel, groups within the DEPFET collaboration will contribute to the detector optimization studies of ILD VXD.

Timeline and milestones:

- spring 2010: read-out ASICs with integrated ADC, 12.5 MHz line rate
- autumn 2010: first thin (50µm) DEPFET sensors, 50% of final Belle II ladder in size, thin 128x128 matrices with ILD pixels, to be read out with new ASICs
- autumn 2010 or summer 2011: beam test of thin DEPFETs, both for Belle II and ILD
- end 2010: Data Handling Processor (DHP: ASIC for data handling and reduction placed on the ladder)
- during 2010: engineering of thin Belle II ladders (all-silicon ladder) and overall integration scheme
- during 2010: development of third metal layer in Cu, and UBM for flip-chip of ASICS to DEPFET ladder
- spring 2011 to spring 2012: final production of Belle II ladders (and possibly larger samples of ILD DEPFET matrices on this wafers)
- until summer 2013: ladder assembly and integration of pixel detector in Belle II
- first Belle II data expected 2013, taken with an ultra-transparent DEPFET pixel detector