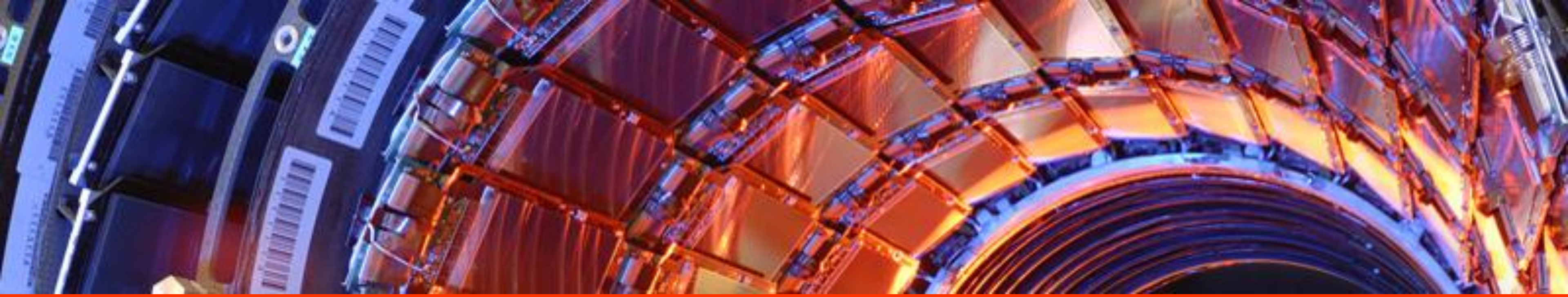
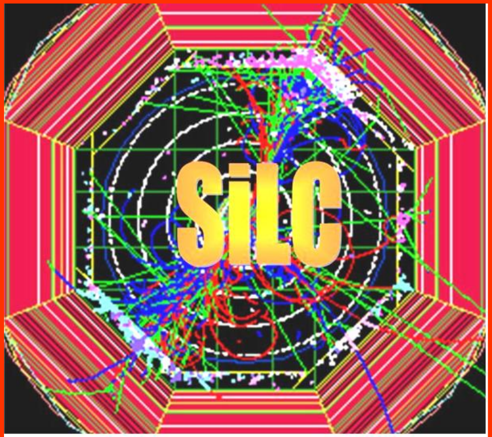


SiLC R&D new outcomes & results

IWLC2010, International Workshop on L.C. 2010

October 18-22, 2010, Geneva (CH)



A.Savoy-Navarro, Université Pierre et Marie Curie/IN2P3-CNRS

on behalf of the SiLC R&D Collaboration

THE GOALS of SiLC R&D Collaboration:

To develop the next generation of Large area Silicon Tracking system for the Future Linear Collider

THE GOALS of SiLC R&D Collaboration:

To develop the next generation of Large area Silicon Tracking system for the Future Linear Collider

Better performances:
Momentum & spatial resolutions
Time stamping
Power cycling

THE GOALS of SiLC R&D Collaboration:

To develop the next generation of Large area Silicon Tracking system for the Future Linear Collider

Better performances:
Momentum & spatial resolutions
Time stamping
Power cycling

Radiation hardness is not an issue

THE GOALS of SiLC R&D Collaboration:

To develop the next generation of Large area Silicon Tracking system for the Future Linear Collider

Better performances:
Momentum & spatial resolutions
Time stamping
Power cycling

Radiation hardness is not an issue

Lower Material Budget

THE GOALS of SiLC R&D Collaboration:

To develop the next generation of Large area Silicon Tracking system for the Future Linear Collider

"Generic": Working on 2 tracking concepts: Si+TPC (ILD) & All Si (SiD), applied to ILC case and now CLIC case.

Radiation hardness is not an issue

Better performances:
Momentum & spatial resolutions
Time stamping
Power cycling

Lower Material Budget

The SiLC R&D Collaboration

(Till Oct. 2010)

USA

Michigan University
UCSC & SCIPP

Close connections:
FNAL(M. Demarteau +B. Cooper; t.b.)
SLAC (test beam tbc)

Europe

Barcelona U.
CNM-IMB/CSIC, Barcelona
Rutherford Lab, Didcot
HIP, Helsinki U./VTT
IEKP Karlsruhe
Moscow St. U. & SiLAB
NRNU, Obninsk
LPNHE/UPMC, Paris
Charles U. in Prague
IFCA/CSIC-Cant U. Santander
INFN Sez. Torino & Torino U.
U. Trento & FBK
IFIC/CSIC, Valencia
HEPHY, Vienna

Close connections:
CERN (bonding Lab, Test beams)
DESY (EUDET, ILD,test beams)
Synergy with LHC construction & Now upgrades

Asia

Korean Universities around KNU & ETRI
KEK & Tokyo U.
Hamamatsu HPK
Close connections:
BELLE II
And now
Muon g-2/EDM J-PARC
KEK test beam

EUDET (06-10)
AIDA≥11

Outline

- Latest advances on the 3 basic R&D objectives:
  - New sensors
  - New FE and readout electronics
  - related mechanical issues
- Tools developed to achieved R&D objectives
  - Simulations
  - Lab test benches and test beams
- Outcomes from detector concepts LOI's & preparation of DBD's
- Synergies, Outcomes & perspectives

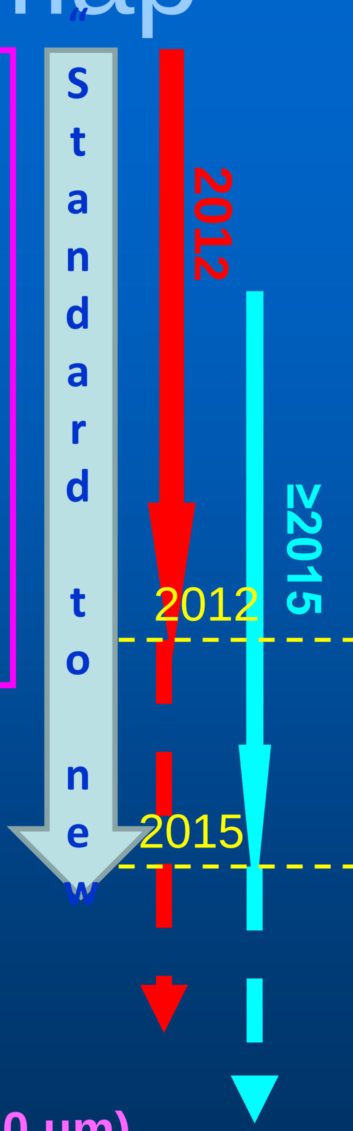
I.- R&D BASIC OBJECTIVES

- **R&D on sensors**
- R&D on FEE and READOUT
- RELATED MECHANICAL ISSUES

R&D on sensors: the roadmap

BASELINE

- The microstrip sensors
  - => Standard but **new planar strips**
  - => *Alignment-friendly* strips
  - => **Edgeless** planar **strips**
- 3D technology based sensors
  - => “SOI-like” **Edgeless strip sensors**
  - => 3D short strips
  - => 3D pixels



GOALS = get the industrial firms to produce:

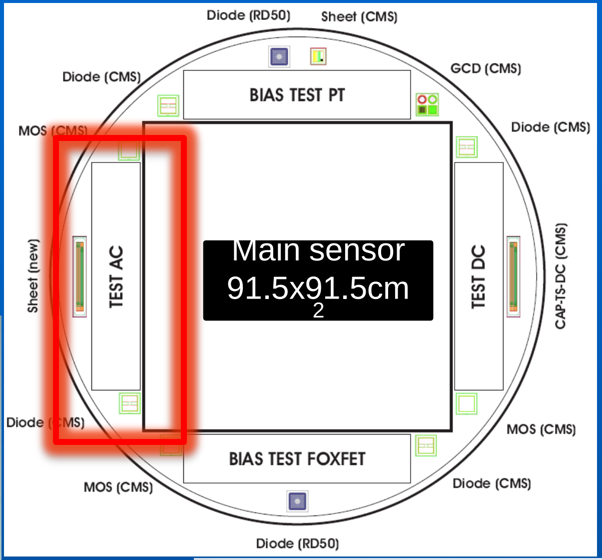
- **Larger wafer (6”to 8”), thinner 200 µm, smaller pitch (50µm)**
- **Possibly DSSD, now 6”, 320 µm thick, 50 µm pitch (new HPK)**
- **Decreased non-active edge (from a few hundreds down to 10-20 µm)**
- **Direct connection of FEE onto the strip sensor.**

One remark:

Strips are not old hat!

See next….

Standard new planar strips from HPK



HPK order: STARTING POINT for SiLC

SiLC Collaboration order at Hamamatsu HPK:

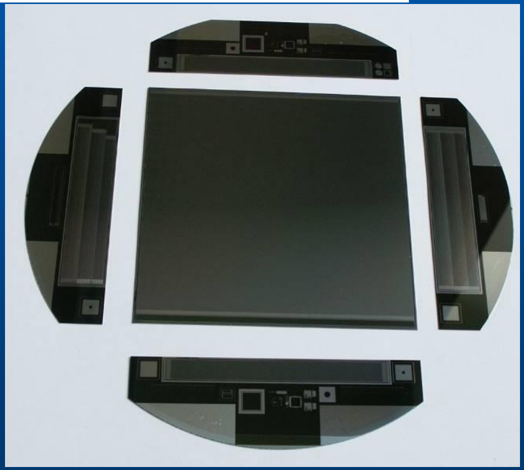
- 30 pieces single-sided 6” wafer
- 5 pieces. alignment sensors of same layout, but hole for laser in backplane metallization

(no anti reflection coating: ARC) =>

measured T=20% (as CMS)

Specifications:

- Wafer thickness : 320 μm
- Depletion voltage around 75V
- 1792 AC-coupled strips, individually biased via poly-Si resistor (20MOhm)
- Strip pitch: 50 μm pitch,
- Strip width: 12.5μm
- No intermediate strips
- Additional test structures around the wafer

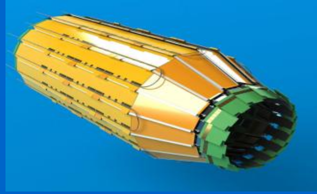


A new step w.r.t those in current LHC trackers.

HEPHY fully tested them in order to establish the next steps (test structures).

HEPHY & LPNHE built Si modules with these HPK sensors & characterize them in test beams (see later)

New sensors: DSSD

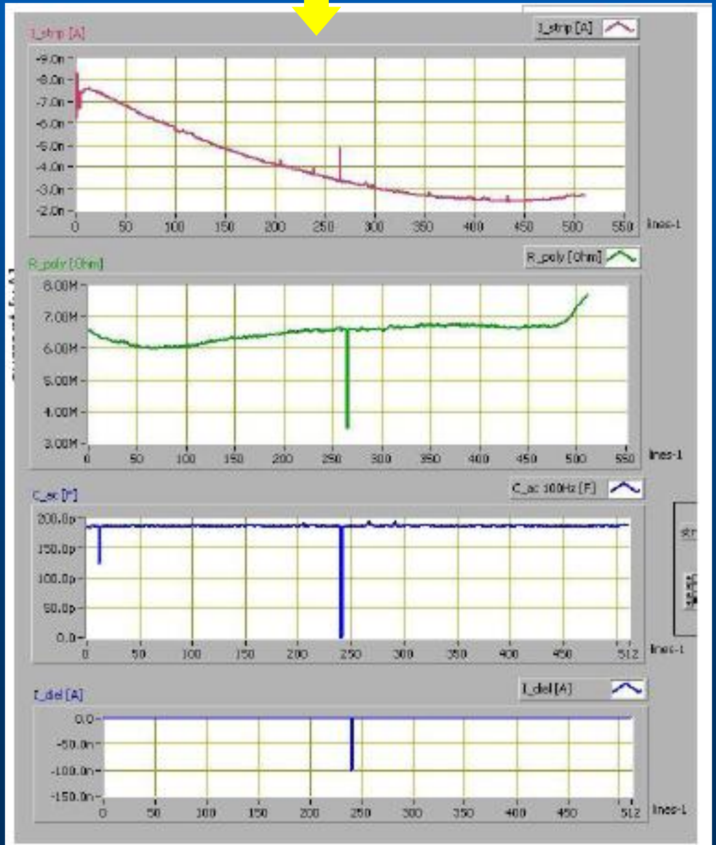


After 2 years of intense search for 6"DSSD and negotiations with CANBERA, SINTEF, MICRON=>

- ***2009/8: HPK starts 6" DSSD production line.***
- 2009/9: 6" design submitted to HPK
- 2010/3: Prototype sensors from pilot batch delivered to KEK
- Electrical characterization (97% strip yield)

	p side (r-ϕ)	n side (z)
Sensor Area	124.88x59.60 mm	
Active Area	122.90x57.72 mm	
Wafer	6" diameter 320 μm thick	
Full depletion Volt.	100 V	
Strip pitch (μm)	75	120
Readout pitch (μm)	75	240
Readout channels	768	512

AC coupled & Poly-Silicon resistor biasing

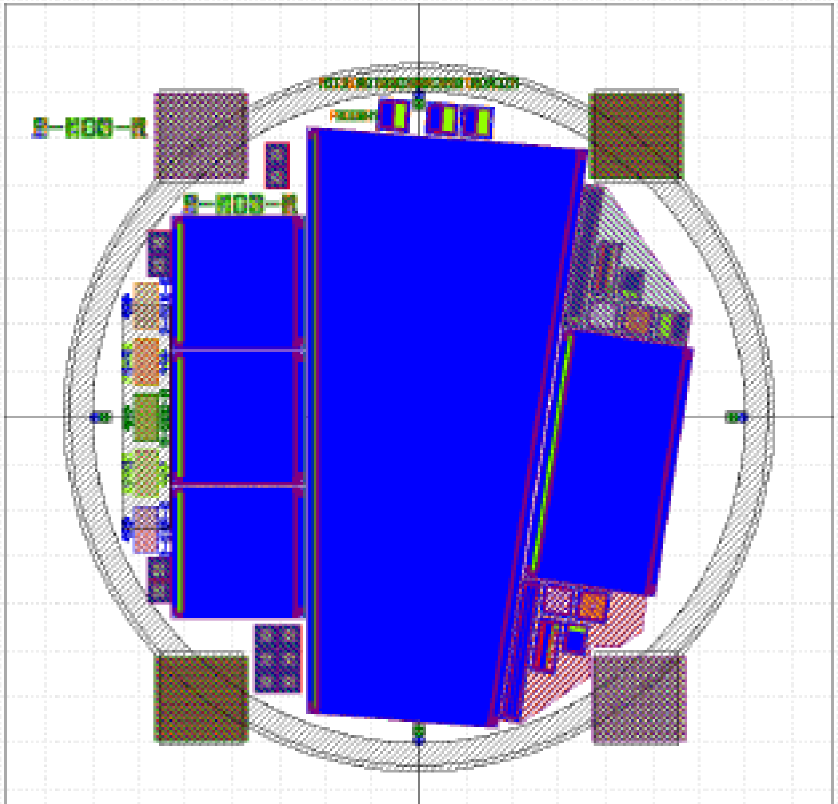


New trapezoidal 6'' DSSD

Trapezoidal Sensors (Micron)

- Full wafer designed using self-developed framework
- Including test structures and mini sensors to test different p-stop designs

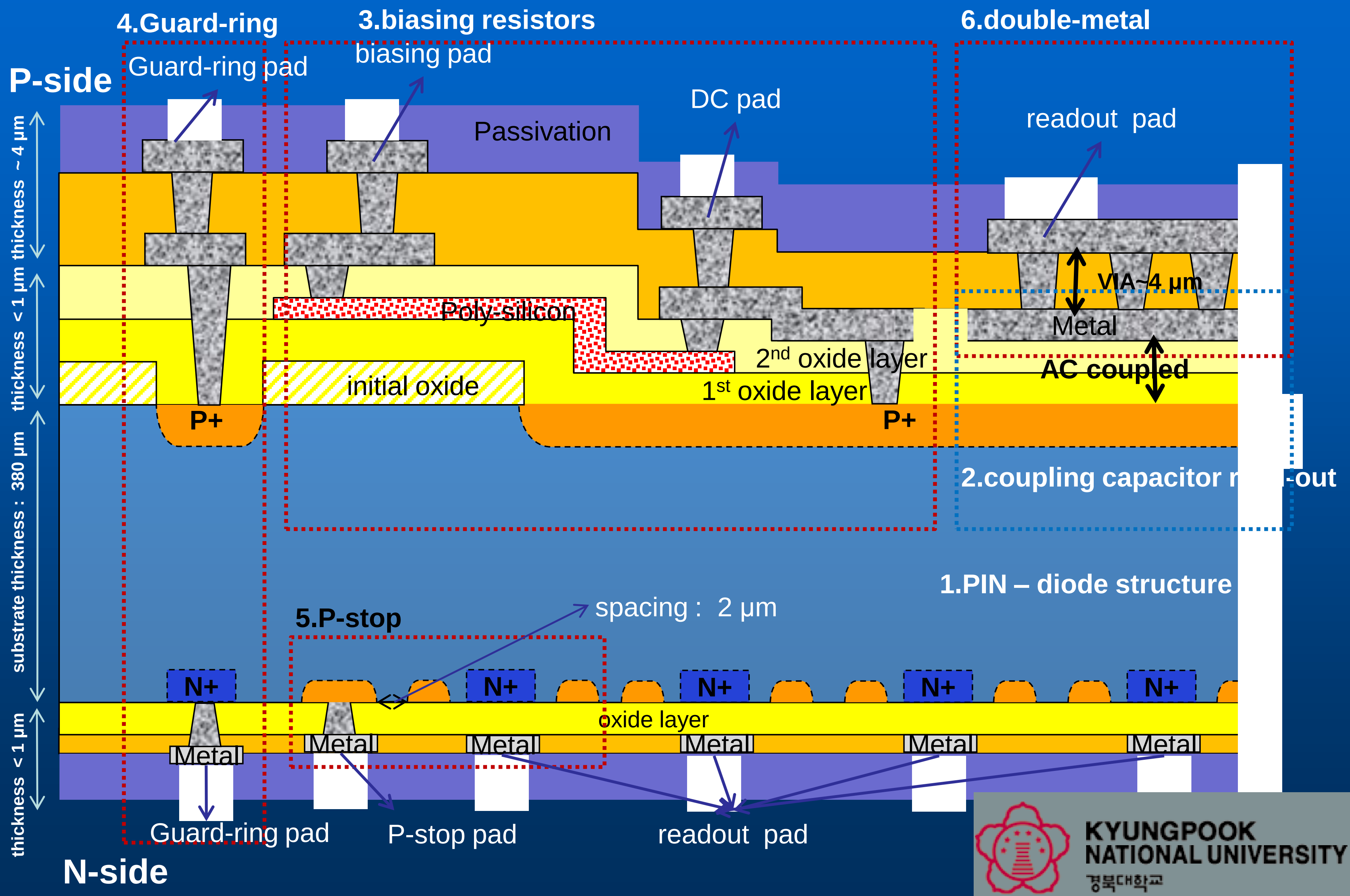
Trapezoidal sensor with test structures



- ❖ These sensors were delivered in July by MICRON
- ❖ Electrically characterized at HEPHY
- ❖ Tested at the SPS test beam less than 2 weeks ago; analysis in progress.

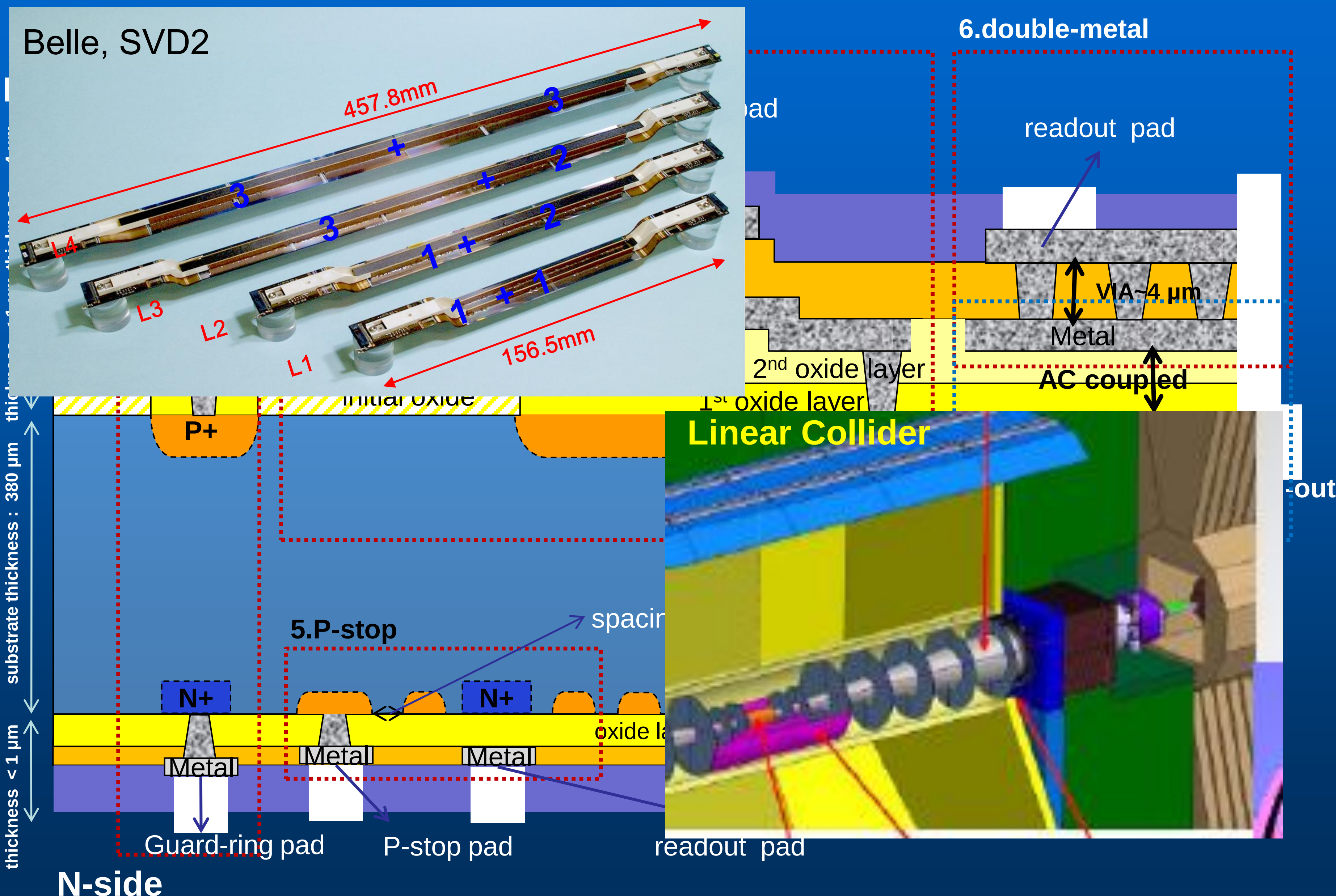
NOTE: These trapezoidal DSSD sensors could be a good baseline for the 4 last FTD disks

New developments on "standard planar strip" in Korea (KNU & ETRI)



KYUNGPOOK NATIONAL UNIVERSITY
경북대학교

Goals for these new sensors



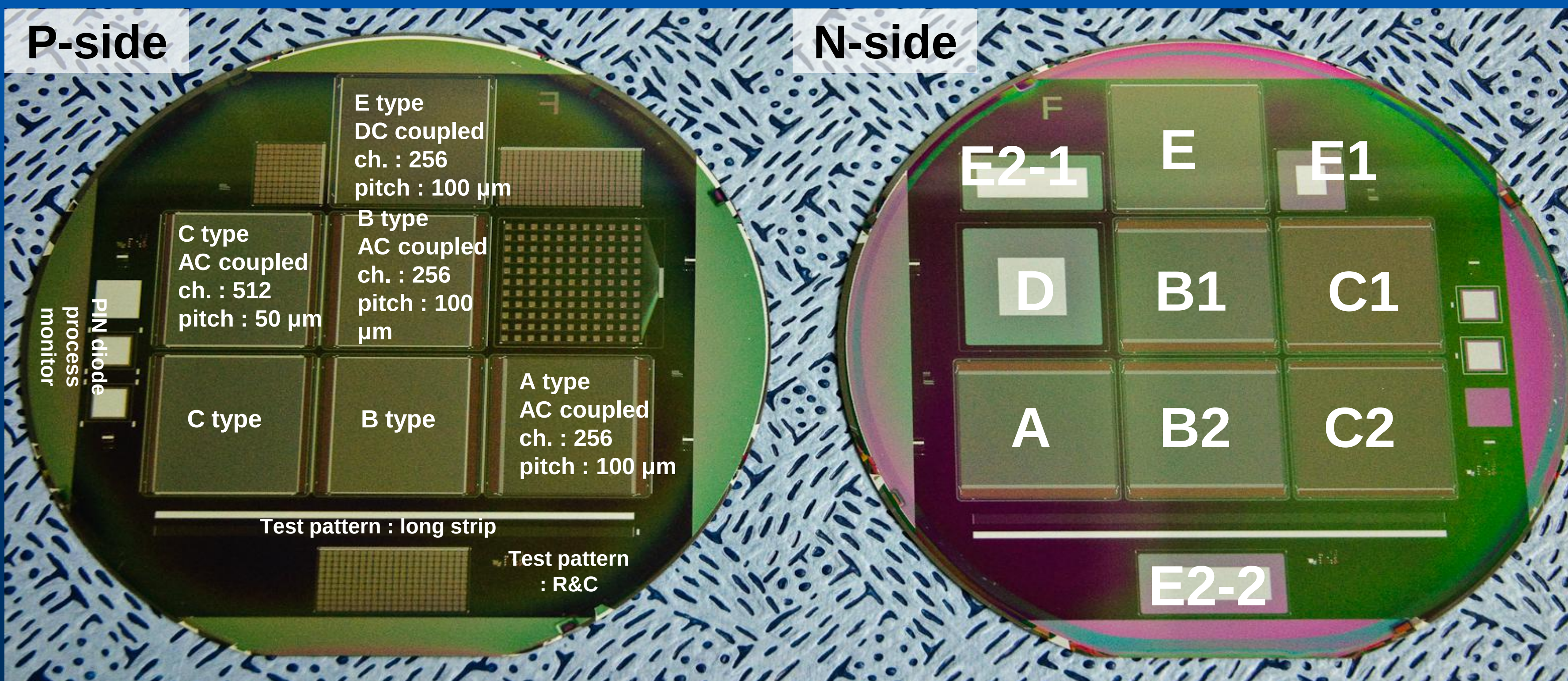
Sensor type		Size (cm^2)	No. of ch.	Pitch (μm)
Single-sided	DC-coupled	3.5 × 3.5	32	1000
		3.8 × 2.8	64	200
	AC-coupled	3.5 × 3.5	64	500
		3.8 × 2.8	128	200
		3.8 × 2.8	256	100
Double-sided	DC-coupled	5.5 × 3.0	512	50
	AC-coupled	2.8 × 2.8	256	100
		2.8 × 2.8	512	50

KYUNGPOOK NATIONAL UNIVERSITY
경북대학교

Sensor prototypes:

- Fabricated in <100>, high resistivity
- 380μm, n-type, 5”/6” wafers
- Electrically characterized
- Tests Radioactive Source
- SNR>15

=> ETRI proven Fab. line



ETRI

NanoFab

Going to 8'' wafers

- **Fabrication facility in Korea**
  - **ETRI** is proved to be good fabrication facility (5/6'' wafer process)
  - We discuss the **NanoFab center** for production of DSSD (8'' wafer process)

    - **could not get the high resistivity double-sided polished 8'' wafer**
    - **decided using the single-sided polished high resistivity 8'' wafer**
    - **and did mechanically polishing the other side**
    - **takes more time than what we expected (still in fab.)**
    - **this is their first time doing DSSD fabrication on 8'' wafer**

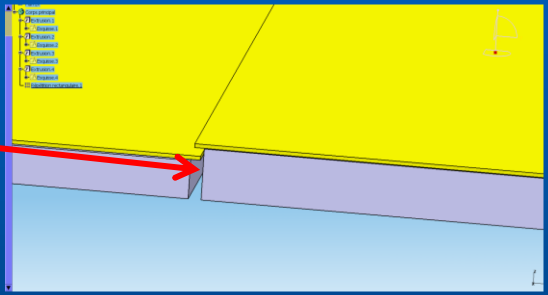
Here also competition between founders could be the best way to get 8" wafer techno

Edgeless strips sensors: Why?

Edgeless sensors decrease the non active edge regions of sensors (usually of a few hundreds of microns) down to about 10 to 20 µm.

Our interest in edgeless or active edge sensors is motivated by:

- ✓ allow building large area Silicon trackers seamlessly tiled detector matrices,
- ✓ thus no need for sensor overlap
- ✓ easier to build
- ✓ decrease of the material budget
- ✓ improvement of the tracking performances both in momentum and spatial resolution.



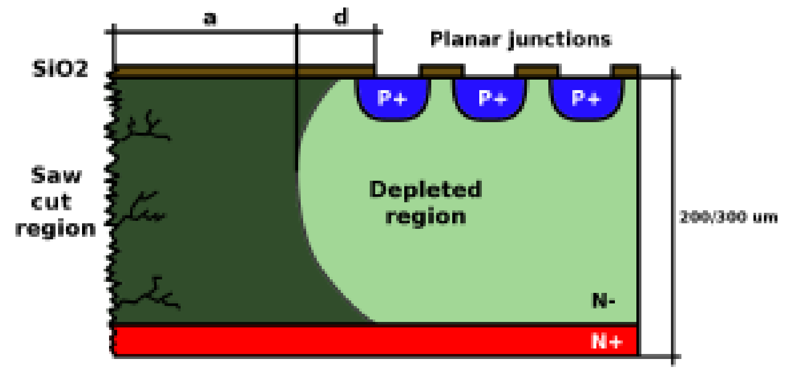
Two solutions based on the edgeless strip based on Edgeless planar and Edgeless SOI technologies are pursued.

EDGELESS STRIP SENSORS

courtesy Dalla Betta & Povoli

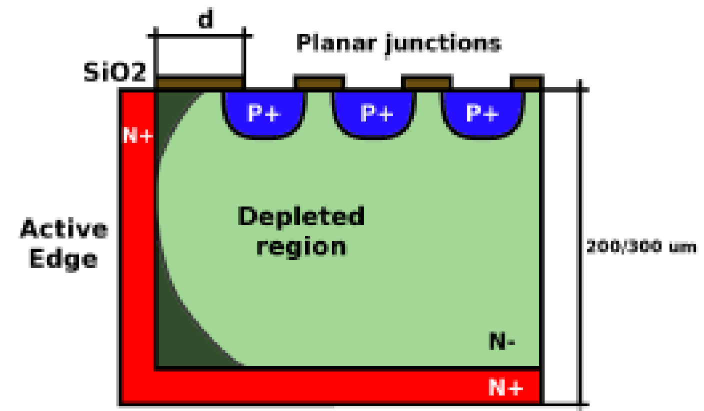
Standard detectors

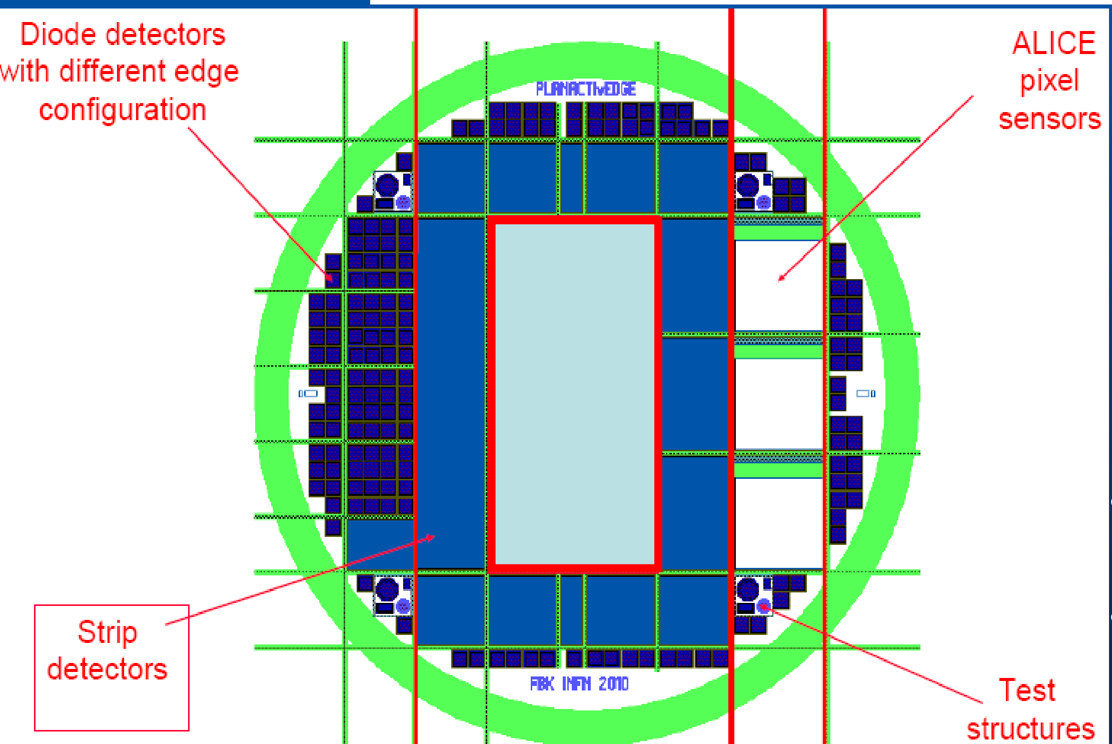
- In standard detectors a dead border region must be present
- In a good design cracks and damages on the edges should be at least at a few hundreds of micrometers away from the depleted region
- Total dead region **a + d** $\geq$ **500**μ**m**



How to limit dead region?

- Cut lines not sawed but etched with Deep Reactive Ion Etchin (DRIE) and doped



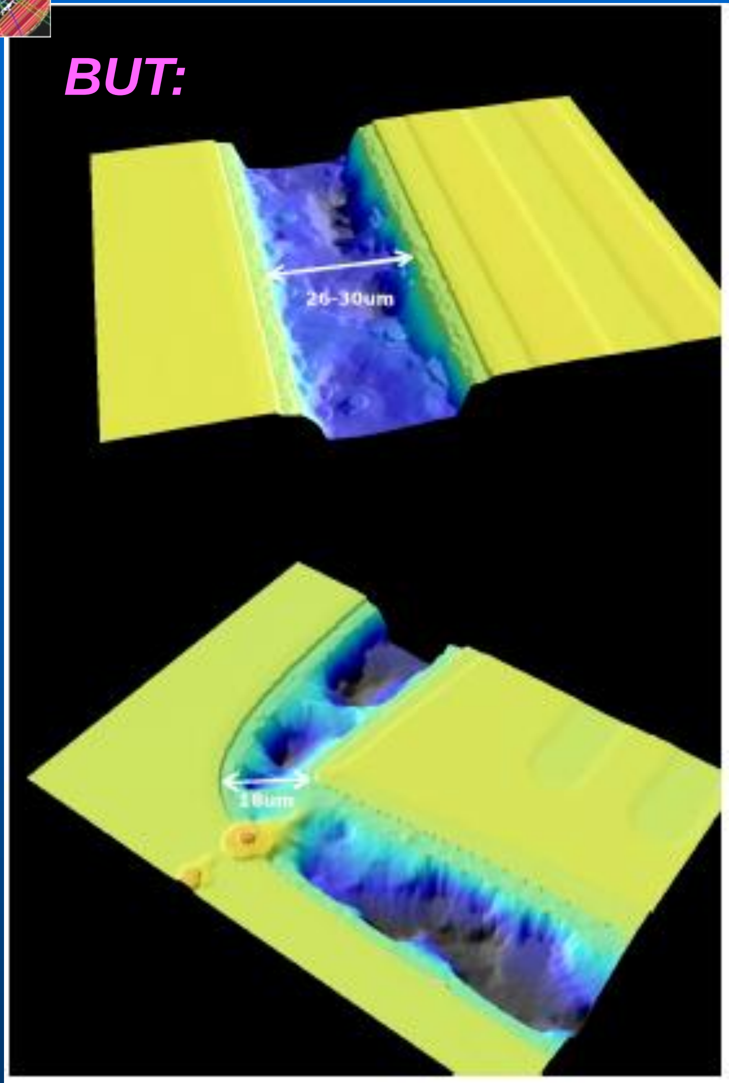


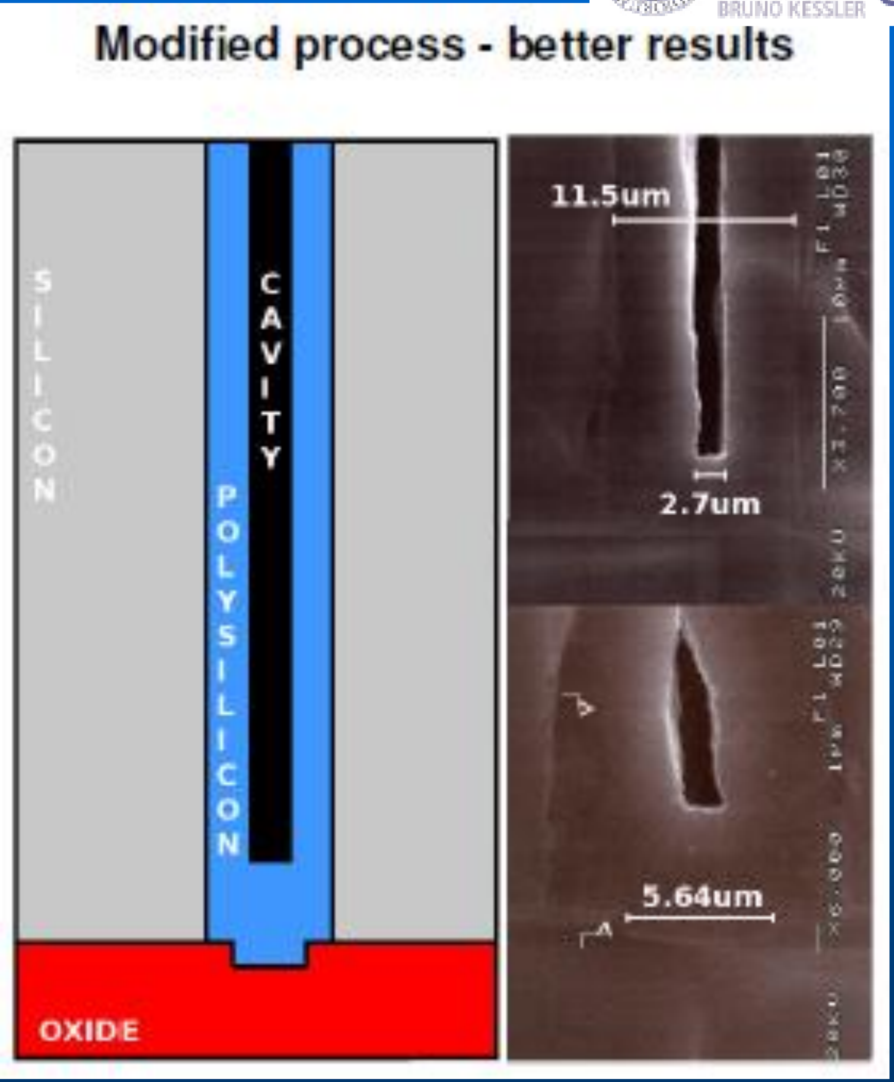
Problems

- Process is more complicated
- Need for support wafer
- Finding the correct "**d**" to limit early break-down phenomena

- **Trench etching steps investigated on test wafers**
- **TCAD simulations for breakdown prediction**

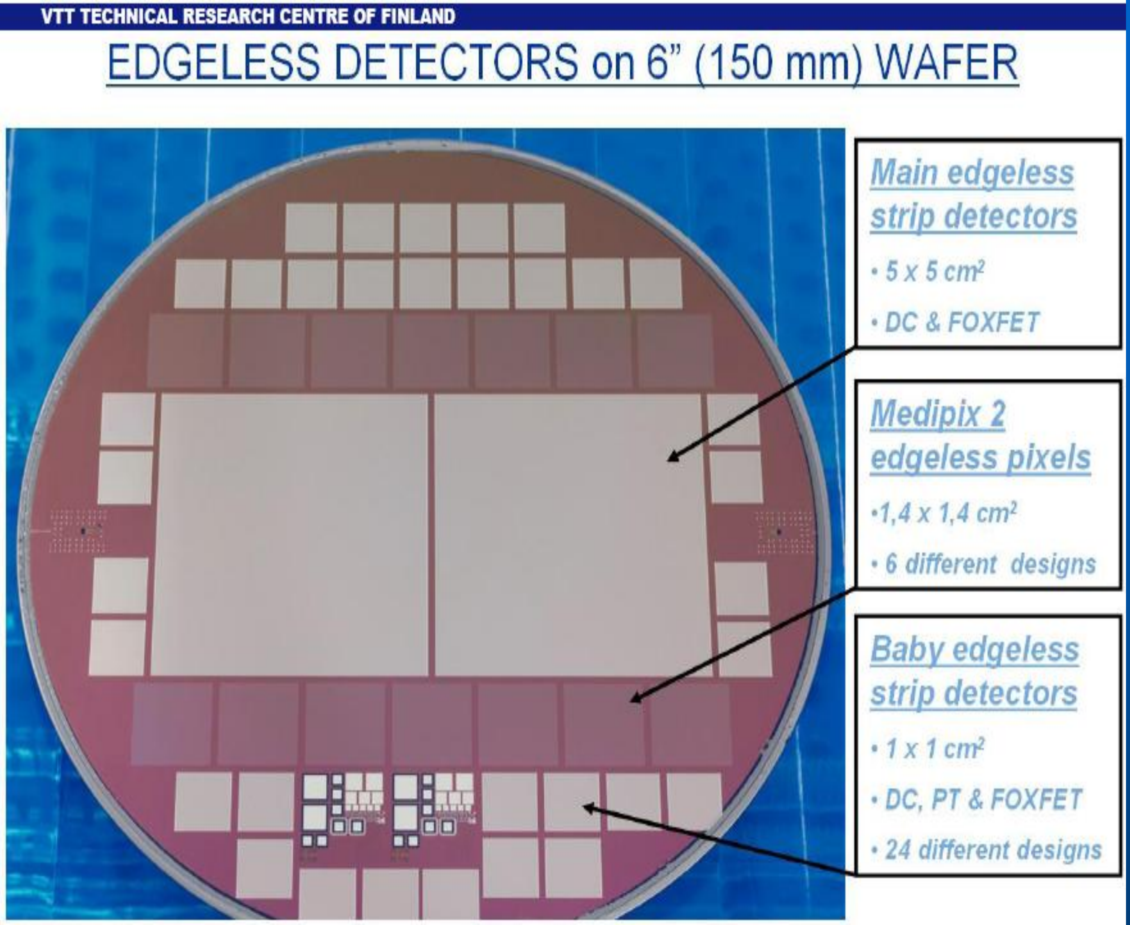
EDGELESS STRIP SENSORS





The previous batch didn’t went as expected => new batch is being made & will be submitted to electrical tests. If OK will be delivered for Nov tests.
Technology will still need some more prototypes to be optimized (next few years)

SOI-like Edgeless strip detectors



VTT achieved fabricating:

- edgeless strips & pixels sensors
- on 6'' SOI wafer
- based on alternative fabrication process w.r.t 3D processing with poly-Silicon filling
- Easier & more feasible fab. line.
- Two different designs produced: p-on-n and n-on-n
- Electrically characterized:

CV, IV and breakdown voltage

- **2 sensors DC coupled delivered**
- **2 AC coupled will be delivered for Nov run**

Alternative Fab. →

- **No need for polySi filling, planarization & separate ICP dicing**
- **Fast process and no bowing of the wafer**
- **Detector sustain handling – no edge cracking**
- **Physical inactive edge region ~ 1µm**
- **Requires non-planar lithography => readiness available at VTT**

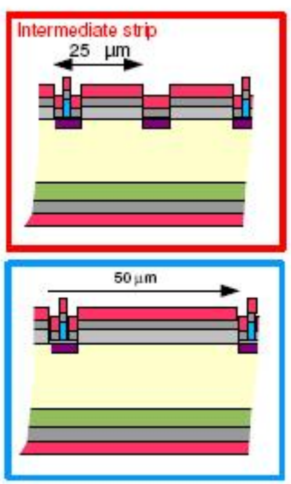
High Transmittance strip sensors

- **Transparent sensors for Si-tracker position monitoring (AMS idea)**
- **R&D line – Improve photodetection characteristic of “conventional”microstrips**
- **Two handles:**

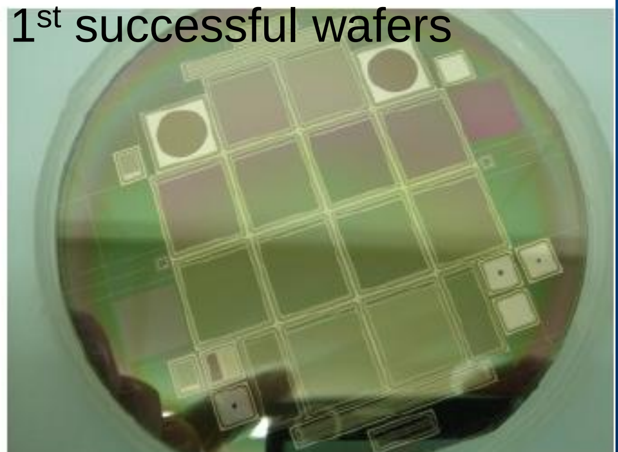
- Replacing non-transparent Al electrodes by a Transparent Conductive Oxide (ITO, AZO, Poly)
- Adjusting the layer thickness to reduce reflectance, including ARC in default sensor design.

Unique detailed simulation to study/optimize the sensors developments !!

- 5+1 wafers
- 12 μstrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50 μm RO pitch (25 μm interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3,5,10,15 μm)

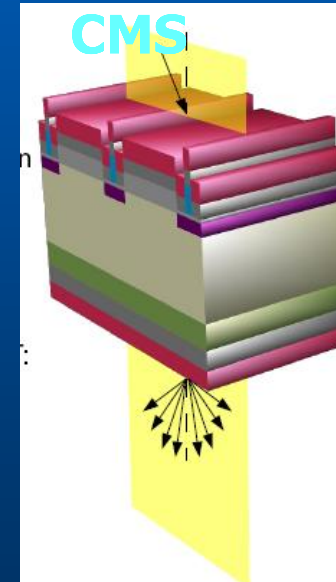


1st successful wafers



After last passivation layer
Tmax about 60% (7 layers)

Compare with 20% @ CMS



See M. Fernandez’s talk

Strip sensors are the baseline

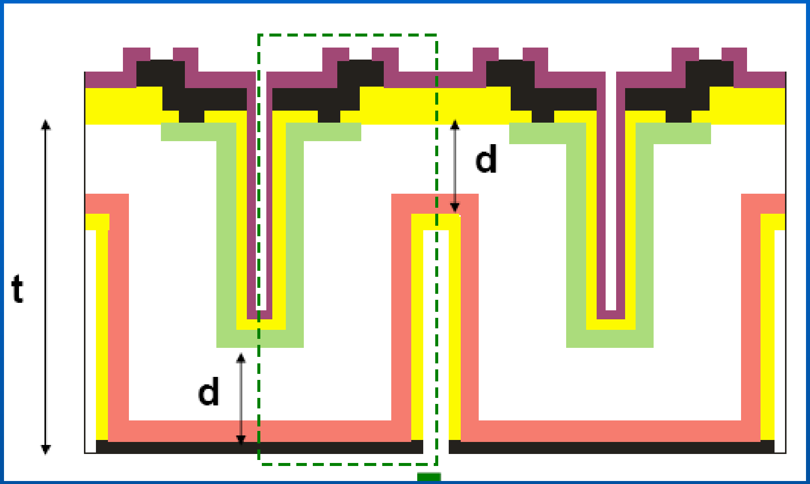
- But SiLC is also keeping an opened eye on smaller sensors: 3D strixels and pixels
- The long term objective could be to mix sensor types => “hybrid Si detector”
- or an all-pixel’ tracker as proposed by Ch. Damerell

Will be starting to be studied with simulations

at the same time new sensors are tested in T.B.

Strixels & pixels prototypes

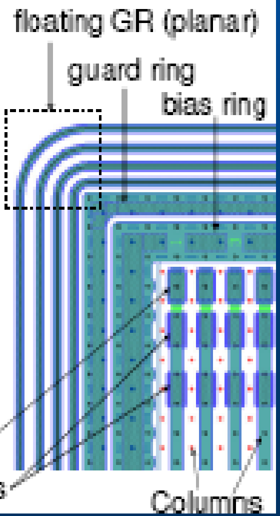
3DDTC-2b produced by FBK



Microstrip detector features

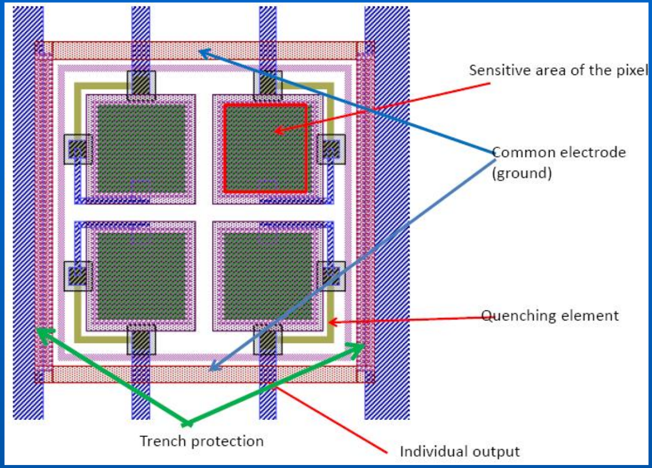
Substrate thickness	220	µm
Junction column depth	120	µm
Back column depth	190	µm
Lateral depletion	~20	V
Strip leakage current	~1	nA
Strip capacitance	~7	pF
Coupling capacitance	50	pF

102 x 102 columns array
80µm inter-column pitch

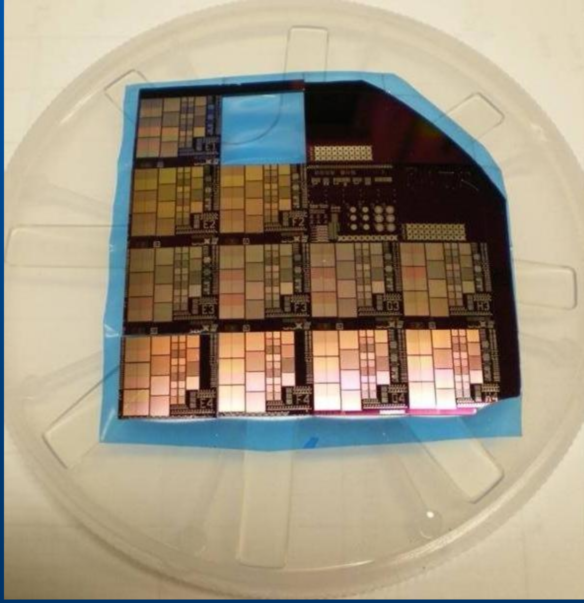


Delivered, to be tested in 2011.

SiPM-based sensors (NRNU): to be tested in Nov.



SPT pixels
(see Ch Damerell's Talk)



I.- R&D BASIC OBJECTIVES

- R&D on sensors
- **R&D on FEE and READOUT**
- RELATED MECHANICAL ISSUES

F.E.E. General description

Baseline: Full readout chain integrated in one chip developed in two steps

EUDET BASELINE

- Preamp-shaper
- Sparsification : Trigger decision on analogue sums
- Sampling : 8-deep sampling analogue pipe-line
- Analogue event buffering: : Occupancy: 8 deep event buffer
- On-chip digitization : 8-bit ADC
- Calibration and calibration management

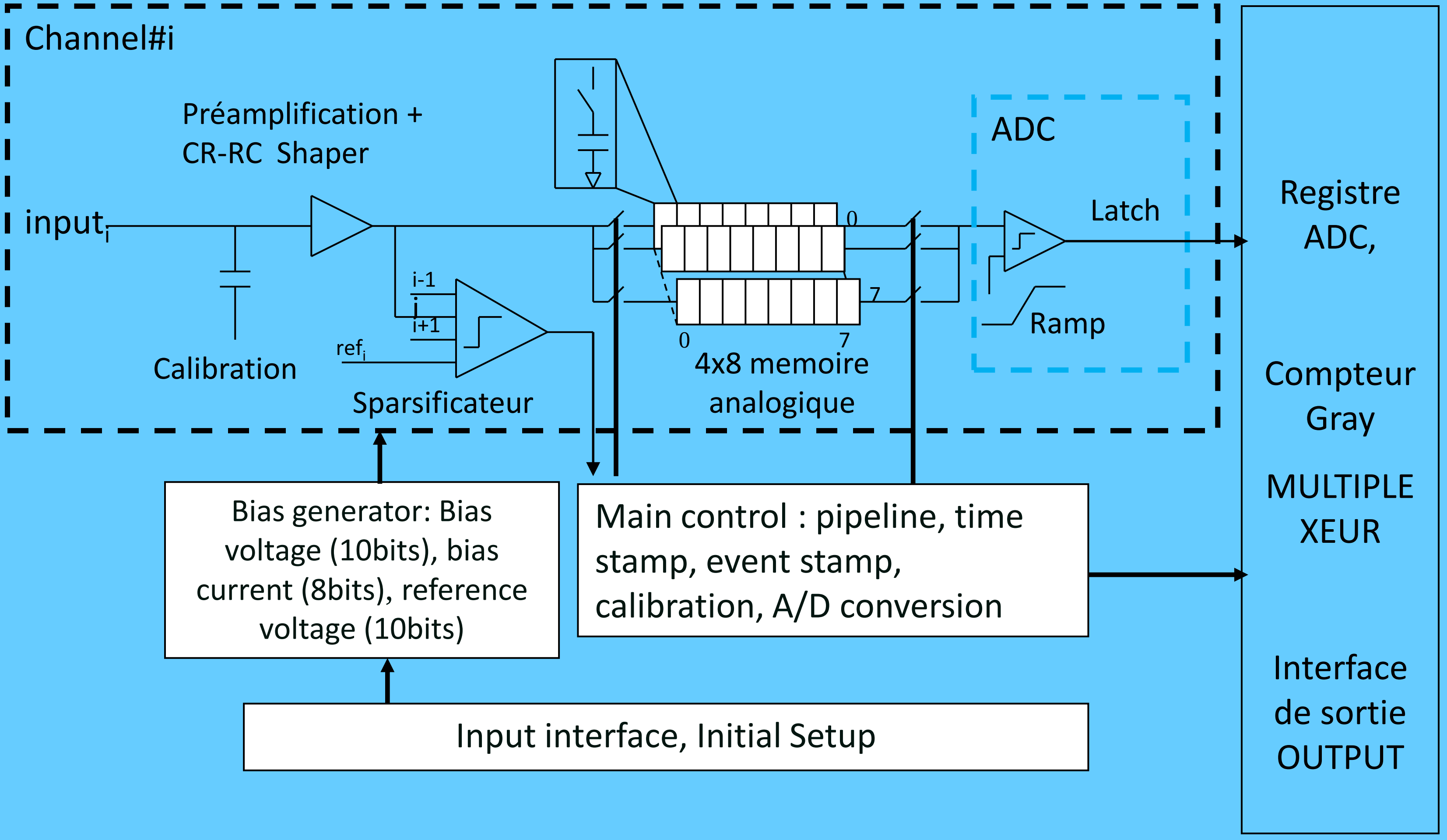
BEYOND

- *Full digital handling of the chip running operation*
- *Power switching (ILC duty cycle)*
- *Fault tolerance*

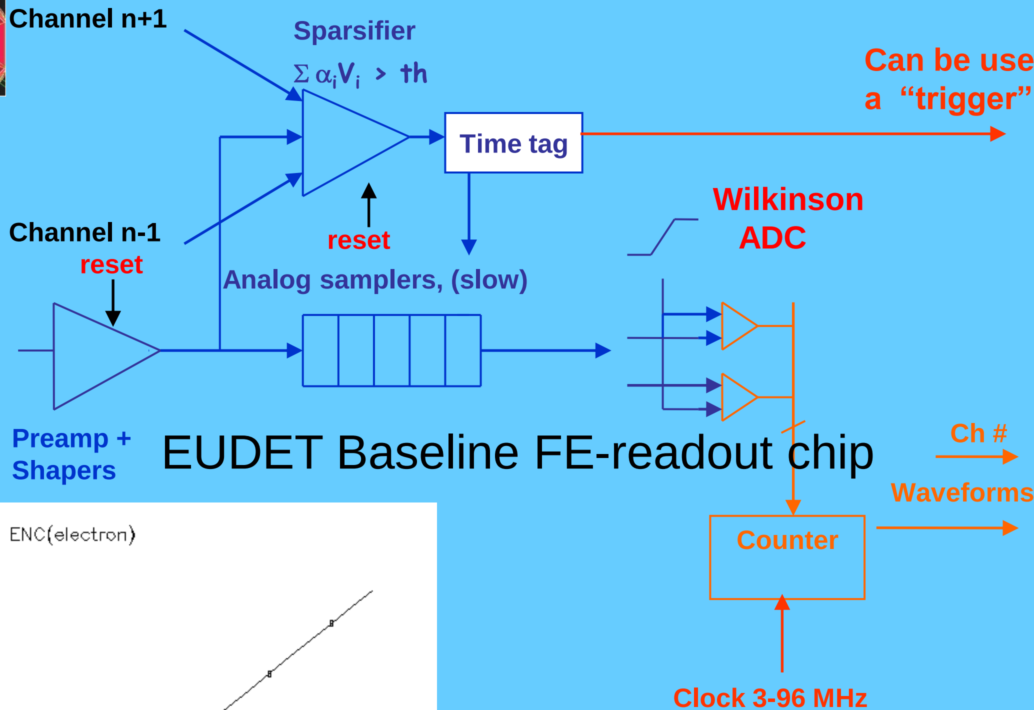
In addition: two “conventional” FE ASIC: VA1’ and APV25

Developed up to now: the ILC case (slow machine) starting the work on the fast cycle case (see later)

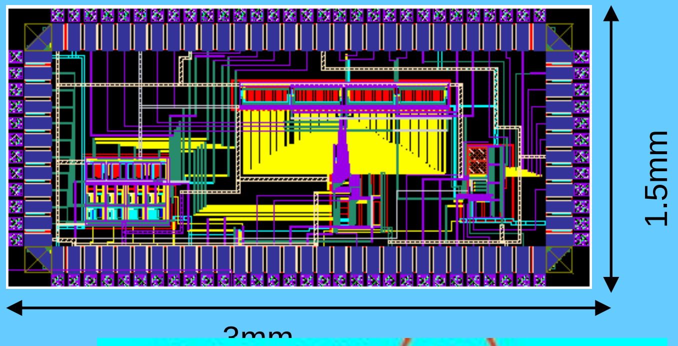
Ultimate goal: Developing a mix-mode FE readout with pulse-height reconstruction, zero suppression, full digital control (highly fault tolerant, flexible/robust) power cycling, in DSM CMOS technology

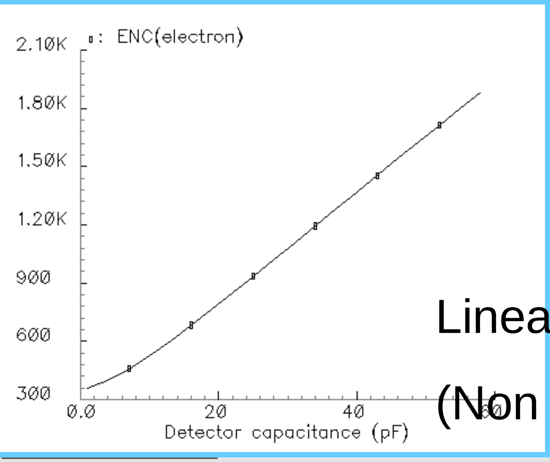


SiTR_130-4



EUDET Baseline FE-readout chip

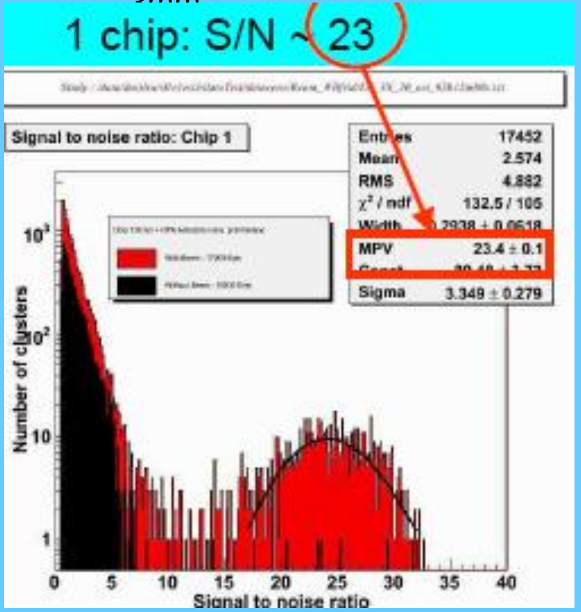


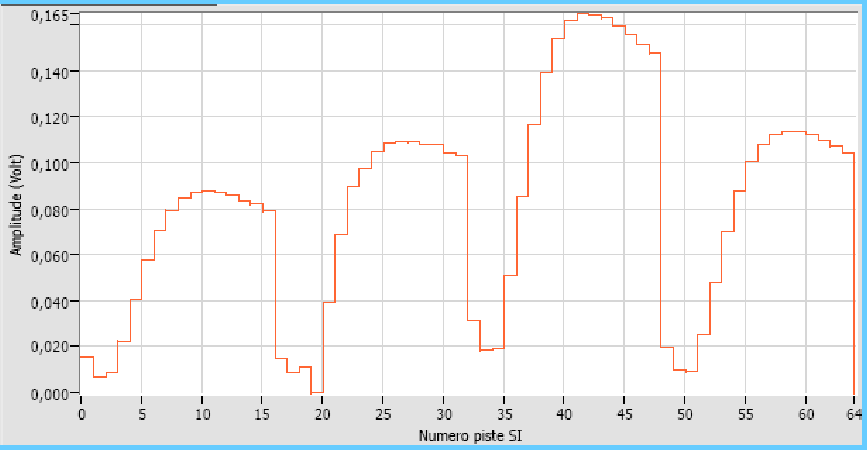


Linear up to 23MIP

(Non linearity 5%)

SPS-CERN
Nov 2007





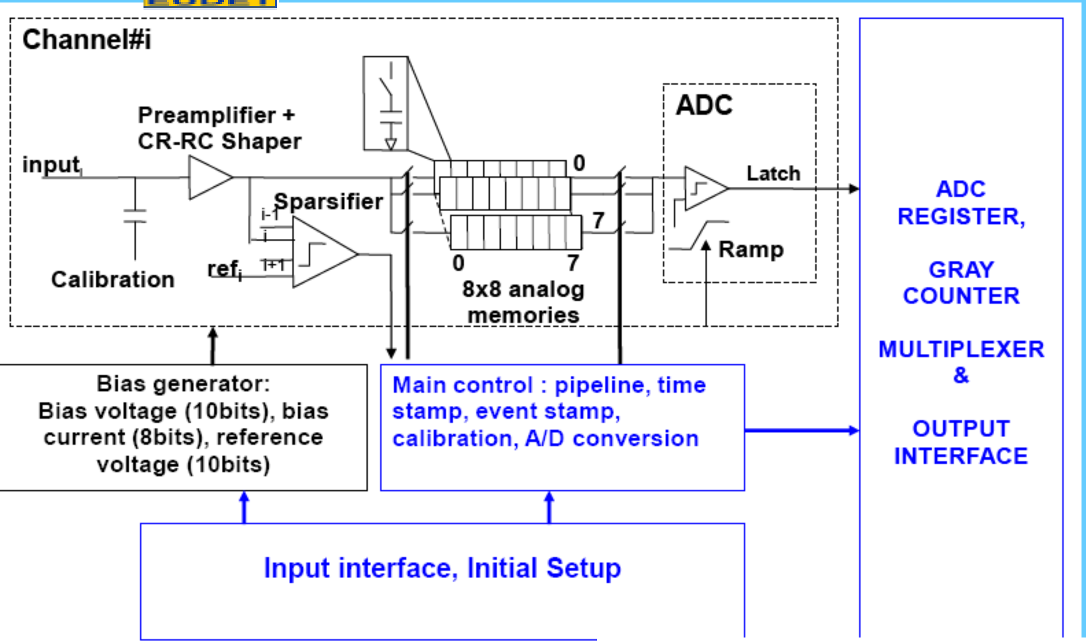
HPK sensor, MPV of S/N = 23

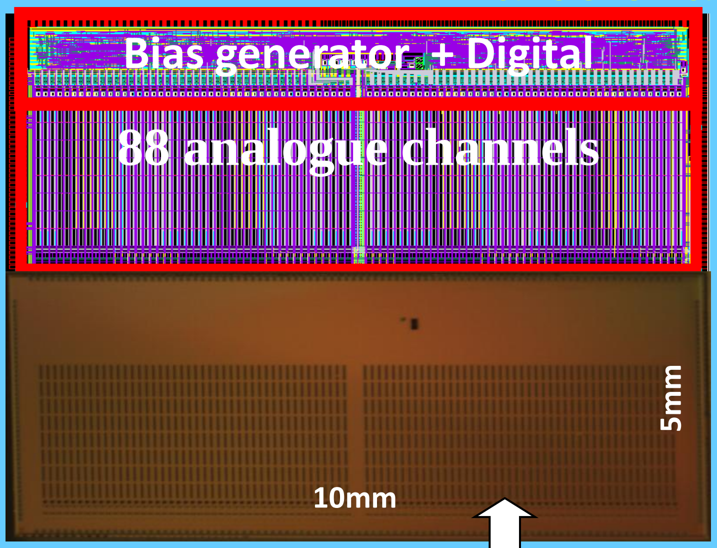
(4 channels clustering with refine algorithm)

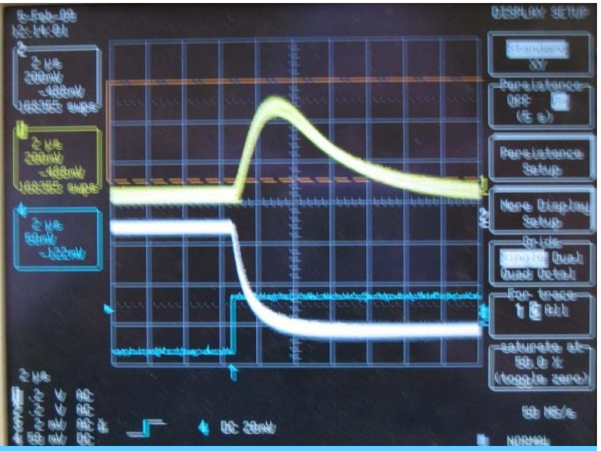
(9.15x2=18.3 cm strip length)

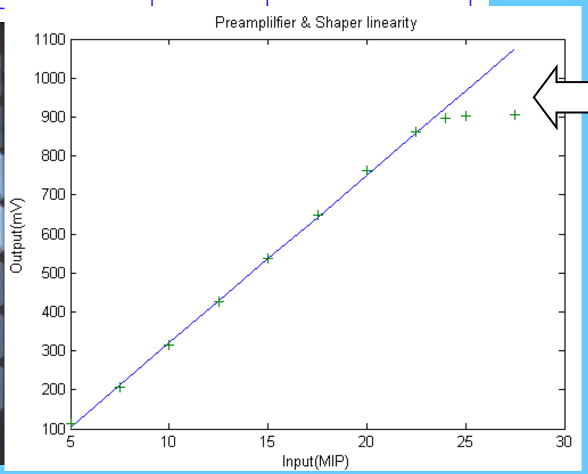
Beyond #1: SiTR_88-130UMC version

Barcelona U.









SiTR_88-130 first full mixed mode analogue/digital achieved Using DSM CMOS UMC 130nm

Analogue part well within the specs.

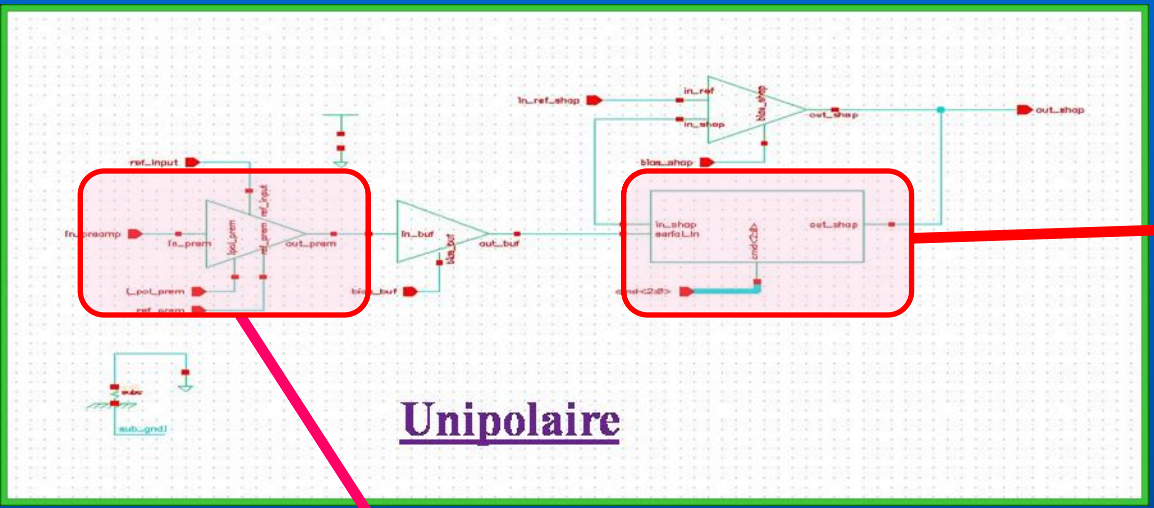
Overall power dissipation per channel: 1.2mWatt

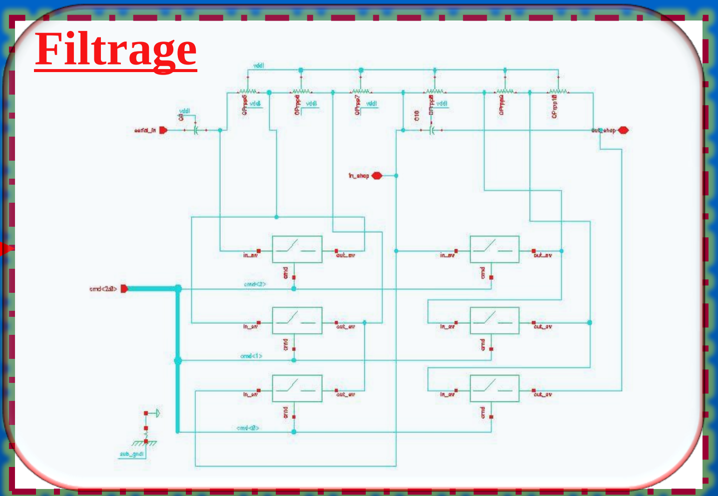
BEYOND #2: Development of SiTR_130IBM-128 full mix mode FE readout ASIC

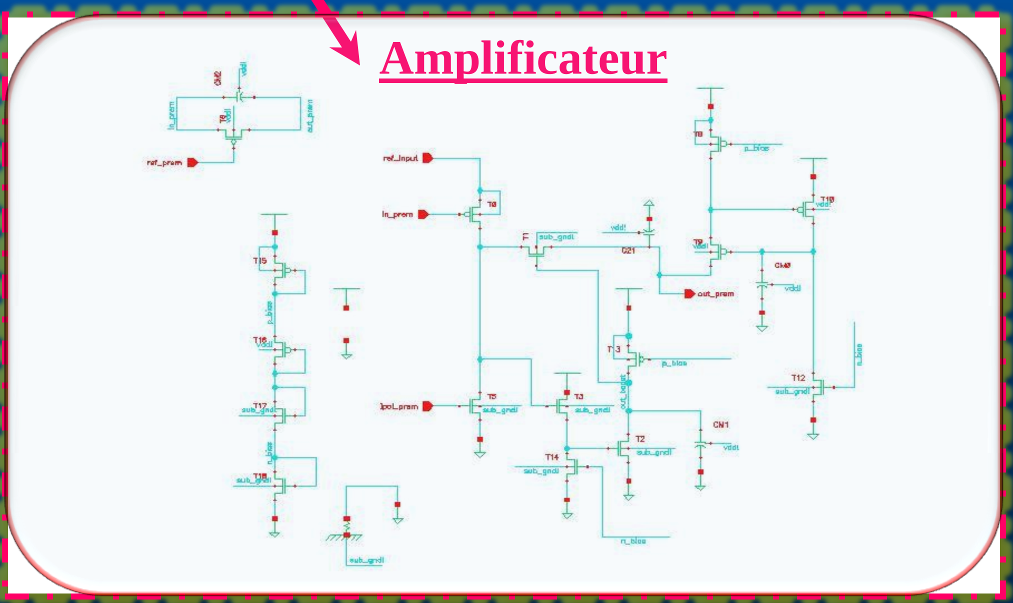
1st step: SiTR_BLOCS

- Revised Design of the main components of the analogue FE architecture of the SiTR ASIC, following the recommendations of the Review Committee of March 15, 2010 (International experts from CERN and E.U. Institutes).
- Work performed at LPNHE with collaboration of Microelectronics Pole Alsace (T.H. Pham & Software experts) and CERN Microelectronics Group
- CMOS IBM 130 nm (1.5 V)
- 3 different amplifier-shaper designs (CR-RC programmable; 3 bit)
- Single ramp Wilkinson ADC (8 bits)
- Analogue memory cell with write/read switches.
- Successfully submitted to IBM Foundry via CERN on June 15

Amplifier - Shaper V1







Gain : 19.4 mV/MIP

Sh _Time: 600ns – 1us

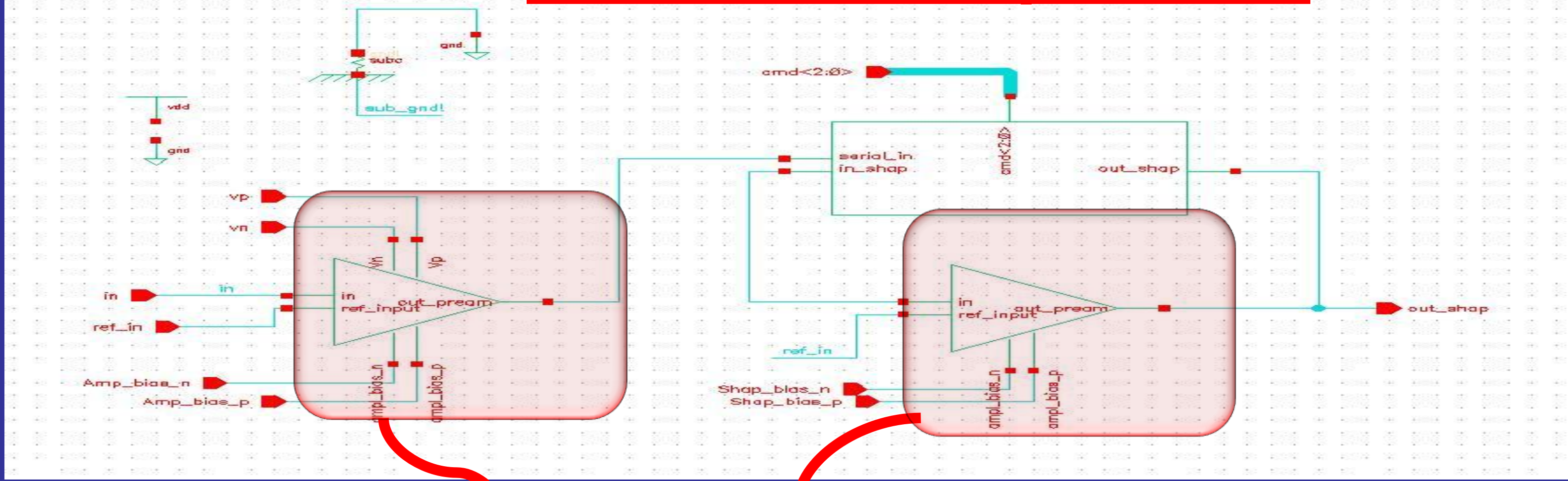
Noise @ 1 us : ~ 346 + 19,5 e/pF

Linearity < 1% (15 MIP)

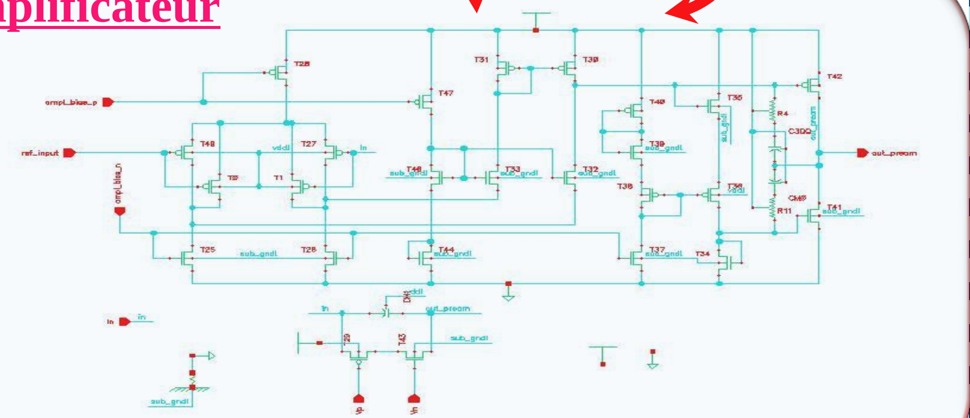
Power dissipation: 450 uW

Amplifier - Shaper V2

Différentiel en entrée et unipolaire en sortie



Amplificateur



Gain : 20 mV/MIP

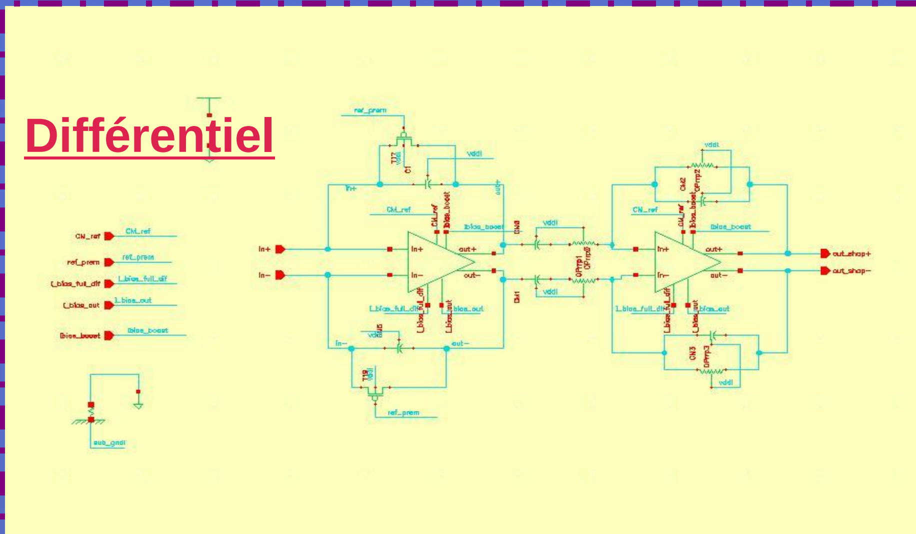
Sh _Time: 550ns – 1us

Bruit @ 1 us : ~ 189 + 18,9 e/pF

Linéarité < 1% (15 MIP)

Consommation : 334 uW

Amplifier - Shaper V3



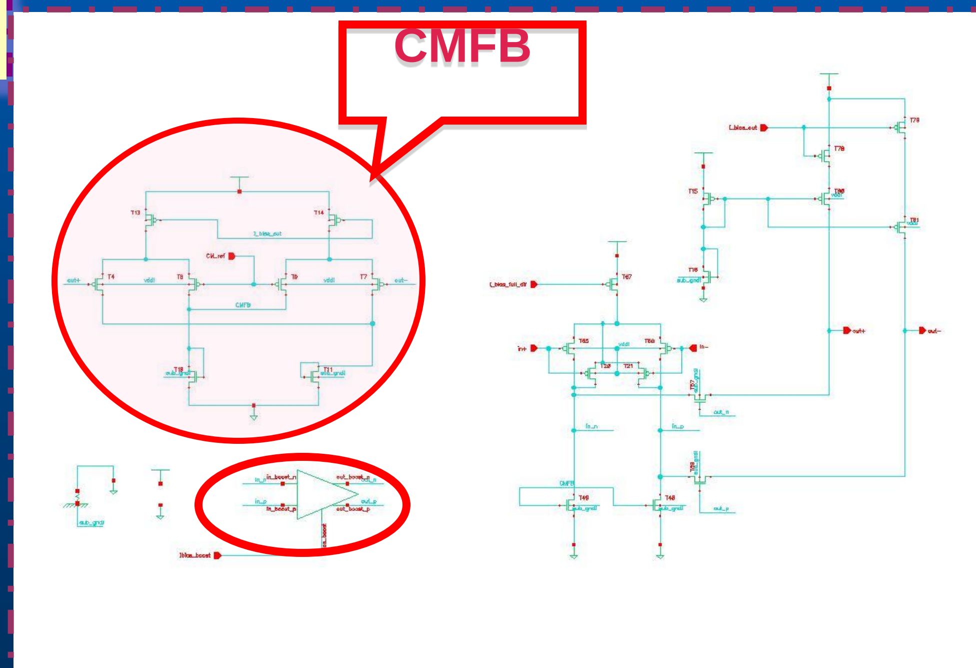
Gain : 20 mV/MIP

Sh _Time: 700 ns – 1 us

Bruit @ 1 us : ~ 698 + 17.7 e/pF

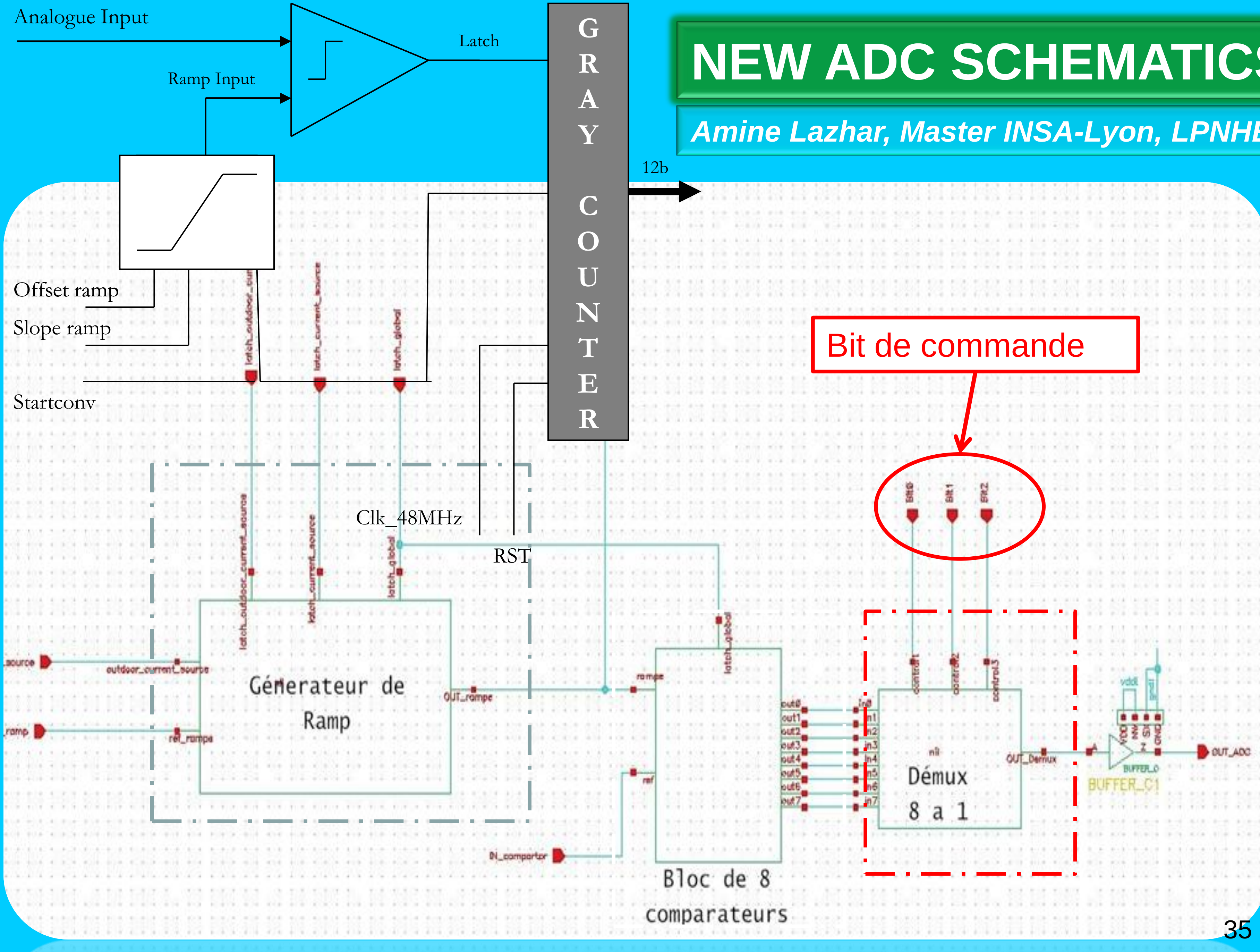
Linéarité < 1% (15 MIP)

Consommation : 540 uW



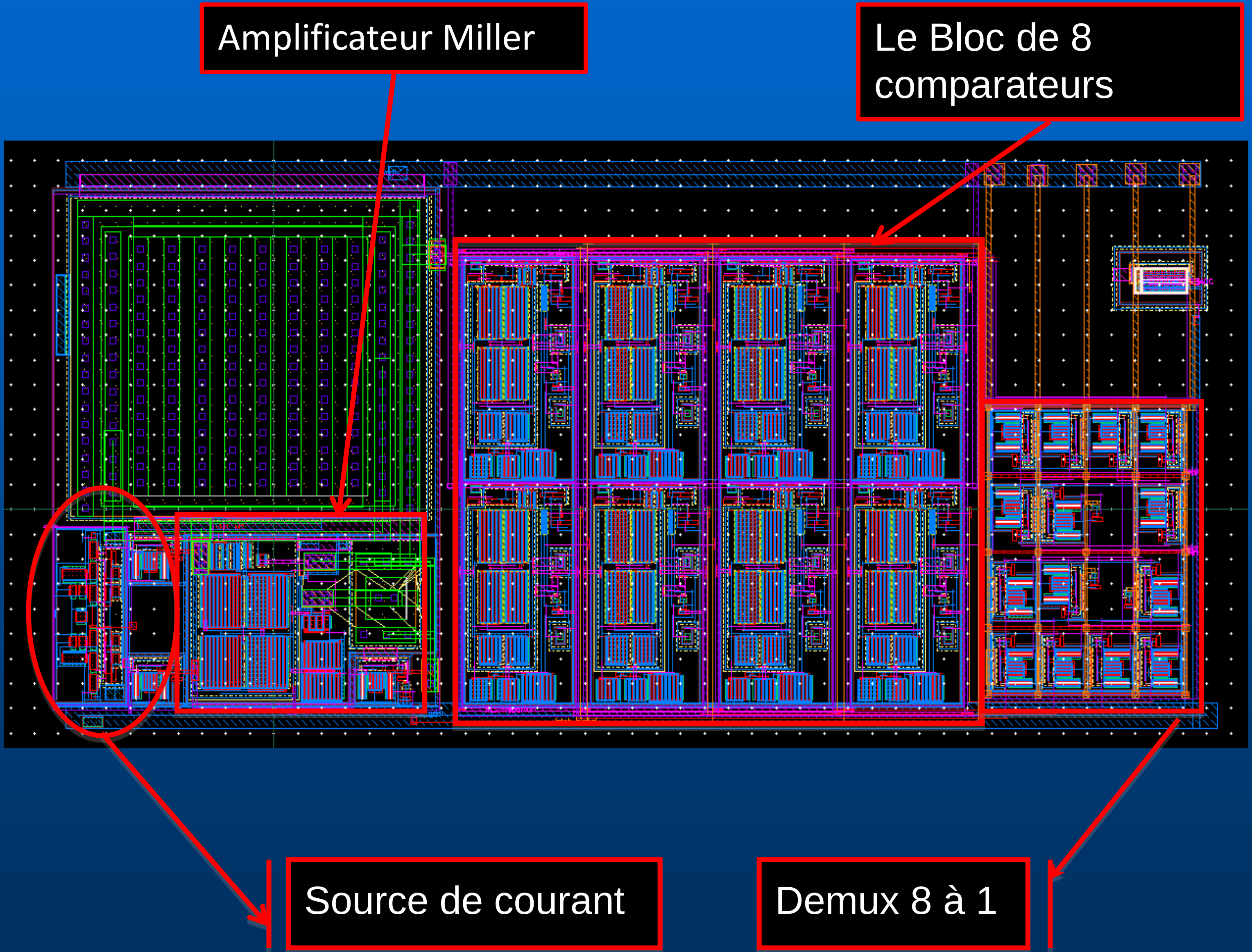
NEW ADC SCHEMATICS

Amine Lazhar, Master INSA-Lyon, LPNHE

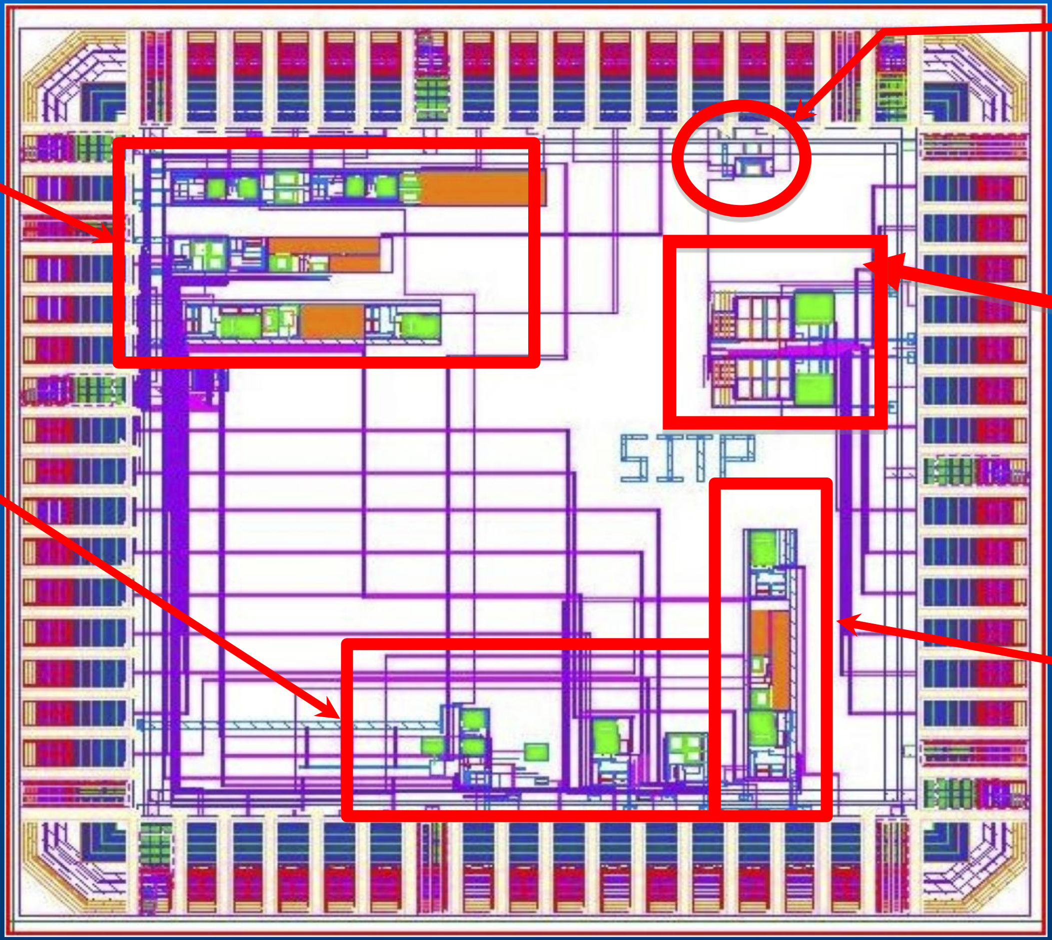


New ADC Layout

Amine Lazhar, Master INSA-Lyon, LPNHE



SiTR_Blocs Layout



3 solutions preamplifier - shapers

3 prototypes operational amplifiers

Analogue Pipeline Cell

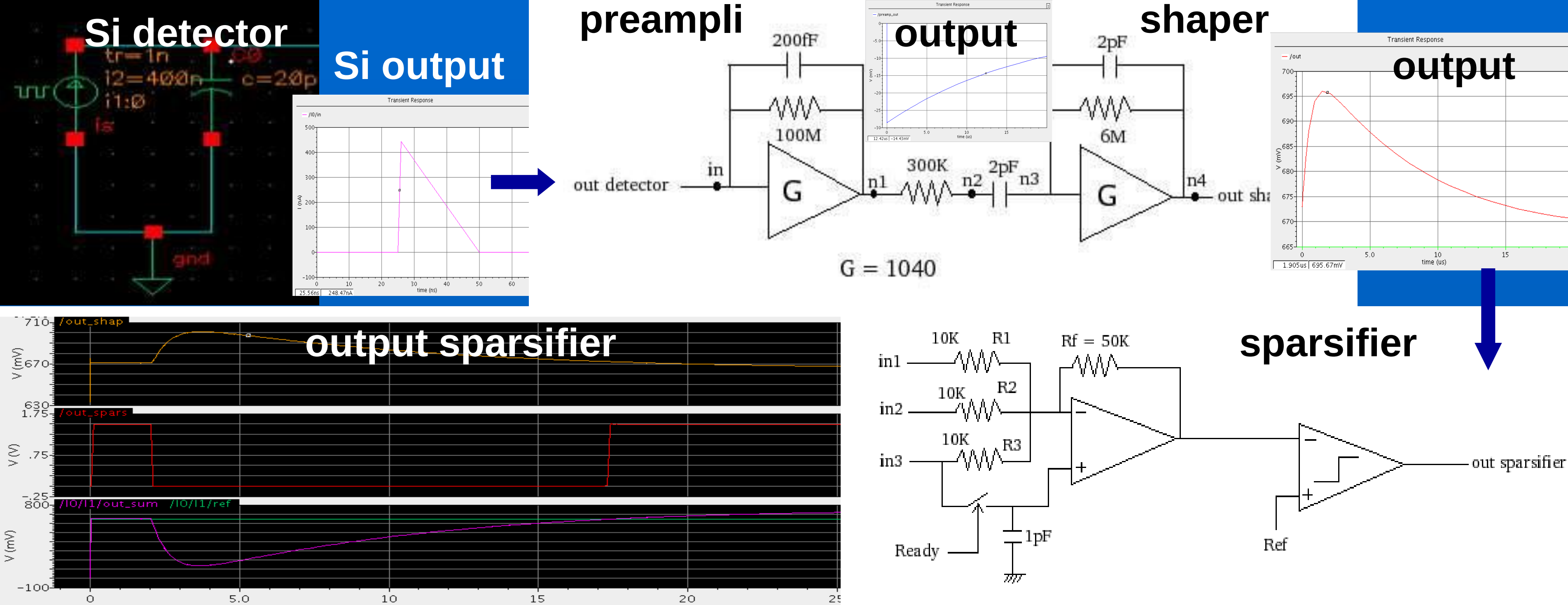
2 A/D solutions

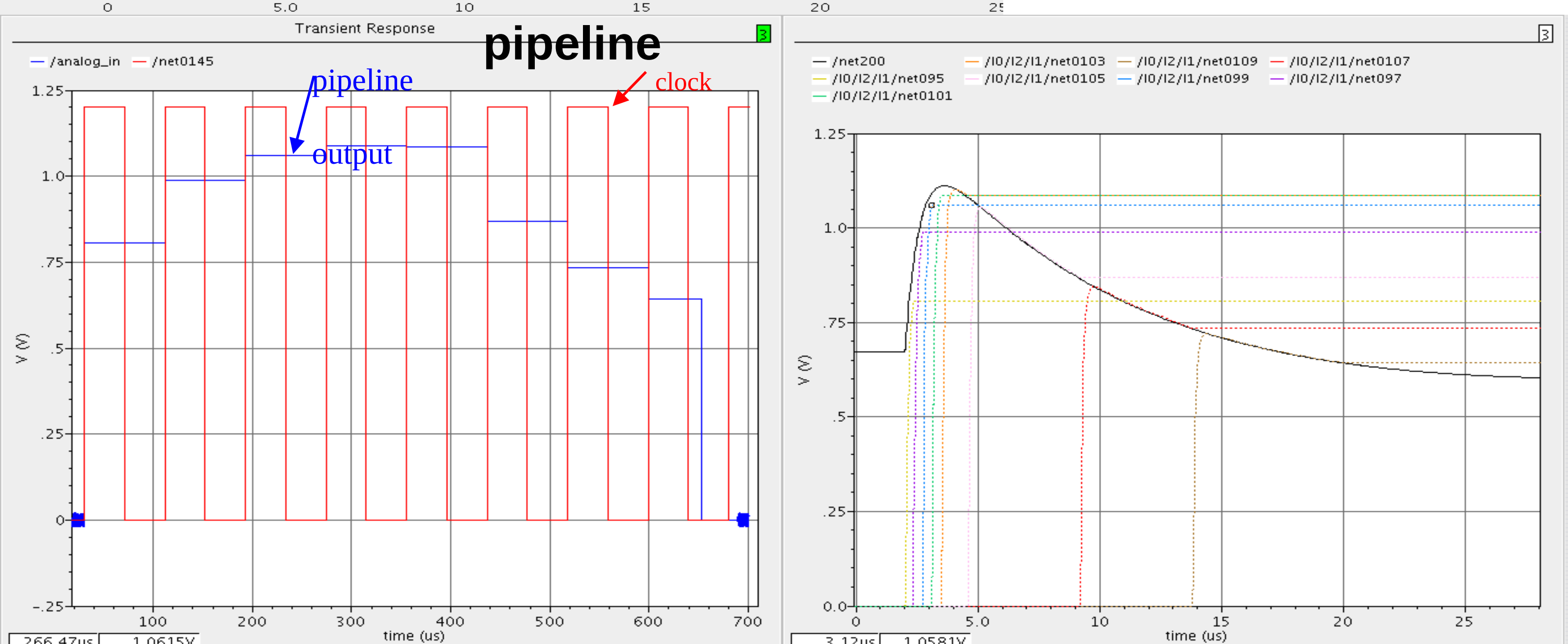
One prototype RC amplifier

Area= $4mm^2$

68 Pads (17 pads*4).

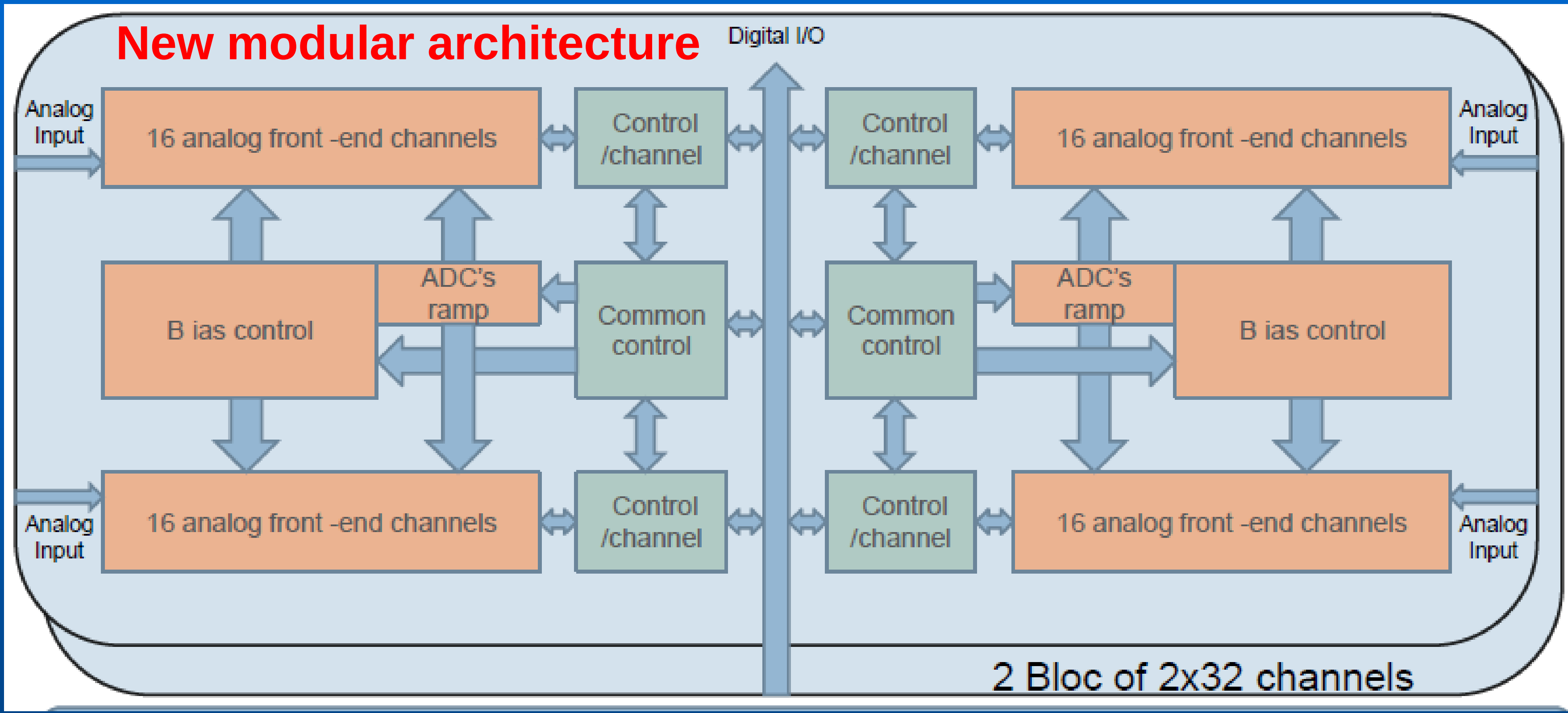
Submitted to IBM Foundry June 30, 2010





Mixed Analogue/ Digital => SiTR Chain Modeling

the 128 ch Si-FE ASIC



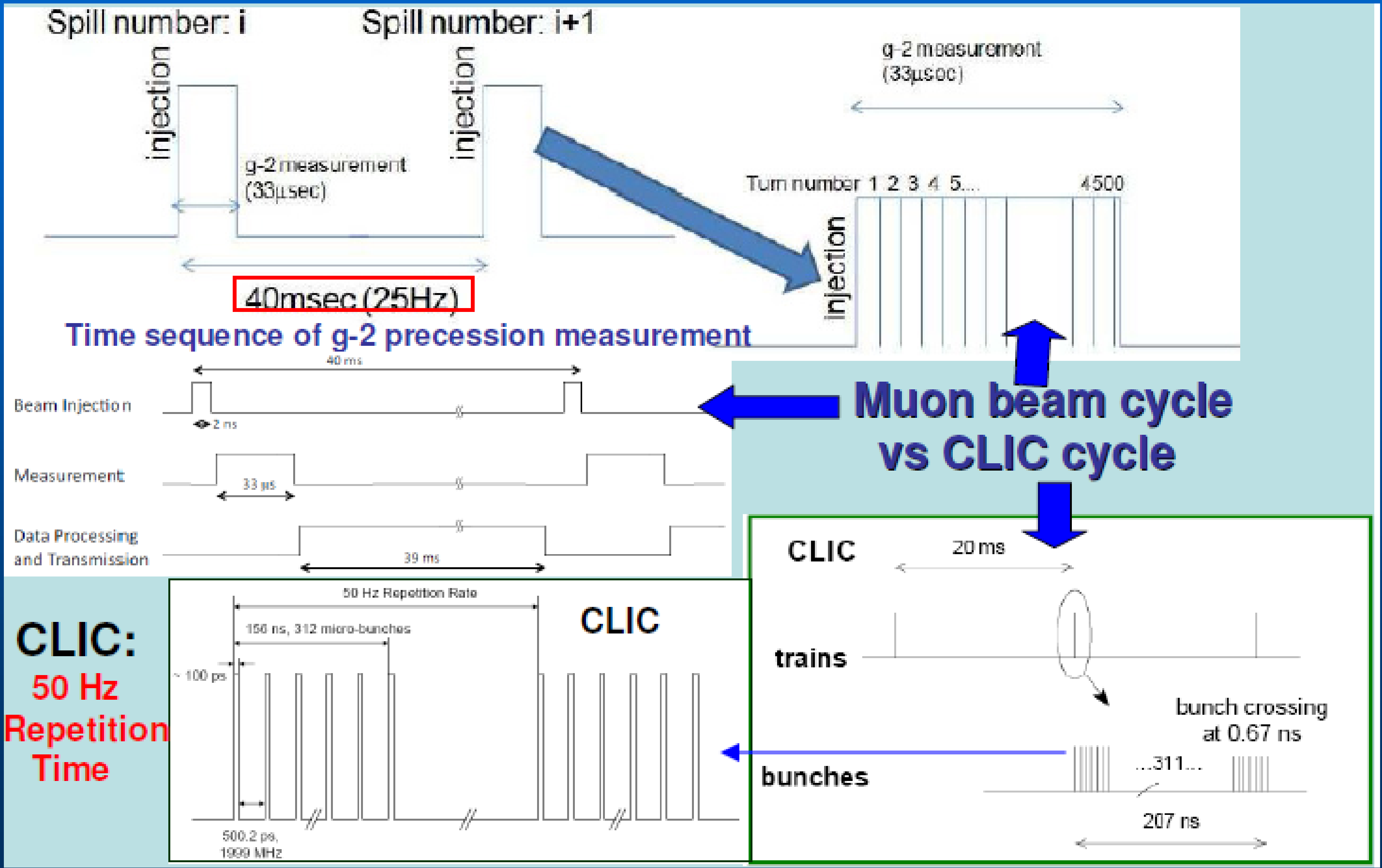
Beyond the SiTR_130-UMC deliverable achieved in 2007 with test beam on Si prototype, a new version is developed in two steps and aims to a full mix mode Analogue/Digital chip

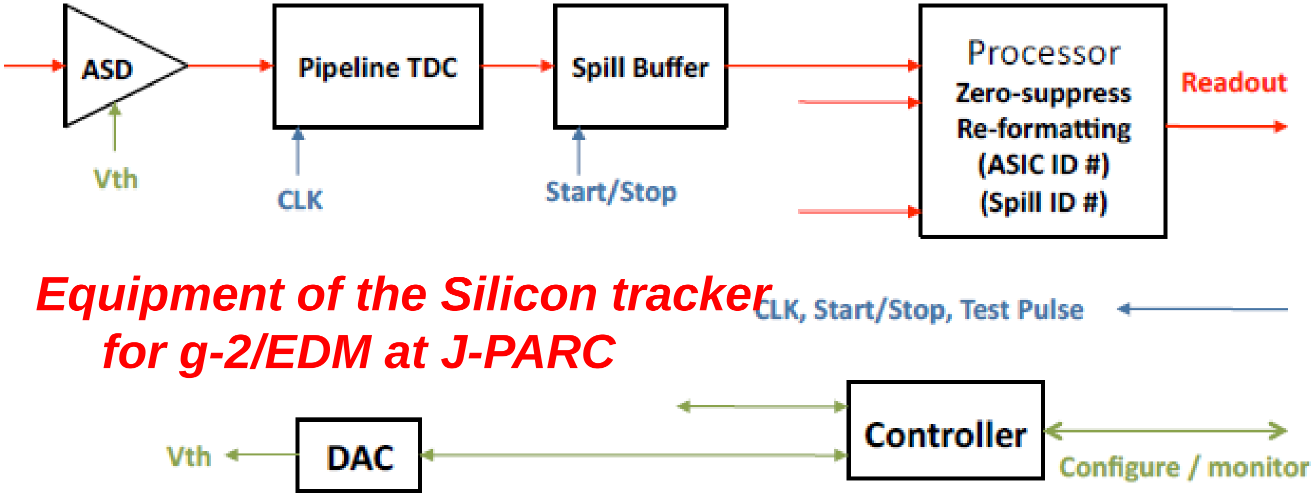
- The first step was keeping the UMC technology -> SiTR_130-88
- The second step now underway, with IBM-130 technology and upgraded analogue FE & digital parts will give the 128 ch ASIC. This chip will then be able to equip larger size Si prototypes, these coming years.

It is also requested for other applications (see next slide)

Muon g-2/EDM experiment projected at J-PARC is interested in an adaptation of SiTR to its case:

Comparison between time sequence of g-2 precession &CLIC cycle





Equipment of the Silicon tracker for g-2/EDM at J-PARC

New electronics

Shaping time ~20 ns

Peaking time

Noise <1000 ENC

Time stamp :

A few nsec

Power consumption

Power cycling?

Effect on B-field?

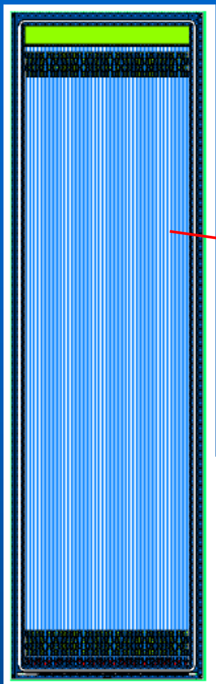
F.E. Items	*LC*	*g-2/EDM*
Machine cycle	Similarities CLIC	(See previous figure)
ASICTechnology	CMOS DSM	CMOS DSM
ASIC Architecture:		
• Mixed Mode	Yes	Yes
• Fast VFE	Yes (CLIC)	Yes
• Full signal processing	Yes	Yes
•Common blocks	ASD+pipeline storage	ASD+pipeline storage
• A/D	ADC	Wilk-ADC→TDC
•A/D Multiplexing Factor	≥128 (256)	128
Time stamping	Yes (two cases:10 ns or 0.1ns eventually CLIC)	Yes (2 ns)
Power cycling	Feasible	Feasible
Low power dissipation	Yes	Yes

130nm CMOS tech.

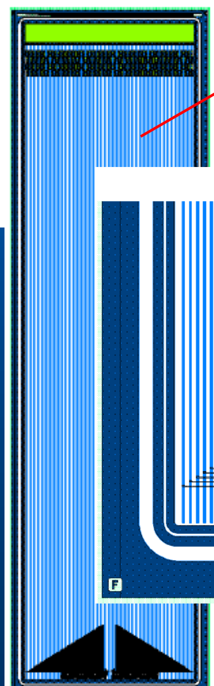
Many common points with ILC design & even more with CLIC

+ ITE (Poland)

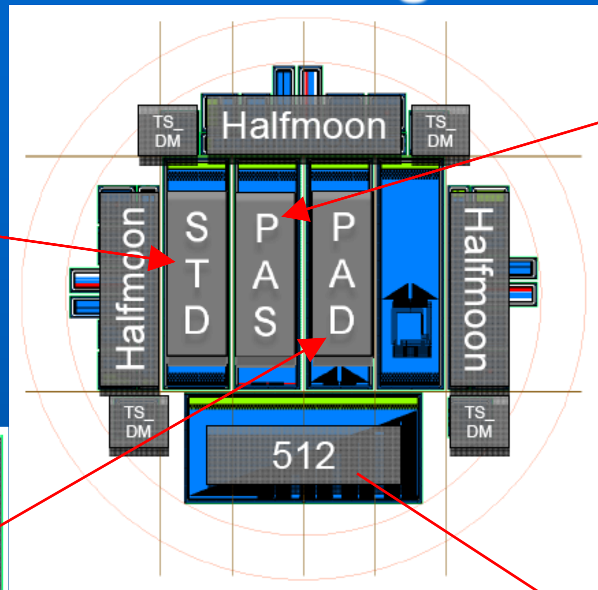
Sensors with integrated pitch adapters

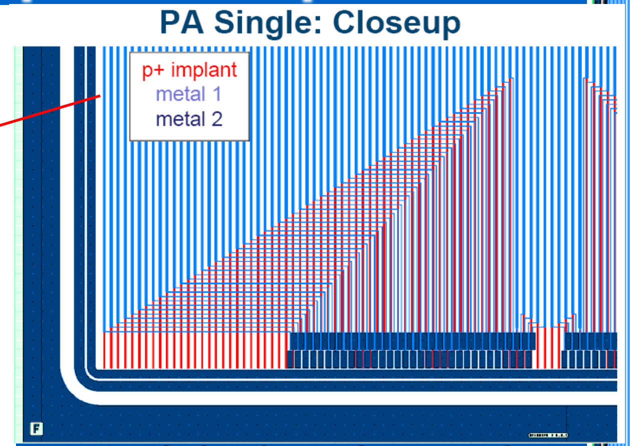


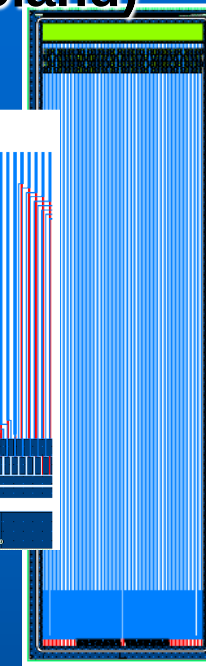
STA=standard



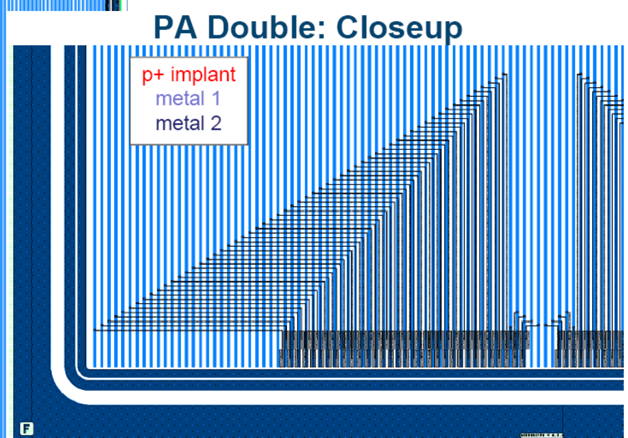
PAD=Pitch Adapter integrated with Double metal layer



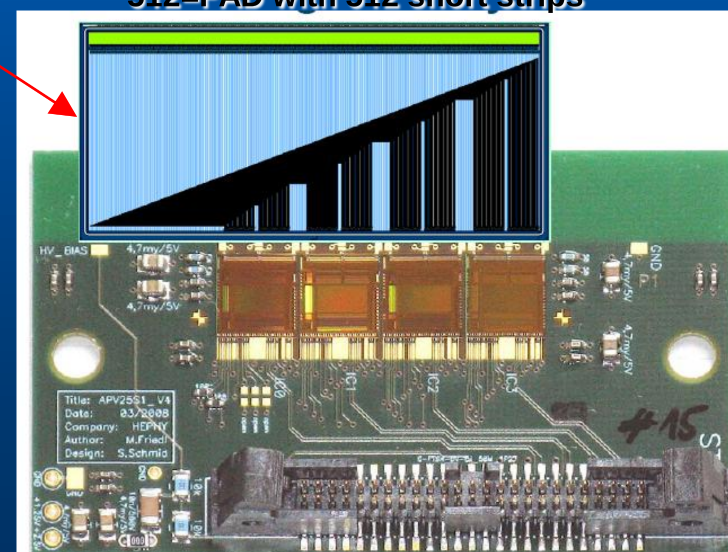




PAS=Pitch Adapter integrated with Single metal layer



512=PAD with 512 short strips

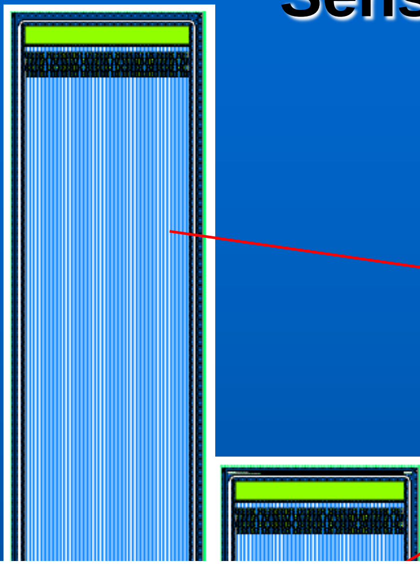


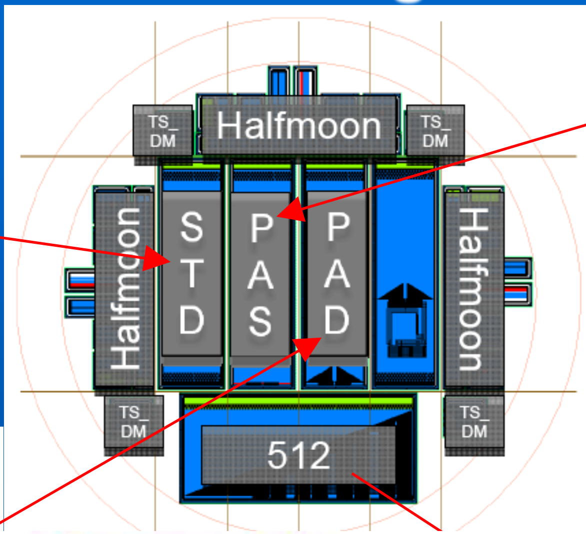
Courtesy of Th. Bergauer

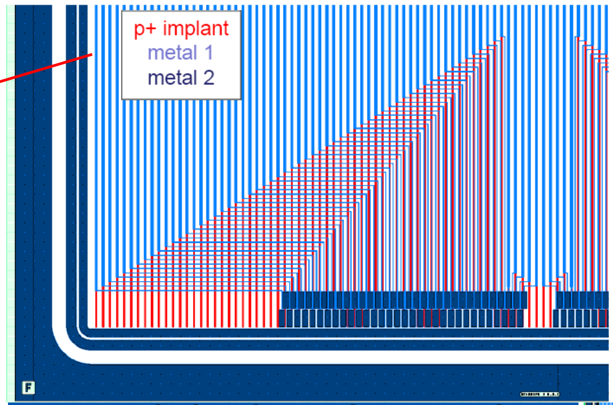
(Also under consideration for CMS upgrade)

+ ITE (Poland)

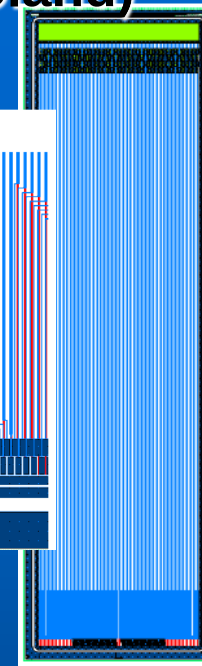
Sensors with integrated pitch adapters





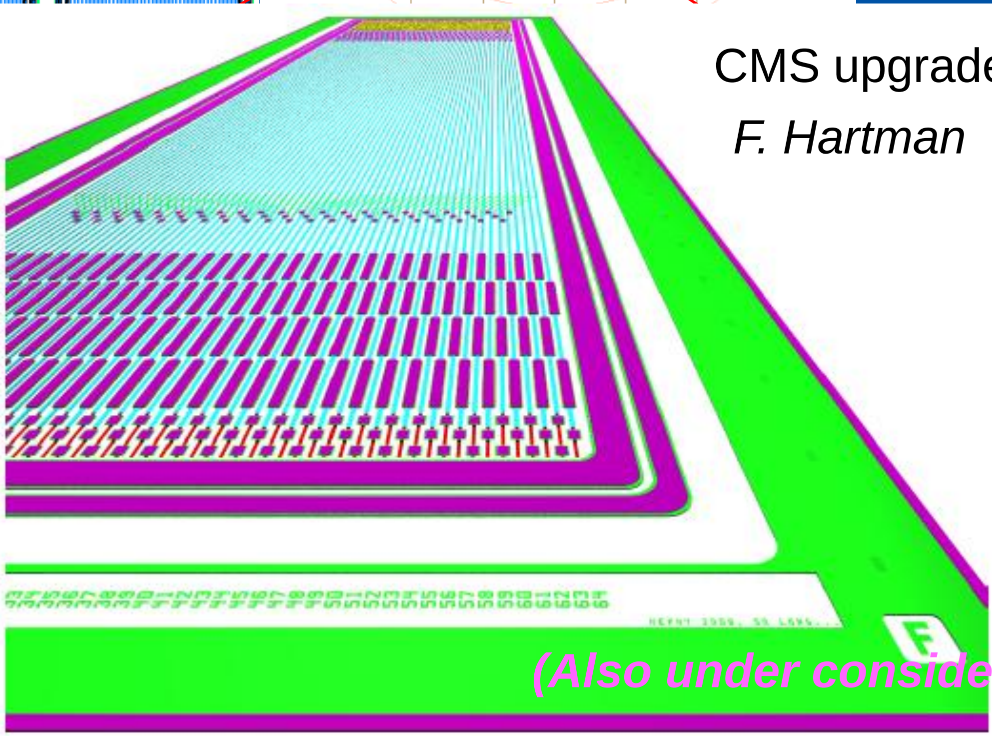


PAS=Pitch Adapter integrated with Single metal layer



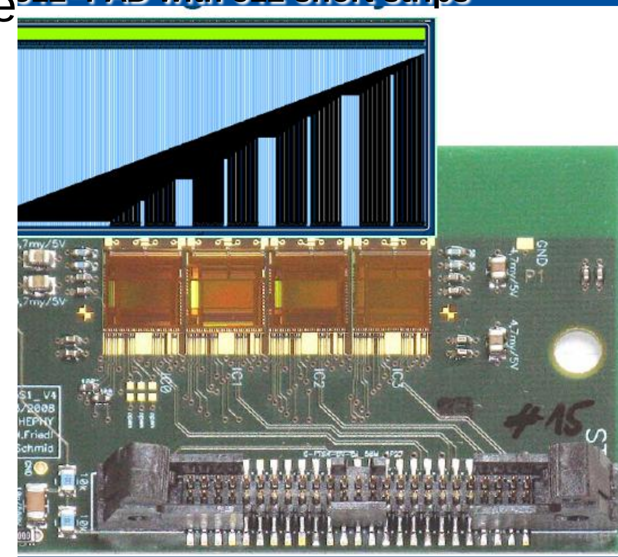
512=PAD with 512 short strips

Fig. 4. 3D view of a silicon strip detector utilizing routing lines with a dedicated metal layer (green) on top of the aluminium strip layer.



CMS upgrade

F. Hartman

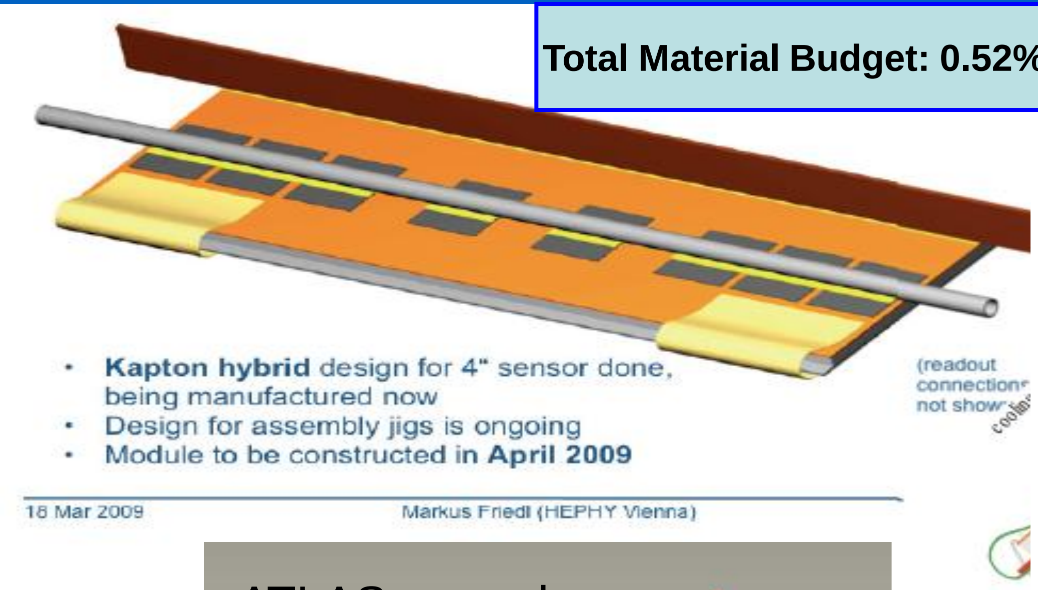


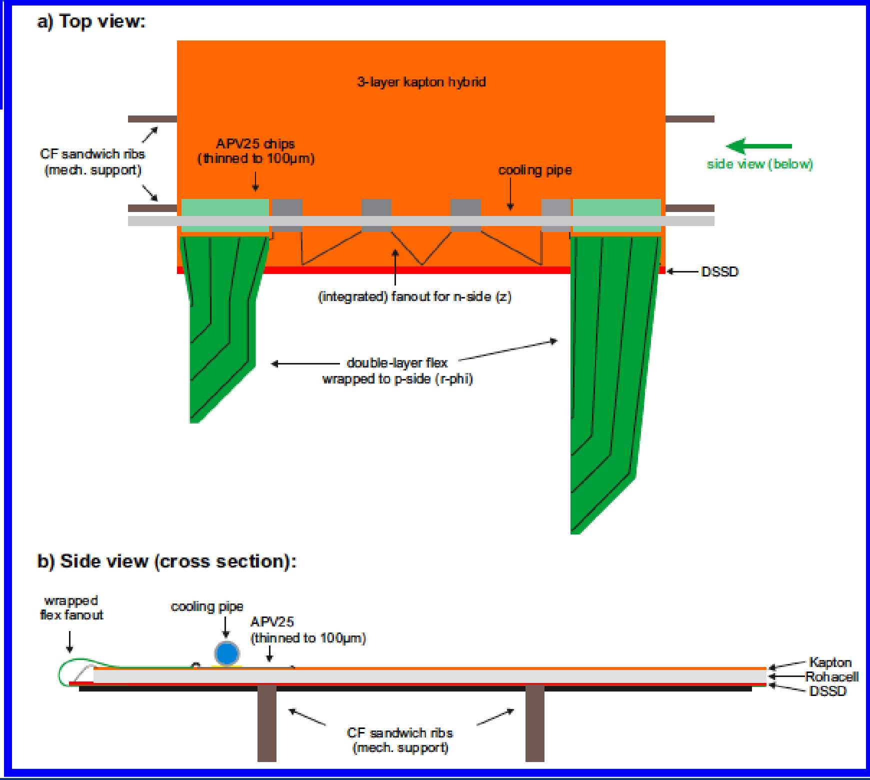
(Also under consideration for CMS upgrade)

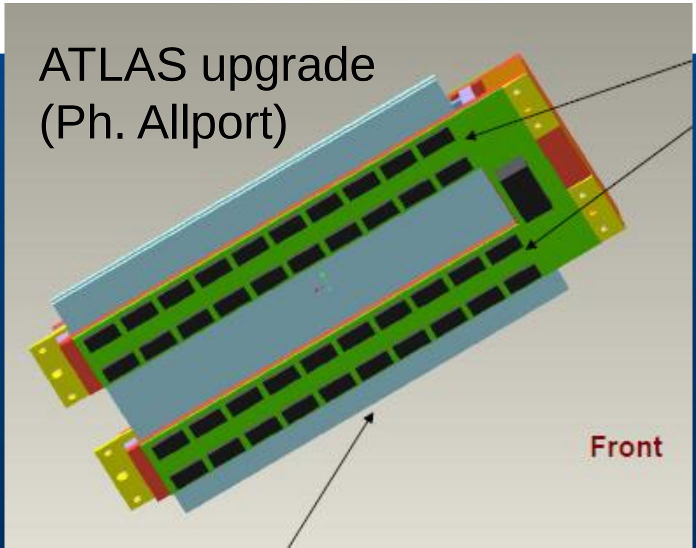
Chip on sensor readout

A kapton flex circuit with several APV25 chips (thinned to 100 μm) will be mounted on a DSSD and both sides of strip signal will be readout. The opposite side strips are read with folded kapton tabs. The kapton "hybrid" buses signals from strips &services to strips

Total Material Budget: 0.52%





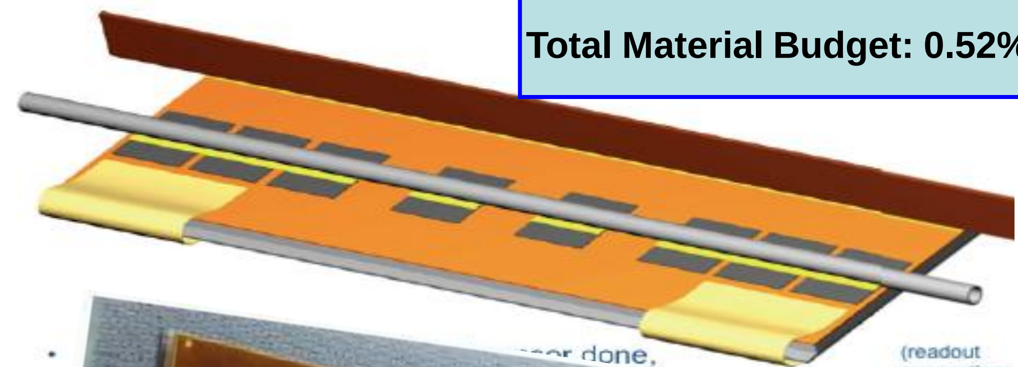


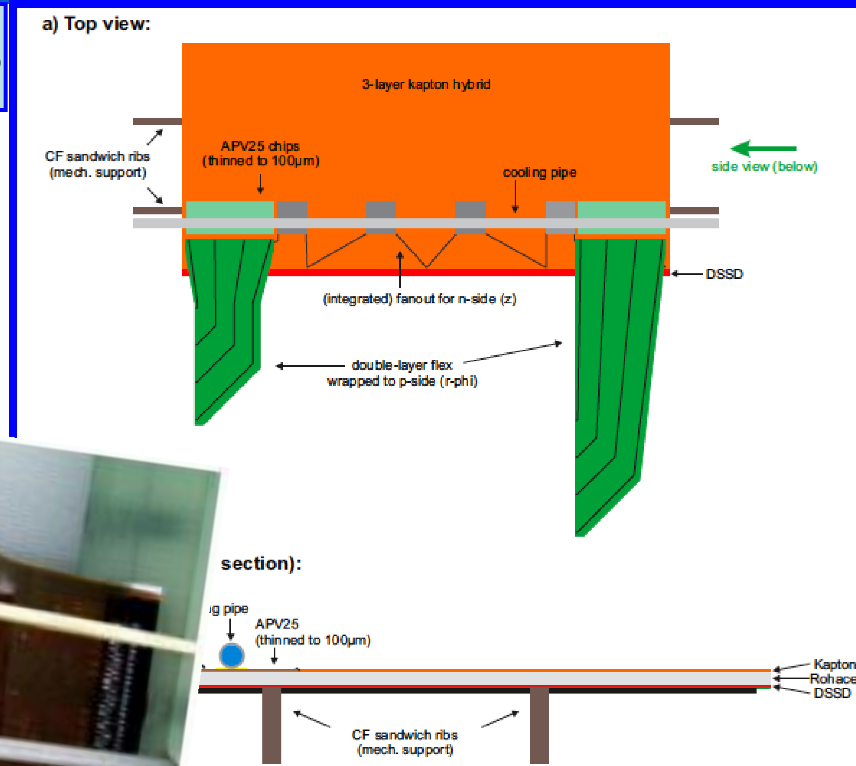
N.B. ATLAS upgrade is also developing TAB based connection

Chip on sensor readout

A kapton flex circuit with several APV25 chips (thinned to 100 µm) will be mounted on a DSSD and both sides of strip signal will be readout. The opposite side strips are read with folded kapton tabs. The kapton "hybrid" buses signals from strips &services to strips

Total Material Budget: 0.52%





Top and Bottom side ORIGAMI for BELLE II (1st try with 4" sensor)

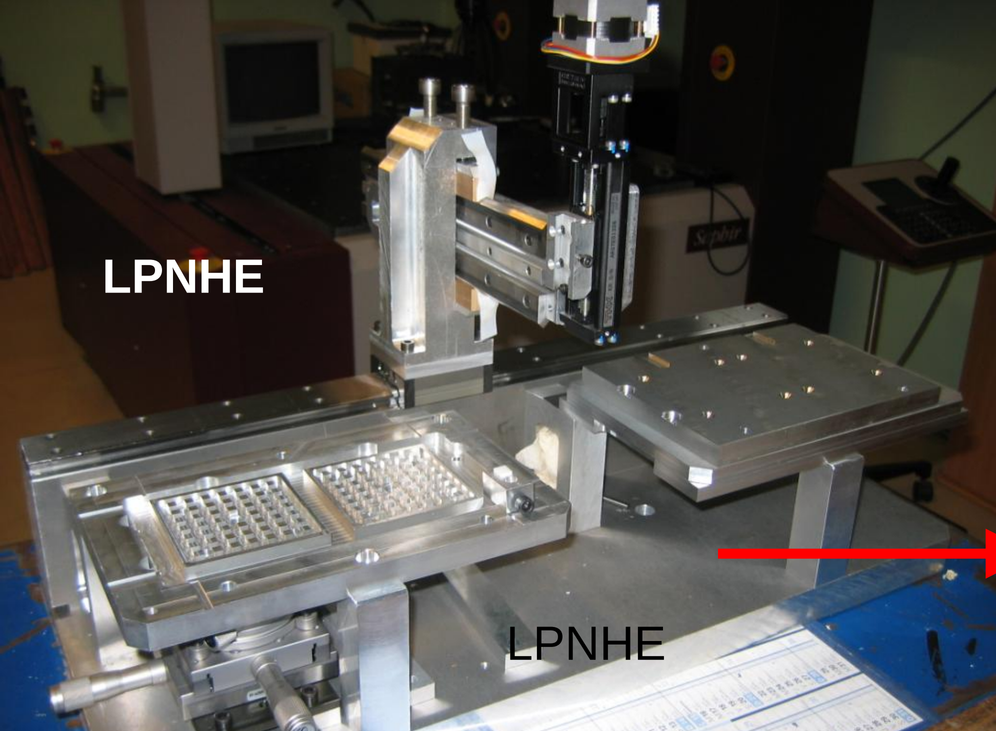
I.- R&D BASIC OBJECTIVES

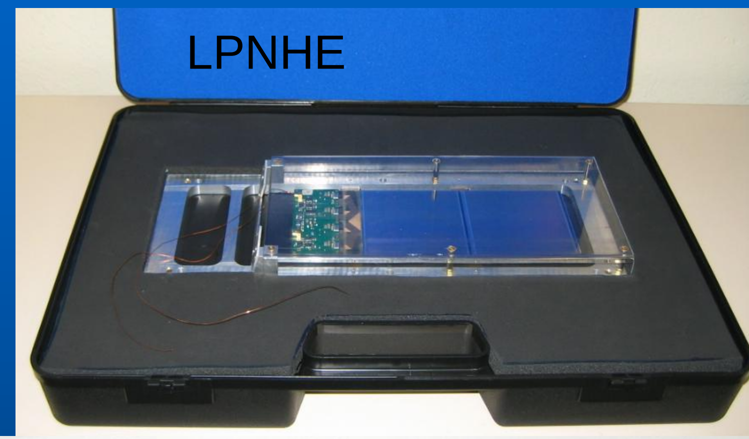
- R&D on sensors
- R&D on FEE and READOUT
- **RELATED MECHANICAL ISSUES**

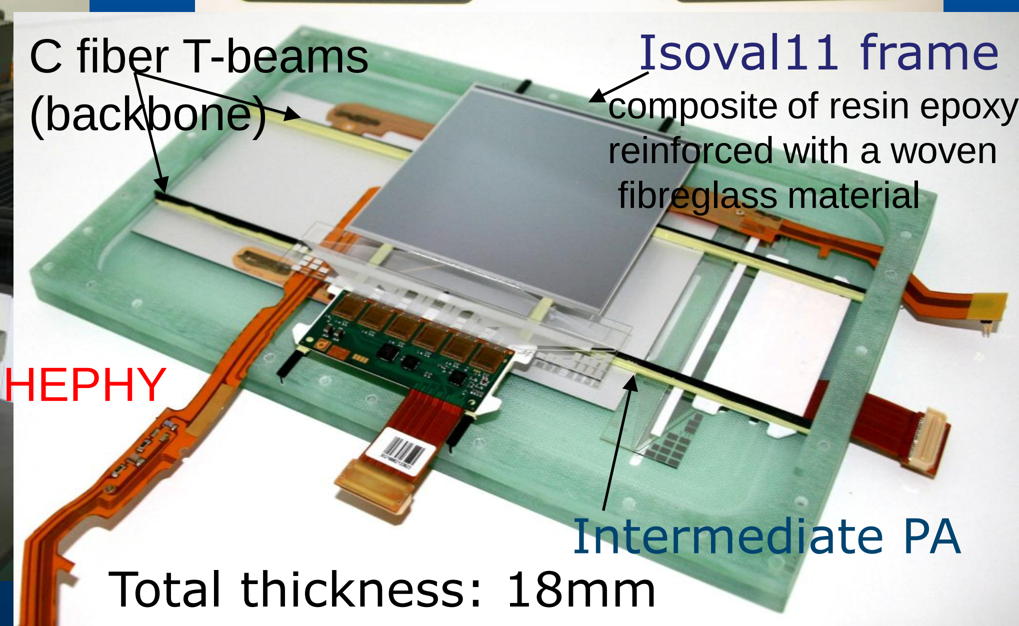
Modules for T.B.

- Developed new expertise & tools: LPNHE
- with bonding Lab at CERN

  or:
- Existing expertise & tools: IEKP, HEPHY

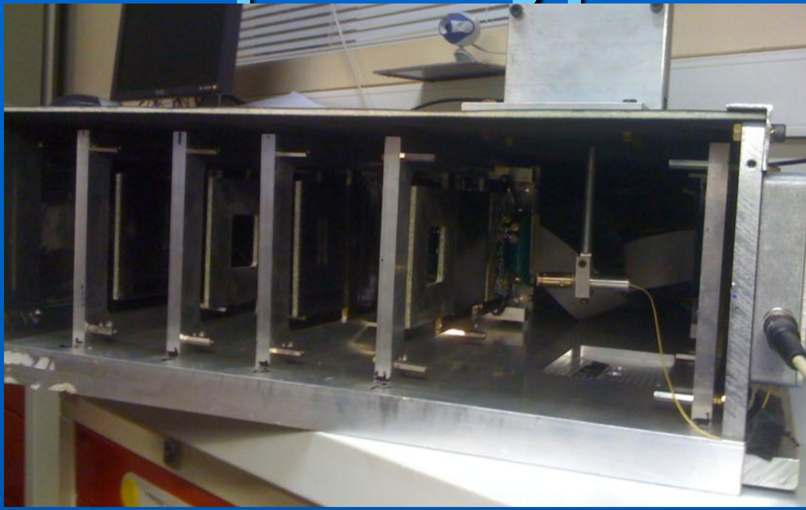


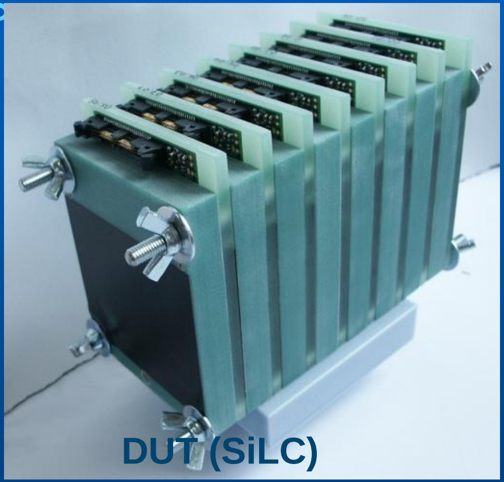




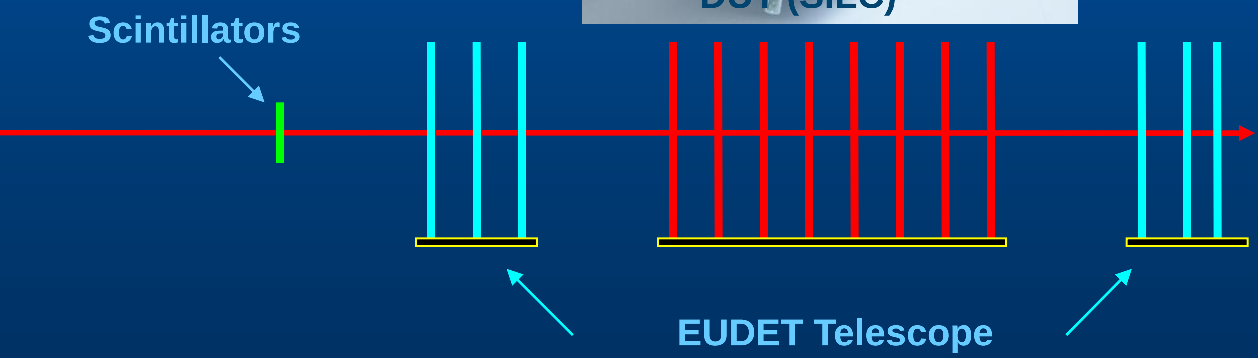
Module Stacks=>Si system prototypes

- 8 Modules have been screwed together
- To be mounted in between EUDET telescope
- Stack of 8 modules allow autonomous tracking





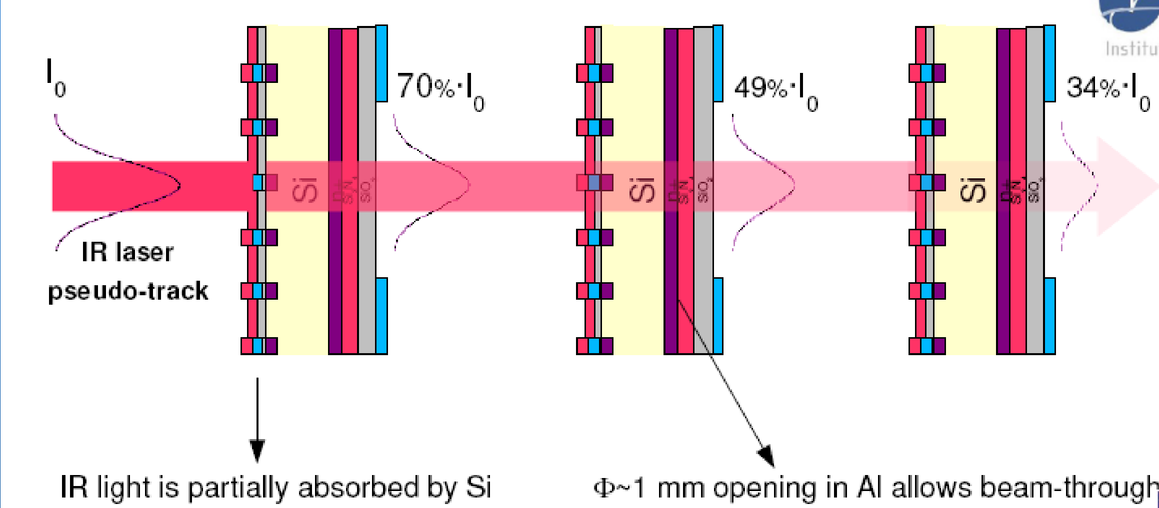
- 5 Modules in faraday c
- autonomous tracking
- Integrated telescope
- Integrated laser
- Multipurpose: test various sensors&FEE



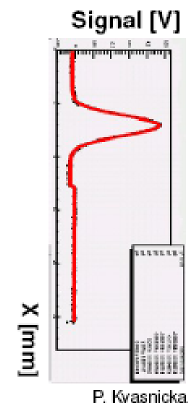
Alignment: special issue at LC (high prec. + push pull)

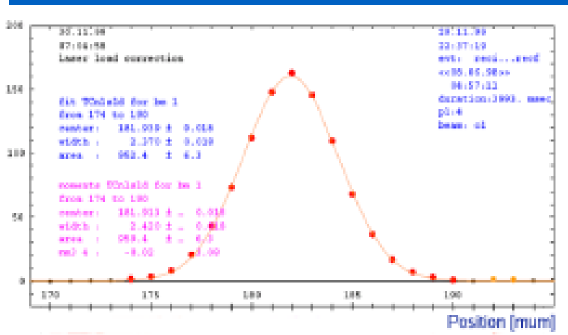
1) ***Fully FEE/DAQ integrated laser system alignment when several Si layers to align***

• Aim: align Si microstrip sensors using IR laser tracks



Precision:σ=2.3 µm

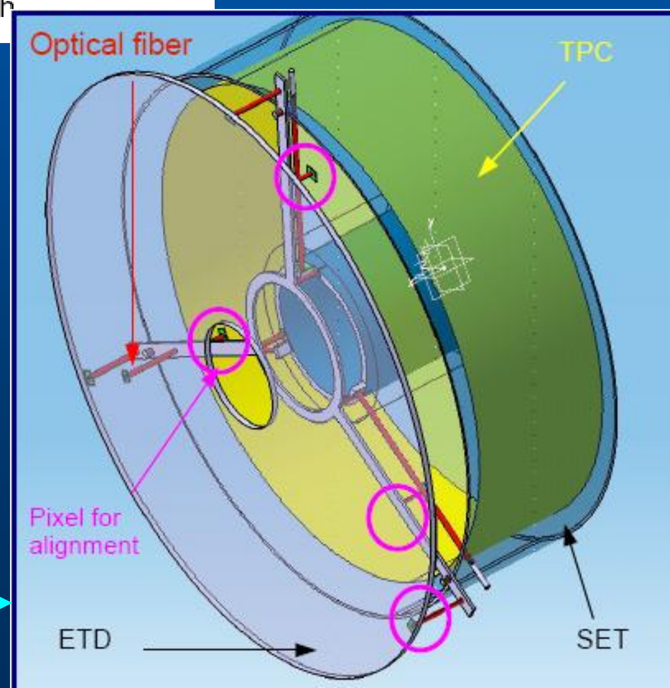




2) ***Another laser system*** to shine on dedicated gratings connected to detector elements: position of different sub-detectors relative to each other and variation on alignment of each detectors. Can be used *during or outside data taking*:

independent DAQ ***=> PUSH PULL CASE!***

Laser + dedicated pixel sensors at the strategical points



TOOLS

- **Simulations**
  - **Fast Simulations: LiCToy**
  - **Detailed GEANT4 based simulations**
  - **Forward simulations studies**
- Test benches and test beams

FAST SIMULATION: LiCToy

M. Valentan, W. Mitarof et al.

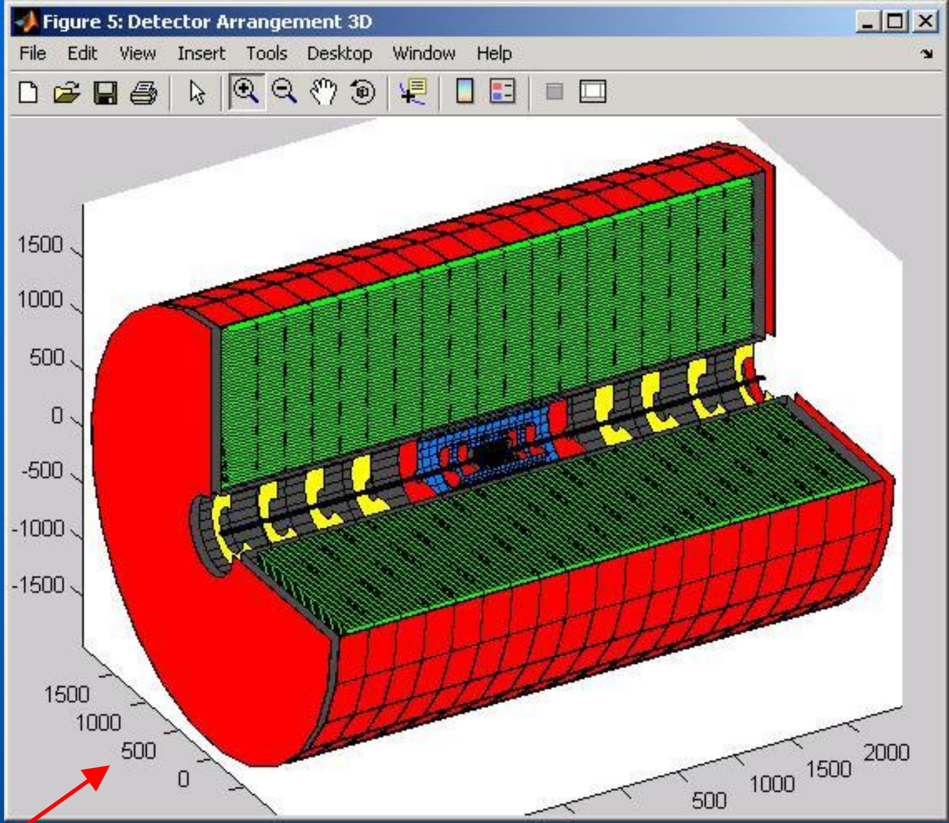
The “LiC Detector Toy” allows investigating the track parameter resolution via Monte Carlo, for optimizing a detector set-up.

It features:

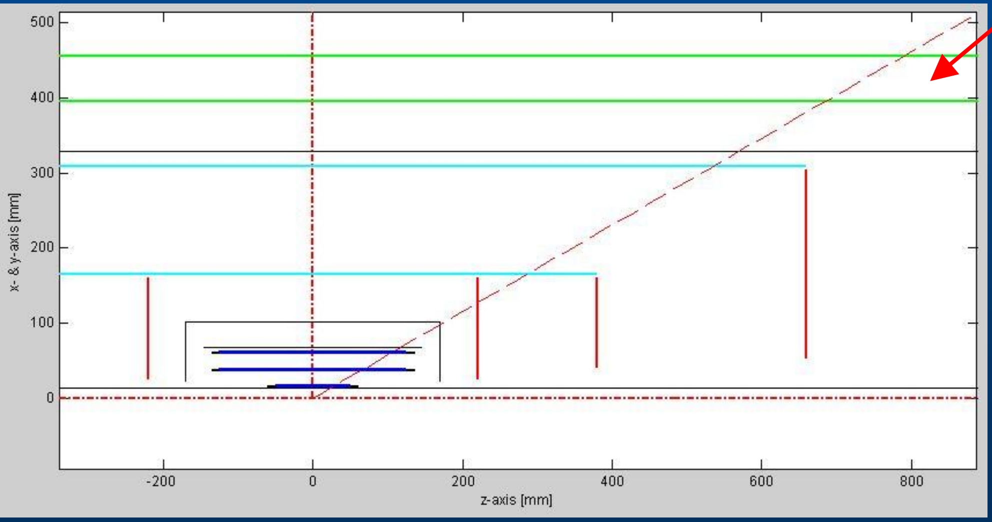
• Simulation of the track sensitive part with a B- field, and its material budget;

• Support of measurements by Si pixel and strip detectors, and a TPC;

• Track reconstruction by a Kalman filter, including tests of goodness of the fits.



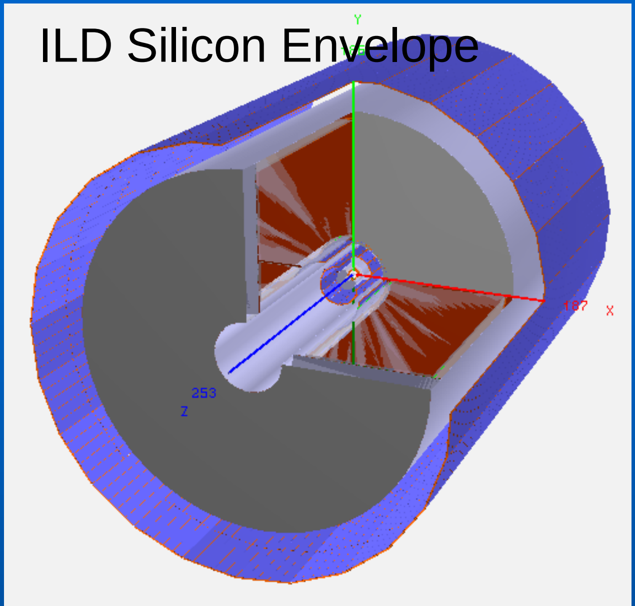
An integrated graphics user interface (GUI) available;

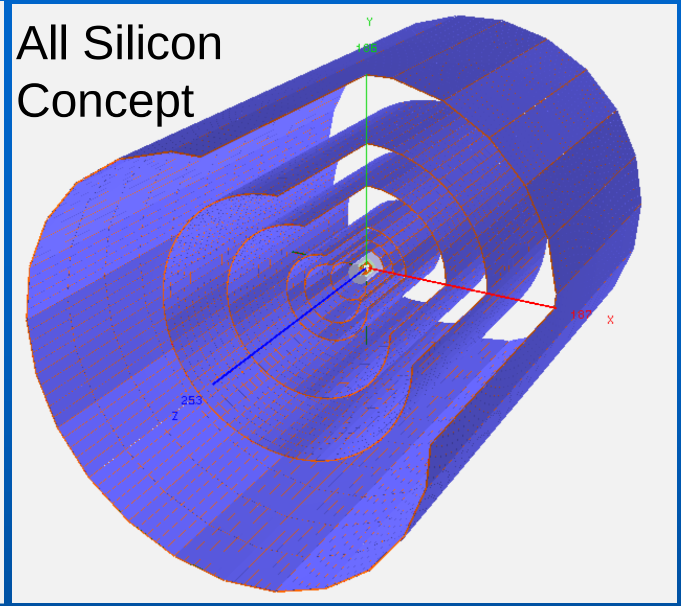


•LiCToy was instrumental for many LOI’s optimization studies (M. Valentan)

•Now very much used for CLIC CDR studies

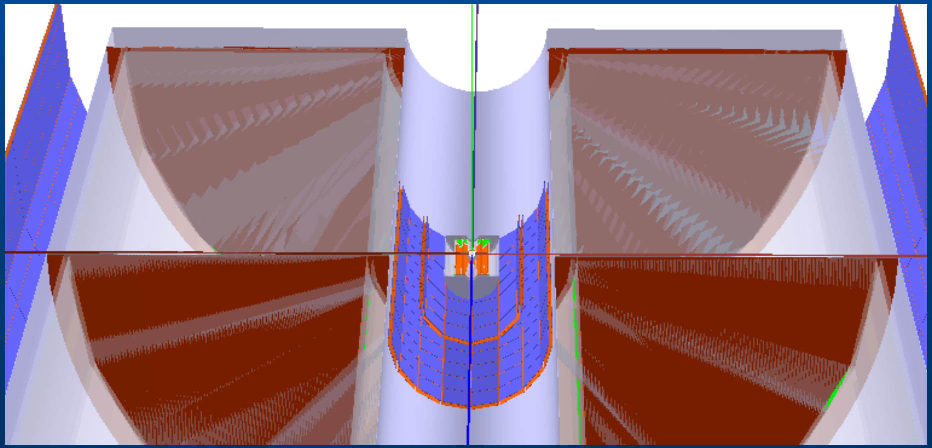
DETAILED SIMULATIONS

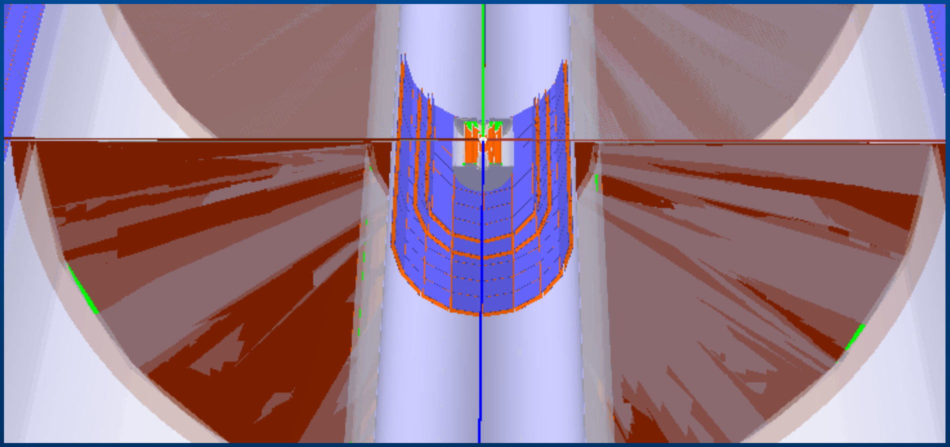




Forward region:
M. Vos, J. Duarte *& al.*
(B.U.+IFIC+IFCA)
✓Lot of work dedicated to the Forward Region in ILD concept
✓More recently in CLIC WG3 context.
✓*See also W. Mitarof (HEPHY) presentation*

Ex of CLIC studies: changing number of internal layers in “ILD-CLIC”





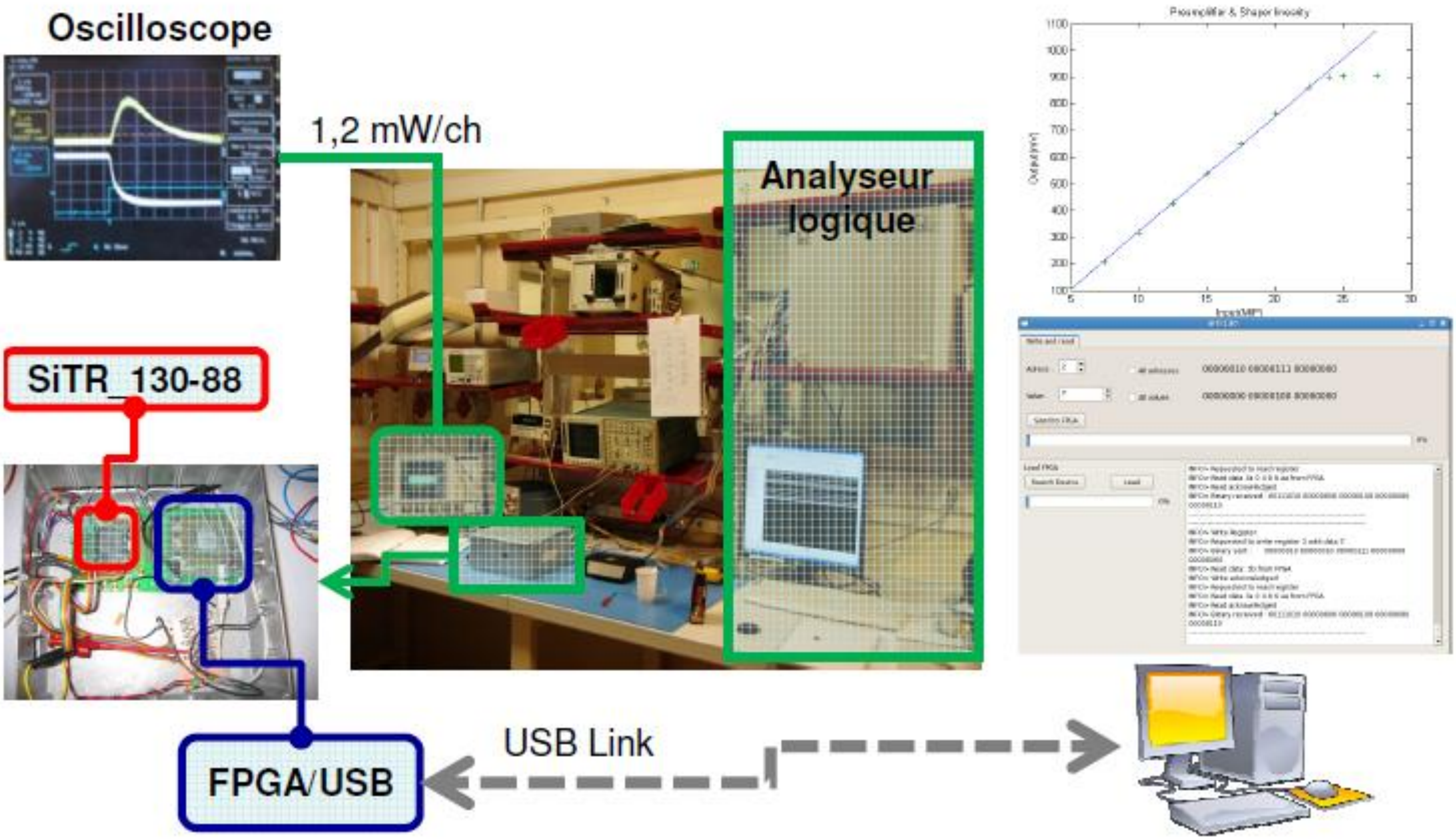
Latest on GEANT4 based simulations: Silicon tracking in MARLIN-MOKKA, preparing for DBD in 2012 *and also CLIC-CDR (flexibility)* *See A. Charpy’s presentation*

TOOLS

- Simulations
- **Test benches and test beams**
  - ❖ **Developments of tools for test bench**
  - ❖ **Test beams focusing on testing performances of “standard strips structures & new direct connections**
  - ❖**Test beams for tests of novel sensors &/or new FEE edgeless, A.F. , others…new FEE chip versions**
  - ❖ **Combined tests with other subdetectors:**

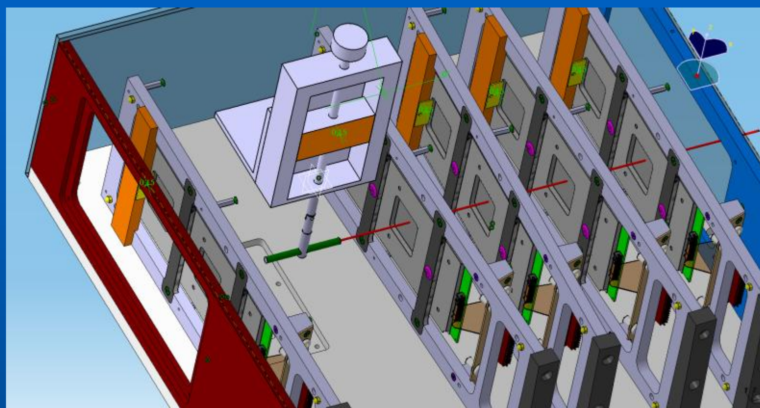
    TPC + Si Envelope prototype

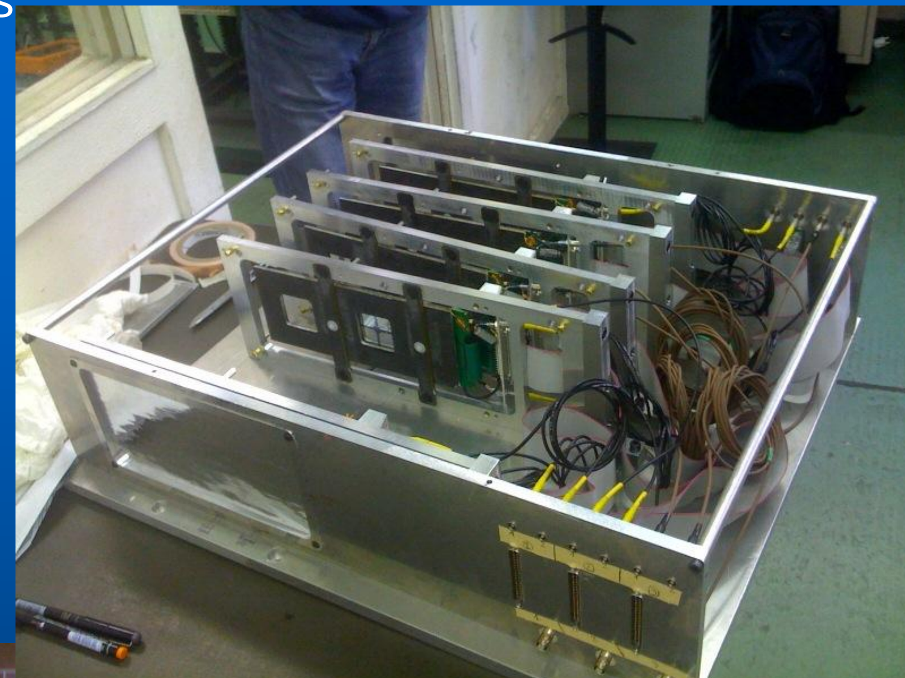
Example of test bench set-up for testing the new FEE readout chip



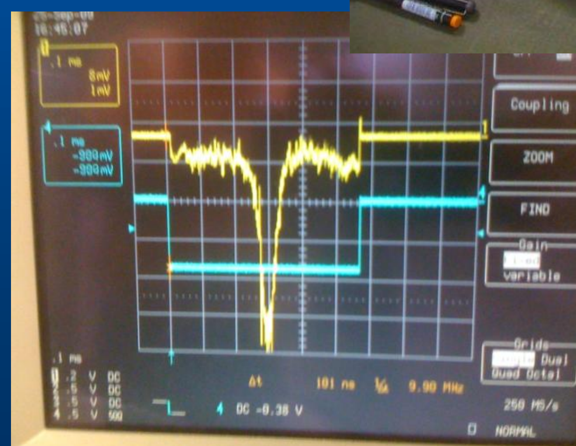
Standalone, portable, multipurpose test set-up

*Ex: Tests at the Lab of the A.F. HPK sensors with IR laser both **by IFCA** and LPNHE*

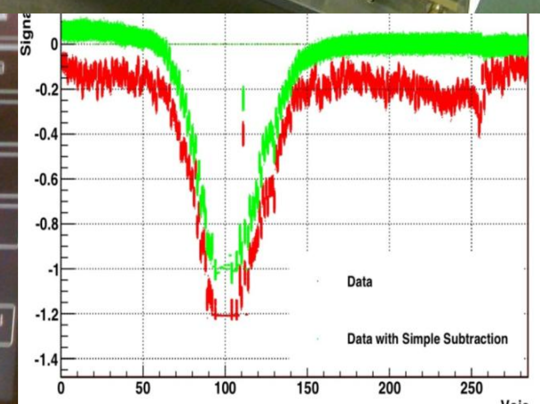




Tests of alignment system based on AF HPK sensors

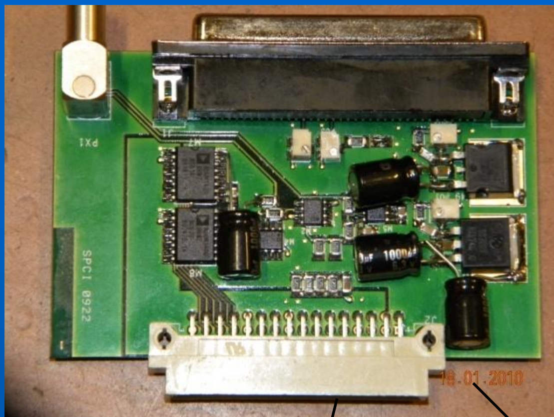


Alignment test with IR laser

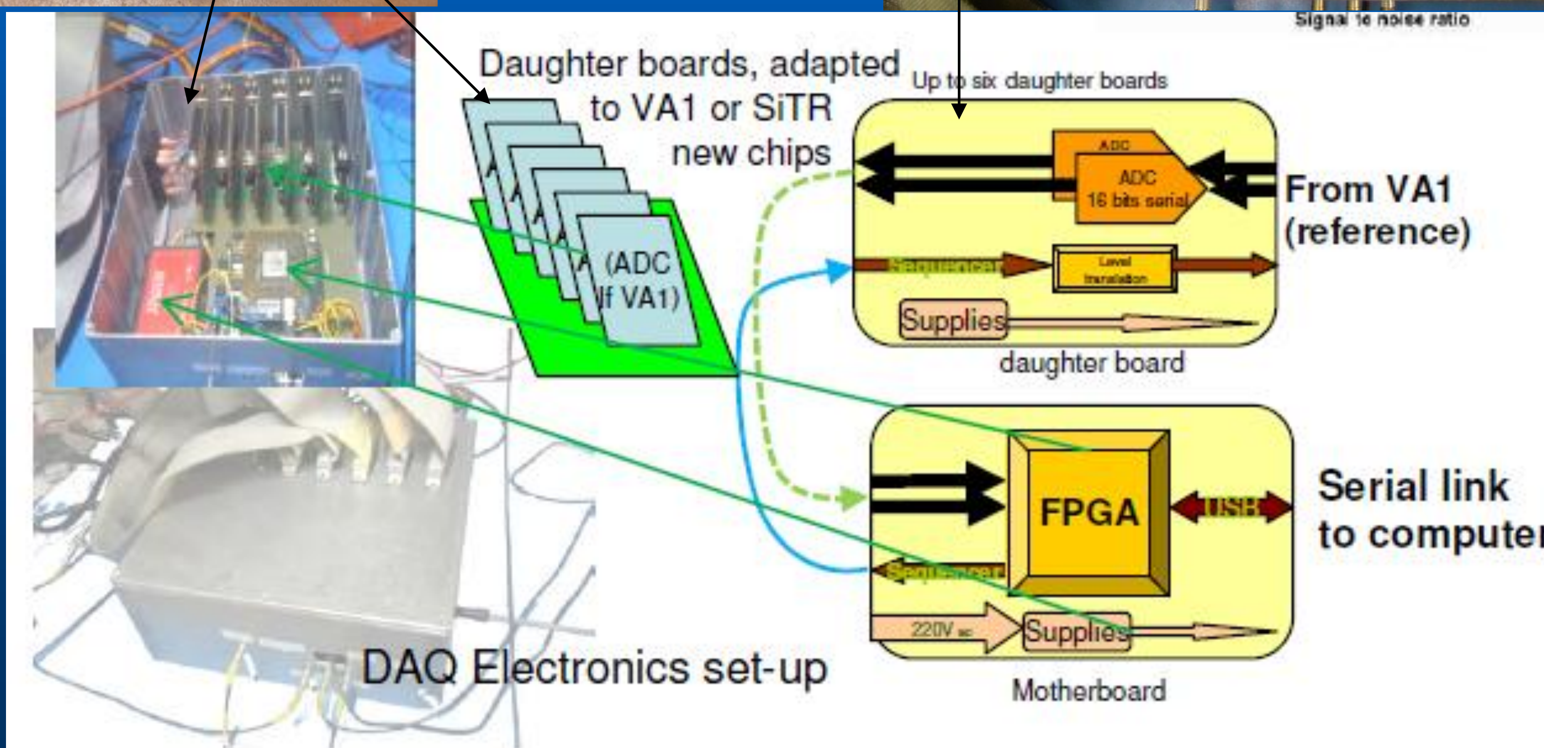


Signal reconstruction with or without pedestal subtraction

DAQ Electronics

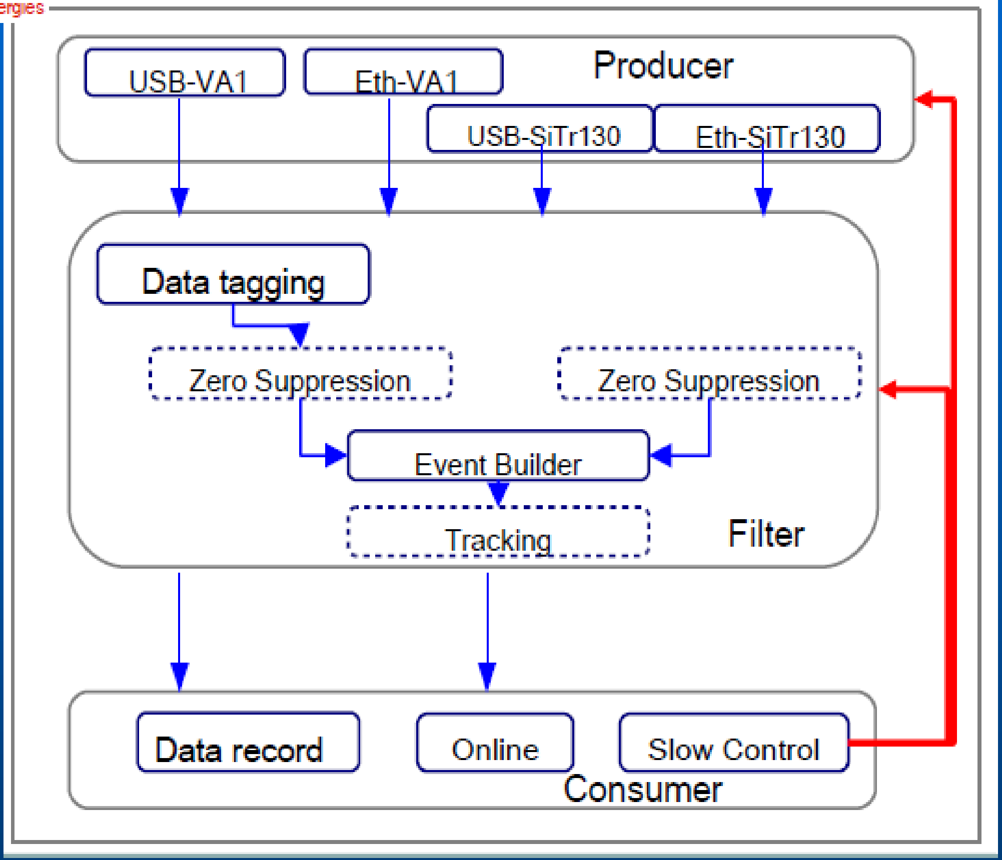


VA1' ASIC used as reference devices



DAQ software (new for new FEE readout system)

LPNHE
Laboratoire de Physique Nucléaire et des Hautes Energies



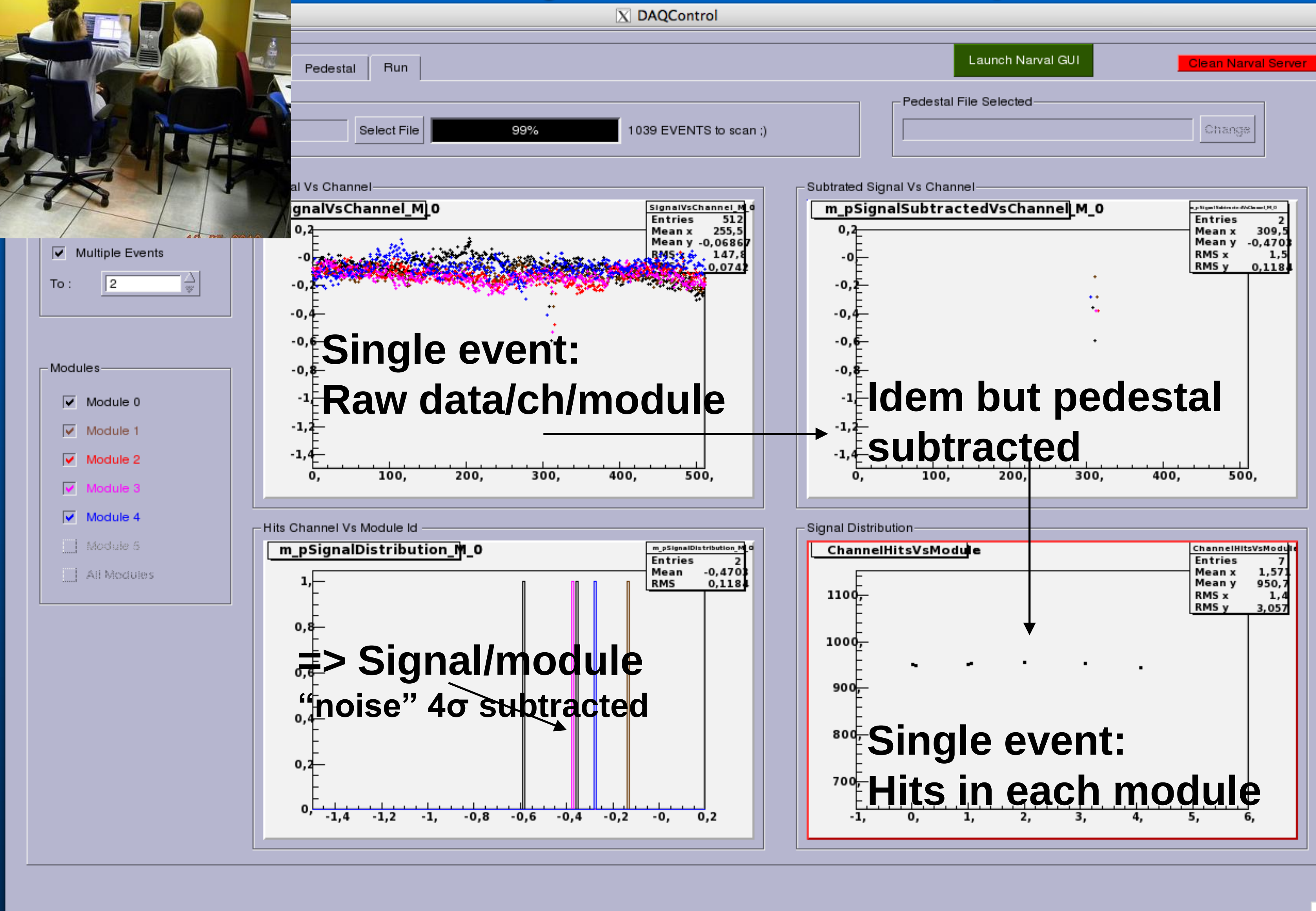
NARVAL:
- o Distributed DAQ written in ADA language
- o Divide the acquisition into activities called actors (ADA)
- o 3 basic actors:
  - ➢ Producers
  - ➢ Filters
  - ➢ Consumers
- o Dedicated Libraries in C/C++/ADA
- o High Flexibility with very simple scripts & xml files

2 other DAQ lines used by SiLC based on system were developed by other experiments (synergy)

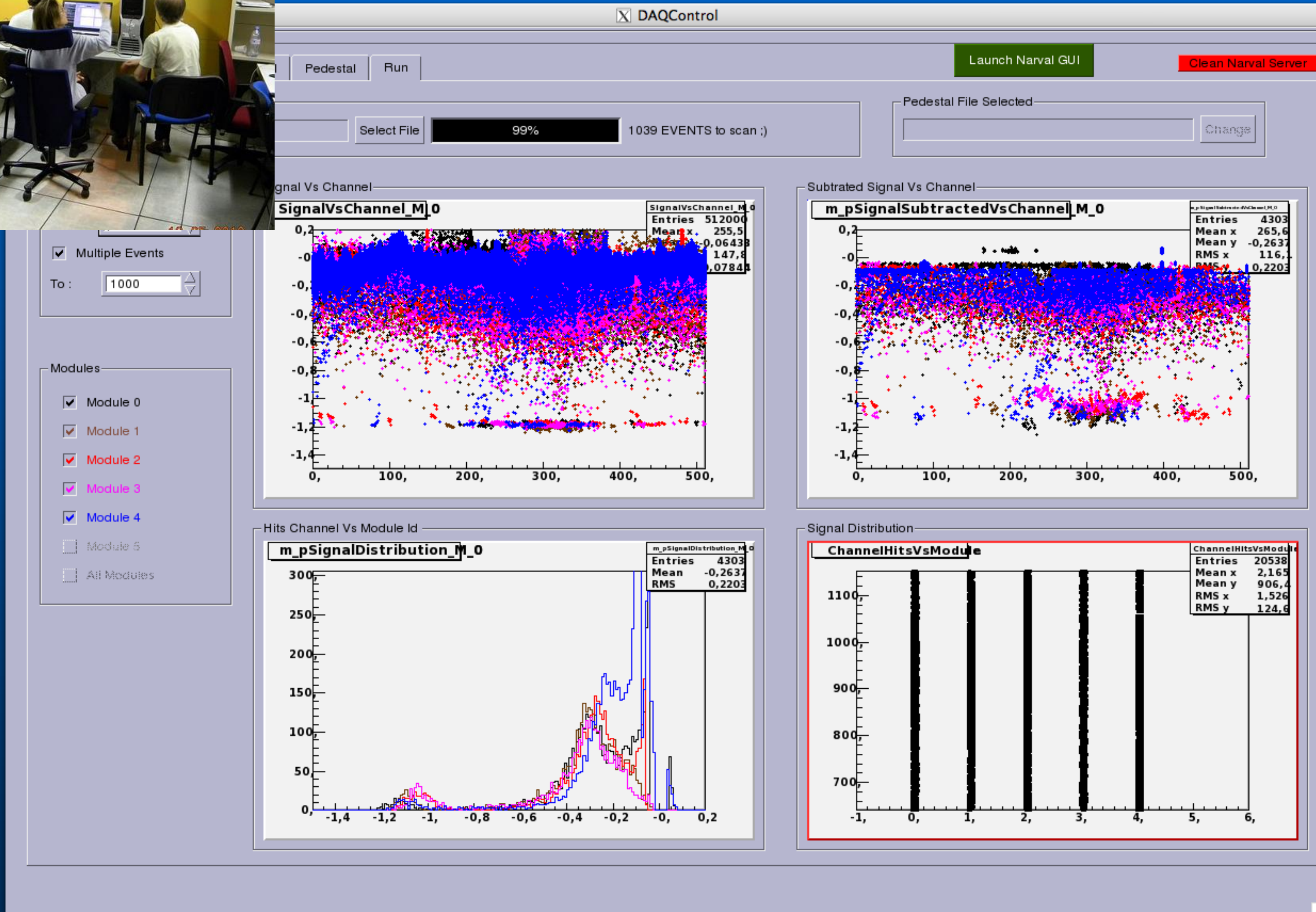
➢ **APV25 based** => hardware & software developed forCMS & also BELLE application.

➢ **ALIBAVA** developed by Liverpool, CNM-Barcelone and IFIC Valencia (ATLAS et al..)

SPS May 2010 T.B.:Online plots



SPS May 2010 T.B.:Online plots

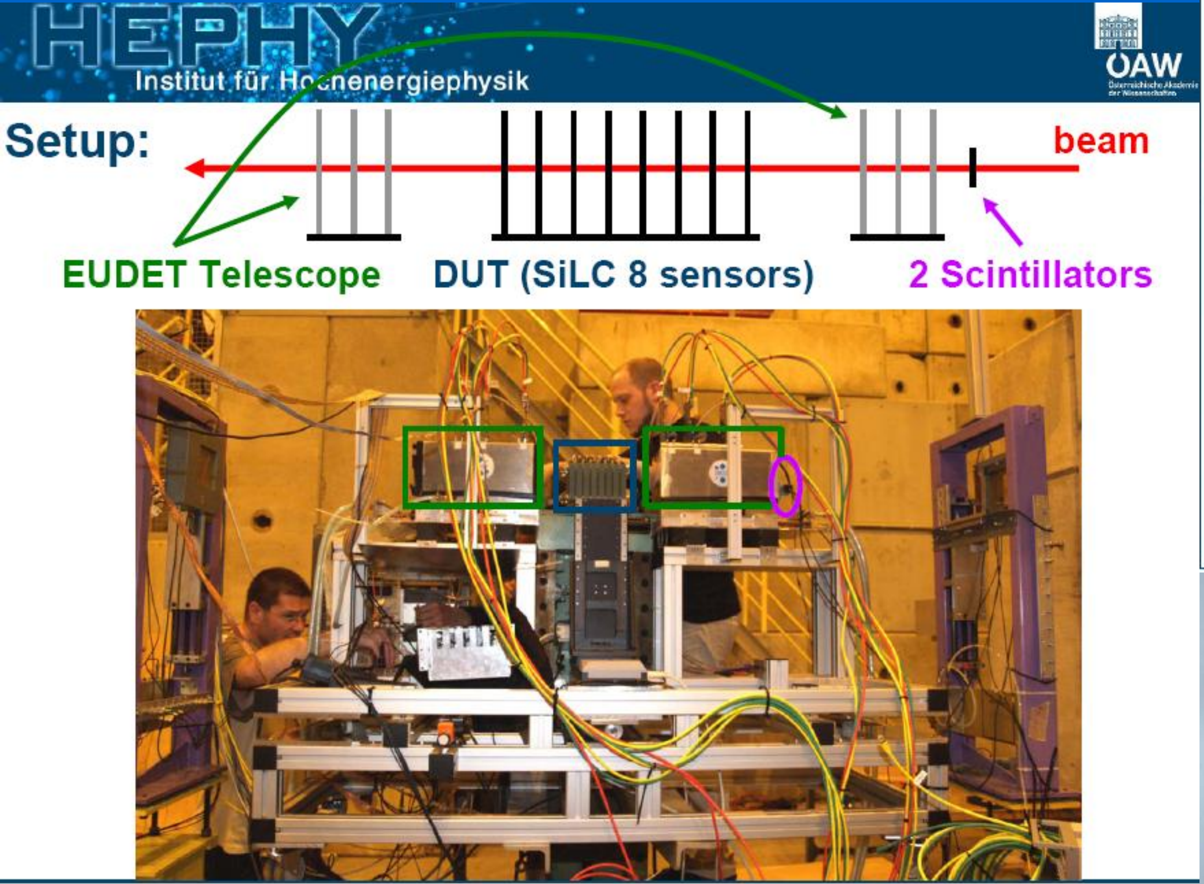


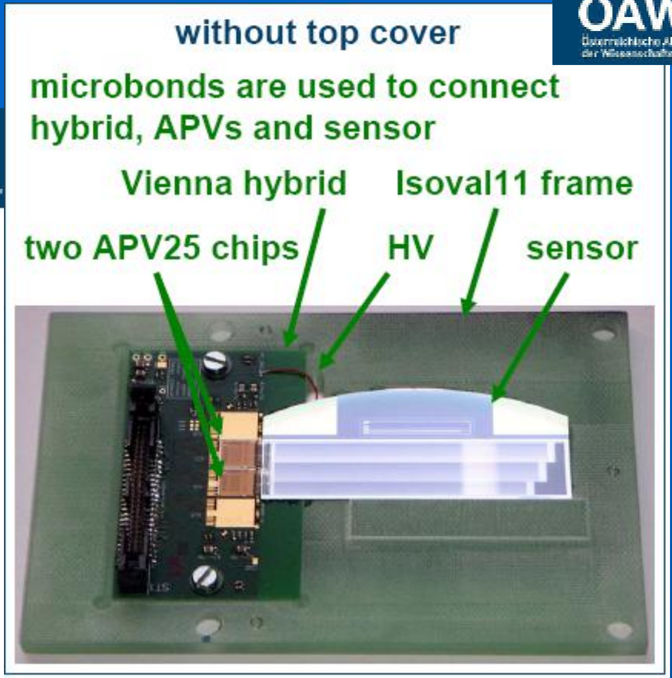
CU Prague

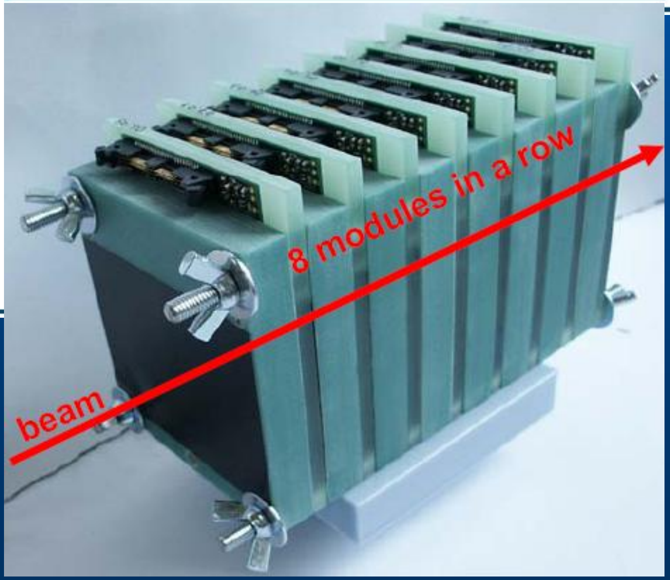
Testbeam Analysis

- **In a testbeam, we study prototype modules (reliability, S/N, charge sharing, resolutions etc.). Therefore,**
  - Geometry of testbeam setups is intentionally made simple
  - Tracking is used for alignment and calculation of resolutions. Simple tracking is used to obtain simple statistics of residuals for resolution estimates
- **So testbeam analysis is different from analysis in big experiments, BUT**
  - Studies of resolutions and detector response statistics can help to correctly define the parameters of tracking engines.
  - Studies of cluster parameters and charge sharing can contribute to better hit reconstruction

Test beam on HPK test strutures







Performed on H6B SPS-CERN in August 2008.

Goal: Characterization of the test structures in the HPK sensors

2008 SPS beam on HPK test structures

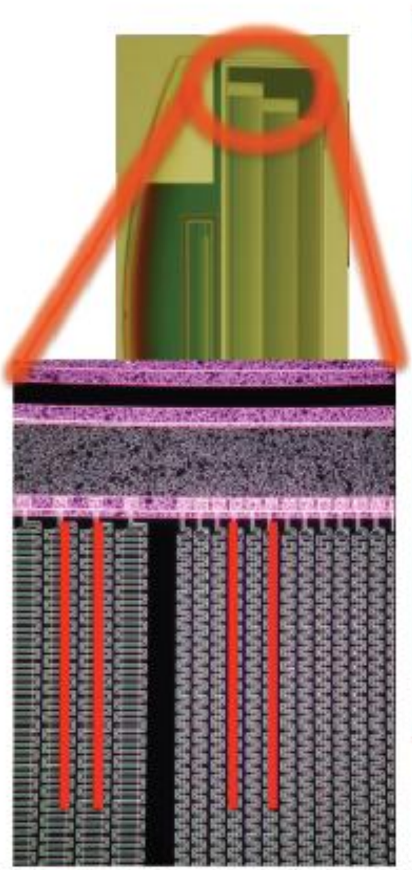


Figure 1: Microscopic image of the poly-silicon resistors at the transition for zone 6 to 7. The red lines indicate the p+ strips underneath the resistors

TESTAC:

strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

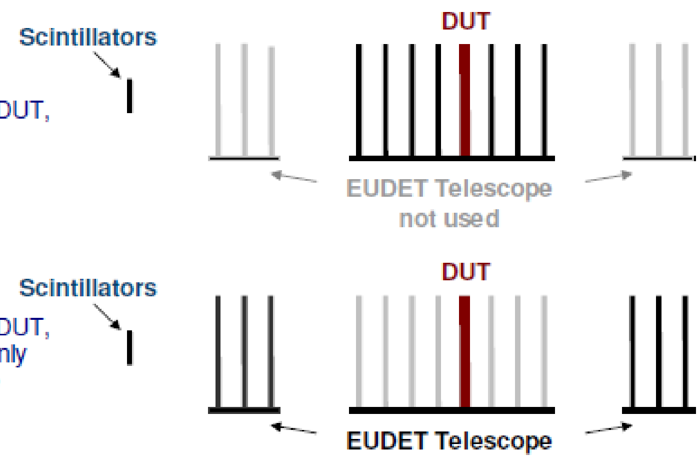
Tracking: Overview

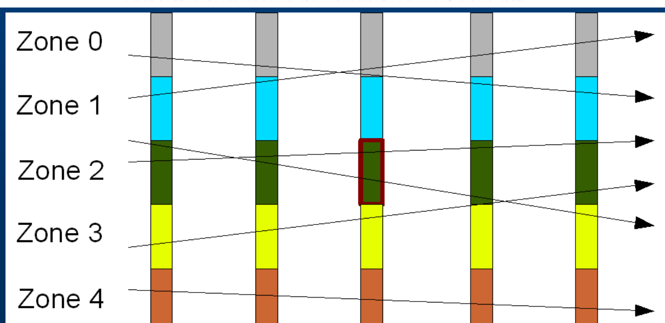
Detailed tracking analysis between differen zones

- Specific tasks:
  - Determine resolutions in individual zones of the sensor to find optimum strip configuration
  - Two independent tracking schemes:

A — Only strips
One strip detector as DUT, other 7 as telescopes

B — EUTels
One strip detector as DUT, other strip detectors only accounted for multiple scattering





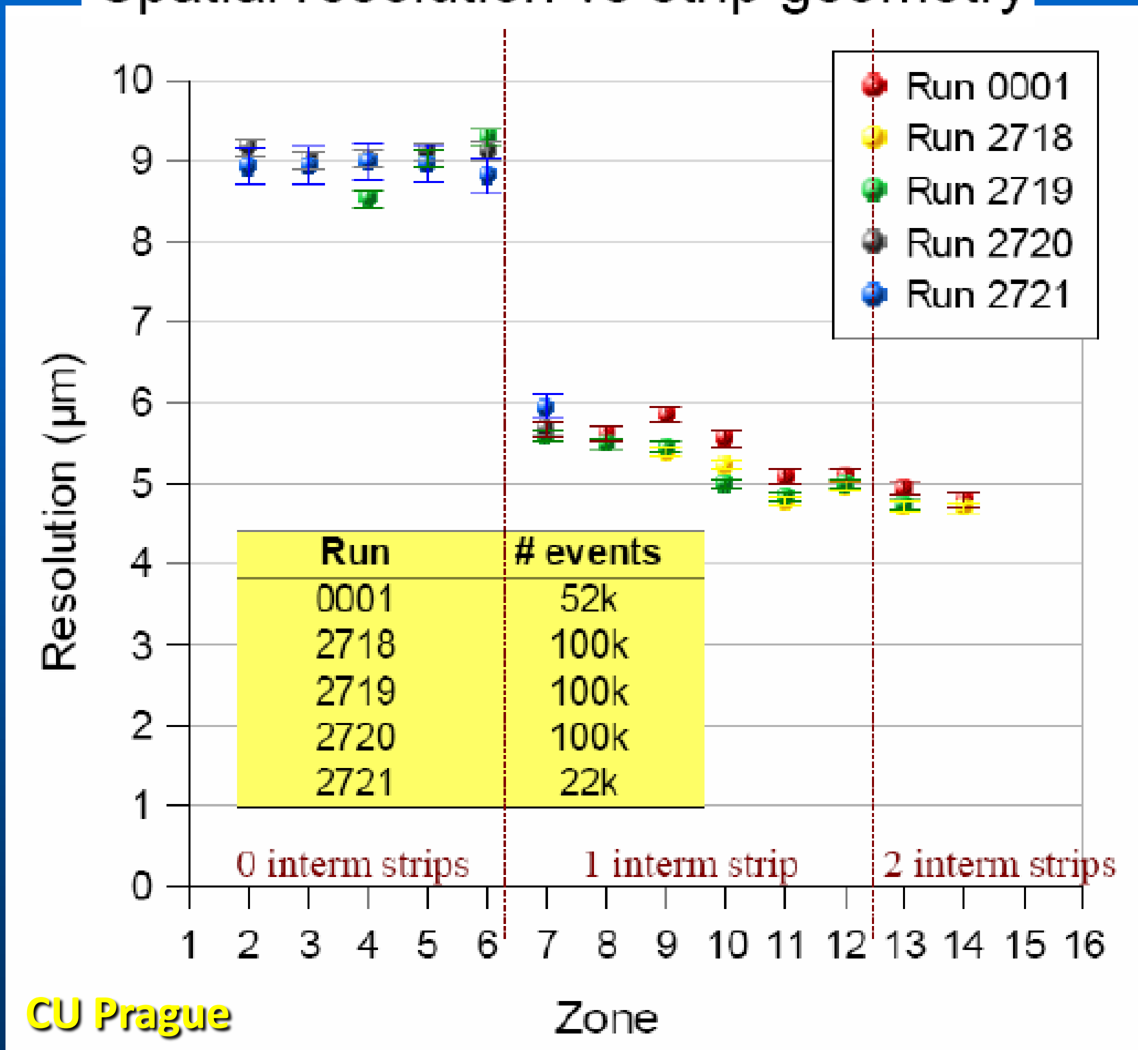
Telescope does not cover the sensor area => need of 3 runs each with 10^5 data

7x7mm2

Figure 9: Area of the sensor covered by the Telescope's active area.

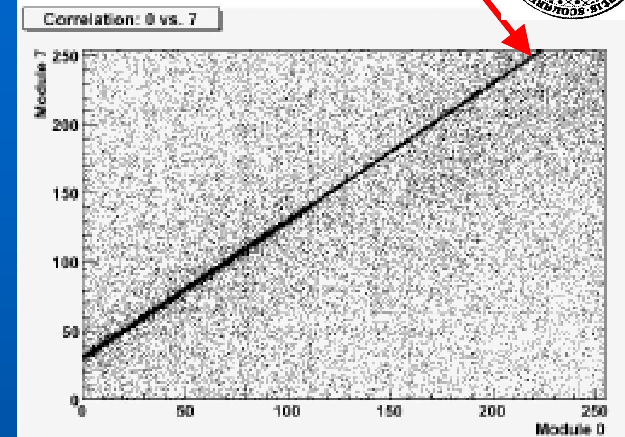
2008 SPS beam on HPK test structures

Spatial resolution vs strip geometry

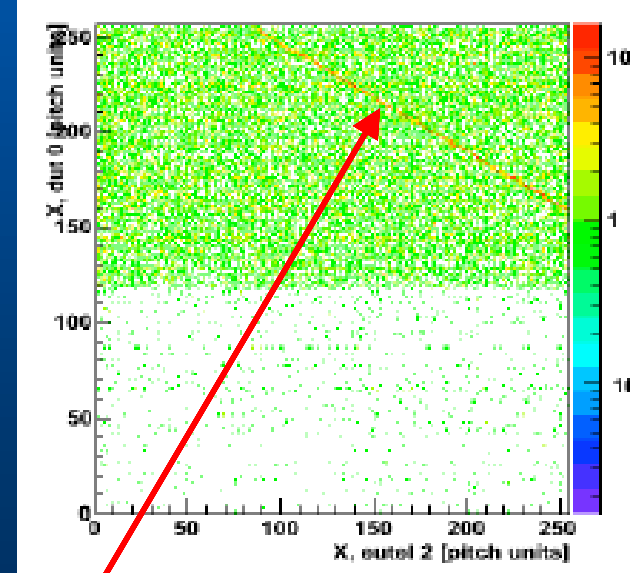


Run	# events
0001	52k
2718	100k
2719	100k
2720	100k
2721	22k

Correlation between 2 extreme modules



X-X correlations, eutel 2 and dut 0

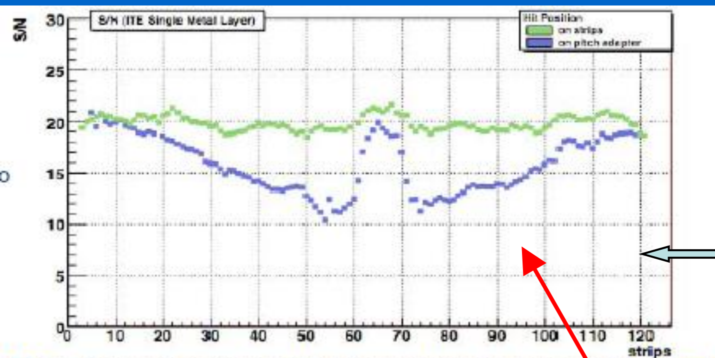


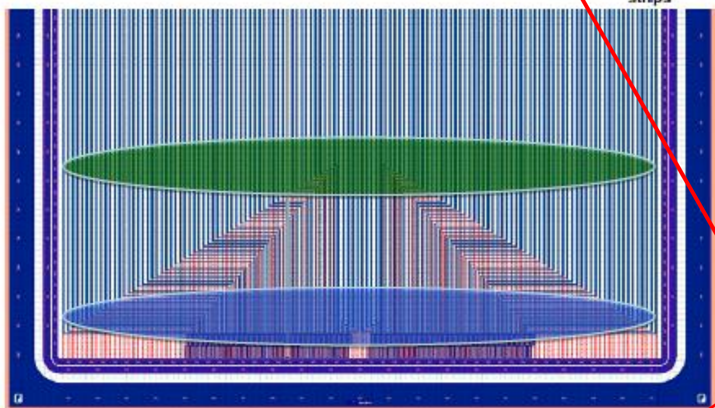
- 9 µm resolution if no intermediate strip
- 5 or 6 µm resolution if 1 or 2 intermediate strip

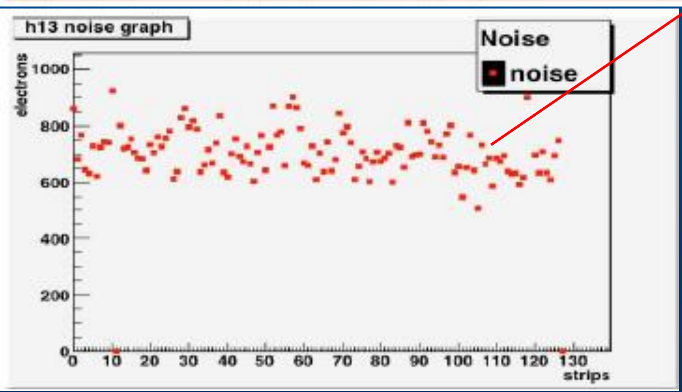
Correlation between EUDET telescope & module 0

ONGOING NOW in 2010

Test beam at SPS-beam 2009 → 2010







Results from 2009 test beam

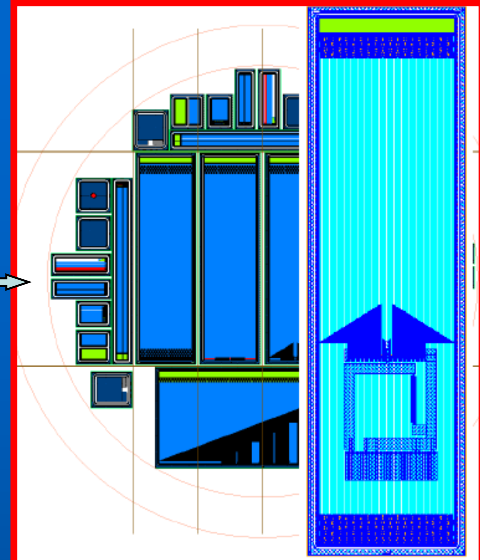
Combined with EUDET Telescope

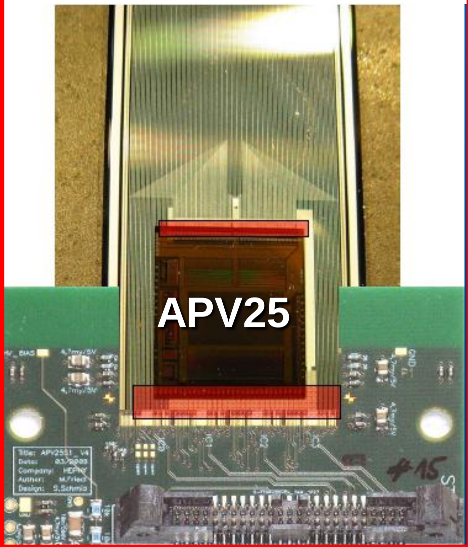
Not due to noise increase but to signal loss

Reason:

- capacitance of integrated coupling capacitor gets extremely low when metal strip moves away from implant in routing region
- Remedy: routing on dedicated, second, metal

Some misunderstanding in J.C. Brient's talk

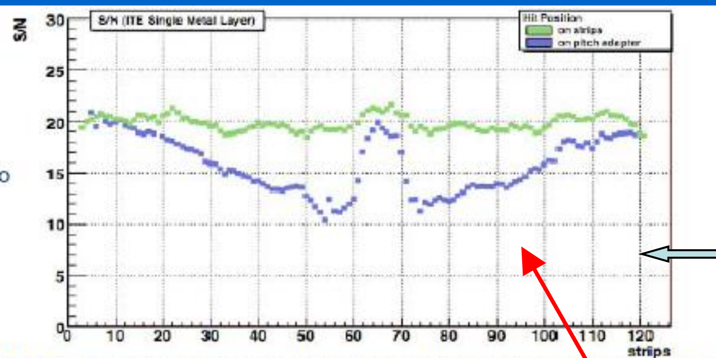


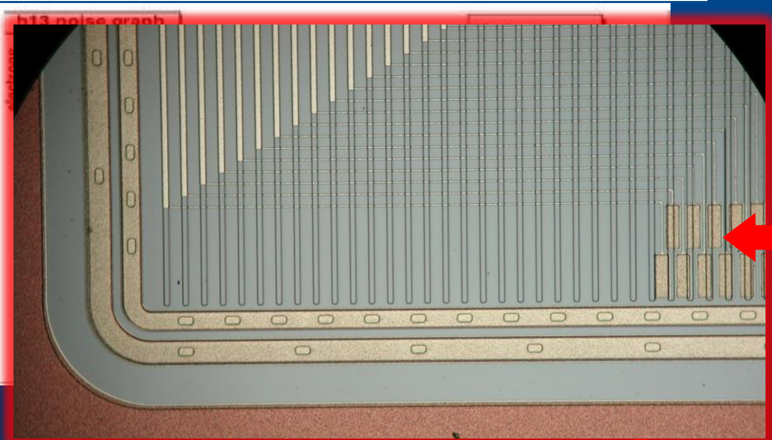


Chip glued on sensor: wire or bump bonding and test new DSSD

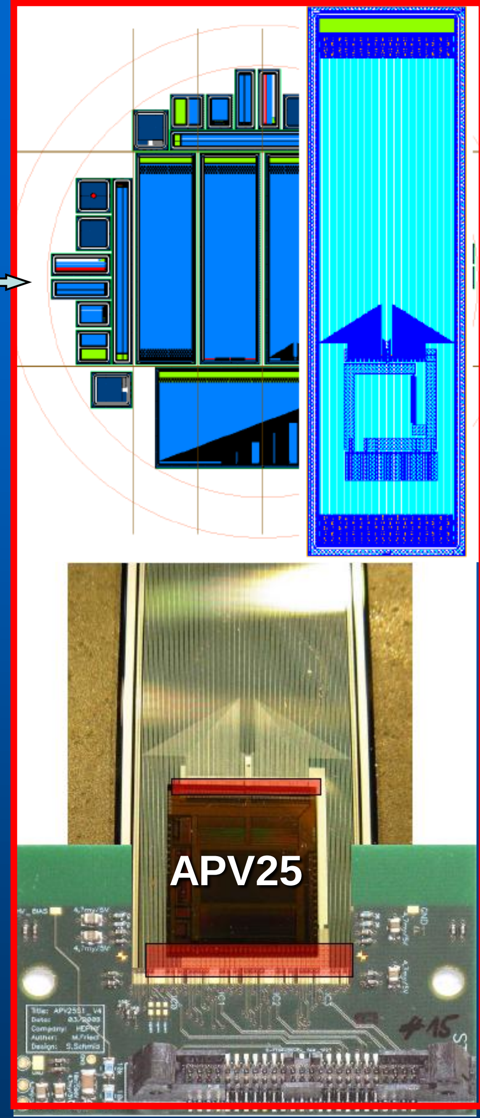
ONGOING NOW in 2010

Test beam at SPS-beam 2009 → 2010





Combined with EUDET Telescope



Not due to noise increase but to signal loss

New run in 2010 with Improved processing technology

To be tested:

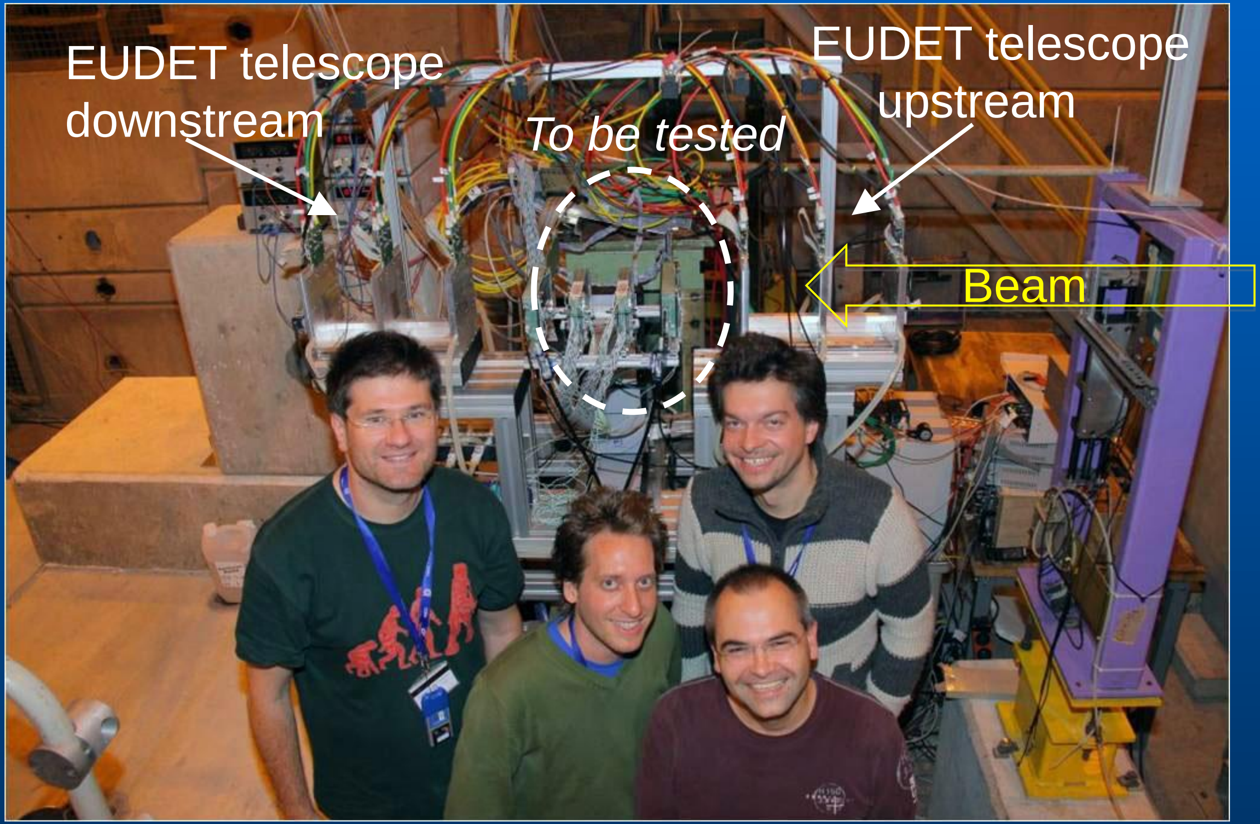
Beam test at SPS-CERN,120 GeV protons

Sept 26 to Oct. 11, 2010

ITE Double metal sensor

Baby DSSD Micron

IFCA Instituto de Física de Cantabria

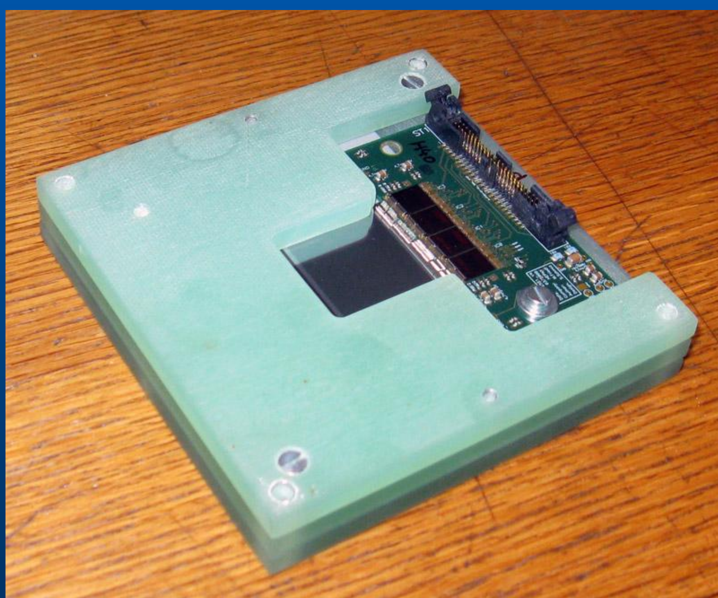


CNM Polysilicon sensors tested both with APVDAQ & ALIBAVA (in parasitic mode)

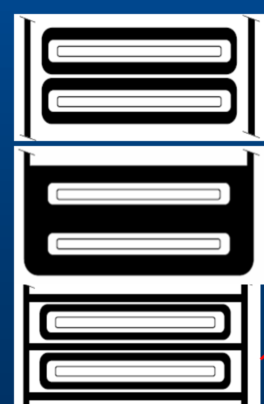
Micron double-sided sensors

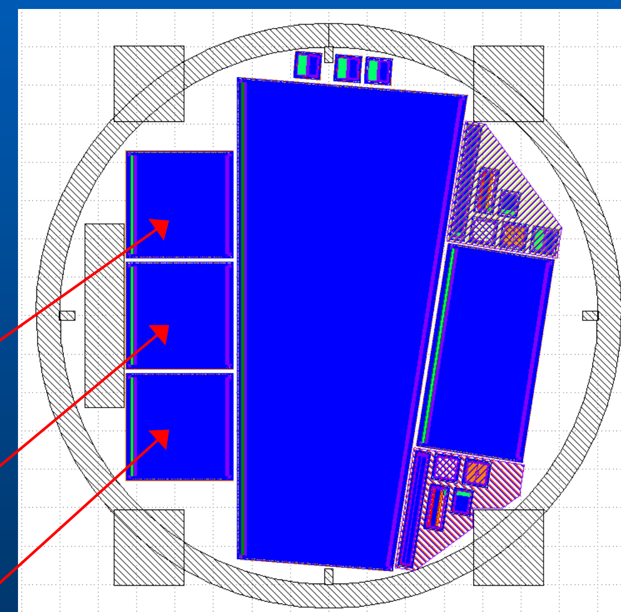
Double sided baby sensors using three different p-stop geometries on n-side:

- Necessary for electrical stop isolation
- Drawbacks: charge loss can occur



Shape of p-stop patterns:

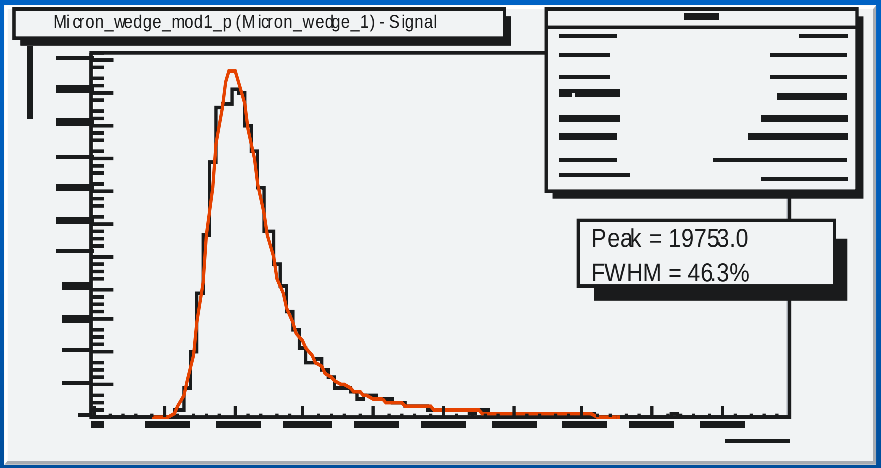


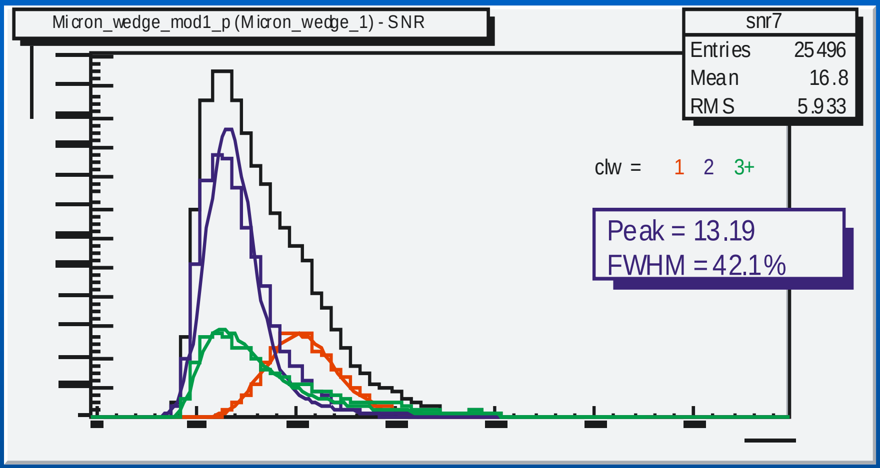


Wafer design for Belle-II experiment

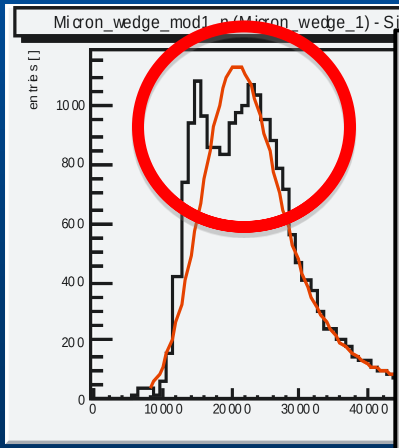
Micron DSSD Signal and SNR

P-side

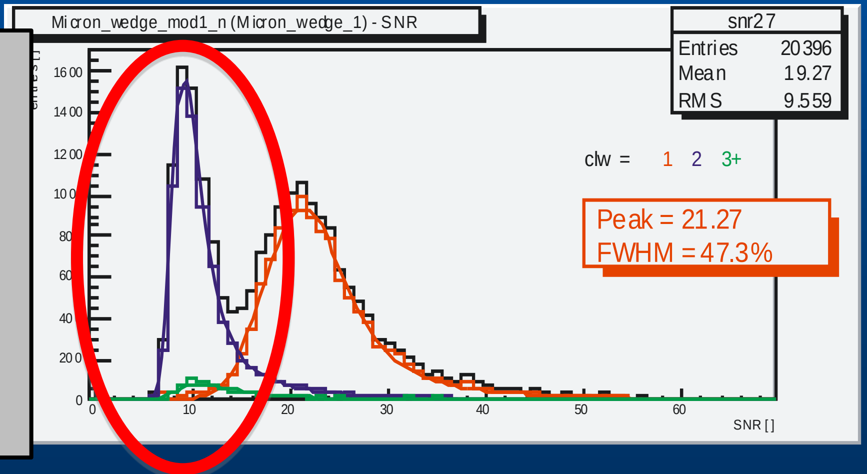




N-side

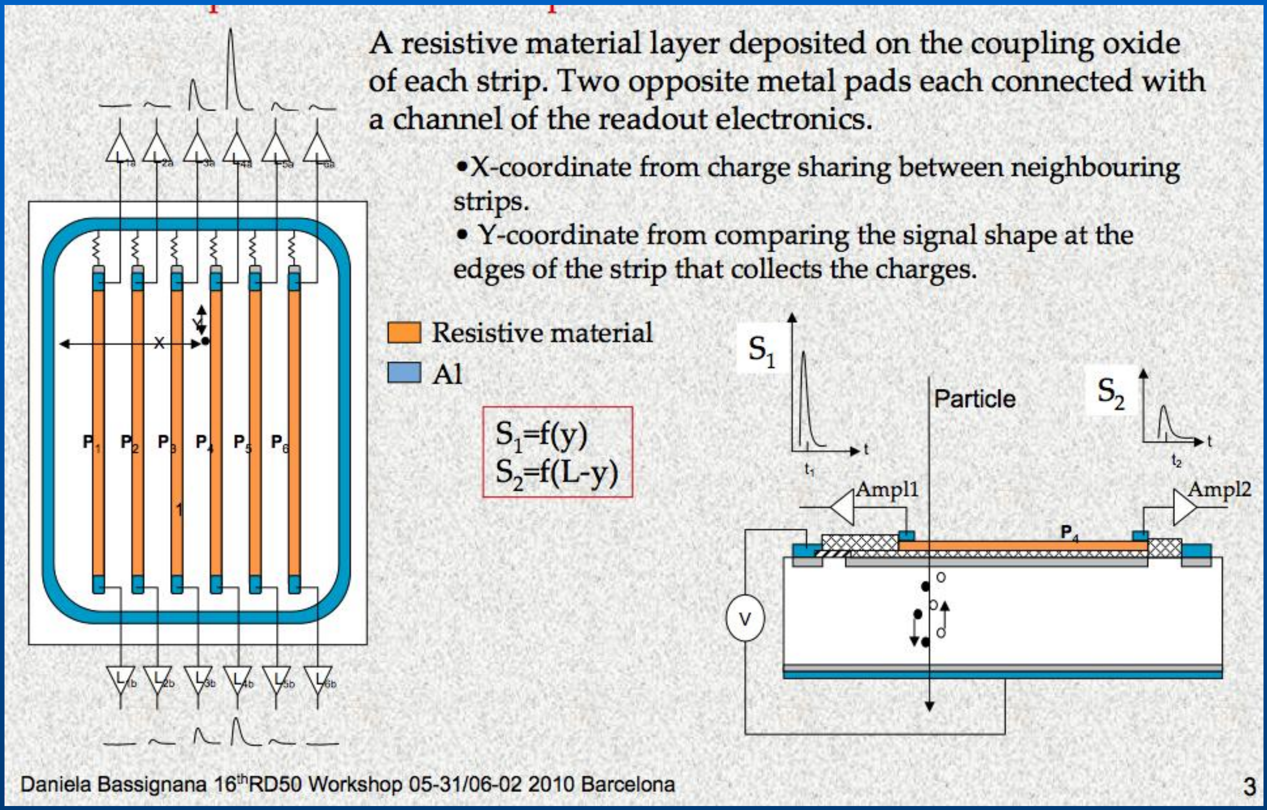


- Signal loss on n-side due to atoll p-stop configuration
- This can also be seen on Signal-to-Noise-plots (right) at cluster sizes > 1



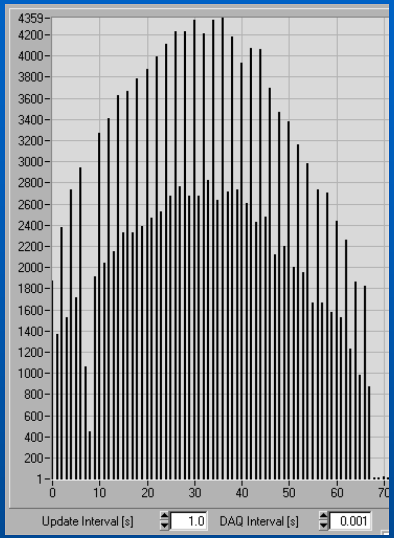
CNM poly-silicon sensors

(see also M. Fernandez and I. Vila)

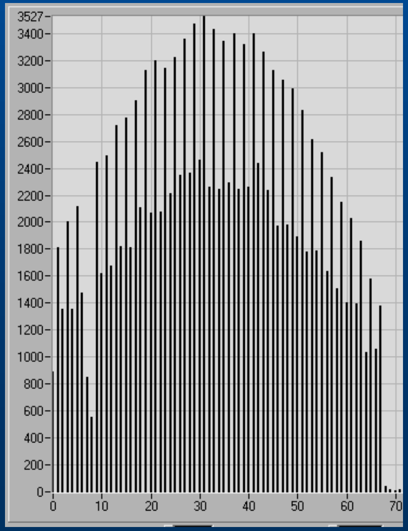


Hitmap

Sensor hit on near side



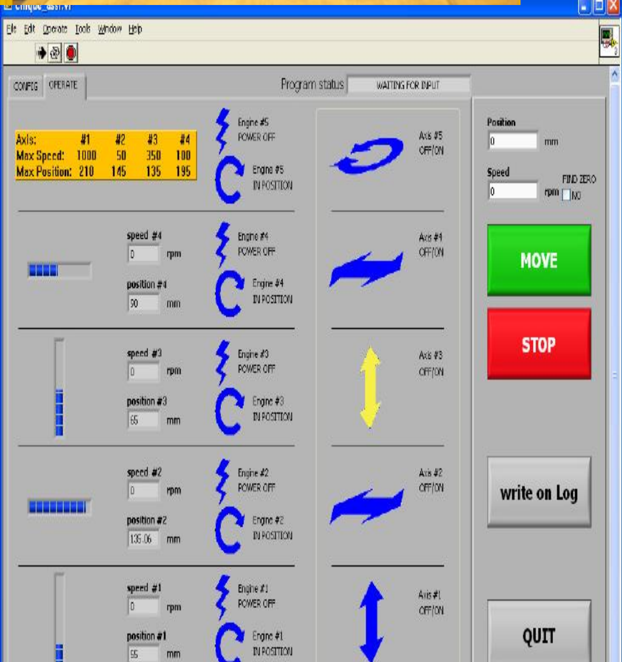
Sensor hit on far side

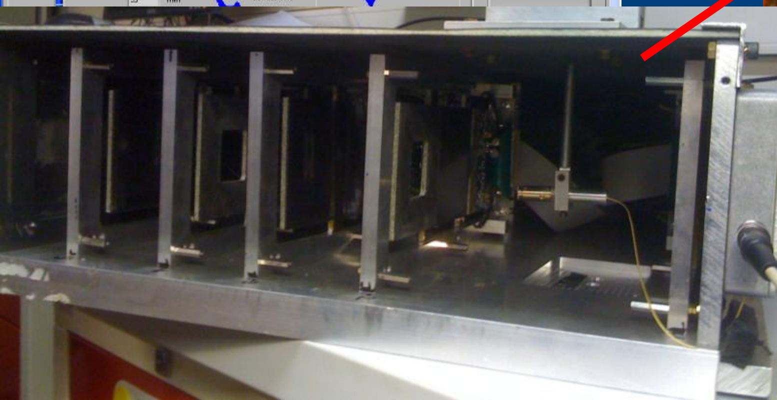


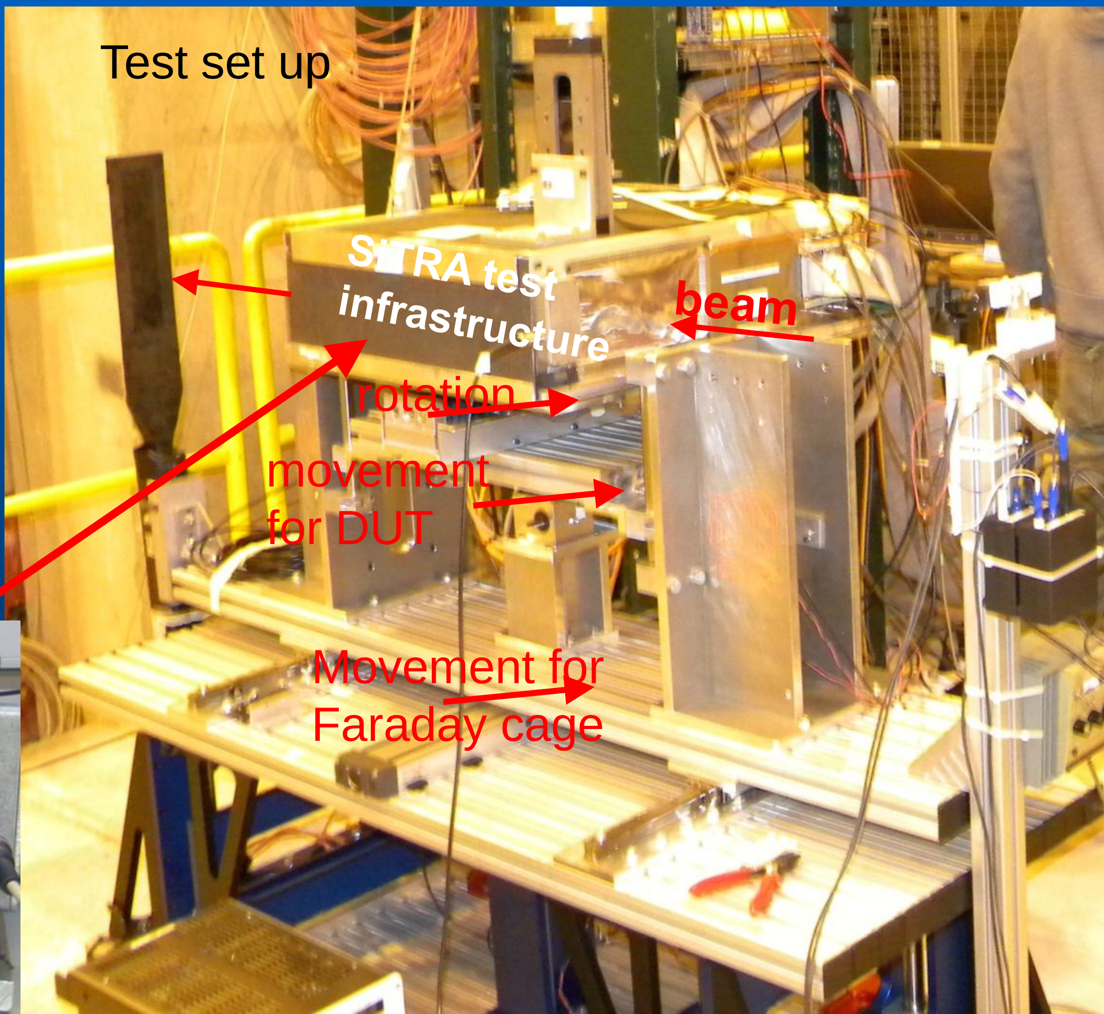
- Sensors with poly-silicon lines act as voltage divider of signal
- Allows to measure coordinate along the strips
- Beam-test: test different positions (right)

STANDALONE & MULTIPURPOSE T.B. INFRASTRUCTURE

- 5 motorized & controlled movements:4 linear+1 rotation;2 movements for test bench; 3 for a 3D DUT scan
- Main feature: highly precise position repeatability: with linear mvt □ 0.1 mm and rot □ 0.01 degree (tested by TB)
- Control by LabView and linked to DAQ-> DUT positions /each run.



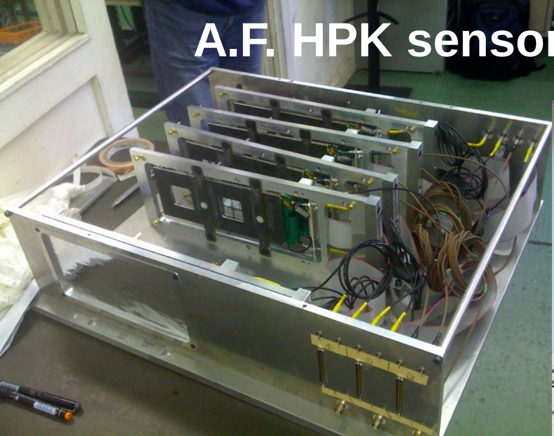


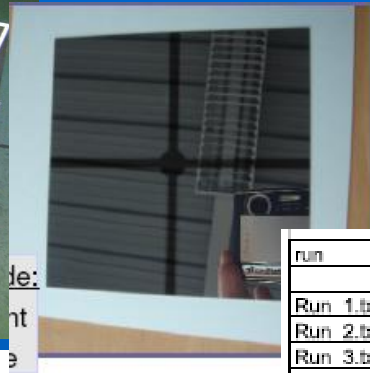


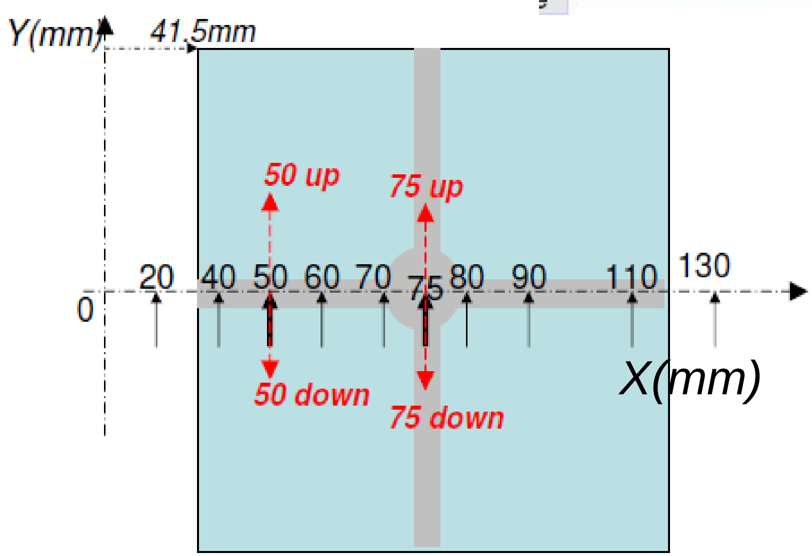
Standalone T.B. infrastructure tests in May 2010

First TB with the new T.B. infrastructure

A.F. HPK sensors







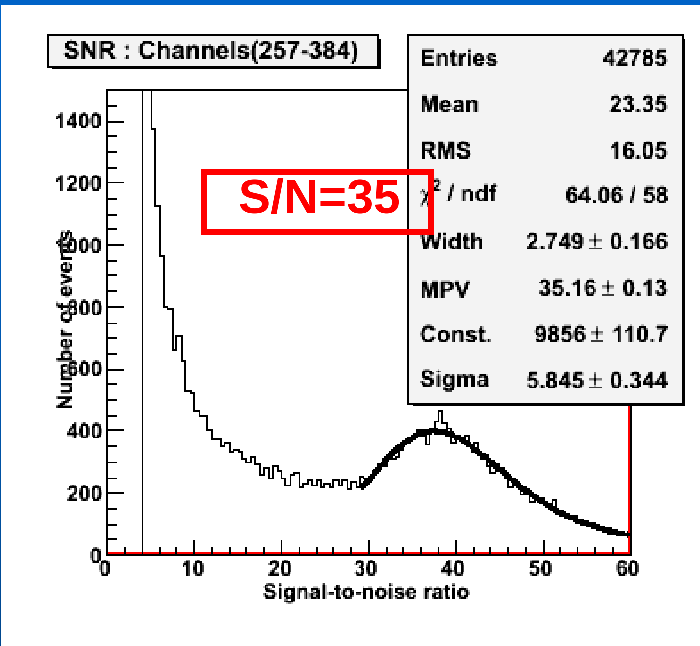
LOGBOOK

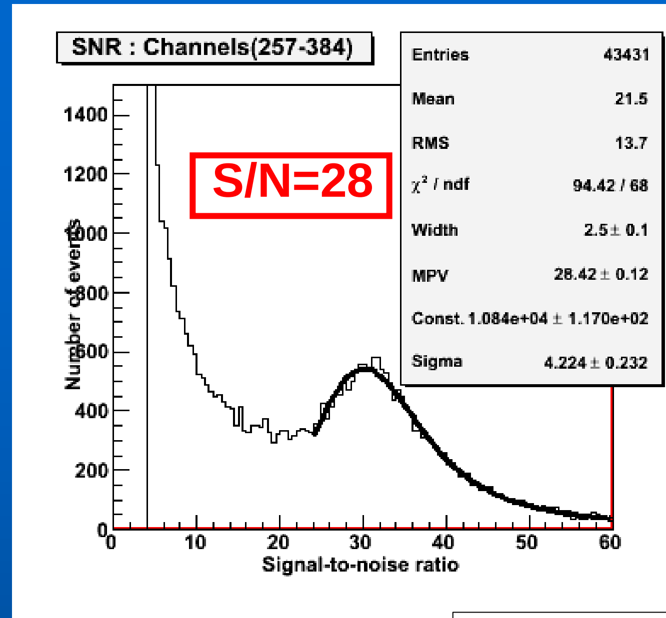
run	jour	heure	Moteur 1	Moteur 2	Moteur 3	Moteur 4	nb evts	plot	file size
Run_1.txt	Thu 13 May 10	19:36	55	102	55	60	5088	Run1Plot.jpg	195M
Run_2.txt	Thu 13 May 10	21:17	55	102	50	60	2004	Run2Plot.jpg	89M
Run_3.txt	Thu 13 May 10	22:04	55	102	45	60	annulé		99M
Run_4.txt	Thu 13 May 10	22:17	55	102	40	60			108M
	Thu 13 May 10	22:52	55	102	40	60			
Run_5.txt	Thu 13 May 10	23:45	55	135	40	60			55M
Run_6.txt	Thu 13 May 10	?	55	135	variable	60			62M
Run_7.txt	Thu 13 May 10	?	55	135	70	60		Run7Plot.jpg	38M
Run_8.txt	Thu 13 May 10	?	55	135	70	60	60000 (?)		1400M
Run_9.txt	Fri 14 May 10	08:46	55	135	70	80	1039		38M
Run_10.txt	Fri 14 May 10	09:10	55	135	70	100	1034		38M
Run_11.txt	Fri 14 May 10	09:25	55	135	70	120	1047	Run11Plot.jpg	38M
Run_12.txt	Fri 14 May 10	09:44	55	135	70	130	1025	Run12Plot.jpg	45M
Run_13.txt	Fri 14 May 10	10:04	55	135	70	20	961	Run13Plot.jpg	42M
Run_14.txt	Fri 14 May 10	10:18	55	135	70	30	1013		45M
Run_15.txt	Fri 14 May 10	10:50	55	135	70	50			956M
Run_16.txt	Fri 14 May 10	16:50	55	135	70	60			791M
Run_17.txt	Fri 14 May 10	16:55	55	135	70	70			948M
Run_18.txt	Fri 14 May 10	20:13	55	135	70	80			951M
Run_19.txt	Fri 14 May 10	23:30	55	135	70	75	57406		2800M
Run_20.txt	Sat 15 May 10	08:25	55	135	70	90	20046		950M
Run_21.txt	Sat 15 May 10	12:38	55	135	70	110	20038		950M
Run_22.txt	Sat 15 May 10	16:01	55	135	65	90	19997		948M
Run_23.txt	Sat 15 May 10	19:54	55	135	75	50			950M
Run_24.txt	Sun 16 May 10	00:17	55	135	65	75			950M
Run_25.txt	Sun 16 May 10	04:45	55	135	75	75	19999		950M
Run_26.txt	Sun 16 May 10	09:00	55	135	70	60			

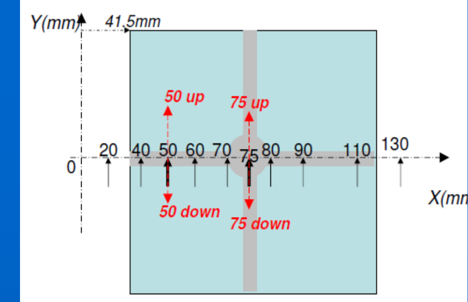
Detailed test response uniformity along the region with Al back plane removed & also wrt region with Al in back plane (still in progress)

- 5 modules
- different run conditions: positions, polar
=> Lot of data!

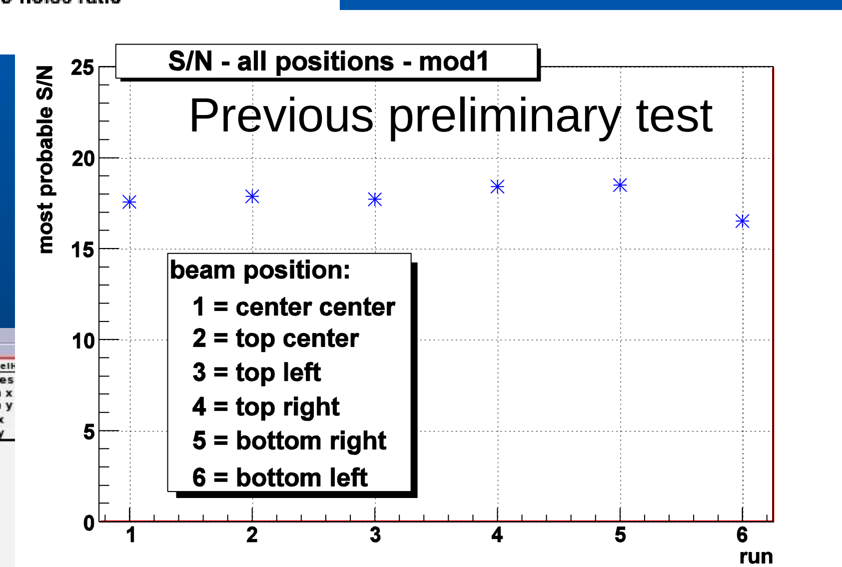
Data Analysis

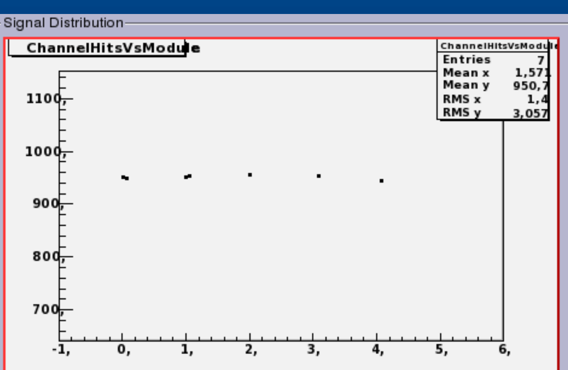


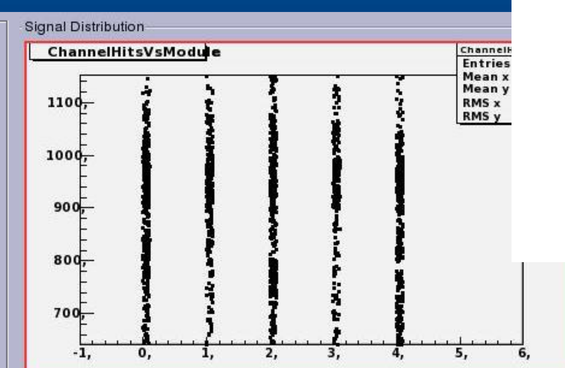




Evaluate S/N for each position and verify result is independent of scan position.

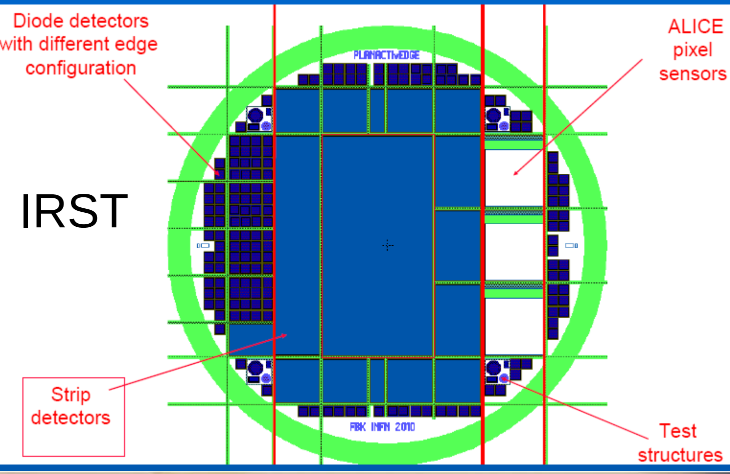


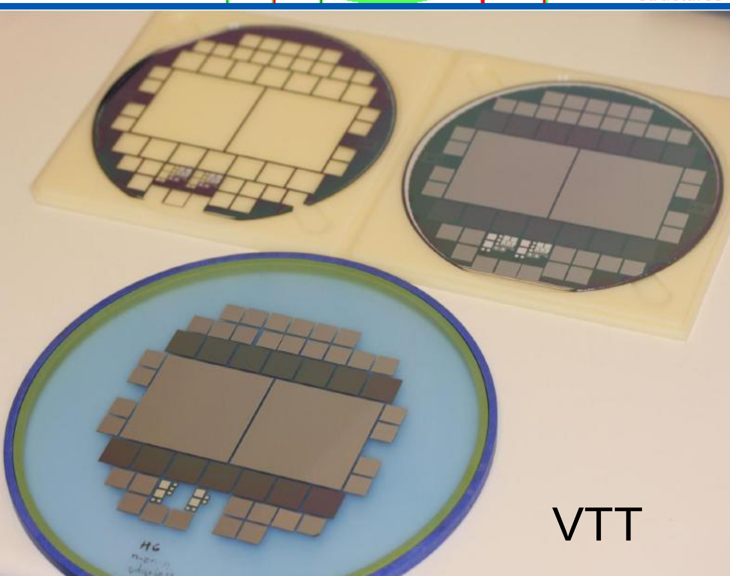




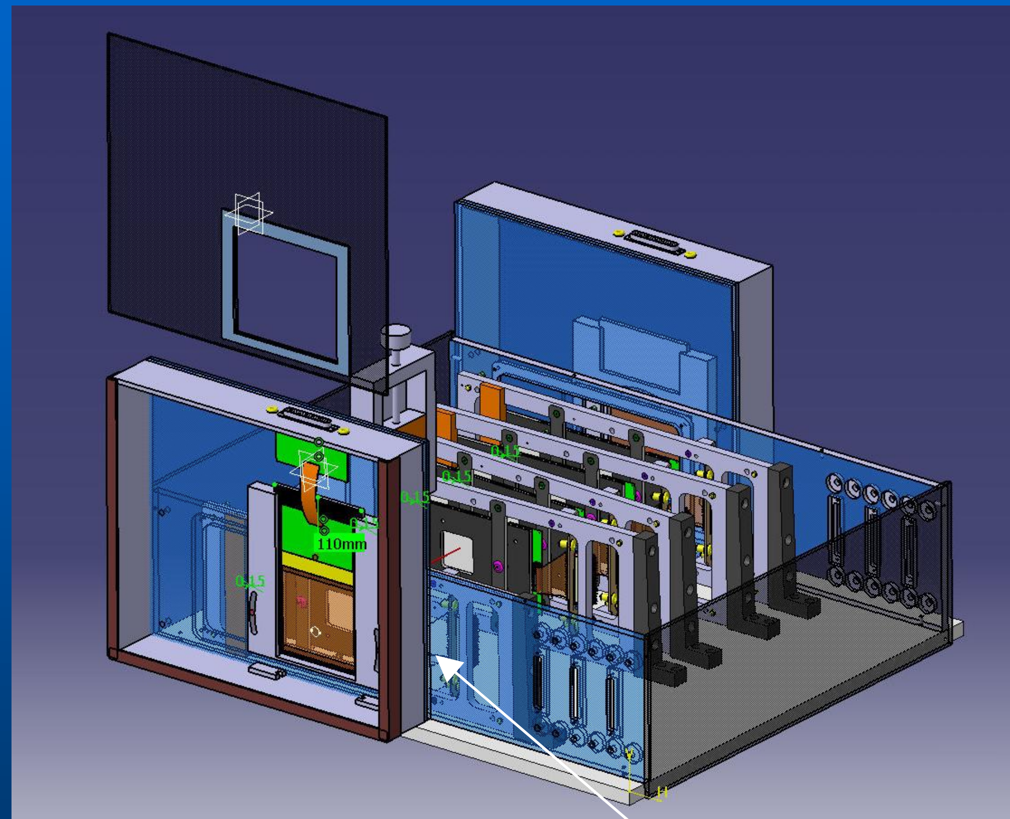
In progress: Tracks reconstruction (5 layers)

Nov'10:Test of new edgeless Si sensors (IRST+VTT+Paris)



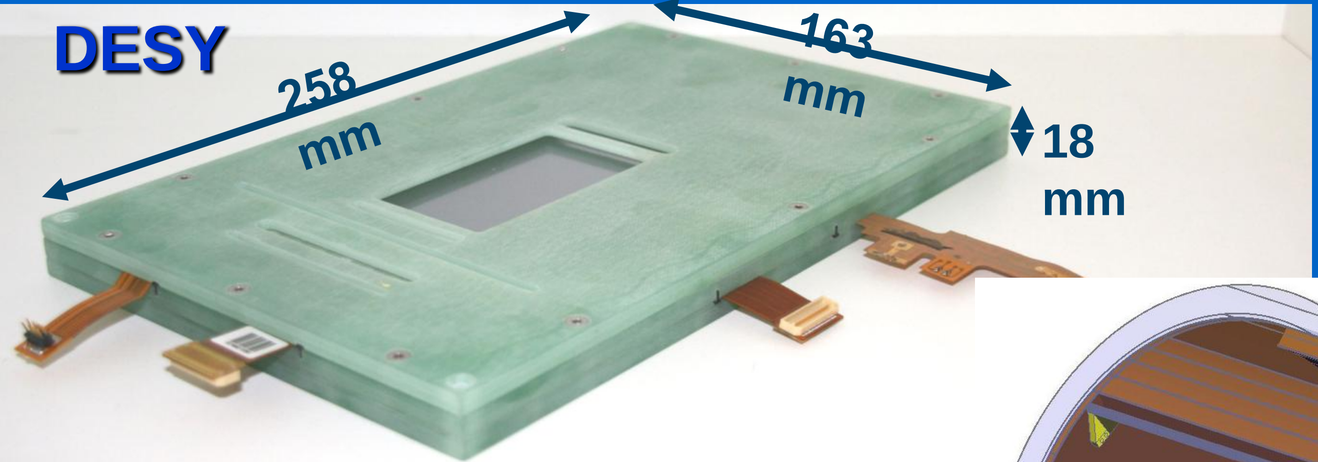


Nov TB at CERN, with standalone infrastructure to test new Si strip technologies



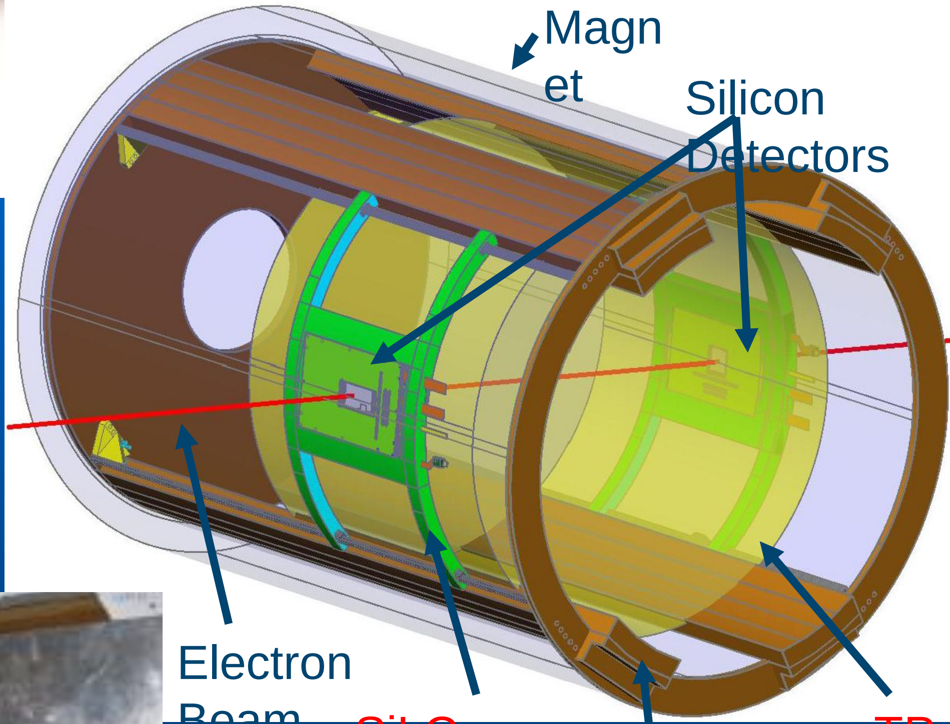
And eventually even more (IFCA & NRNU)

updates on the test set-up are prepared



Final detector module thickness: 18mm+2 mm
=> Safety clearance of 4mm to TPC & magnet

SiLC-LCTPC
(HEPHY-IEKP)



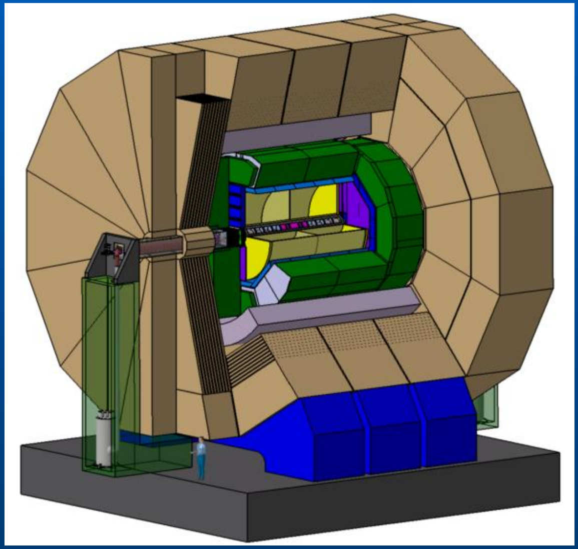
1st with Micromegas:
⇒set-up the test Pb with synchro between 2 DAQs
⇒Now test with 3GEM; more data to be taken
=> Test set-up will continue running

Goal: test Silicon Envelope to TPC

Developing Si tracking concepts:

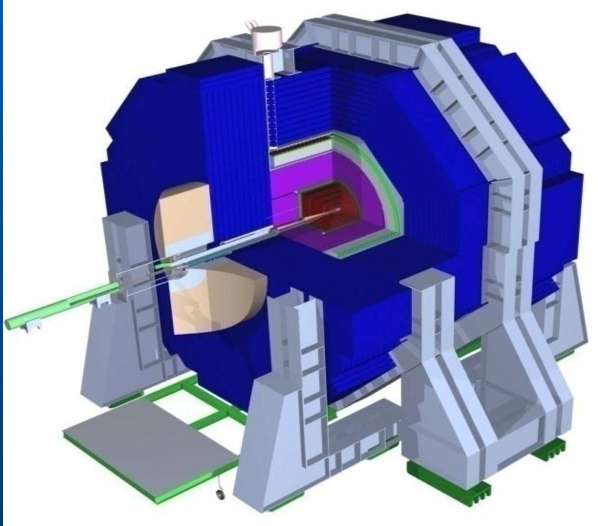
- Preparation of the LOI's of ILC detector concepts:
  addressing integration issues for 2 tracking concepts

Hybrid: TPC+Si



Fully developed in ILD concept by SiLC:
(Evaluation by IDAG for LOI)

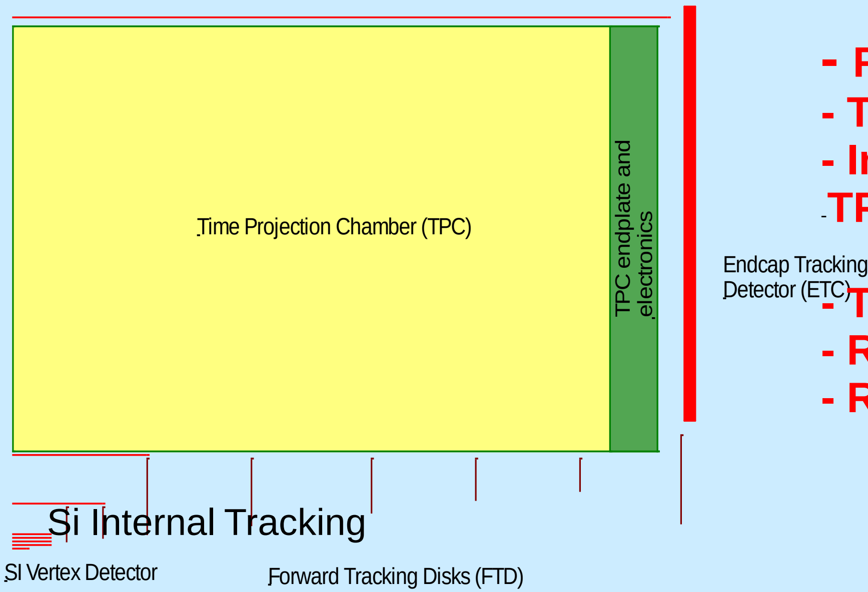
All Si-tracking



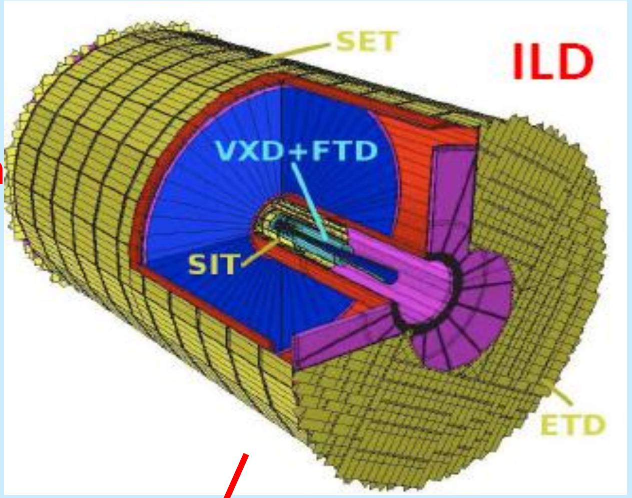
Several SiLCcollaborators in SiLC LOI
SiLC is working on developing further the all-Si tracking concept (including longer term idea: strips-> pixels)

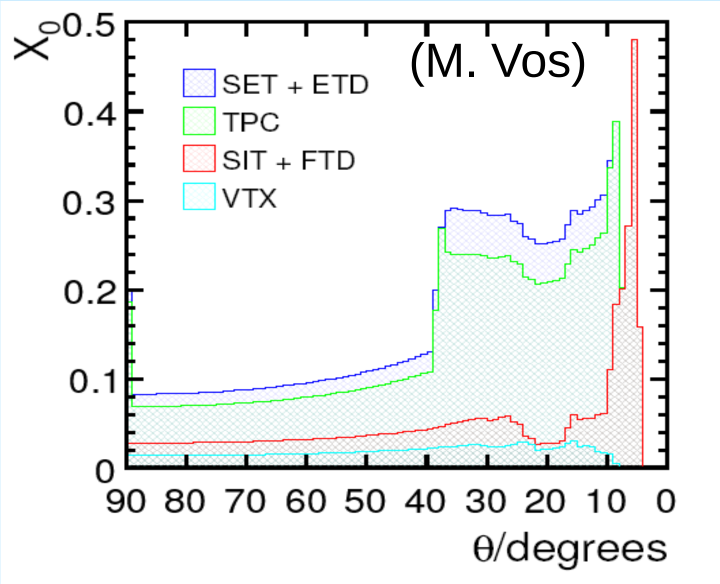
- Now preparing for the DBD 2012

The ILD Si Tracking Baseline System : the Si Enveloppe (SiLC)



- Full coverage
- Tracking hermiticity
- Improve P-resolution
- TPC distorsion monitoring
- Time stamping
- Robustness
- Redundancy

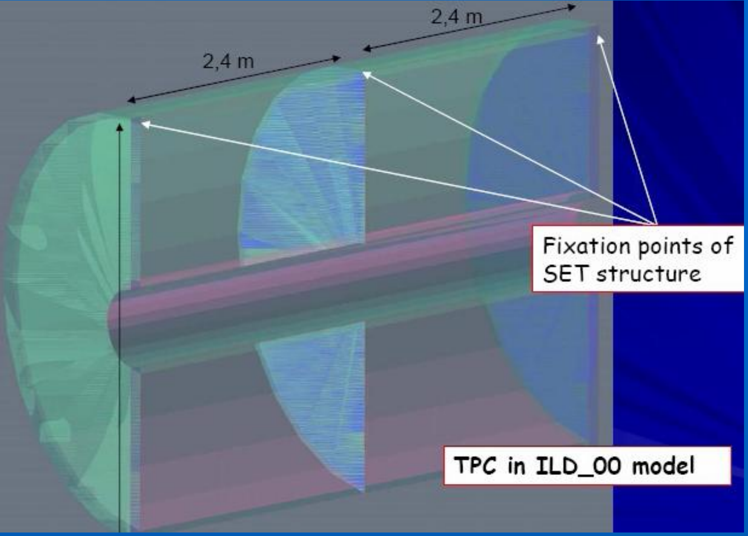


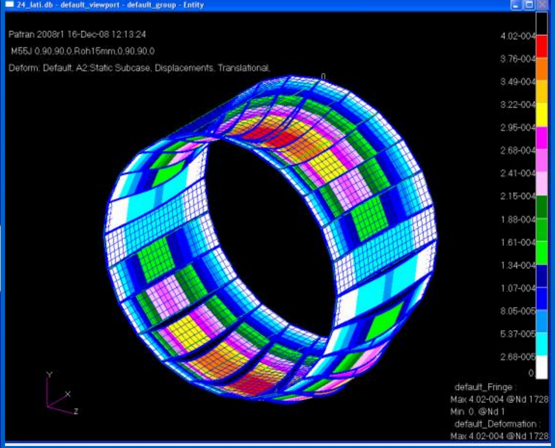


Low material budget

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

SET/ETD: CAD & INTEGRATION

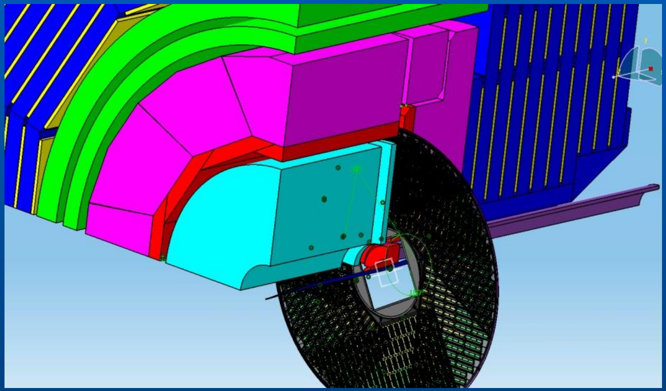


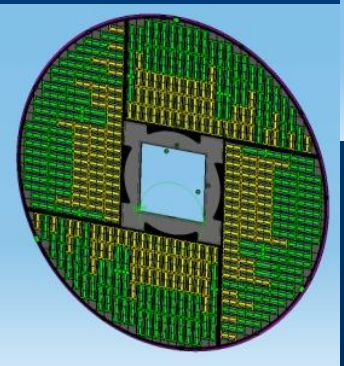


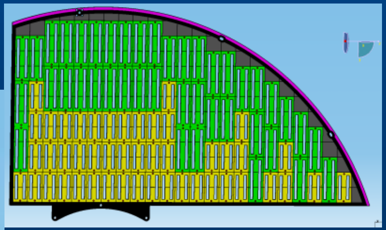
CAD design of the SET & SIT/SET possible common support (Torino)

SIT: Korea+Torino+LPNHE

CAD for ETD (LPNHE)

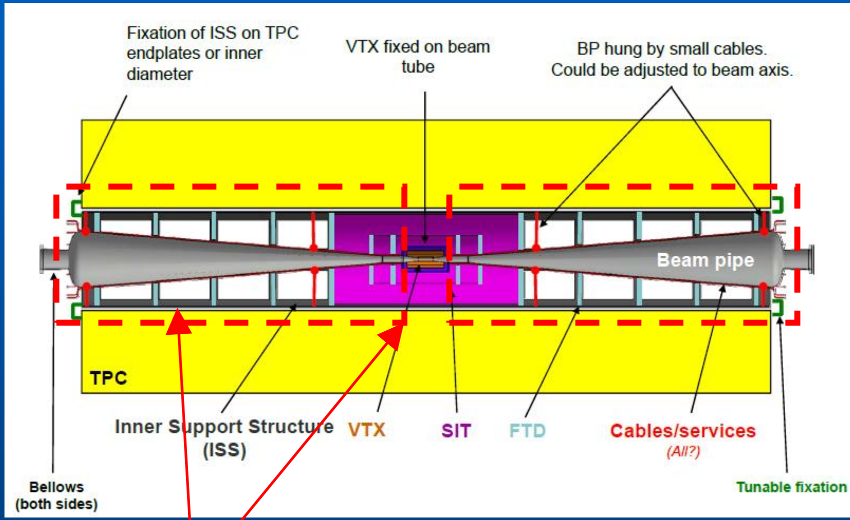




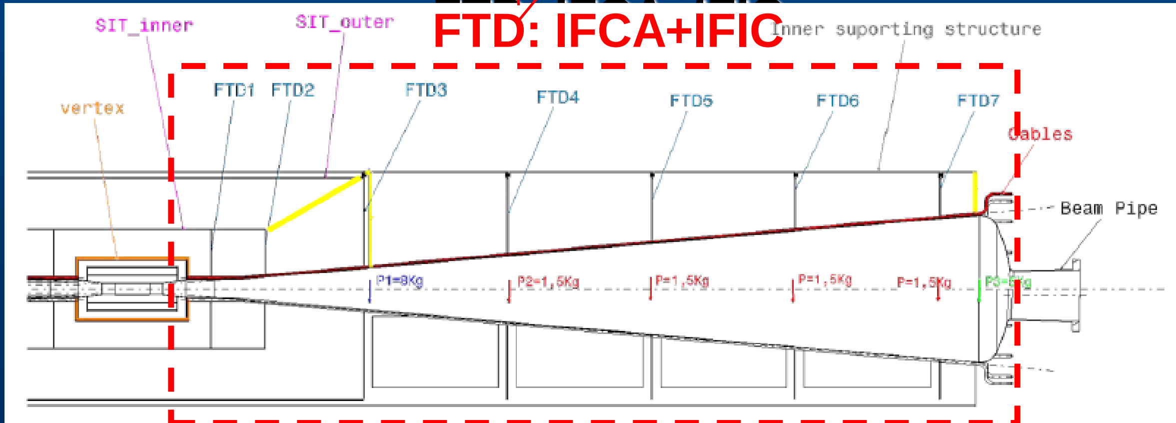


FTD:

mix pixels + strips + A.F. strips system



FTD: IFCA+IFIC

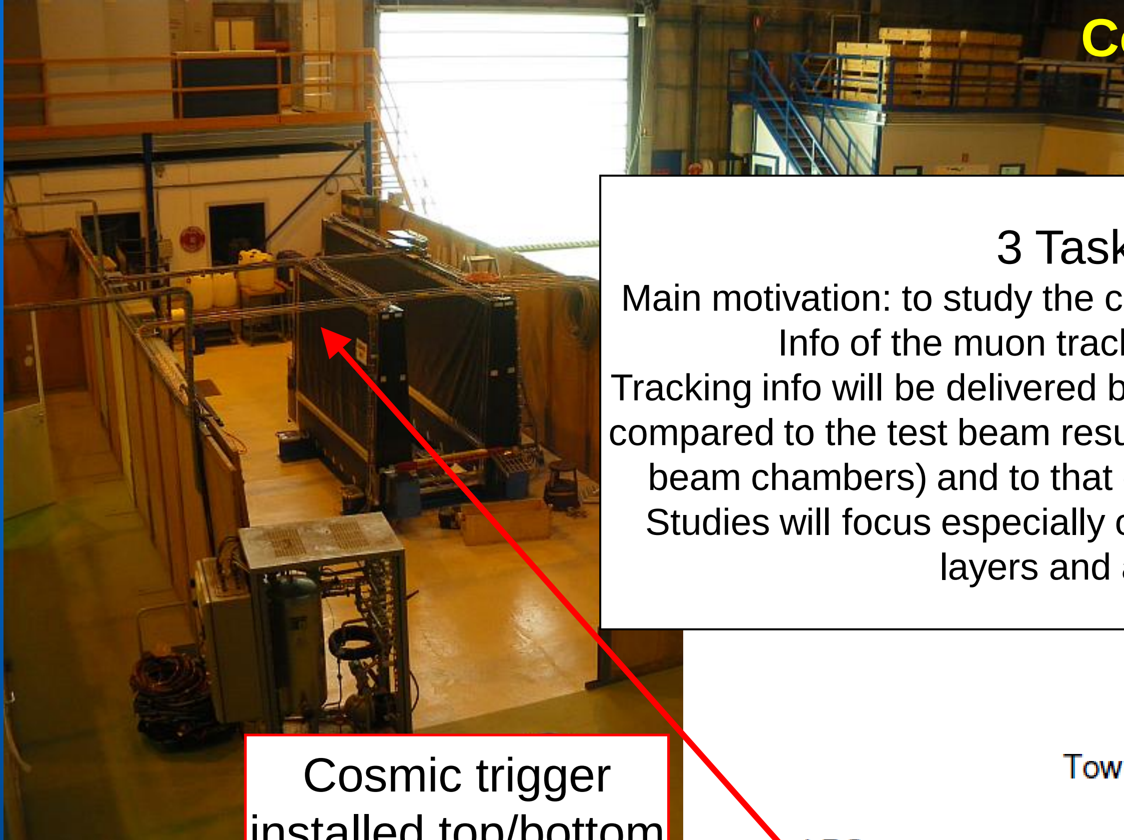


Outcomes and perspectives

Apart from the **synergy with the *upgrades of the large area Si tracker at LHC (ATLAS & CMS)*** there are new important outcomes and perspectives for SiLC R&D:

- Opening to CLIC (FEE, time stamping, sensors, simulation studies & detector performances etc.)
- ATLAS TileCal
- ***Interest from short term future experiments***
  - BELLE II
  - g-2/EDM JPARC experiment

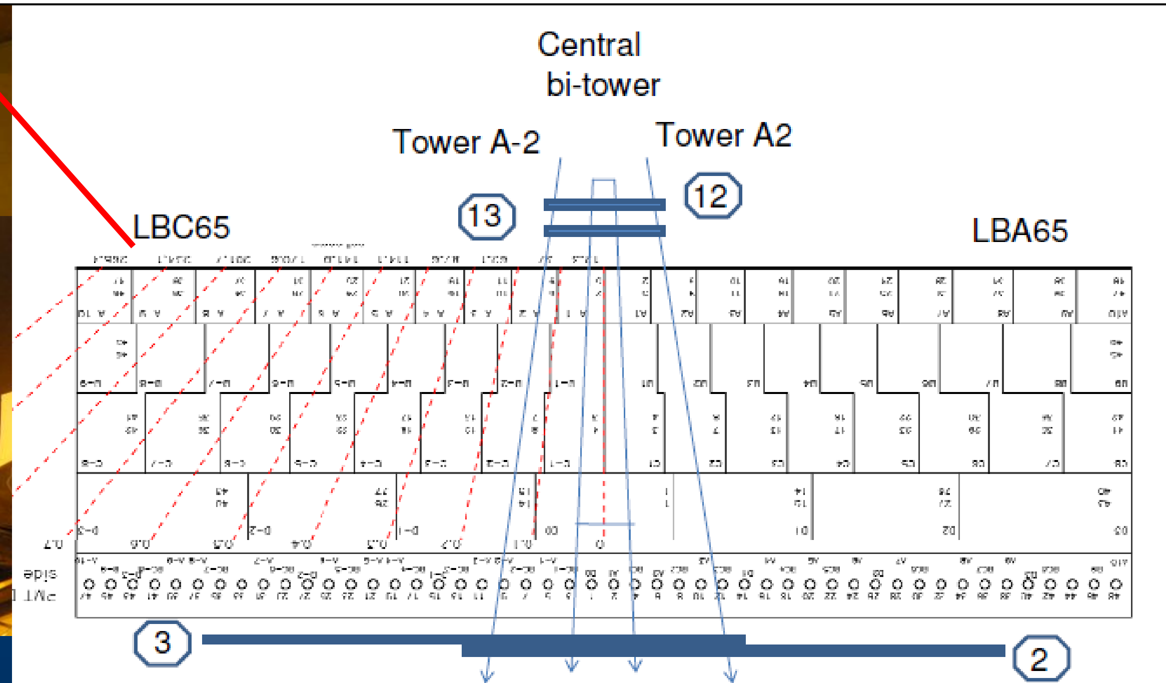
Cosmic ATLAS TileCal test set-up at CERN



3 Tasks to be studied

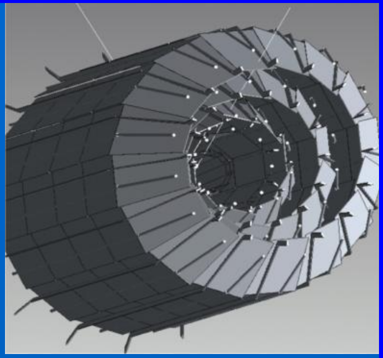
Main motivation: to study the cosmic muon response using rather precise Info of the muon track passing through the calorimeter.
Tracking info will be delivered by the Si strip detector. The response can be compared to the test beam results (where tracking info was provided by the beam chambers) and to that of cosmic muons in the full ATLAS setup.
Studies will focus especially on the intercalibration of the TileCal radial layers and associated systematics.

Cosmic trigger installed top/bottom scintillator pairs

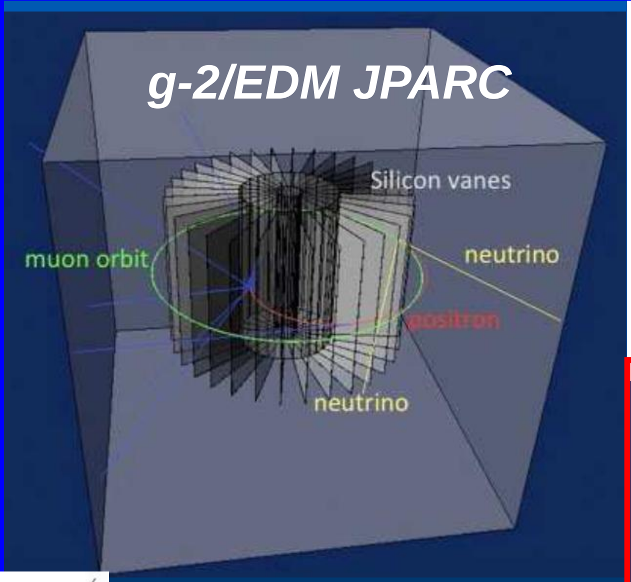


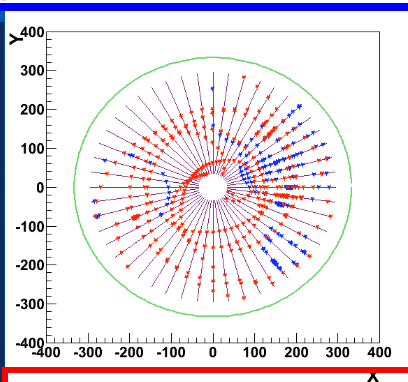
This test set-up will be pursued these next coming years

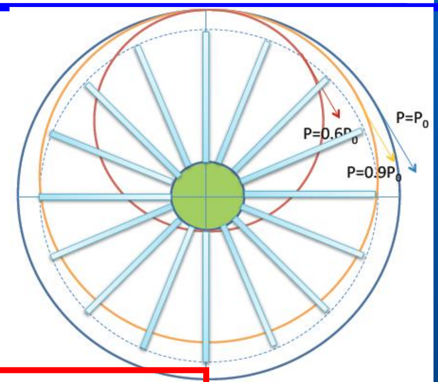
BELLE II	Belle SVD	Belle upgrade SVD
Vertex detector (radius, cm)	4 layer DSSD (2.0<R<10.0)	2 layer DEPFET (1.8<R<2.2) 4 layer DSSD (4<R<14)
Readout / shaping time	VA1TA / 0.8 μsec	APV25 / 0.05 μsec
Silicon area (m^2)	0.6	1.2



2009/8: HPK starts 6" DSSD production line
2009/9: 6" design submitted to HPK
2010/3: Prototype sensors from pilot batch by KEK & Micron







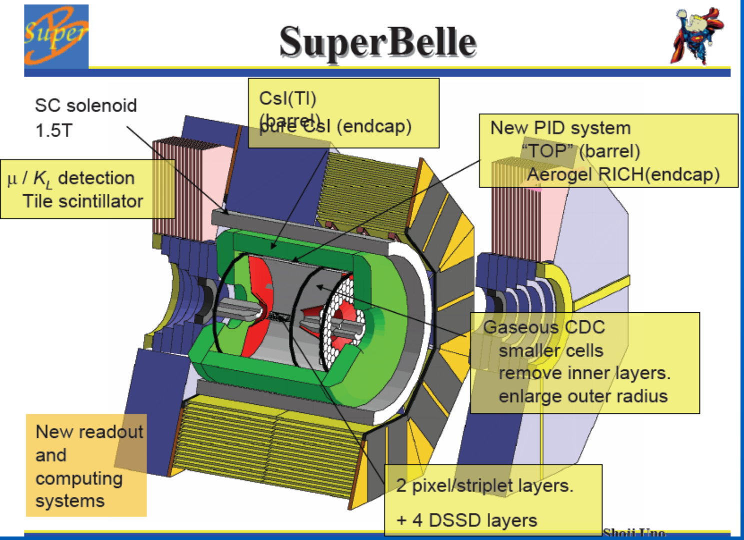
Collaboration:
- ❖Test beam infrastructure => tests
- ❖ FEE
- ❖ Alignment system
- ❖ Direct connect FEE/strips

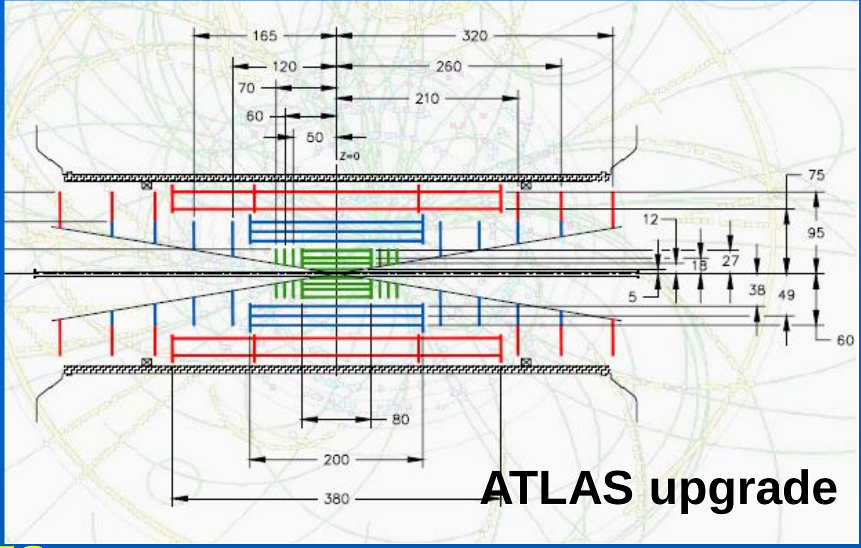
EUDET-memo in preparation

Will be pursued these next years

Concluding remarks

- Lot of progress on all the fronts of R&D objectives, **focusing on well defined baselines**
- Very **intense test bench and test beam activities** that are **validating the advances** on the various R&D basic objectives
- With development of the needed tools (hard & soft)
- Developments of the **simulations**
- **Instrumental** participation **to the LOI's** (esp. ILD)
- Pursue **LHC synergy** (upgrades) & Opening to CLIC
- Launched **contributions** to other applications (**experiments**) **well focused and of direct interest for SiLC R&D goals:**
- **REAL ASSETS for speeding up the developments of the various R&D basic objectives**
- EUDET was instrumental for financing & job positions





SYNERGIES

SYNERGIES

SYNERGIES

SYNERGIES