The LP Setup at DESY: a Status Report

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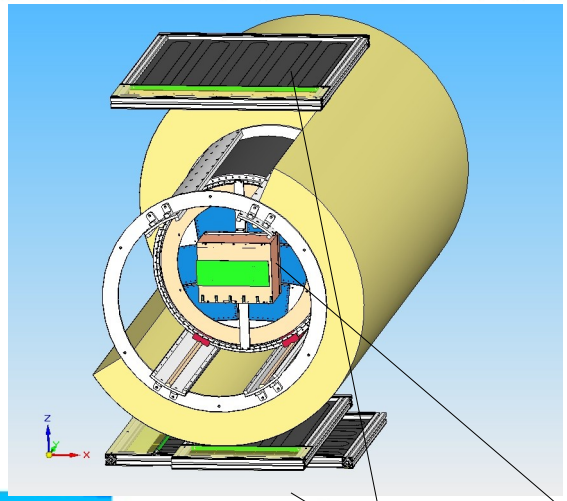
DESY

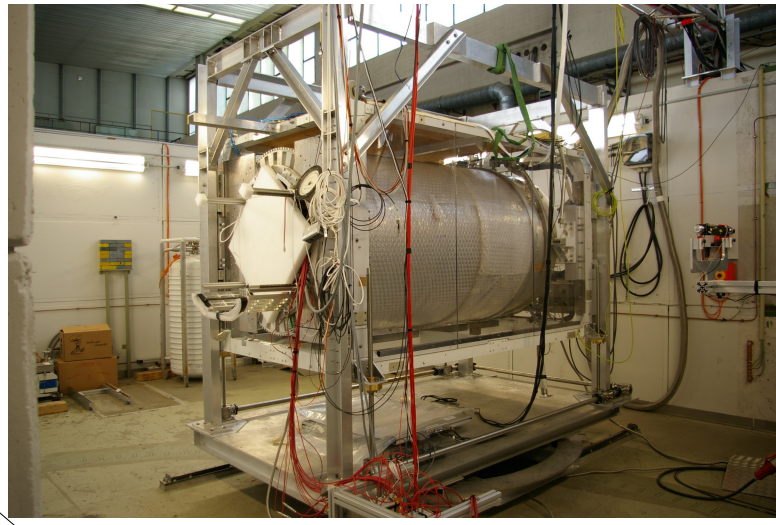
IWLC 2010 - CERN/CICG

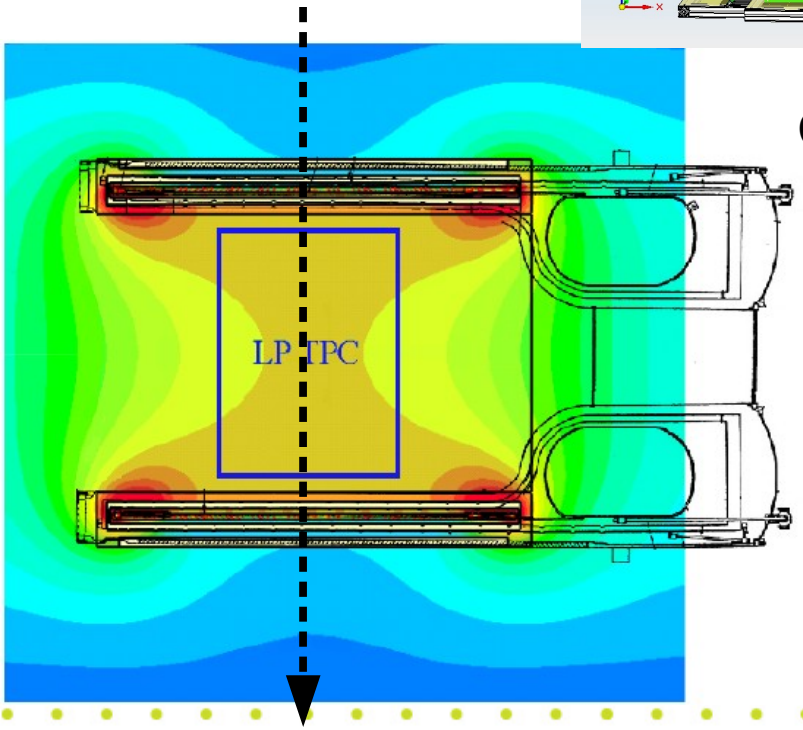
October 20th, 2010

The LP Setup

- *LP: Large Prototype*
- *PCMAG:* superconducting magnet, up to 1.25 T
- e^- test beam @DESY (1GeV/c<p<6GeV/c)

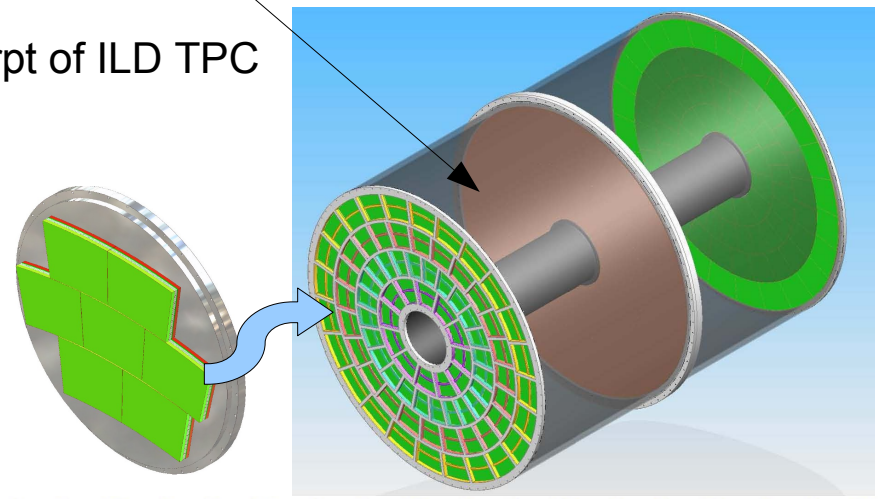




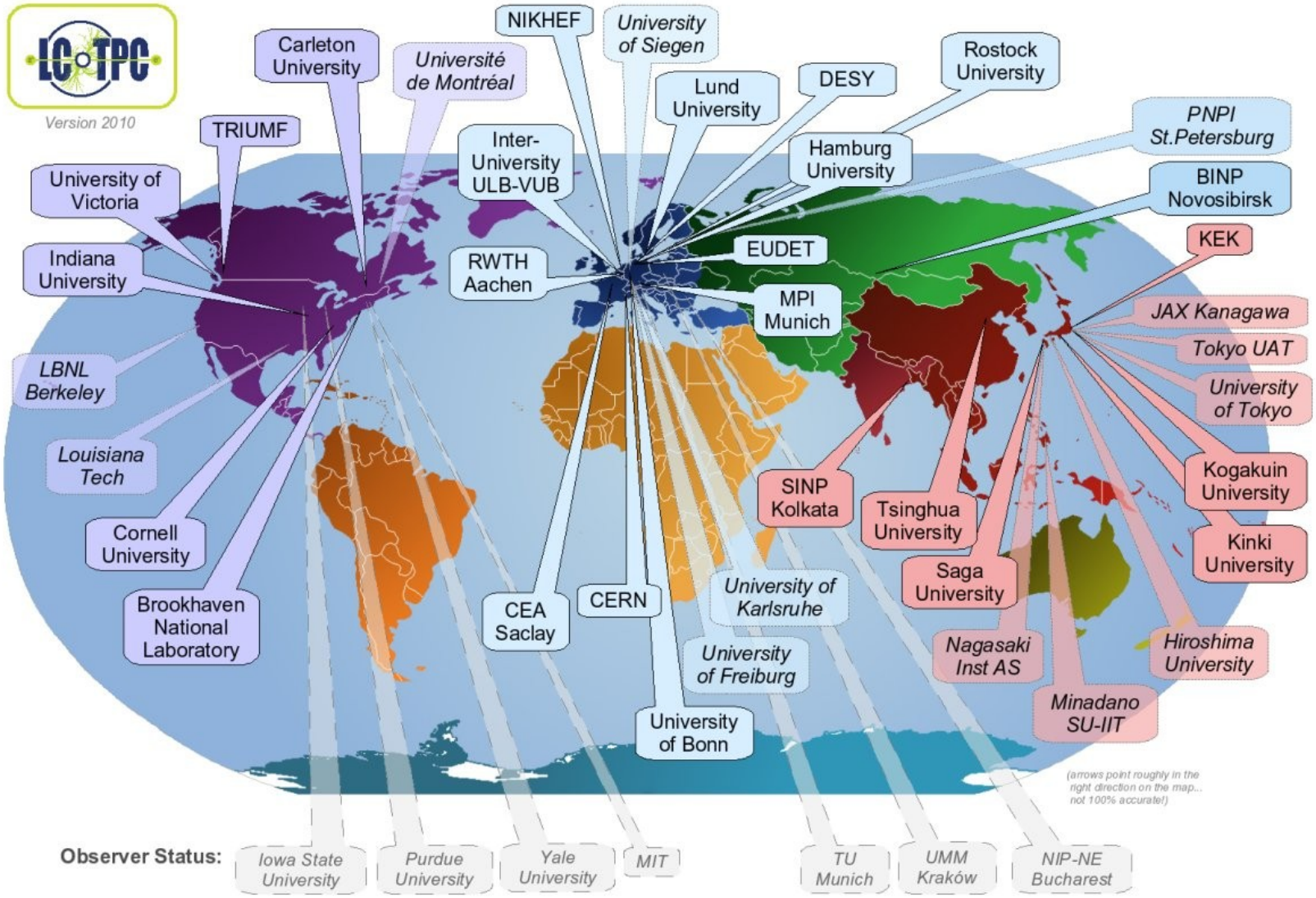


Cosmic Trigger Setup

LP as excerpt of ILD TPC



LCTPC, the Collaboration



The TPC and the ILC

Size	$\phi = 3.6$m, L = 4.3m outside dimensions
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 9 \times 10^{-5}$/GeV/c TPC only ($\times$ 0.4 if IP incl.)
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 2 \times 10^{-5}$/GeV/c (SET+TPC+SIT+VTX)
Solid angle coverage	Up to $\cos\theta \simeq 0.98$ (10 pad rows)
TPC material budget	$\sim 0.05 X_0$ including the outer fieldcage in r
	$\sim 0.25 X_0$ for readout endcaps in z
Number of pads/timebuckets	$\sim$ 1 - 2×10^6/1000 per endcap
Pad size/no.padrows	$\sim$ 1mm$\times$4–6mm/$\sim$200 (standard readout)
σ_{point} in $r\phi$	$< 100\mu$m (average over $L_{sensitive}$, modulo track ϕ angle)
σ_{point} in rz	$\sim$ 0.5 mm (modulo track θ angle)
2-hit resolution in $r\phi$	$\sim$ 2 mm (modulo track angles)
2-hit resolution in rz	$\sim$ 6 mm (modulo track angles)
dE/dx resolution	$\sim$ 5 %
Performance	$>$ 97% efficiency for TPC only ($p_t > 1$GeV/c), and
	$>$ 99% all tracking ($p_t > 1$GeV/c)[6]
Background robustness	Full efficiency with 1% occupancy,
	simulated for example in Fig. 1.2(right)
Background safety factor	Chamber will be prepared for 10 $\times$ worse backgrounds
	at the linear collider start-up

Performance goals and design parameters for a standard electronics ILC TPC

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MPGD

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σ_{point} in $r\phi$	$< 100\mu$m (average over $L_{sensitive}$, modulo track ϕ angle)
σ_{point} in rz	~ 0.5 mm (modulo track θ angle)
2-hit resolution in $r\phi$	~ 2 mm (modulo track angles)
2-hit resolution in rz	~ 6 mm (modulo track angles)
dE/dx resolution	~ 5 %
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Background robustness	Full efficiency with 1% occupancy,
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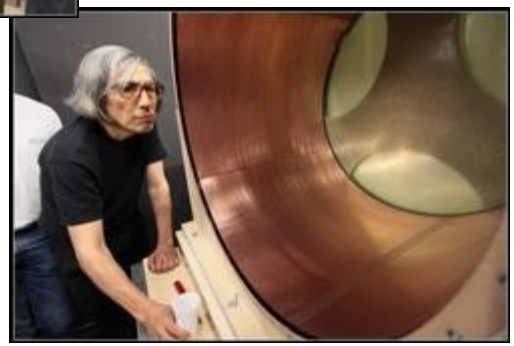
Performance goals and design parameters for a standard electronics ILC TPC

TPC Prototyping

- Large TPC prototype
  - $O(\varnothing) \approx 1$ m
  - low mass field cage
  - modular endplate system for large surface GEM and MicroMegas system
  - development of prototype electronics for GEM and MicroMegas
- Large bore magnet PCMAG JRA2:
  - B $\approx$ 1 Tesla, $\varnothing \approx$ 0.85 m, standalone He cooling, provided by KEK
  - infrastructure (control, fieldmapping etc.) through EUDET
- Si-envelope

The Field Cage



Diameter: Inner 720 mm,

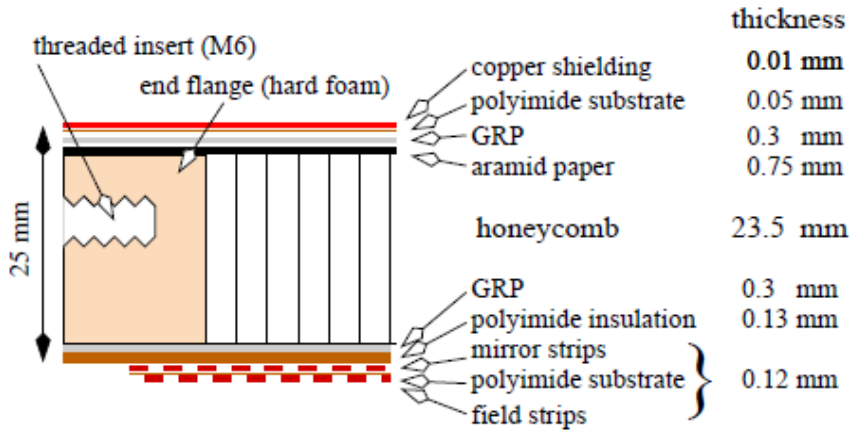
Outer 770 mm

Wall thickness 25 mm

Length 610 mm

HV to be applied: up to 20 kV

Tested up to 30 kV



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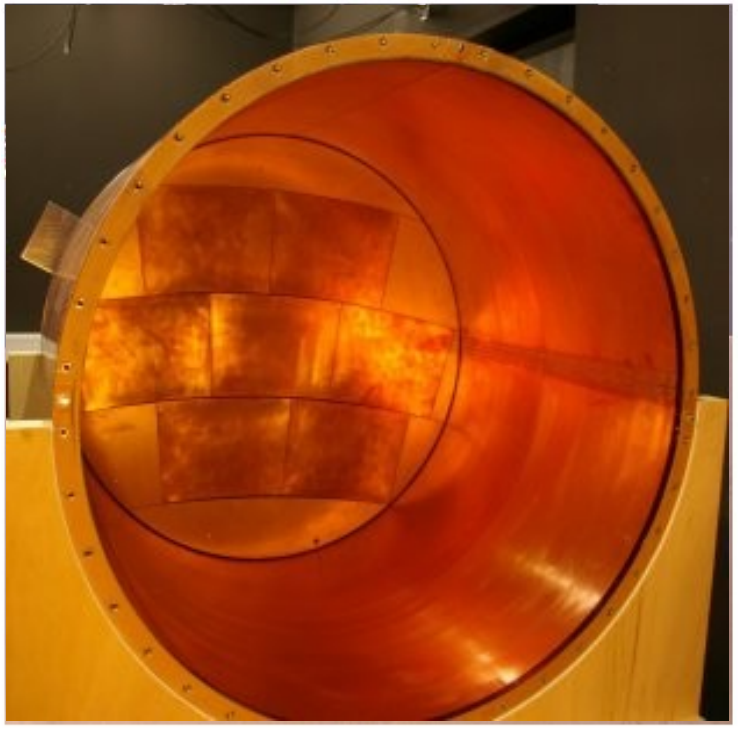
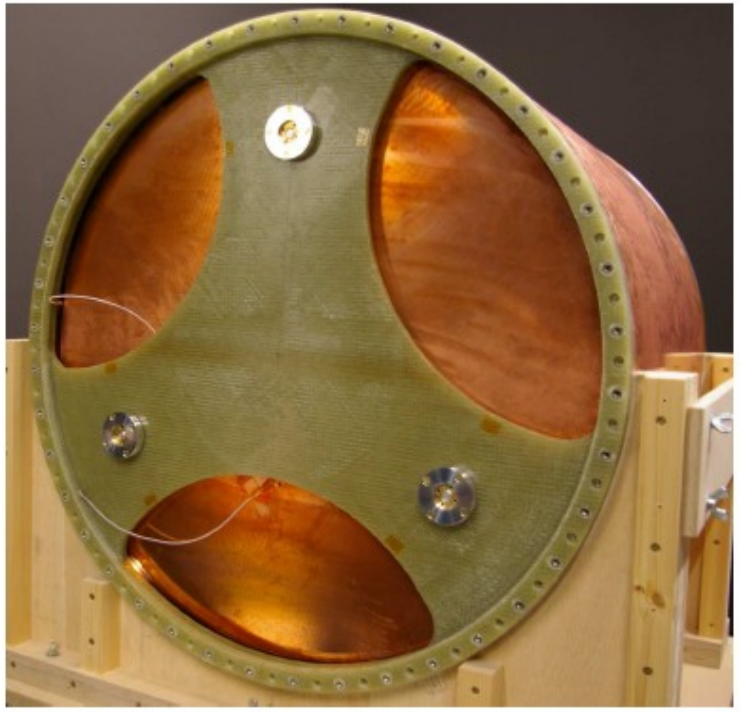
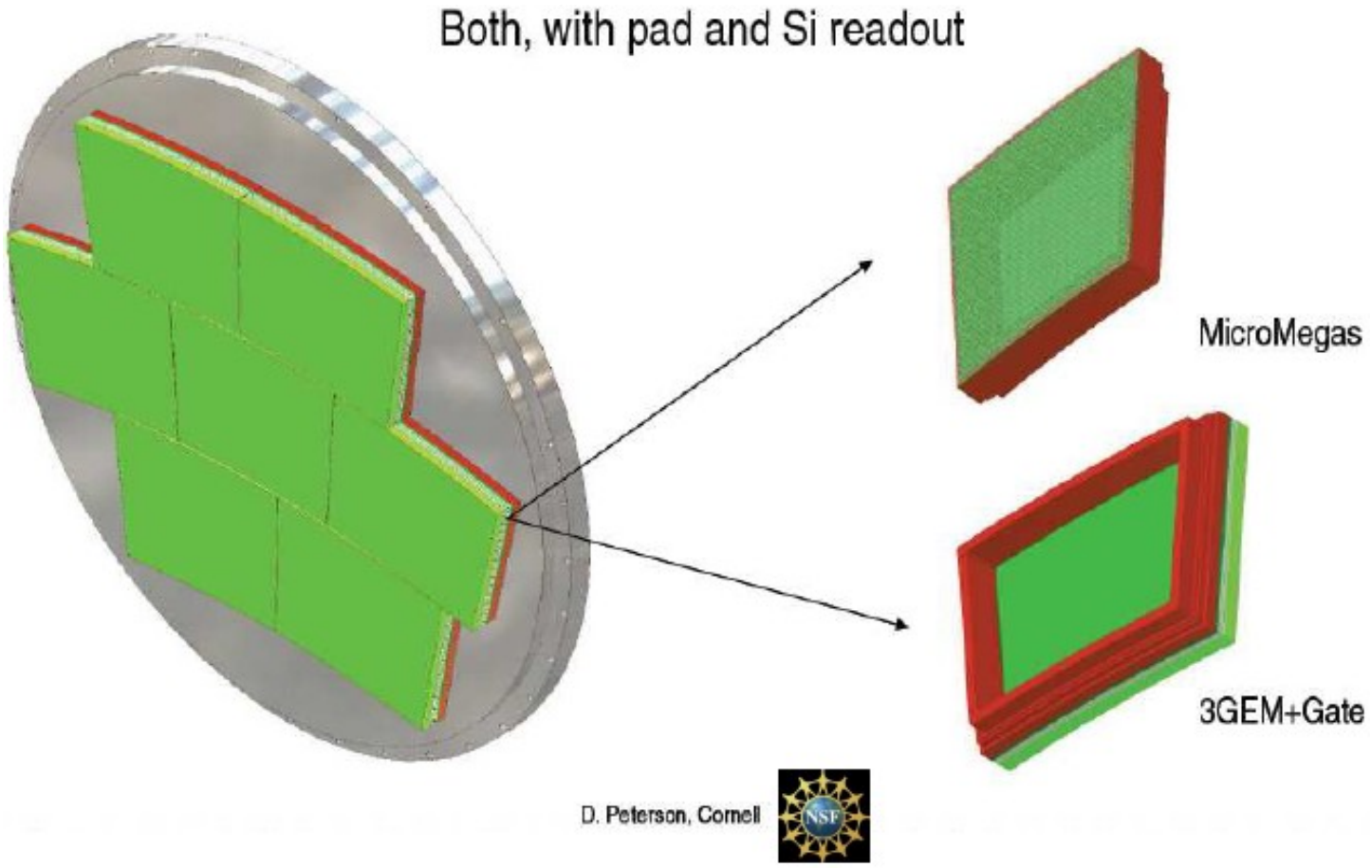


field cage with anode end plate



field cage with cathode end plate

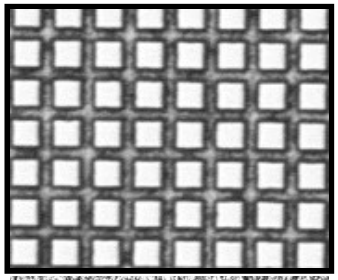
End Plate for Readout Modules

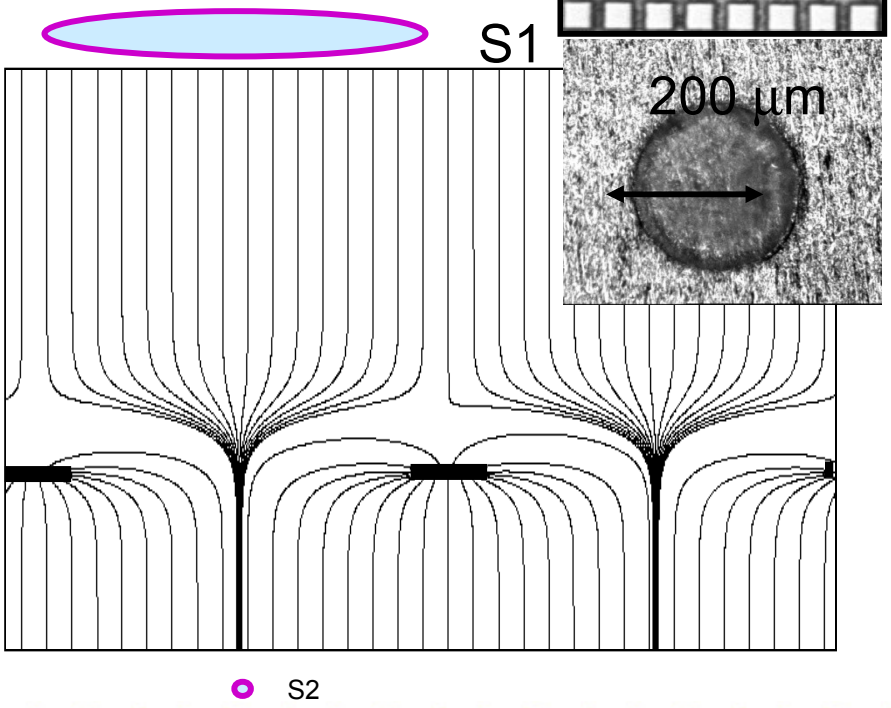


GEM and Micromegas

Micromegas

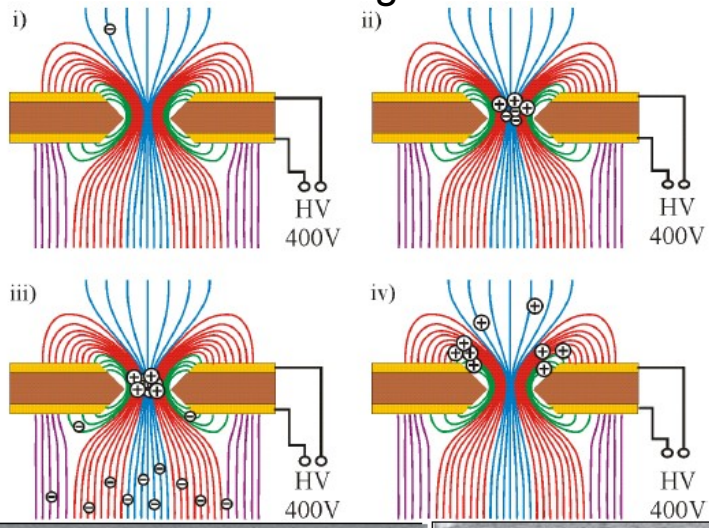
Micromesh supported by 50-100 μm - high insulating pillars. Multiplication takes place between the anode and the mesh

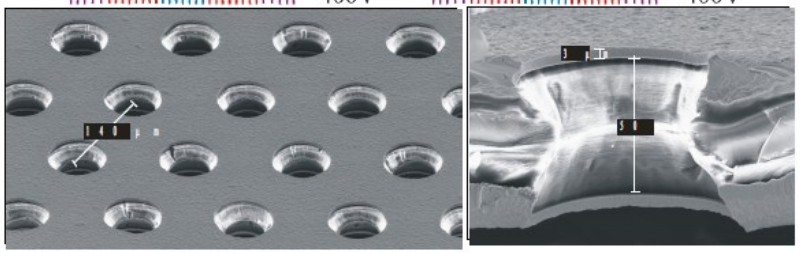




GEM

Polyimide film 50 μm thick, highly perforated with ~ 70 μm holes, copper cladded on both sides. Multiplication takes place in the holes. Usually used in 2 or 3 stages.





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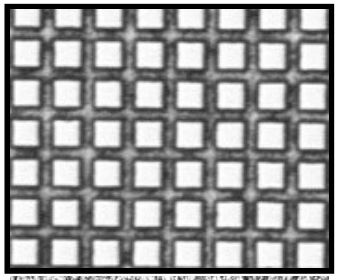

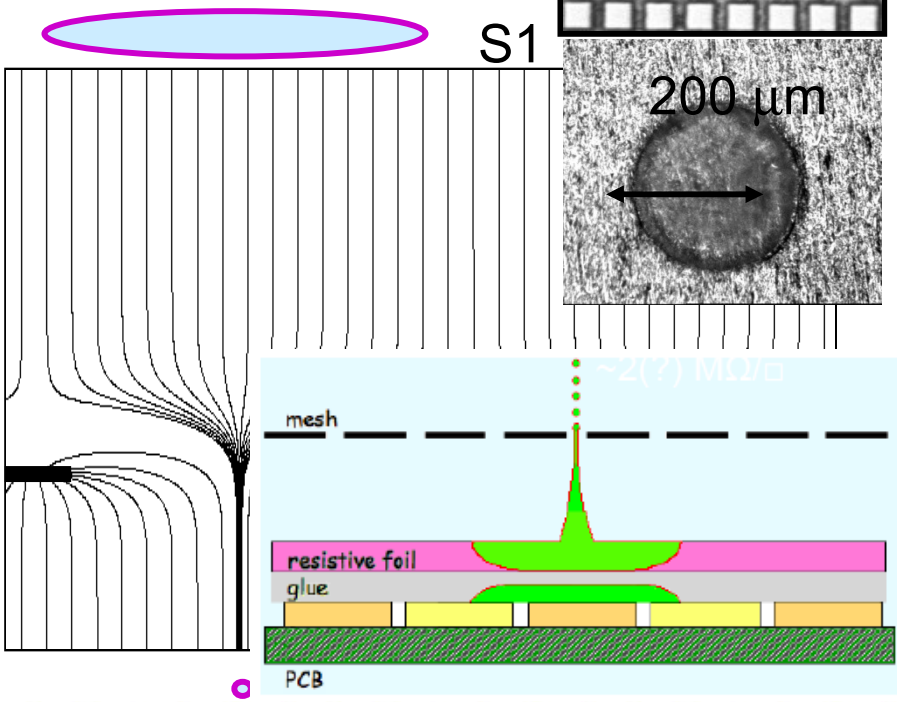

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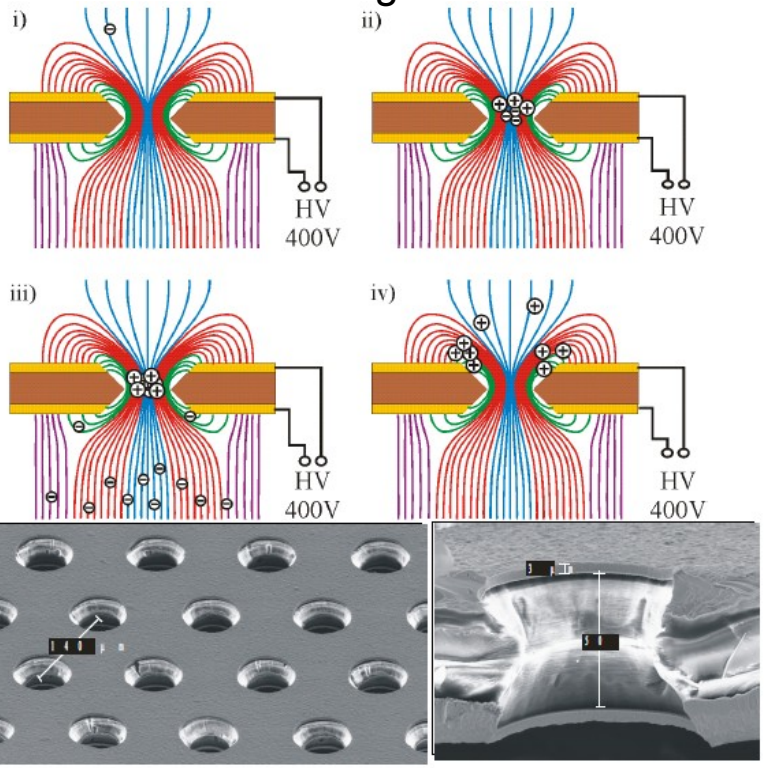

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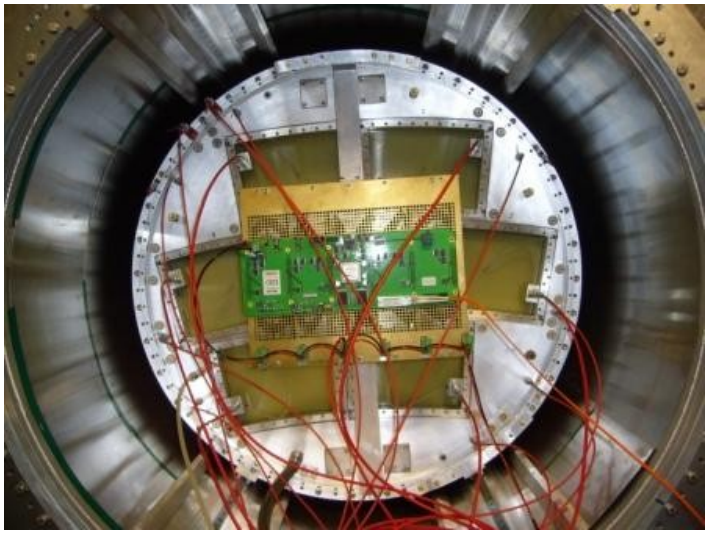
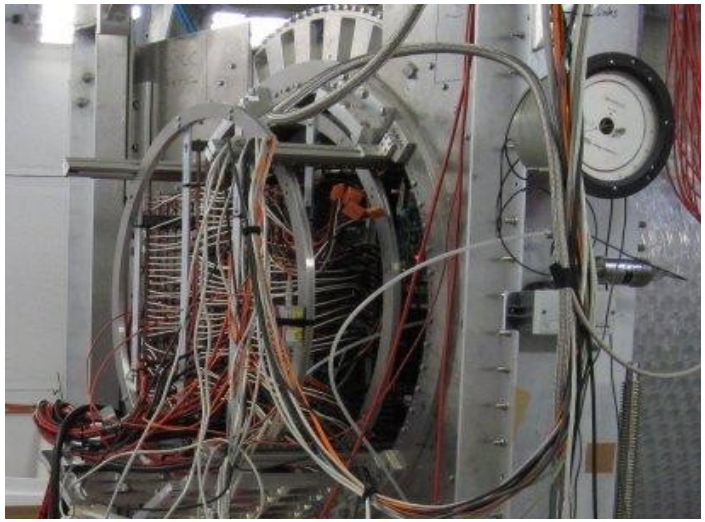


Read out by T2K AFTER-based electronics (Saclay)

GEM



Read out by ALTRO electronics (EUDET, Lund,CERN)

Test beam campaigns from October 2008 to September 2010 with several Micromegas and GEM modules

Perfomance Goals

Double-JGEM modules (100μm thick)

- **28 pad-rows, 176 -194 pads (pad size ~ 1.1 x 5.4 mm²)**
- **Total 5152 pads/module**
- **3 modules partially equipped (7616 channels)**

Micromegas modules

- **24 pad-rows, 72 pads (pad size [2.7-3.2] x 7 mm²)**
- **Total 1728 pads/module**
- **Different resistive layers**
- **1 (2) module(s) (partially) equipped**

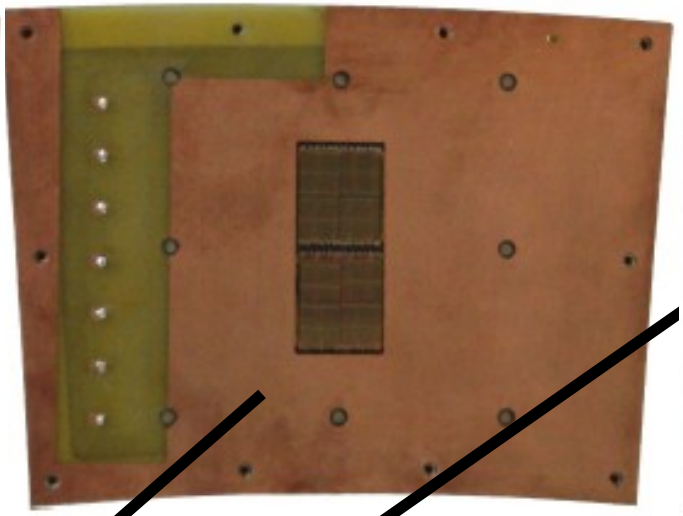
Perfomance Goals

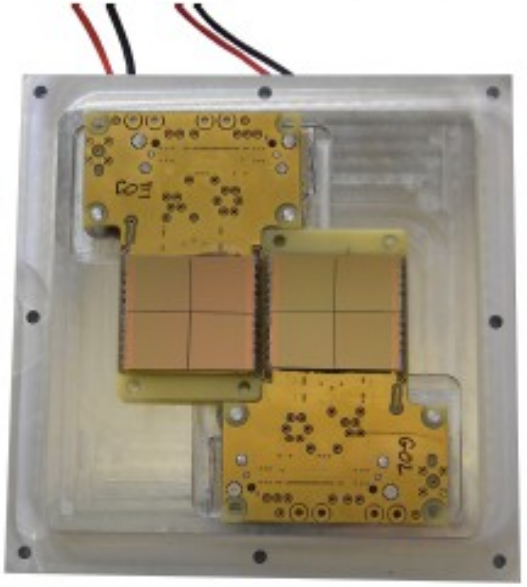
Measured quantities:

- **Drift velocity**
- **Pad response**
- **Track point resolution**
- **N_{eff}**
- **$1/p_T$ resolution**
- **MarlinTPC used as reconstruction and analysis software**
- **See talks by Ryo Yonanime and Wen Wenxin**

Both techniques show similar performance.
Track point resolution extrapolated → results as required or better for ILD-TPC

TimePix and T-GEM Module





anode plane

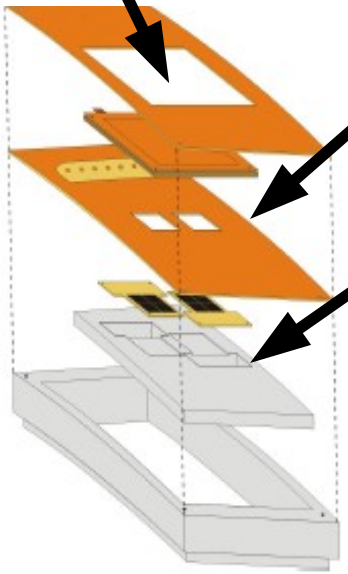
GEMs

readout plane

quad-boards

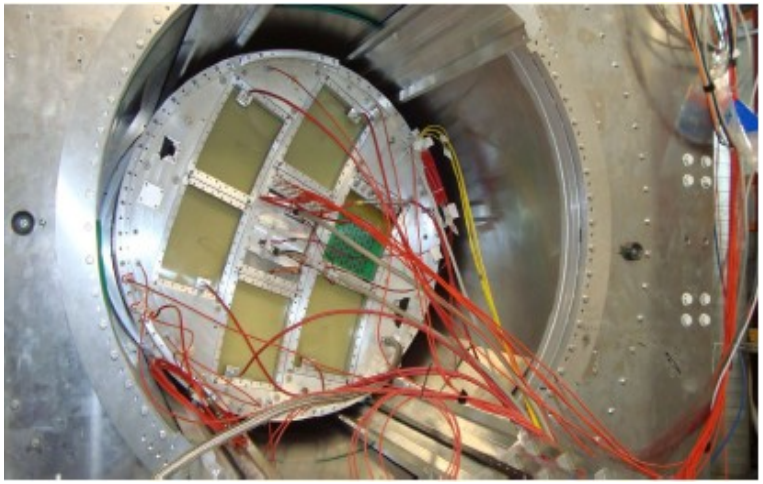
reinforcement of anode plane

redframe



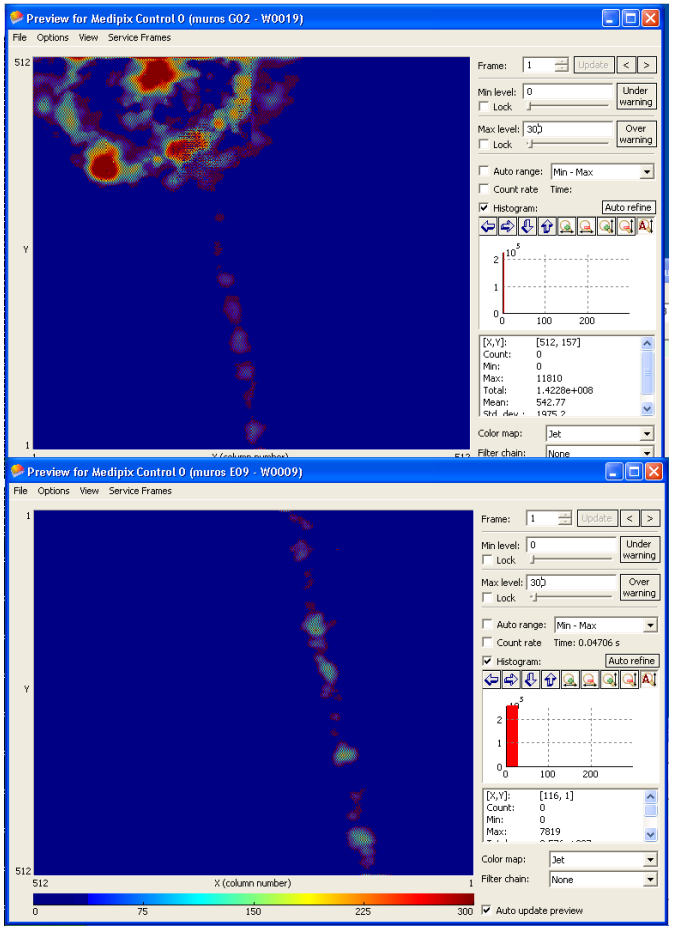
Readout:
2 quadboards
(4 TimePix
Chips each)

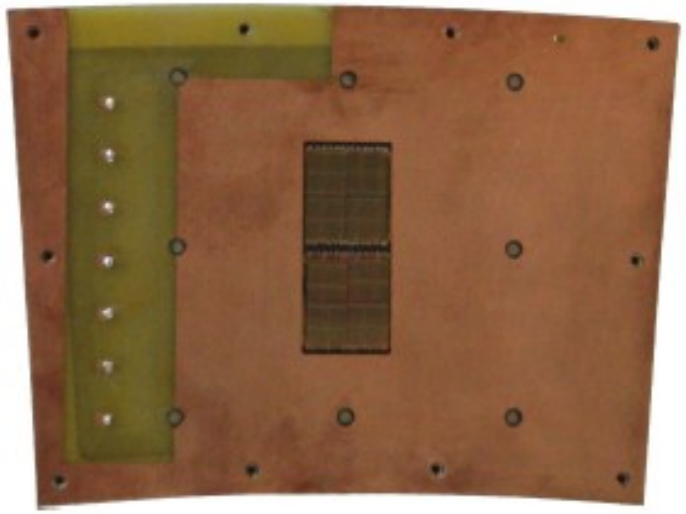
J. Kaminski, Univ. of Bonn

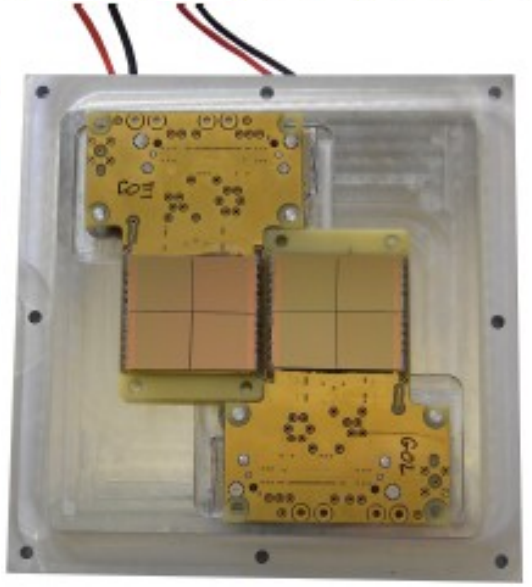


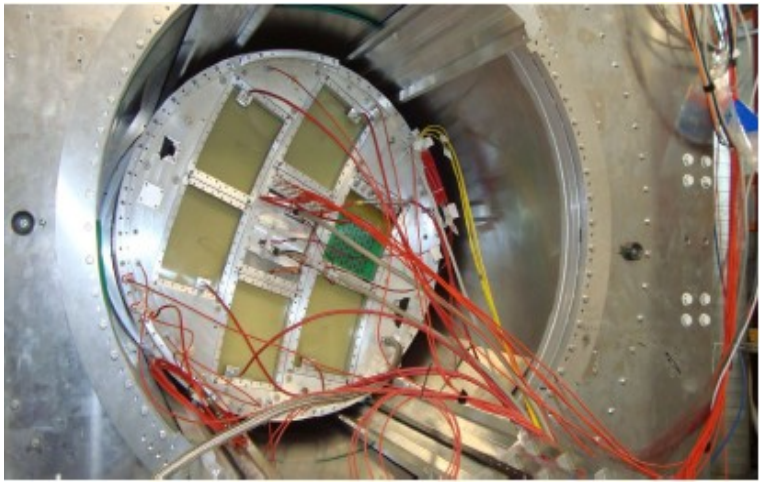
TimePix and T-GEM Module

See Xavier Llopart Cudie's talk



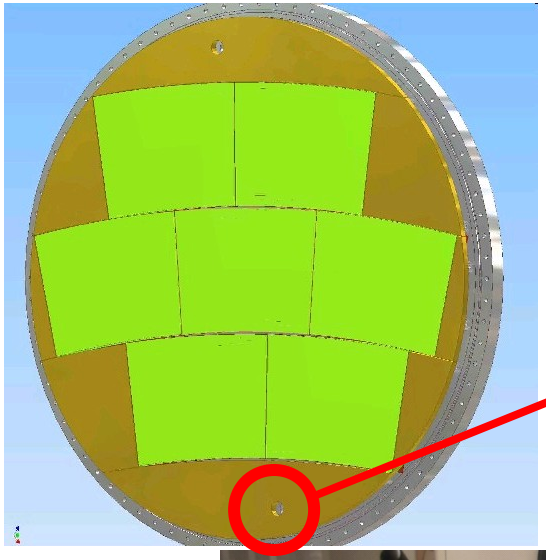


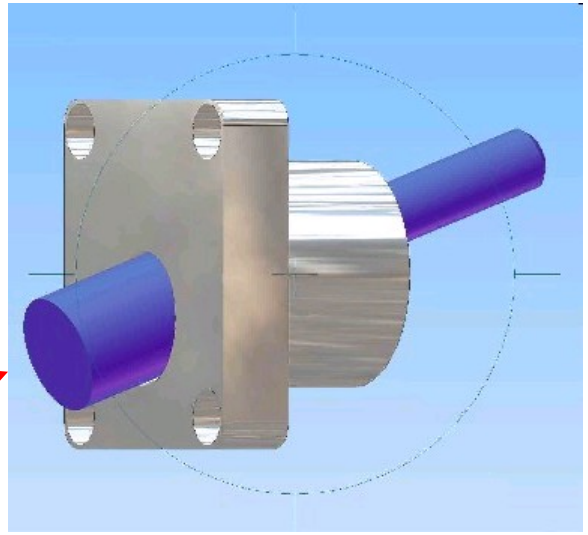


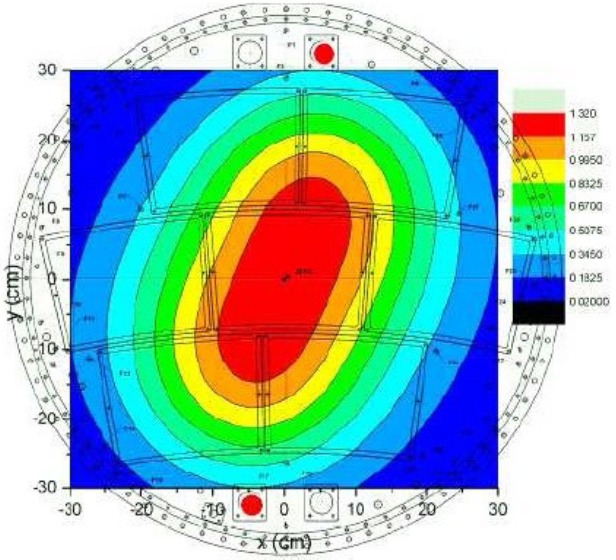


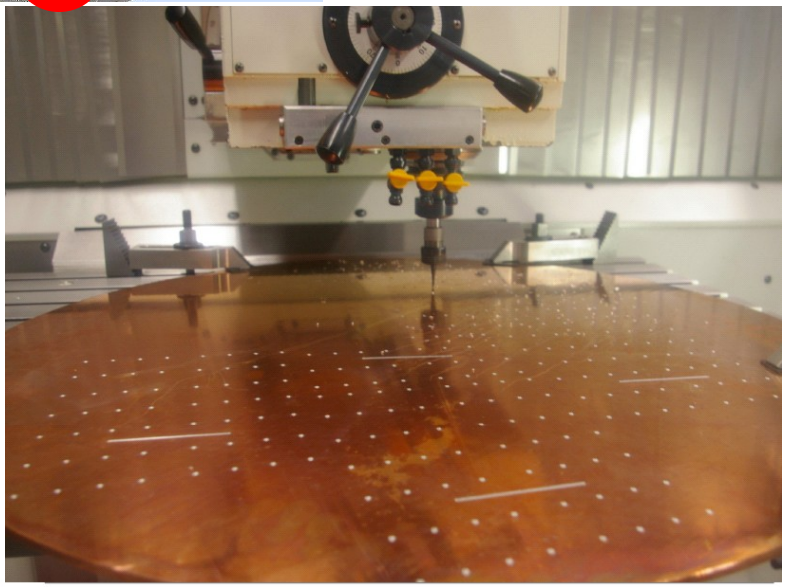
J. Kaminski, Univ. of Bonn

Laser Calibration Setup

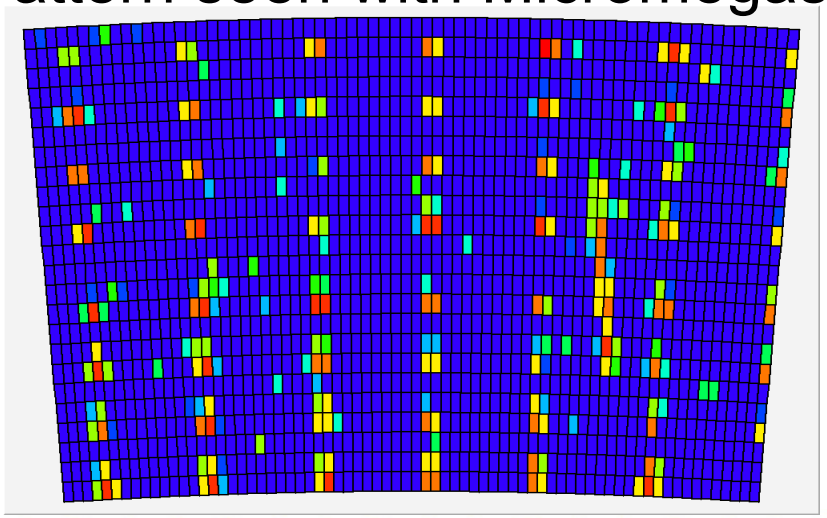








Pattern seen with Micromegas



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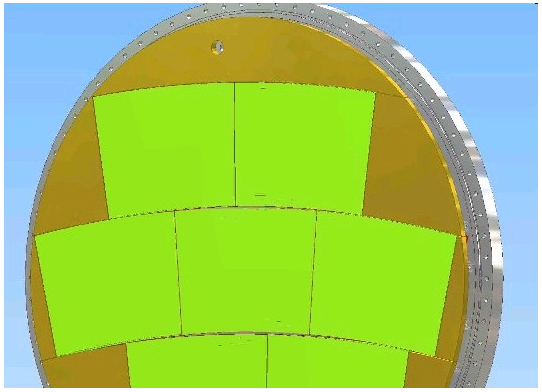

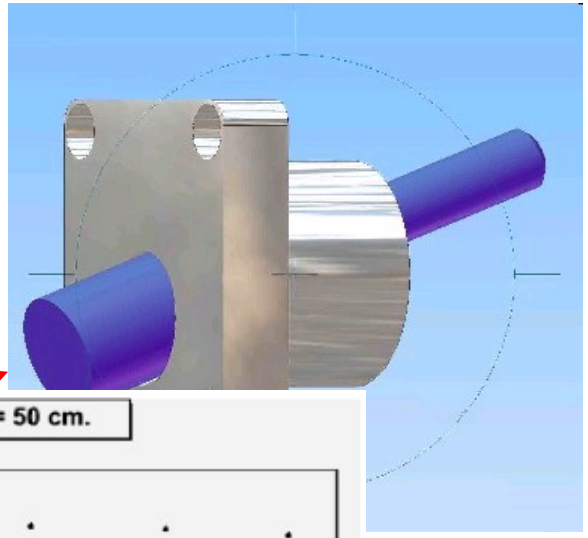

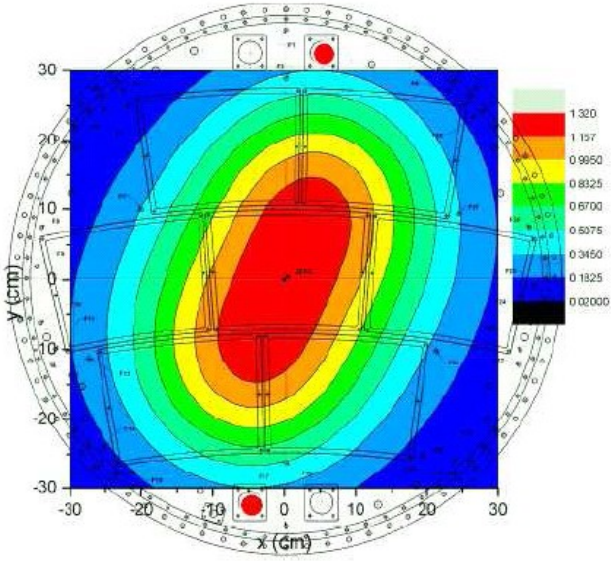

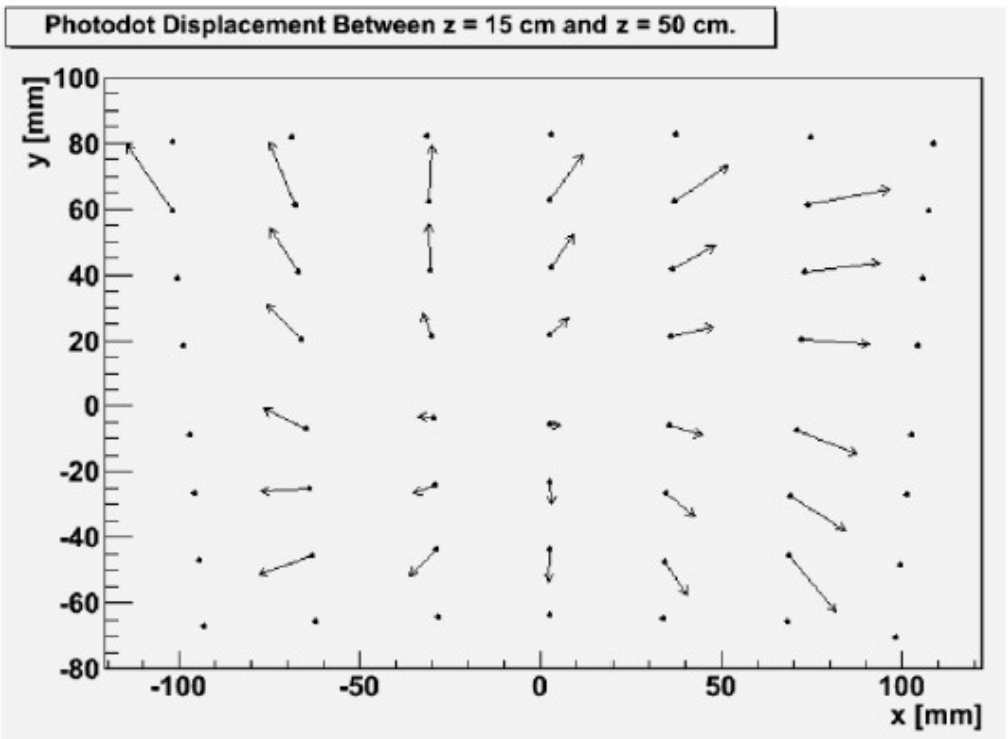

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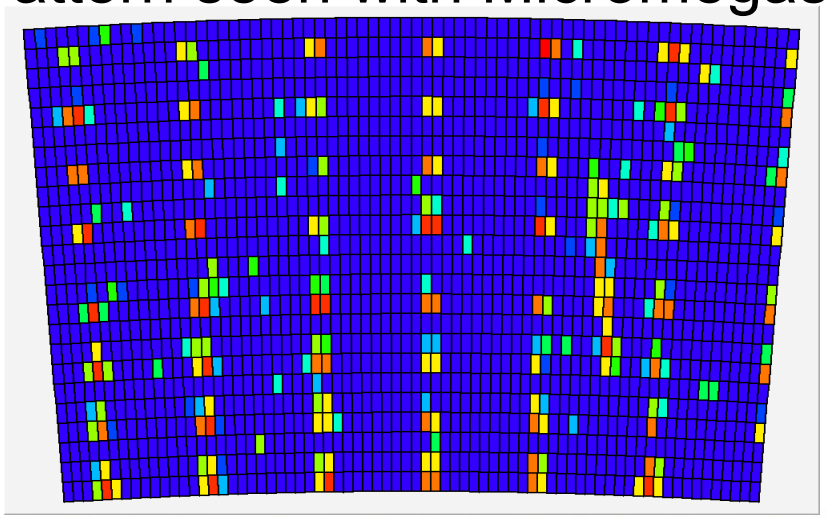
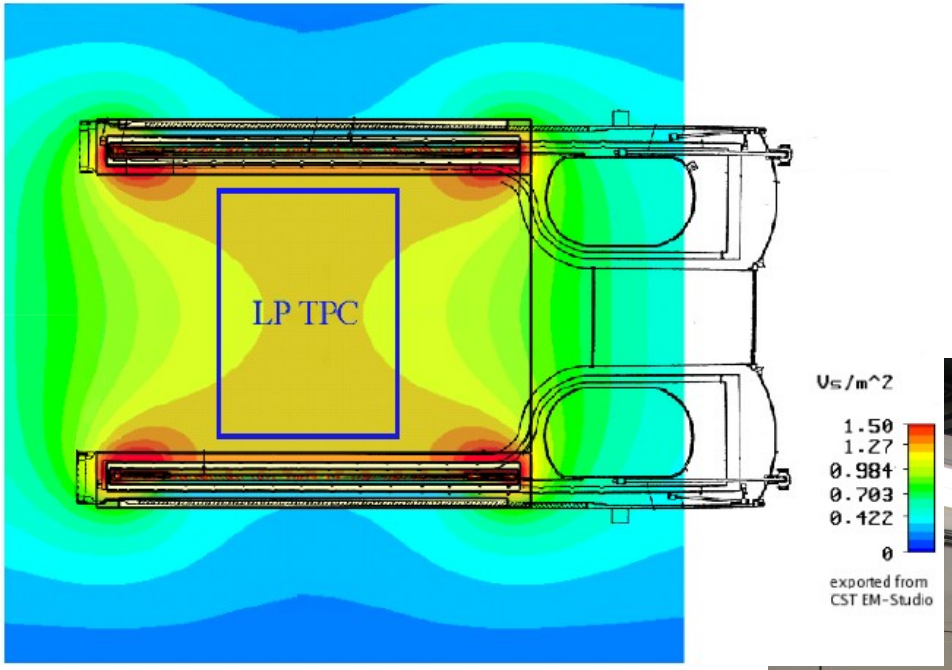
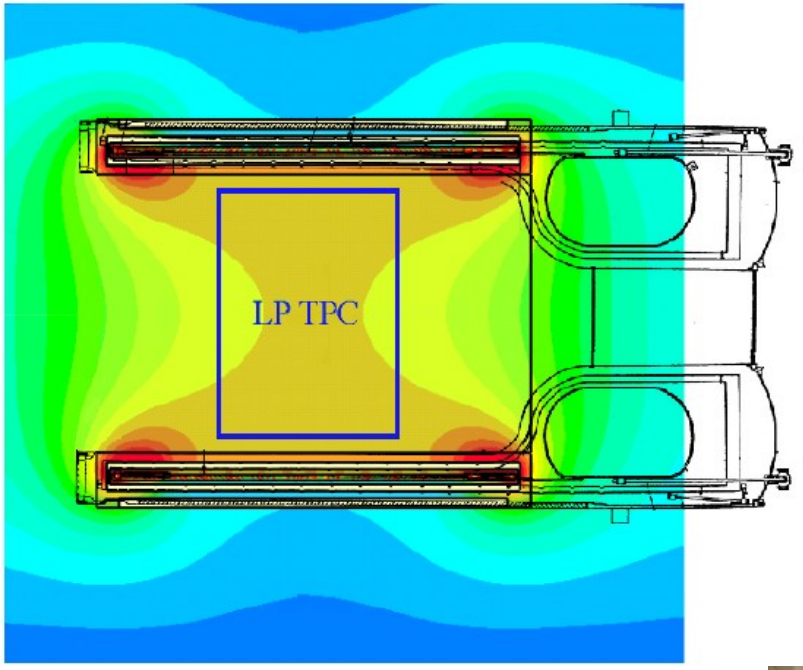


Persistent Current Magnet PCMAG



Then.

Persistent Current Magnet PCMAG



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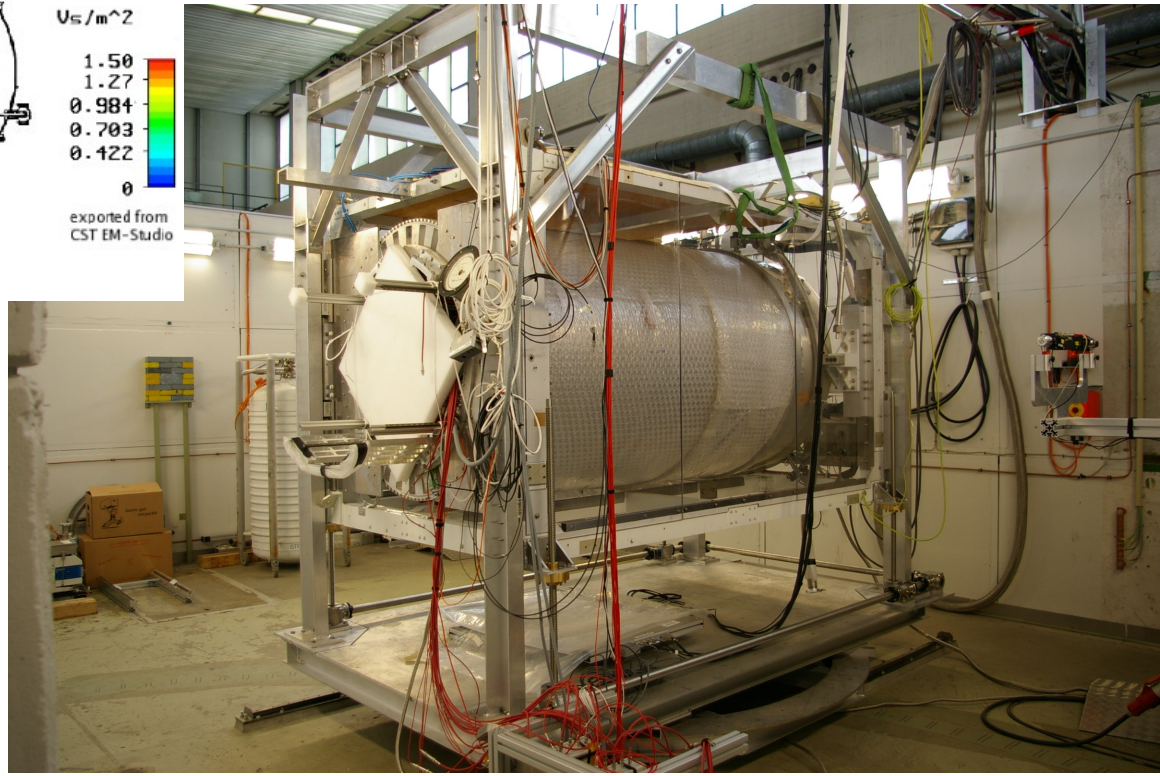
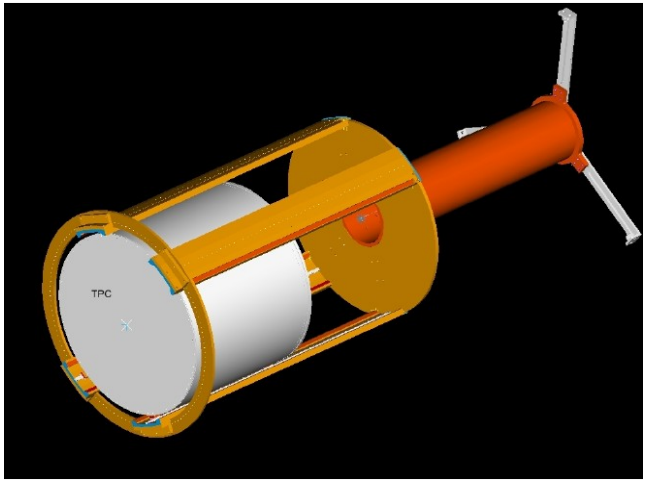
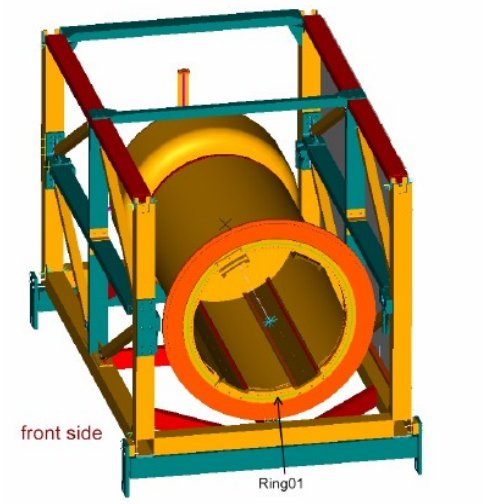
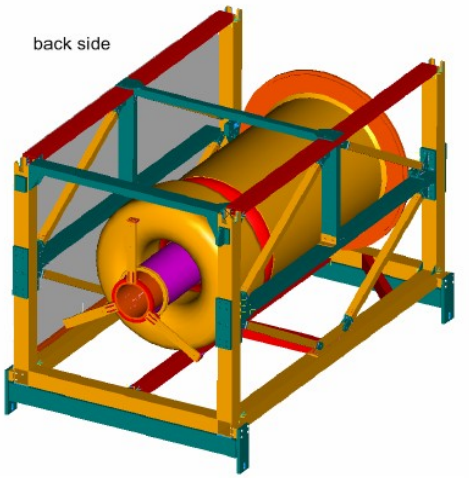


LP Mechanics

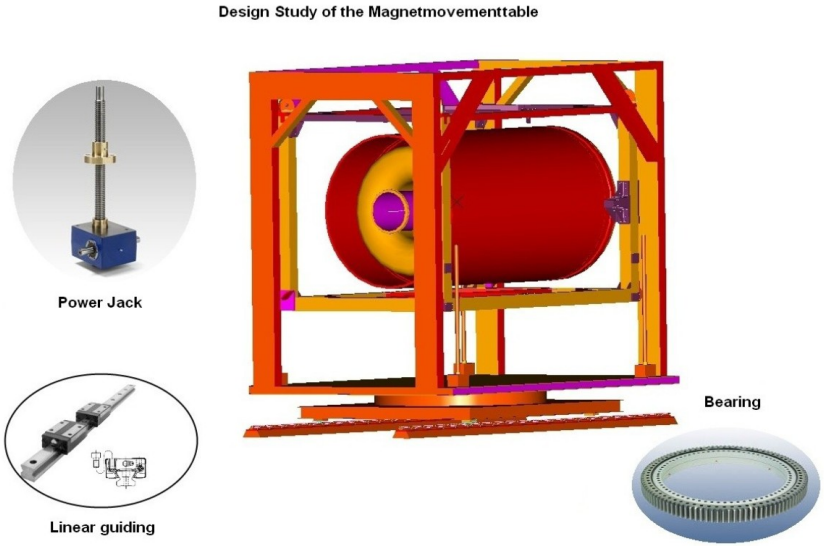






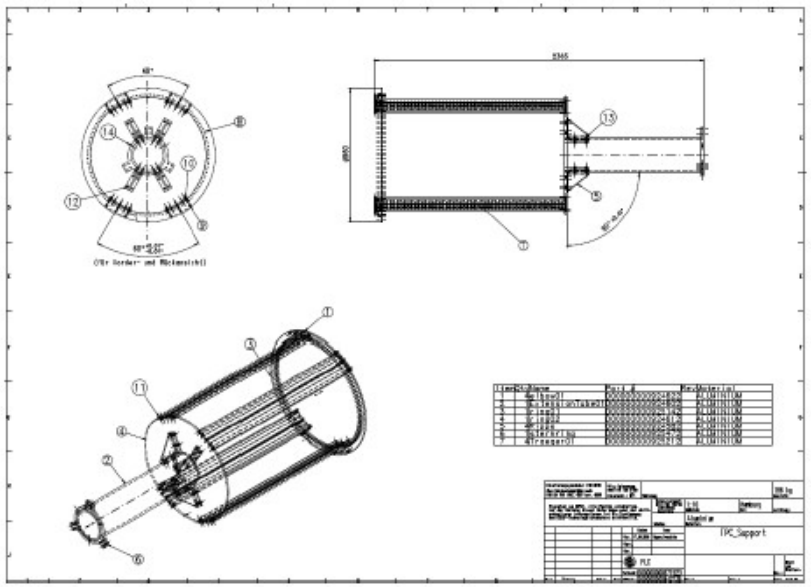
Support structures:

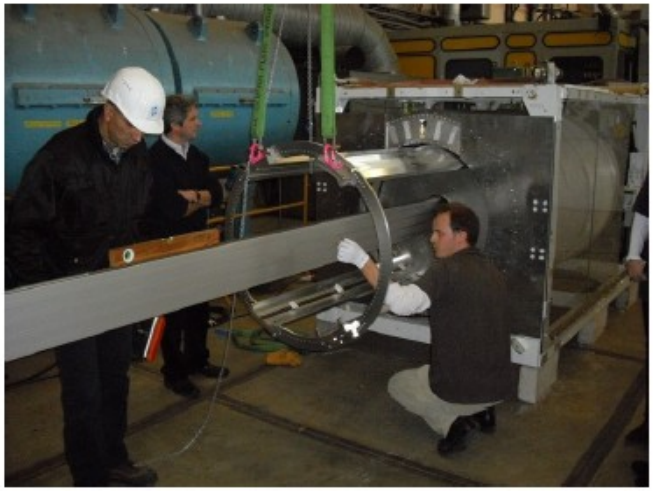
- TPC
- PCMAG

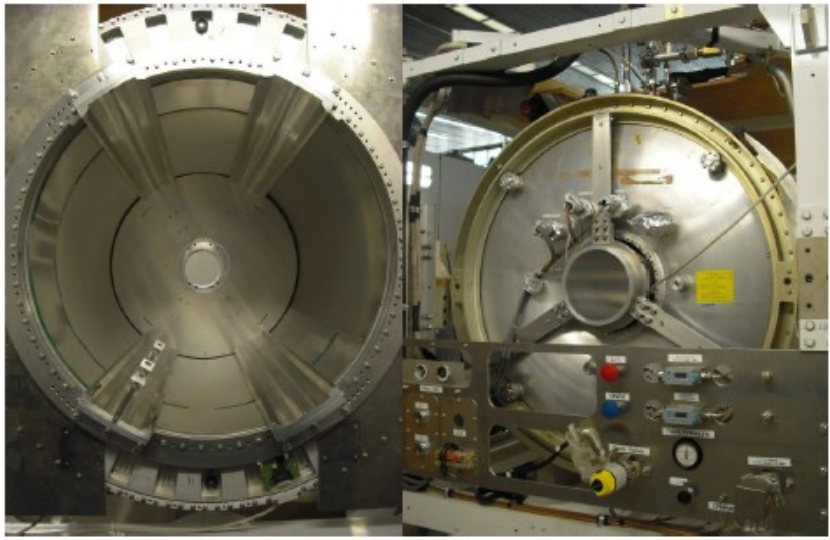


F. Hegner, V. Prahl, R. Volkenborn, DESY

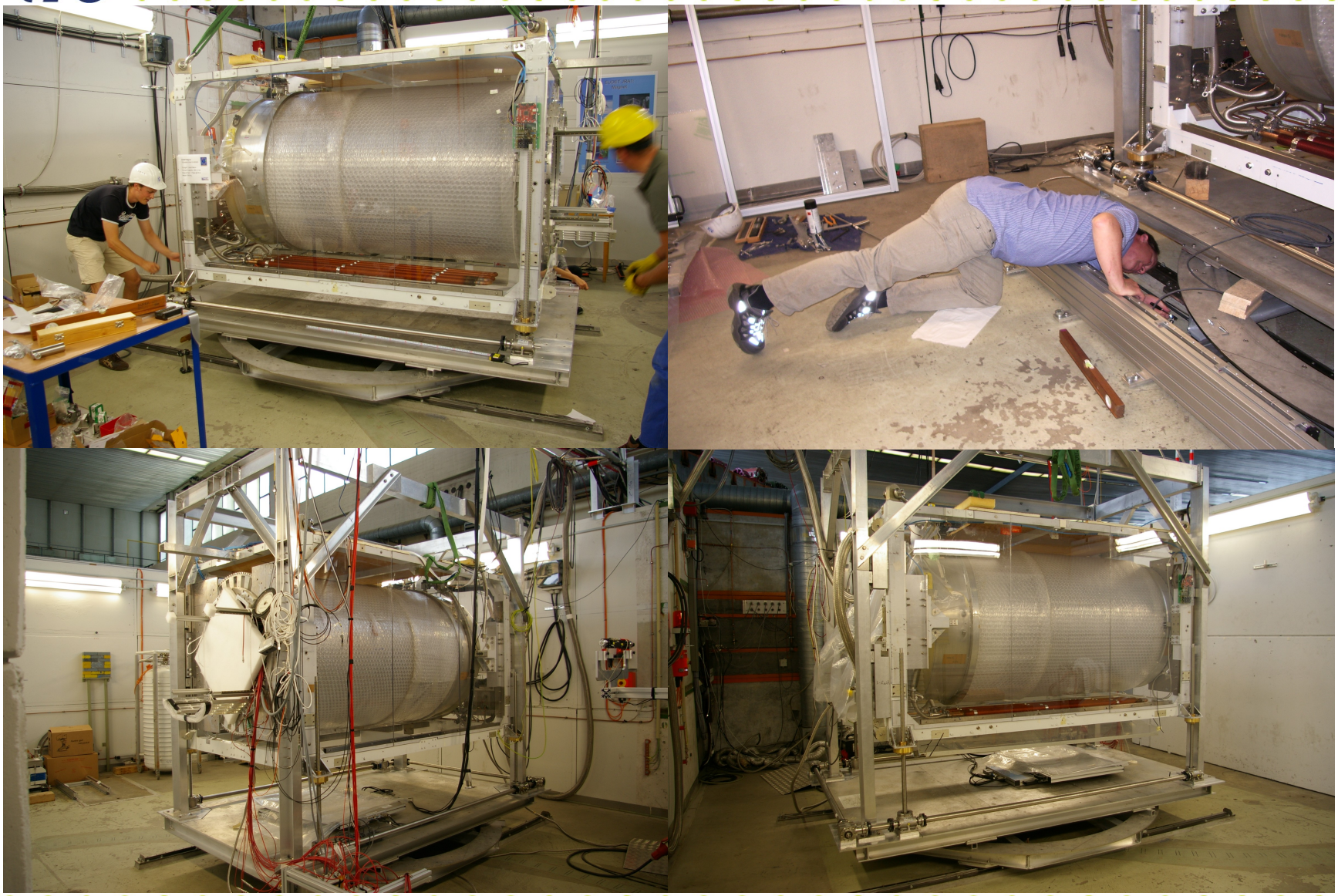
Support for the LP



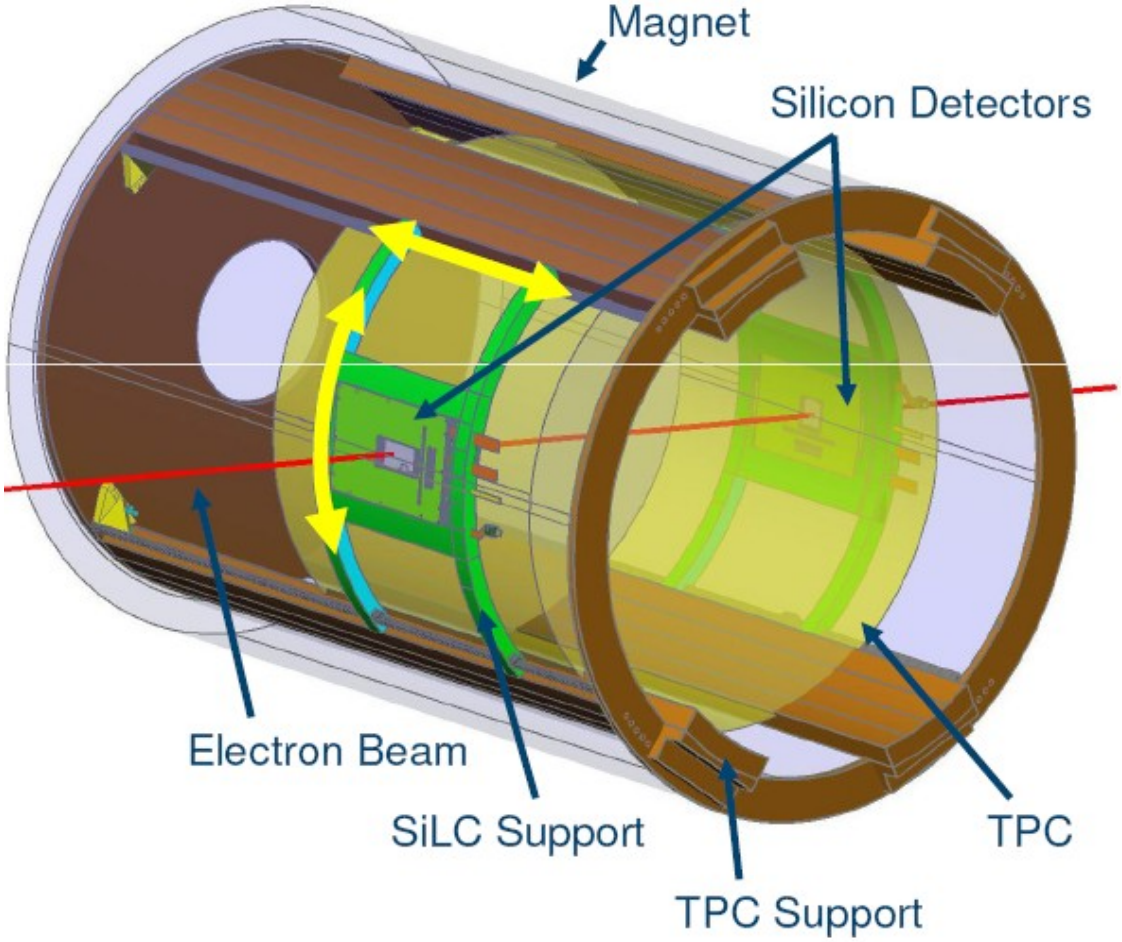


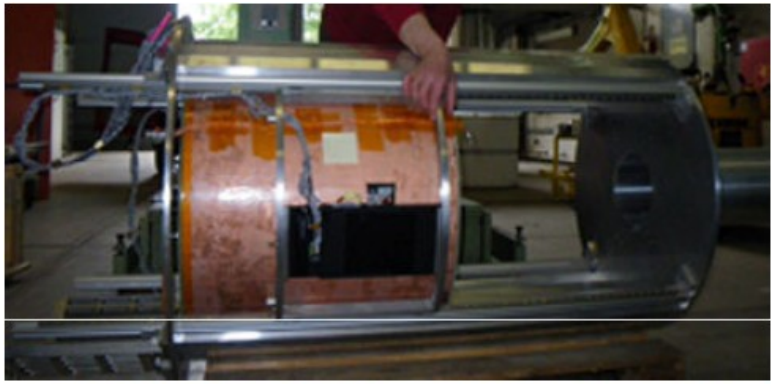


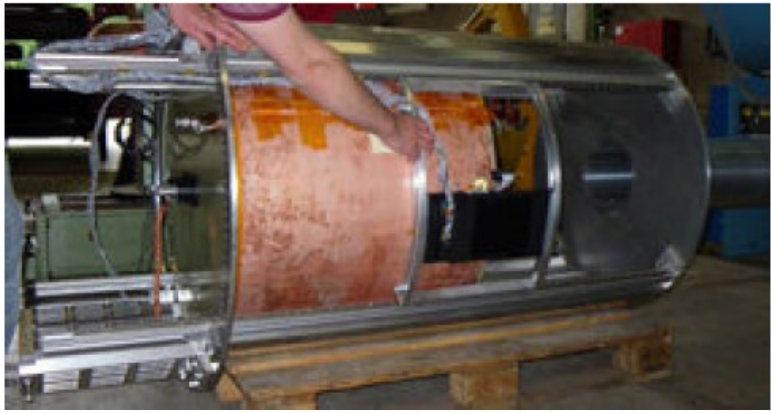
LP Mechanics



Si Envelope

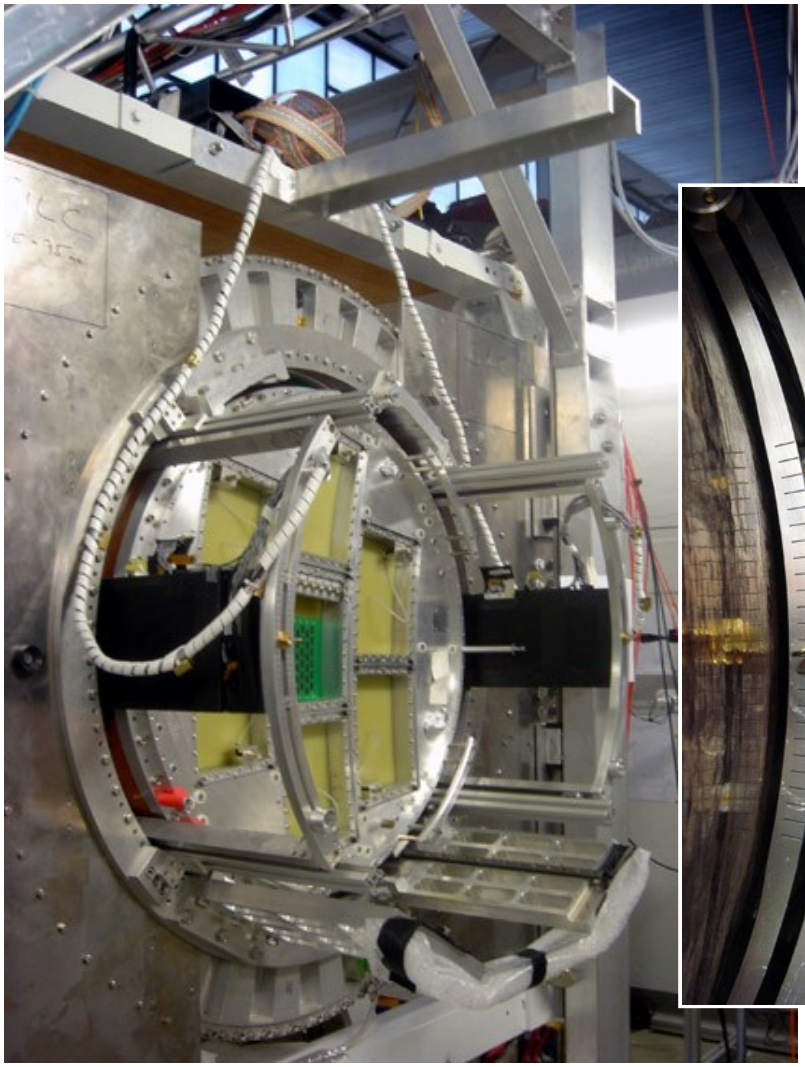




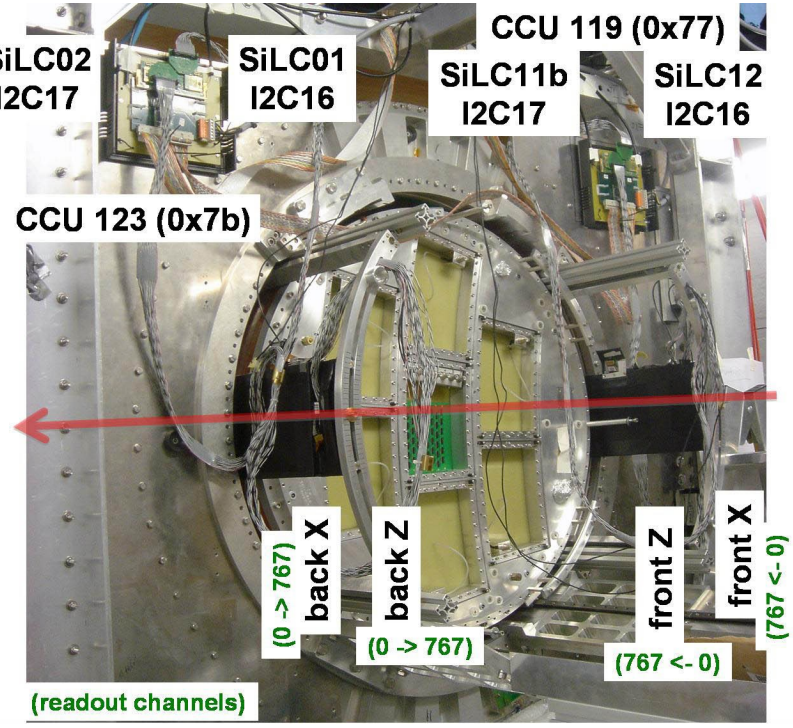


S. Haensel
HEPHY Vienna

Si Envelope



Combined test beam campaign with two Micromegas modules in Nov. 2009



S. Haensel
HEPHY Vienna

Readout Electronics: S-ALTRO

Goal :

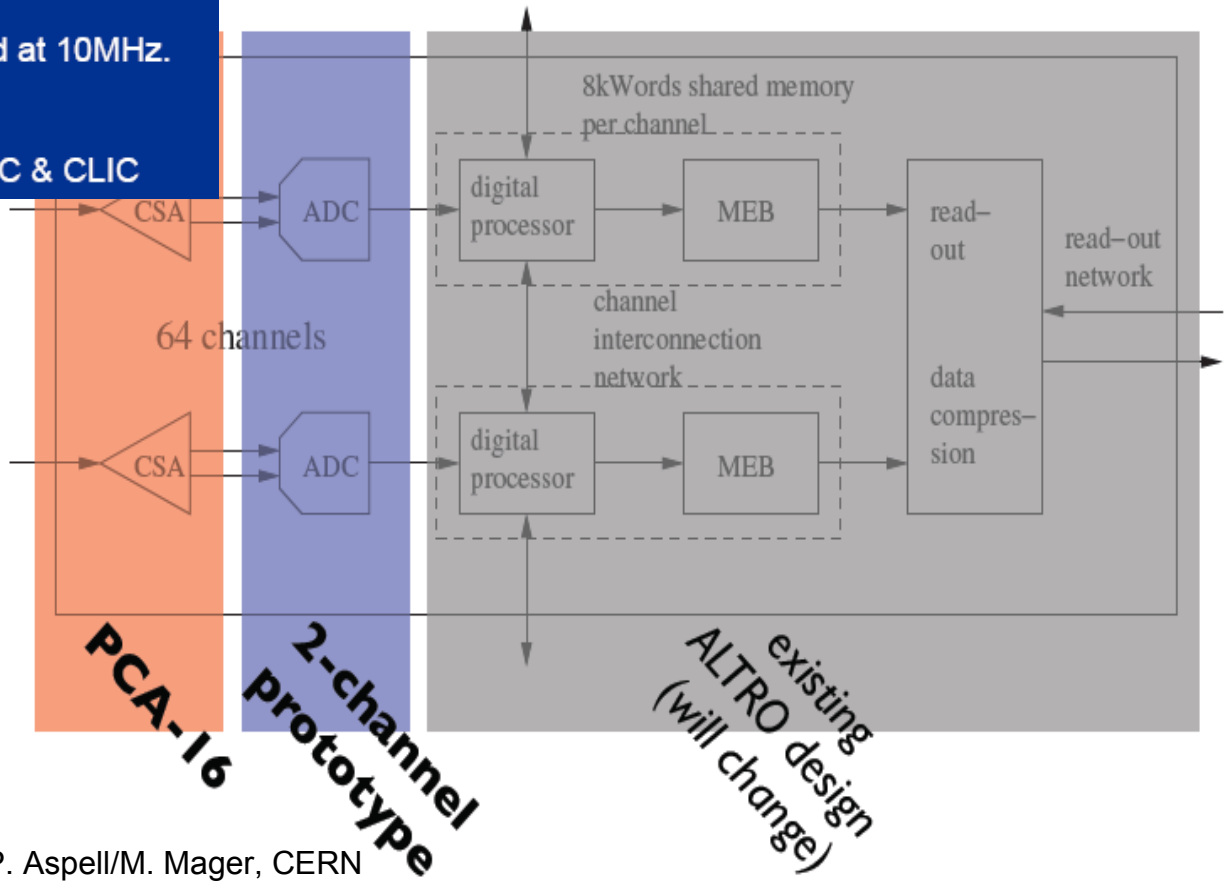
To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

See Paul Aspell's talk

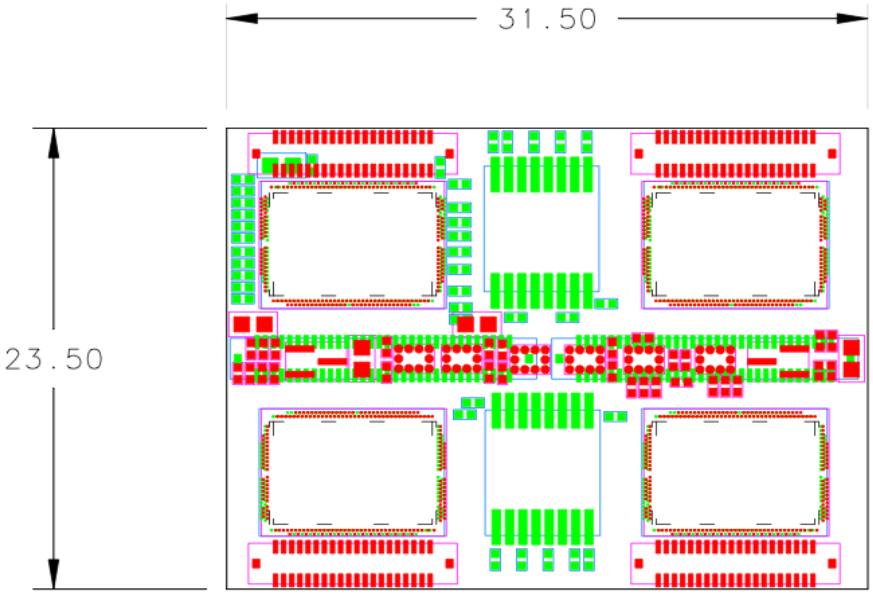
Current Design



P. Aspell/M. Mager, CERN

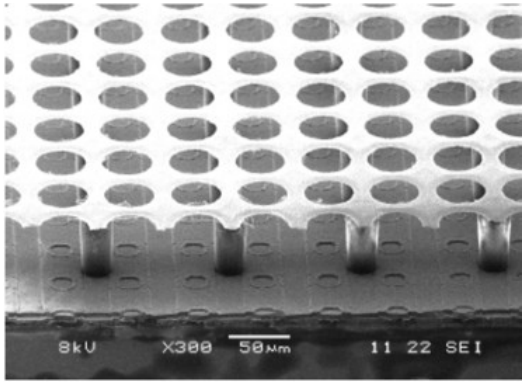
Readout Electronics: S-ALTRO

- Full chain new S-ALTRO16 chip prototype submitted
- Will be mounted on Multi-Channel Modules
- Towards new chip 64 channels
- CO_2 Cooling and power pulsing foreseen (to be tested in a 5T magnet)



The final electronics (could be S-ALTRO 64) will be usable for both GEM and Micromegas

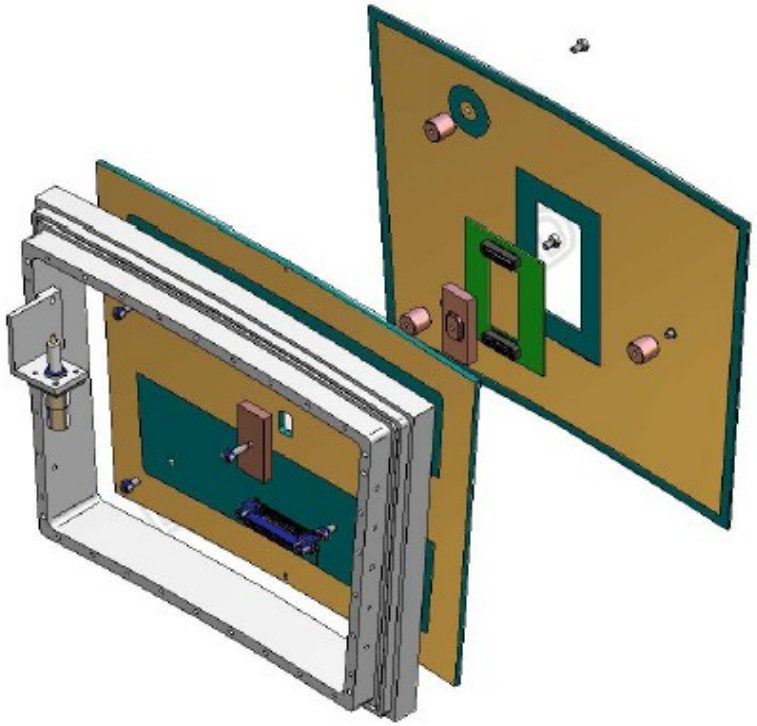
GridPix Octopuce

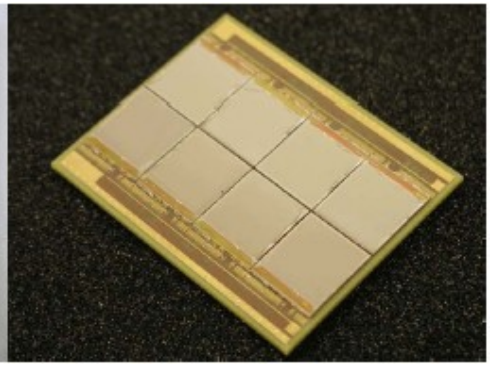


Eight-chip matrix prototype with integrated Micromegas -InGrid-

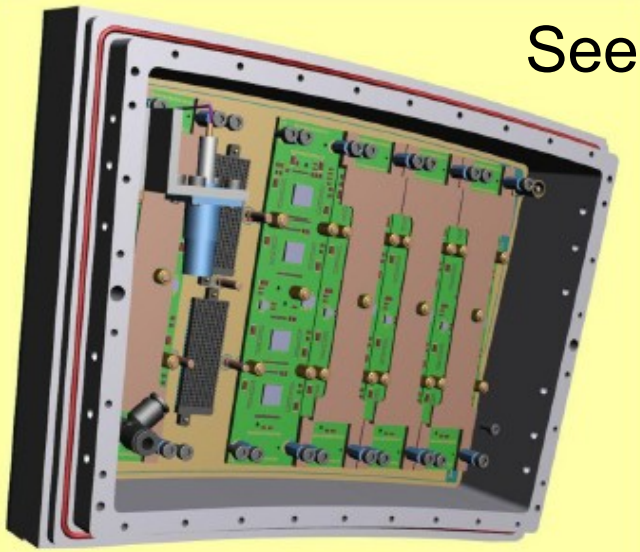
TimePix chip : 65 000 digital pixels (55 x 55 μm^2) with time and TOT measurement

Single electron capability



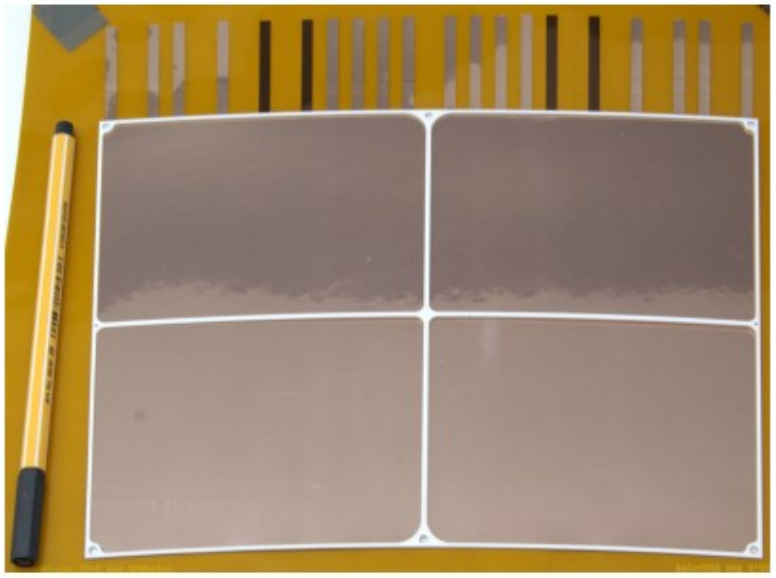


Pad Readout Modules



See Paul Colas' talk

Grid GEM module with self-supporting structure



Seven Micromegas backplane integrated electronics (AFTER) modules

Summary & Outlook

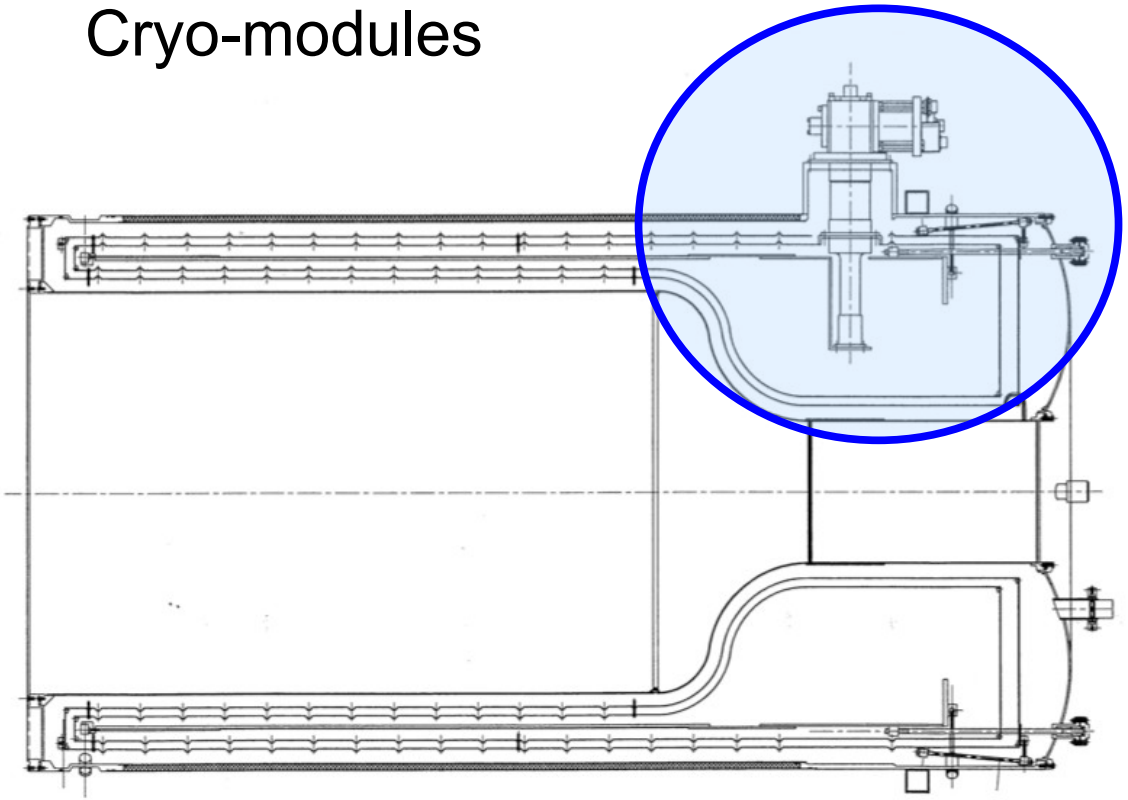
- Infrastructure for LP present and being used
- LP assembled, commissioned and being tested
- LP with three different amplification technologies operated
- Infrastructure for SiLC envelope installed
- First combined TPC-SET run performed
- ~24 weeks of test beam with LP operation so far
- >10M events recorded → ~2TB data on GRID
- → more to come

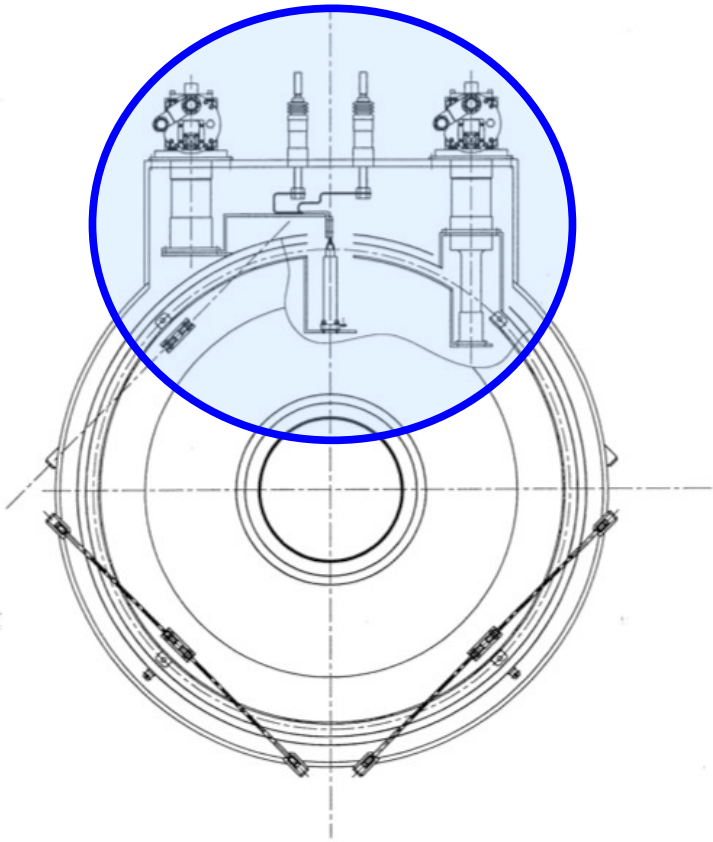
Summary & Outlook

- Items to be completed:
  - Alignment system for LP within PCMAG to be tested/installed
  - DESY GEM module
- Further test beam campaigns (for the rest) of 2010 and beyond
  - DESY-GEM module with ALTRO electronics (end 2010?)
  - Seven Micromegas modules with integrated AFTER electronics (2012)
- PCMAG modifications in 2011

PCMAG Modification

Cryo-modules





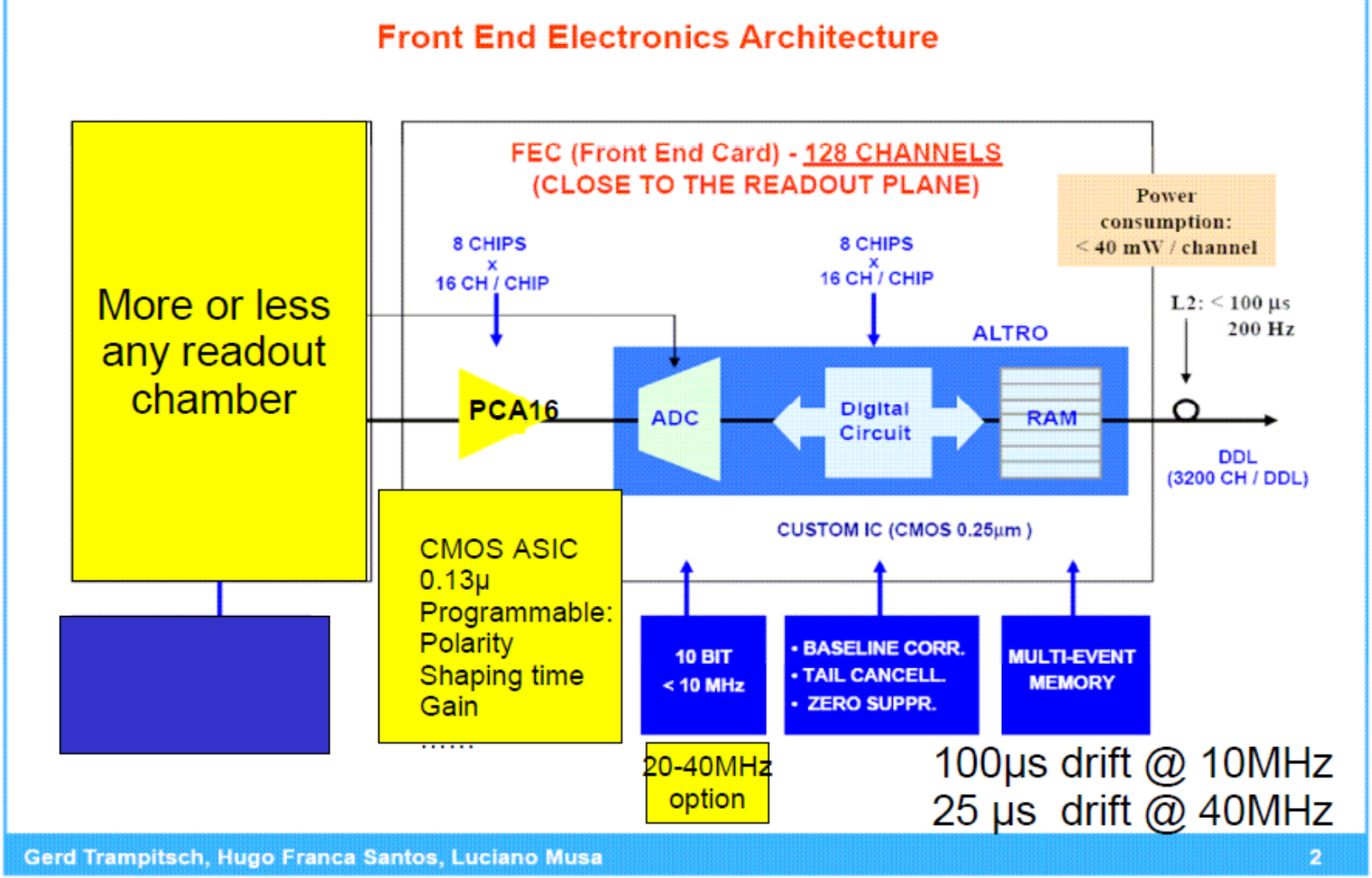
Modification planned for 2011 → ~6 months duration, after “finishing” beam tests

Summary & Outlook

- Items to be completed:
  - Alignment system for LP within PCMAG to be tested/installed
  - DESY GEM module
- Further test beam campaigns (for the rest) of 2010 and beyond
  - DESY-GEM module with ALTRO electronics (end 2010?)
  - Seven Micromegas modules with integrated AFTER electronics (2012)
- PCMAG modifications in 2011
- S-ALTRO16 to be prototyped
- See T. Matsuda's talk

ALTRO Electronics

EUDET readout FEC



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Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

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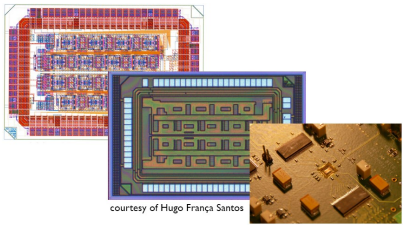
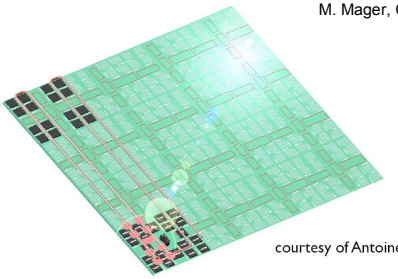


ADC prototype

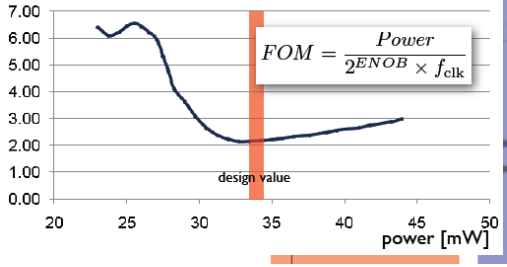
Single ADC area: 1.57 X 0.45 = 0.7 mm²

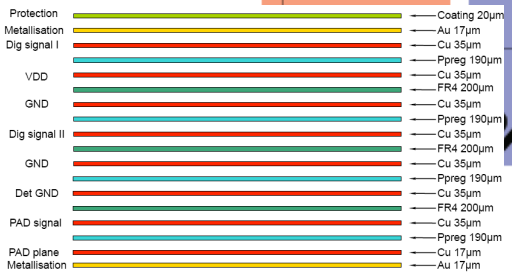
Prototype area: 2.35 X 1.6 = 3.76 mm²

M. Mager, CERN



courtesy of Antoine Junique





P. Aspell/M. Mager, CERN

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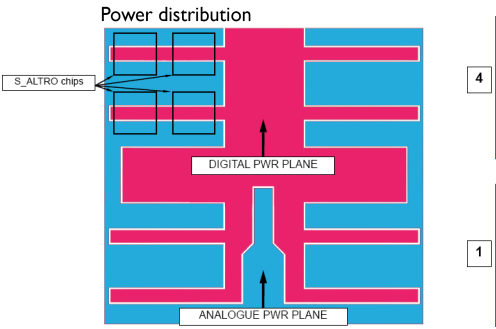
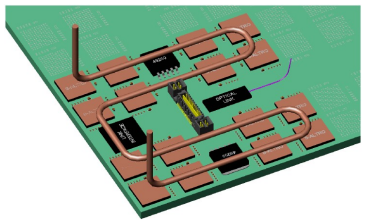
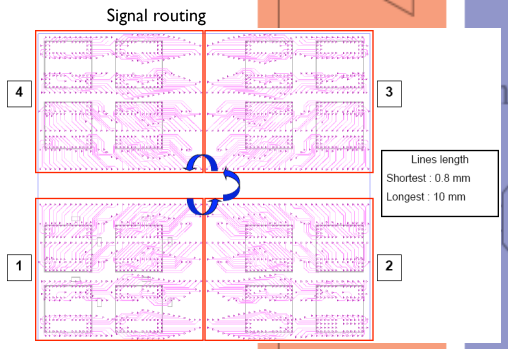
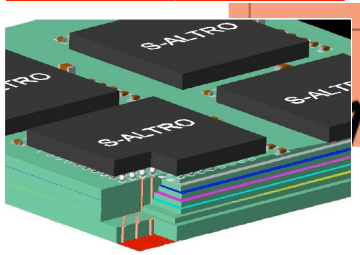


M. Mager, CERN







P. Aspell/M. Mager, CERN

Readout Electronics: S-ALTRO

Goals for the S-Altro16 electronics prototype:

The prototype pad modules has to fit into the present endplate

The chip size should be compatible with a realistic pad size. The final goal is to get down to 1x4 mm^2 pad size. The present pad size is about 1x5 mm^2 and the prototype should be compatible with similar size.

Power pulsing should be prototyped.

A solution for efficient cooling has to be found.

A realistic noise level should be achieved.

Experience with the S-Altro16 chip should guarantee a safe final step to the S-Altro64 chip.

L. Joensson, Lund Univ.

Readout Electronics: S-ALTRO

The are obvious disadvantages in mounting all the electronics directly onto the pad module.

Instead a system with Multi Chip Modules is proposed.

It is a fairly conservative approach, reducing the risks.
Cheaper to produce
It has several advantages in the prototyping phase.
It provides realistic prototyping for safely taking the final step to the S-Altro64 chip.
It offers better separation between analogue and digital circuitry and it offers great flexibility in terms of how the electronics components are organized.
The size of the MCM for the S-Altro64 chip is compatible with
1x4 mm^2 pads
It can be easily moved from a system with GEM readout to a system with MicroMegas readout.
Its modular structure allows re-design of the readout chain without affecting the pad board

L. Joensson, Lund Univ.