Design status of the Timepix2 pixel detector chip

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Outline

- The Timepix chip
  - From Mpix2MXR20 to Timepix
  - Pixel schematic
  - Chip architecture
  - Timepix in TOA and TOT
  - Applications
- The Timepix2
  - Limitations of the Timepix chip
  - Scope & Main Requirements
  - A new pixel floorplan
  - Data push architecture
- Conclusions

From Mpix2MXR20 to Timepix

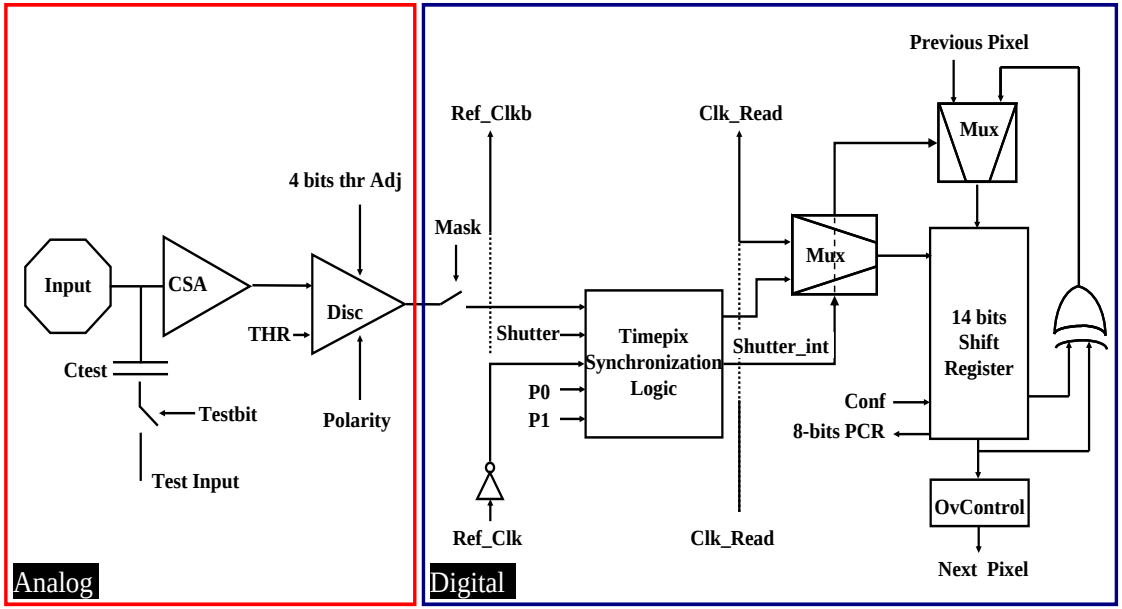
- Design requested and funded by EUDet Collaboration (http://www.eudet.org)

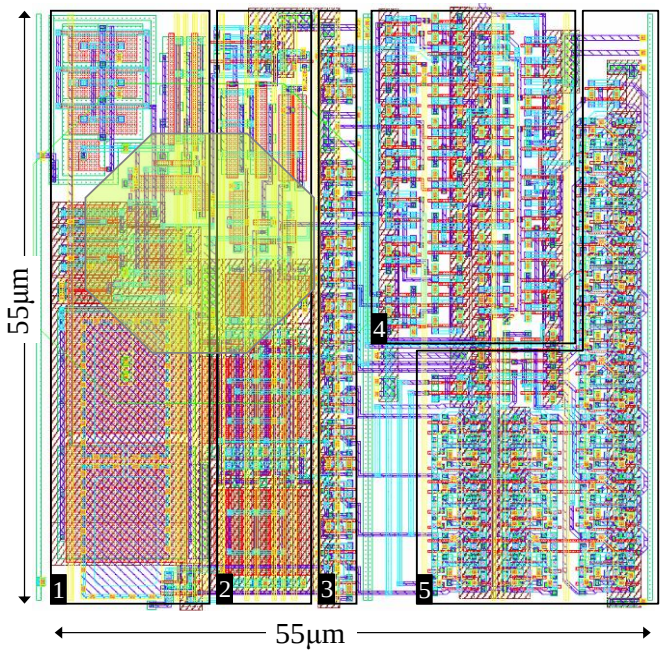
- Main features requested:
  - Change counter function from particle counting to arrival time measurement (clock tick counting) to provided depth dimension in gas detectors
  - Keep Timepix as similar as possible to Medipix2 series in order to benefit from large prior effort in R/O hardware and software

- Features provided:
  - Each pixel is programmable for either of:
    - Particle counting
    - Arrival time with a resolution up to 10ns
    - Time over Threshold

Timepix pixel schematic

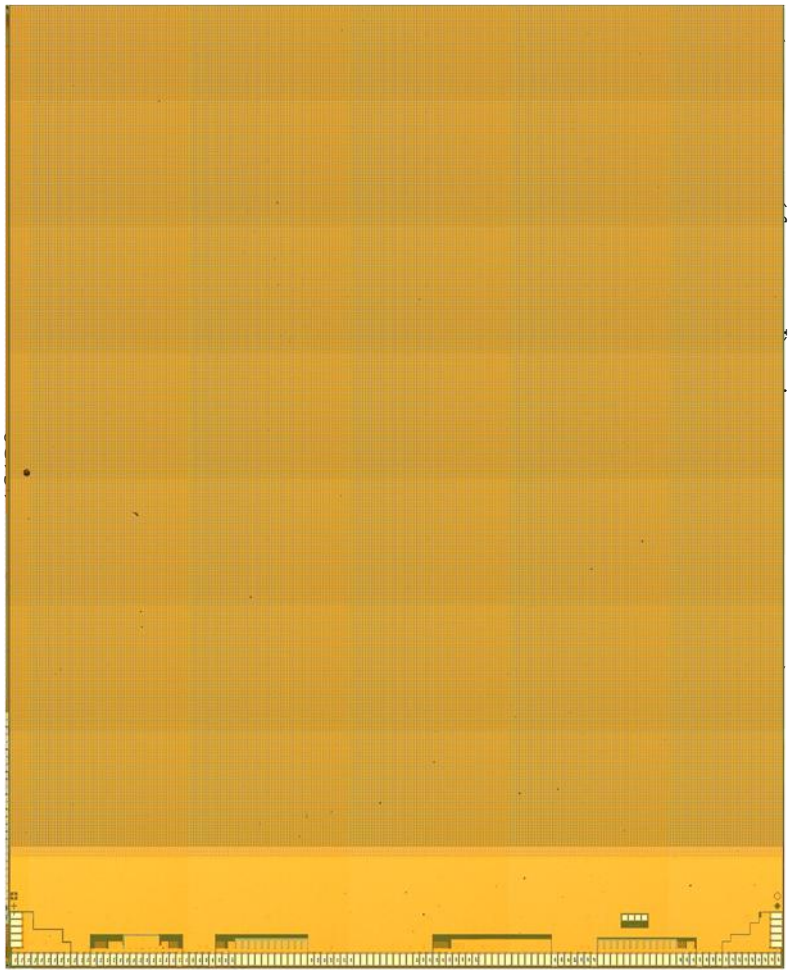
- Improved CSA gain by adding a cascode in the OTA
- There is a single threshold with one 4-bit threshold adjustment DAC.
- Each pixel can be configured independently in three different operation modes:
  - Arrival time mode
  - Energy mode (TOT)
  - Event counting
- In acquisition mode there is a counting clock (*Ref_Clk*) distributed to the entire pixel matrix which is synchronised with the discriminator output (*HIT*)



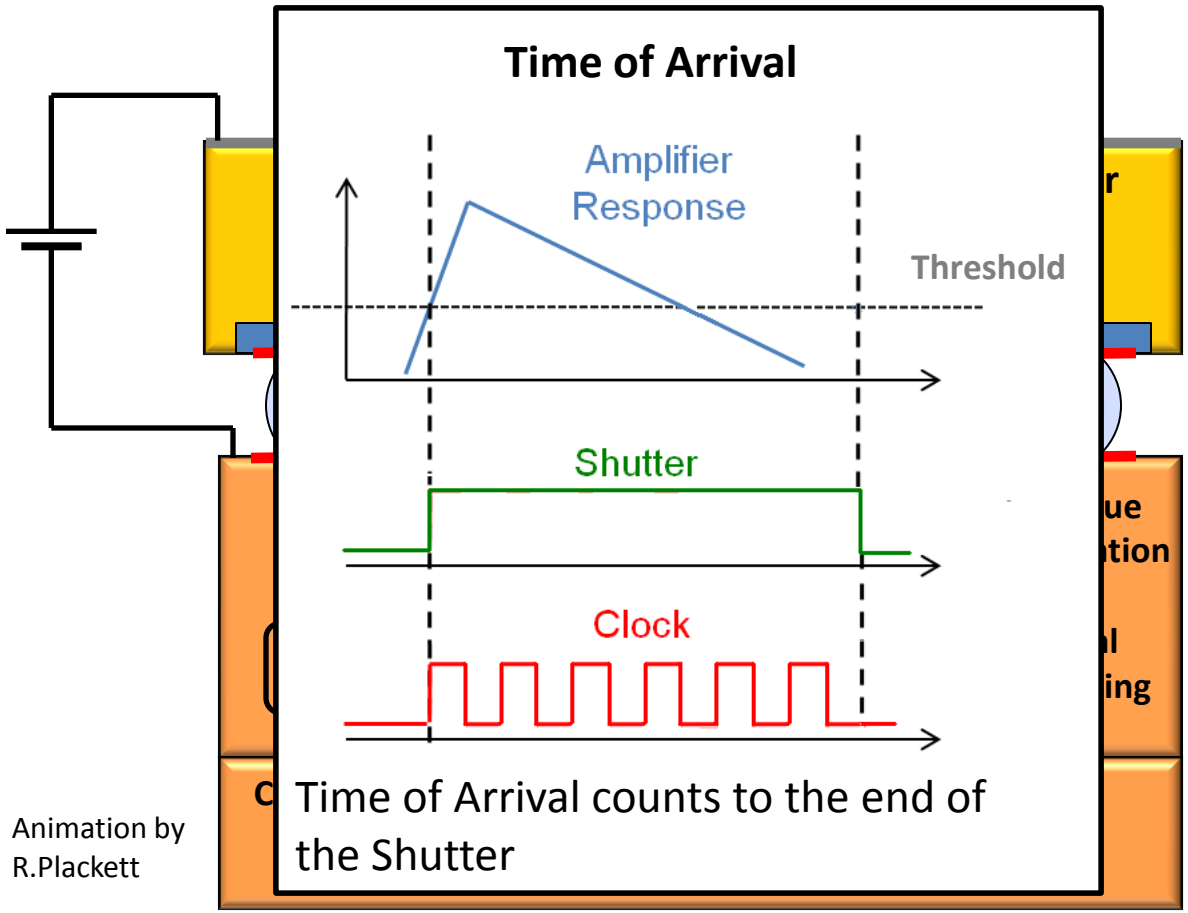


Timepix chip architecture

- Frame based readout architecture:
  - Shutter precision of <5ns
  - Serial readout (@100MHz) → 9.17 ms
  - Parallel readout (@100MHz) → 287 µs
- In acquisition (Shutter On) an external clock is used:
  - As a time reference (up to 10ns)
  - As a energy counter
  - Digital Power (Ref_Clk=50MHz) → 220mW
- 256x256 55µm square pixels
- Static Analog Power → 440mW
- > 36M Transistors



Timepix (2006)



Animation by R.Plackett

Timepix design requestedand funded by EUDET collaboration

Conventional Medipix2 counting mode remains.

Addition of a clock up to 100MHz allows two new modes.

Time over Threshold

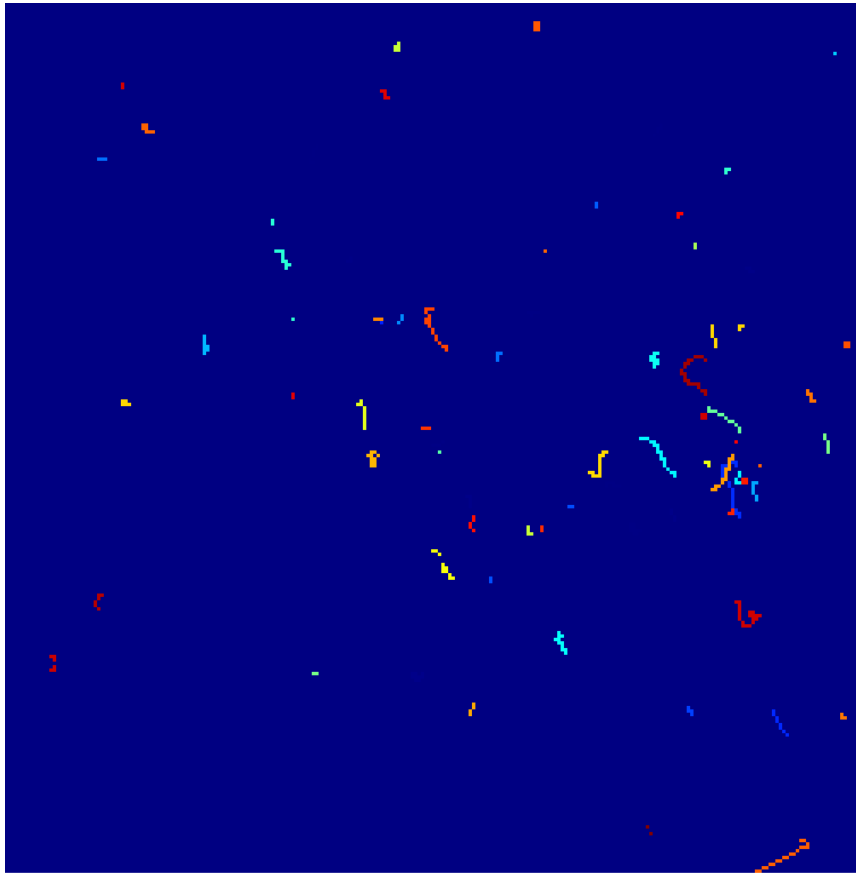
Time of Arrival

Pixels can be individually programmed into one of these three modes

Timepix in TOA and TOT

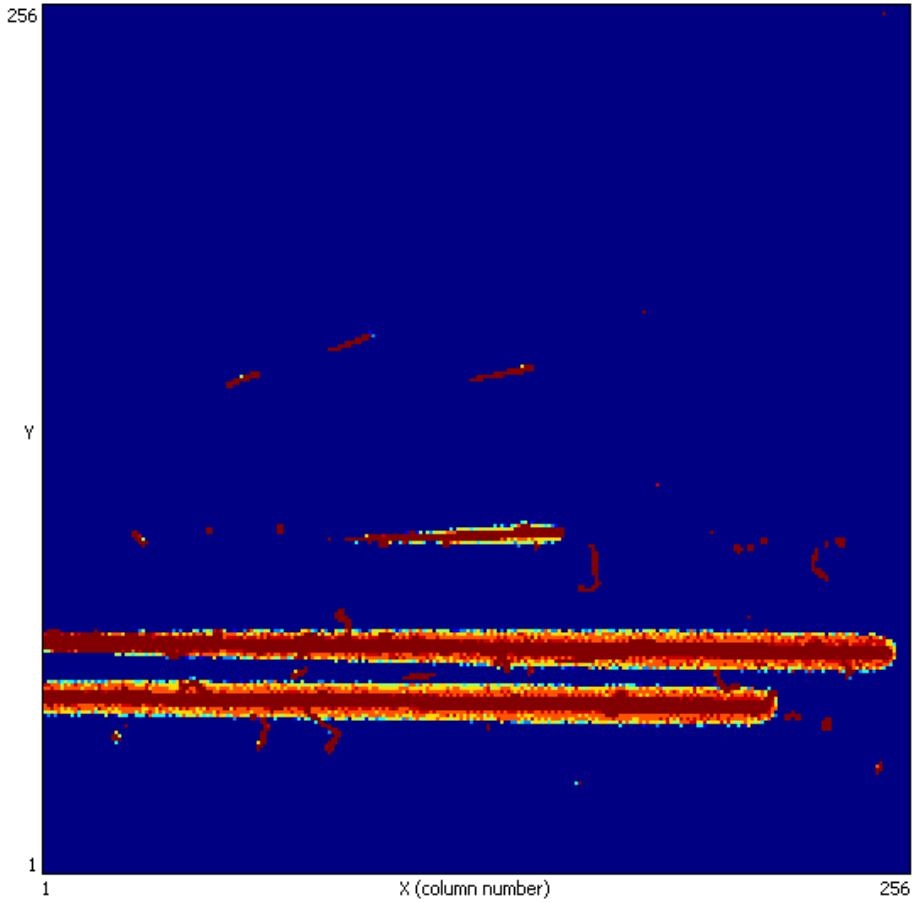
Time of Arrival

Strontium Source



Time over Threshold

Ion Beams at HIMAC



Charge deposition studies with various Isotopes
Space Dosimetry (Courtesy L. Pinsky, Univ. Houston)

Timepix Applications

- New Tracking Technologies
  - LHCb Upgrade
  - Linear Collider detectors
  - Solid state Detector Development
- TPC instrumentation
  - EUDET
- Emission Channeling Crystal Lattice Experiments
  - ISOLDE
- Image Intensifiers / Optical Photon Detectors
  - Adaptive Optics
  - Bioimaging
  - LHCb RICH
- ToF Mass Spectrometry
  - Proteomic Imaging at AMOLF and Oxford
- Imaging Mass Spec
  - Functional Cellular Biology at Kiev
- Photo Electron Emission Microscopy and Low Energy Electron Microscopy
  - Neutron Monitoring at CNGS
  - Space Dosimetry
  - Education - CERN@School

Limitations of the Timepix chip

- Chip architecture originally designed for imaging is used for single (or sparse multiple) event readout
- Non triggerable
- Full frame readout only
  - Serial readout (100 MHz): ~100 fps
  - Parallel readout (100 MHz): ~3000 fps
- Either arrival time OR energy information OR particle counting
- Time-walk > 50ns
- Large periphery -> Non active area (~2000 µm)

Timepix2 Scope

- Several groups in the Medipix3 collaboration have shown interested in a new version of the Timepix → Timepix2

- Large range of applications (HEP and non-HEP):
  - X-ray radiography, X-ray polarimetry, low energy electron microscopy
  - Radiation and beam monitors, dosimetry
  - 3D gas detectors, neutrons, fission products
  - Gas detector, Compton camera, gamma polarization camera, fast neutron camera, ion/MIP telescope, nuclear fission, astrophysics
  - Imaging in neutron activation analysis, gamma polarization imaging based on Compton effect
  - Neutrino physics
  - Particle Tracking – LHCb, LCD interest

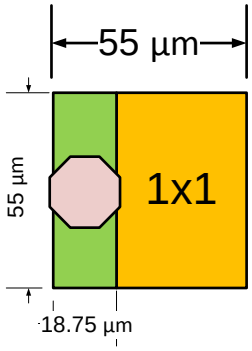
- Reuse many building blocks from Medipix3 chip (2009)
- Timepix2 is an approved project by the Medipix3 collaboration with an assigned budget (2-engineering runs) + partially funded by LHCb
- Designed between CERN (CH), Nikhef (NL) and University of Bonn (DE)

Timepix2 Main Requirements

- Lots of different applications → Very demanding specs !

Pixel size	55 µm x 55 µm
Pixel matrix array	256 x 256
Sparse readout	YES
PC, TOA or TOT recorded simultaneously	YES (2 at a time)
Minimum detectable charge	≤ 500 e-
TOA resolution	>1.5ns (25ns/16) 4bits (Gossipo3 style)
Peaking time	< 25 ns
TOT resolution	<5% channel to channel spread
Technology	IBM 130nm DM 3-2-3
Power consumption	<1.5W/cm^2 (~45 µW/pixel) @1.2 V
Target floorplan	3 sides buttable and minimum periphery
TSVs possibility	YES. Multi-dicing scheme as Medipix3

A new pixel floorplan



Pros&Cons of super pixel architecture

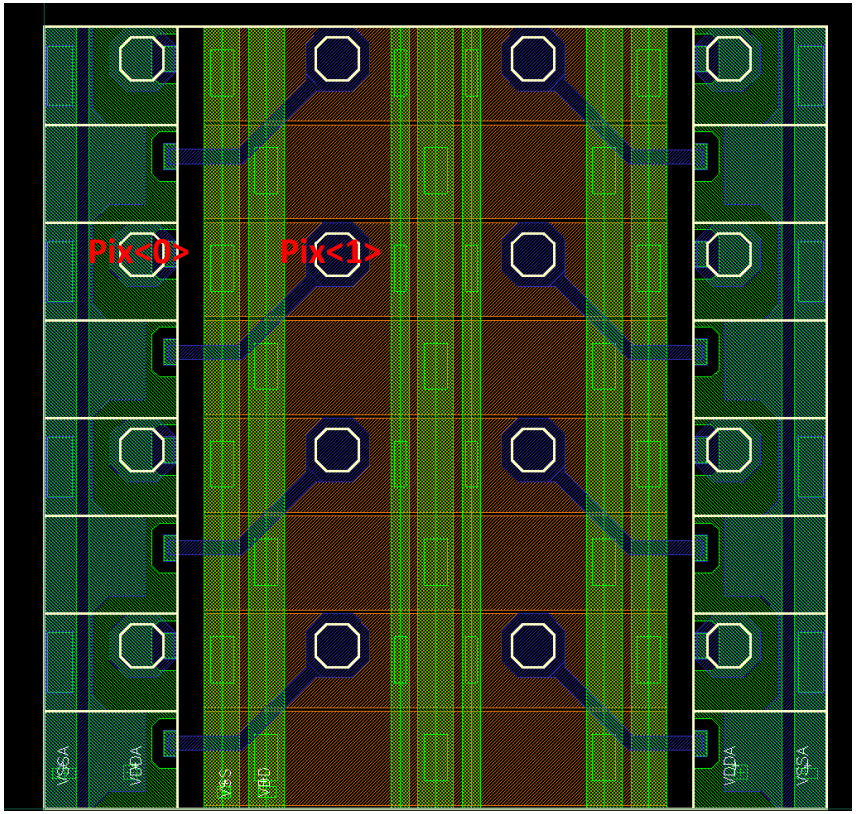
- Advantages:
  - Faster readout: Sparse readout, parallel bus on super pixel column,…
  - Better isolation between digital and analog blocks
  - Resources more efficiently shared:
    - Analog: bias blocks, power supplies, …
    - Digital: 1 clock tree per 4 pixel columns, 1 VCO (voltage controlled oscillator per super pixel), …
  - Possibility to use standard cells in the common digital block
  - More compact end of column logic → Smaller periphery?

- Disadvantages:
  - Routing of analog signal from the input pad to the preamplifier
  - Different analog input capacitance if layout is not carefully done
  - Some analog pads will not be shielded by the analog power planes
  - Loss of uniformity in the analog side

Parasitic layout extractions

- A dummy layout has been done in order to evaluate the coupling between analog and digital power supplies
- In this design the top metal (MA) is used to route the analog signals on the top of the digital side of the super-pixel to the analog section
- E1 and LY are use to drive the power and shielding

	Coupling line	Cap [fF]	Total Cap [fF]
Pix<0>	GND	0.4	
Pix<0>	VDD	0.05	
Pix<0>	VDDA	5.14	
Pix<0>	GNDA	1.18	7.5
Pix<1>	GND	5.2	
Pix<1>	VDD	2.7	
Pix<1>	VDDA	1.3	
Pix<1>	GNDA	0.68	12



Data push architecture

- The ‘ideal’ detector will read out all hits…
- An attempt to get close to this is the ‘Data Driven’ design
- Will push all events off the chip up to a limiting event rate

- Good for low rate and sparse applications
- Problematic for SLS physics or high rate imaging
- Cannot use the shutter to ‘squeeze down’ data rates

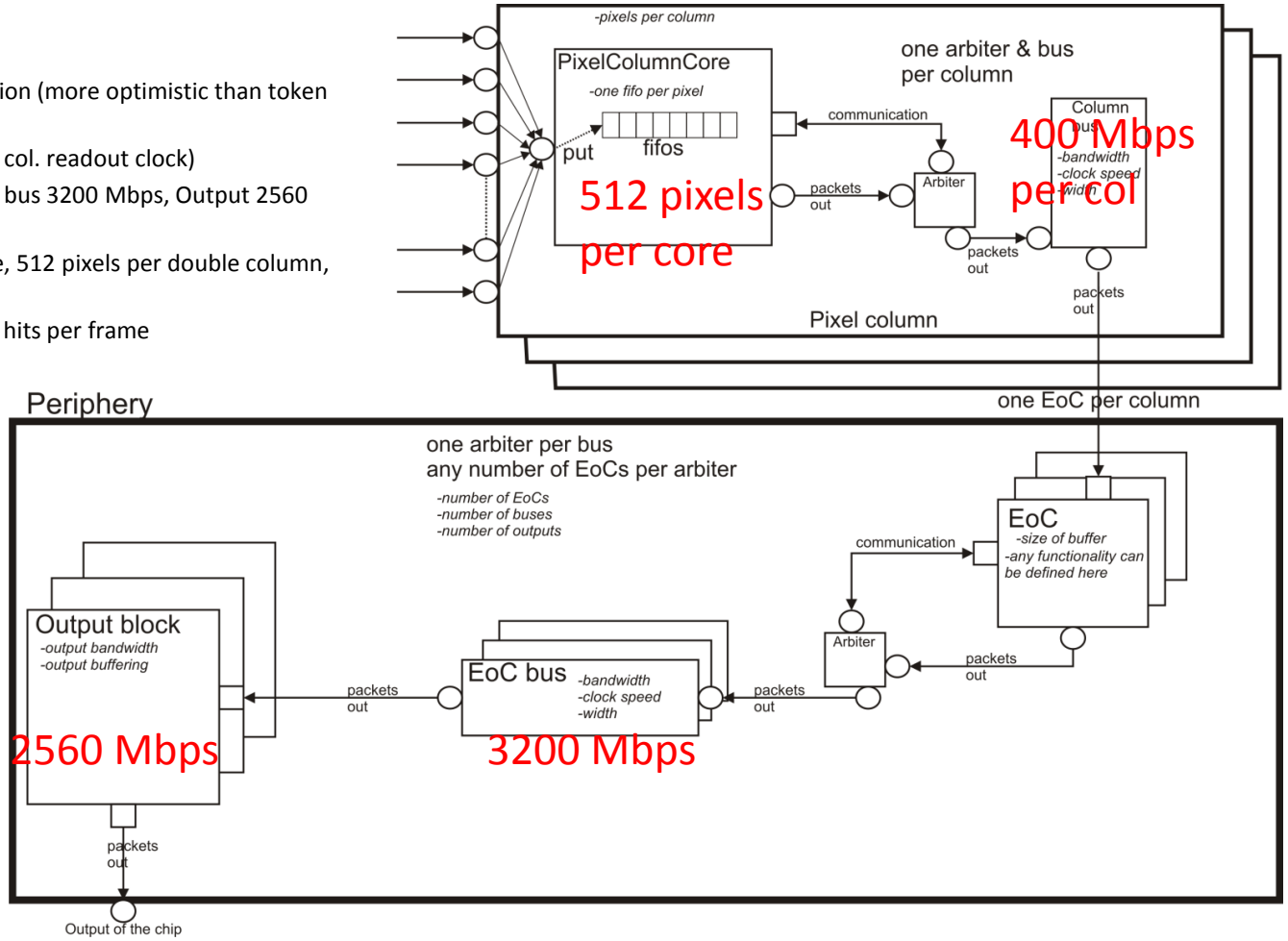
- Closer to ideal but not useable for all applications
- Requires significant on matrix logic and readout infrastructure to achieve high data rates

Timepix2 TLM overview

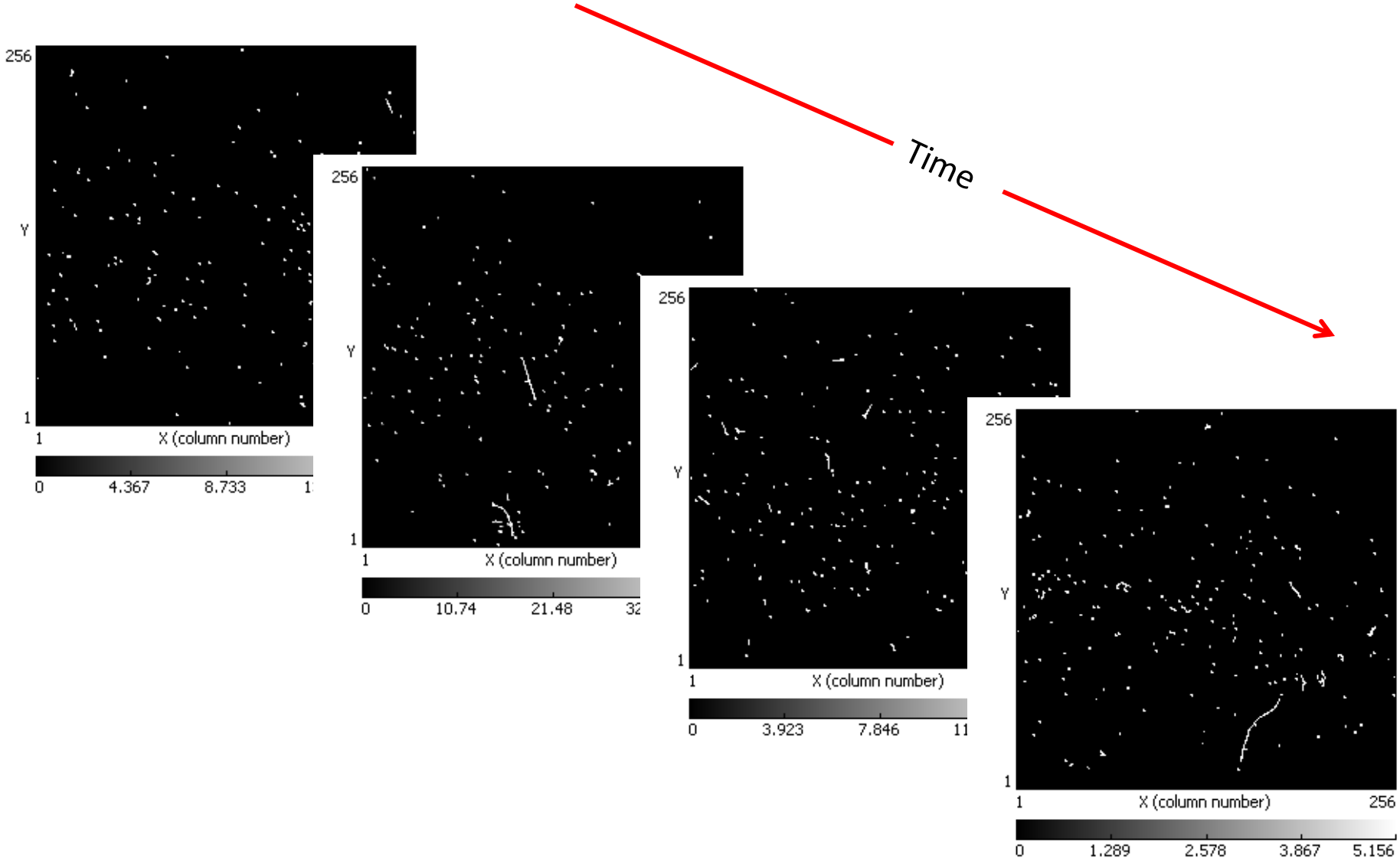
- T. Poikela (CERN) is setting up a highly configurable architectural model for finding optimal readout architecture for Timepix2
- The goal is to have an executable functional specification of the chip before detailed (Verilog) implementation starts
- Model can accept data from external files to simulate its performance in different experiments and applications
- Can simulate architectures with different properties:
  - continuous/triggered/full frame readout
  - different super pixel configurations
  - no super pixels
  - shift register column readout architecture
  - bus-based column readout architecture
  - periphery w/ bus/shift register

Simulation model (T.Poikela)

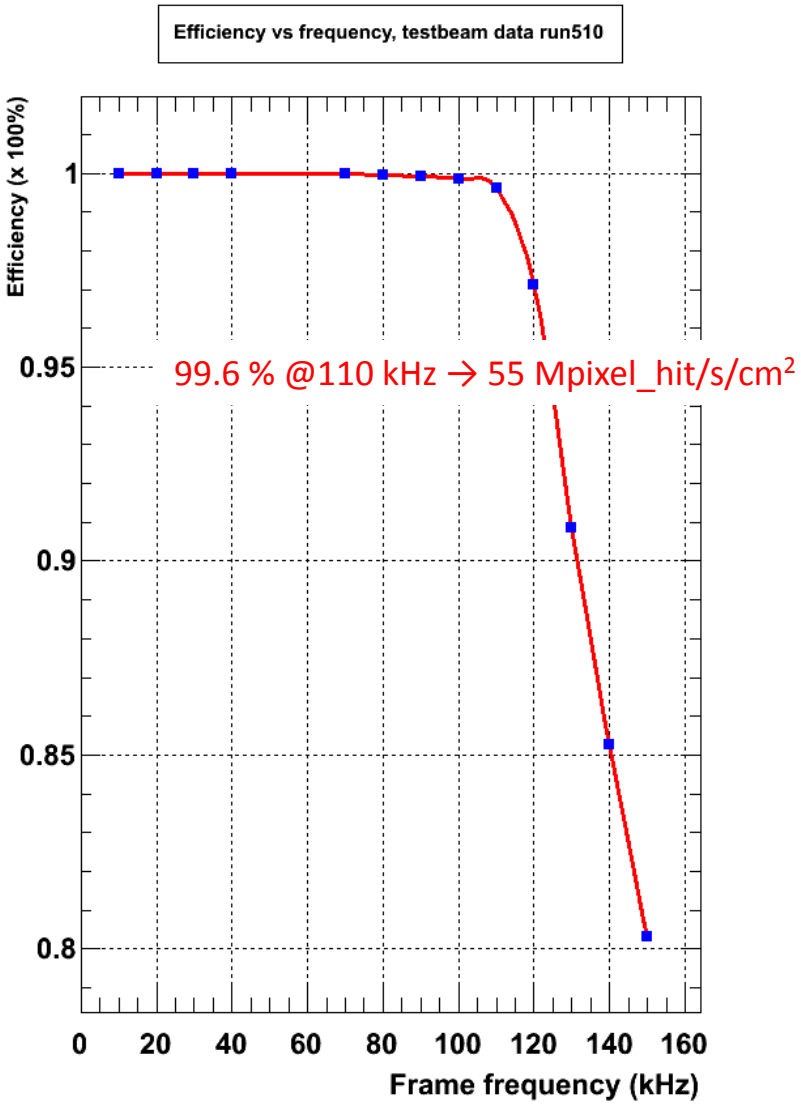
- Simulation example:
  - Packet based readout
  - Centralized parallel arbitration (more optimistic than token arbitration)
  - Ref. clock 40 MHz, (20 MHz col. readout clock)
  - Column bus 400 Mbps, EoC bus 3200 Mbps, Output 2560 Mbps
  - Double column architecture, 512 pixels per double column, no super pixel functionality
  - Input frames: 500 to ~1200 hits per frame

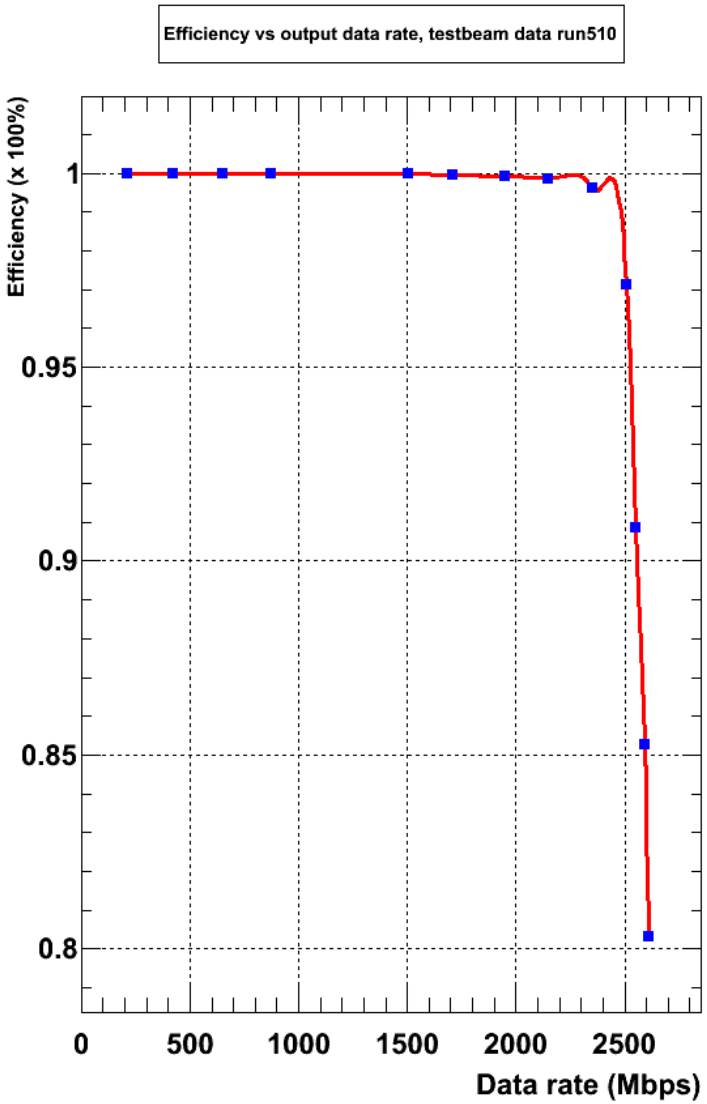


Timepix testbeam run of 510 frames



Simulated efficiency (T.Poikela)





Conclusions

- The Timepix2 chip, funded by the Medipix3 collaboration and partly by LHCb, will be the successor of the Timepix chip
- Designed in a commercial 130nm CMOS 8-metal process will reuse many building blocks designed for Medipix3 (LVDS drivers, DACs, e-fuse, Test Pulse…)
- The main requirements are:
  - TOA and TOT simultaneously in each pixel with a TOA resolution > 1.5 ns
  - Fast sparse readout
  - 55 x 55 µm pixels…

- The analog pixel architecture is well defined: Preamplifier + discriminator + 3 or 4 bits threshold equalization
- The digital pixel architecture is not completely specified since different readout topologies are being evaluated using a highly configurable Verilog architectural model
- Design is still at the specification level (dominated by the readout architecture)
- Chip submission by the end of 2011