The Saltro chip design for TPC pad readout

Talk outline

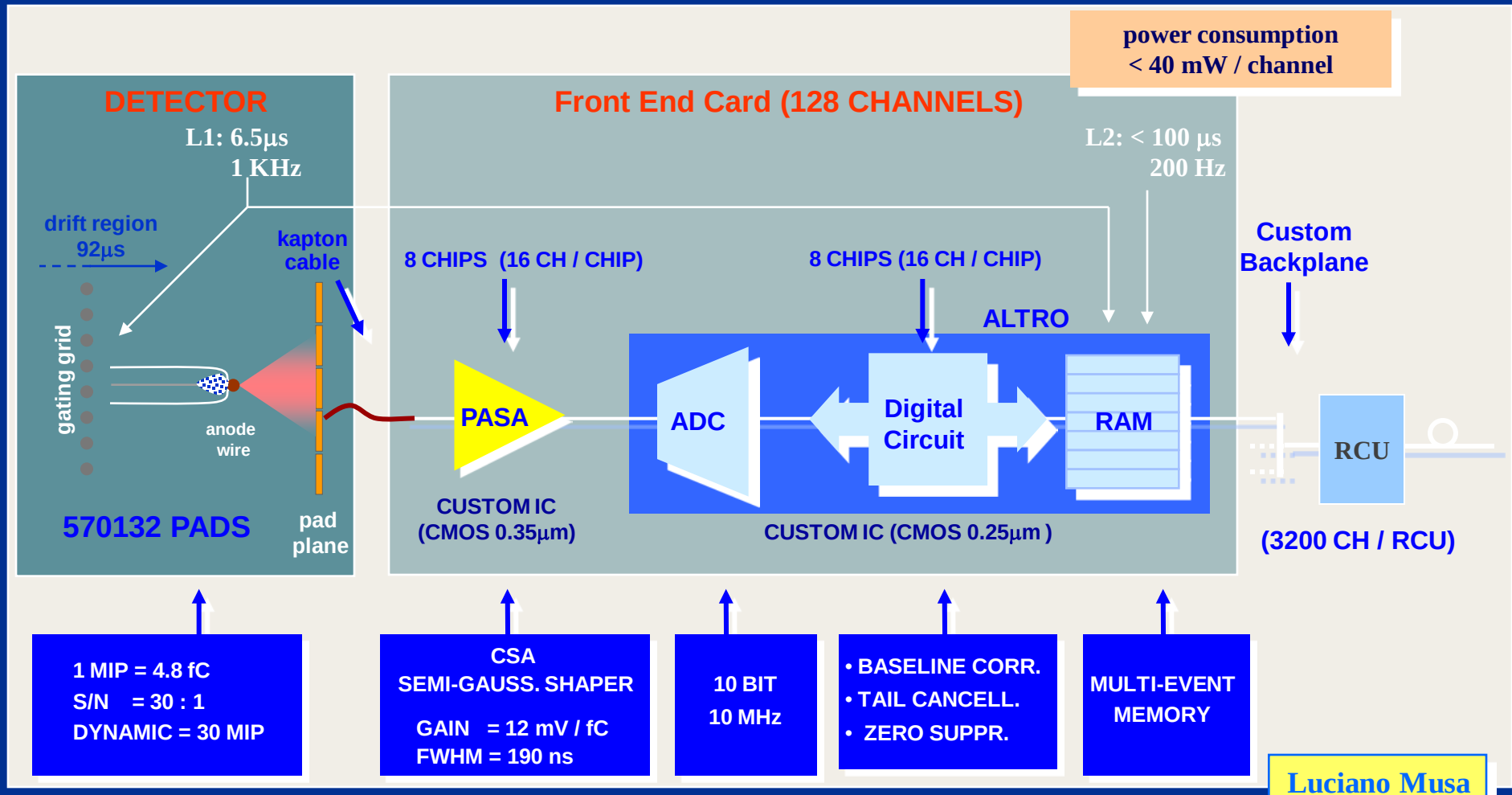
The historical perspective.

The SAltro demonstrator.

Projections and ideas for the future.

S-Altro architecture

Based on the existing PASA + Altro electronics designed for the Alice TPC



Luciano Musa

SAltro Demonstrator

Goal :

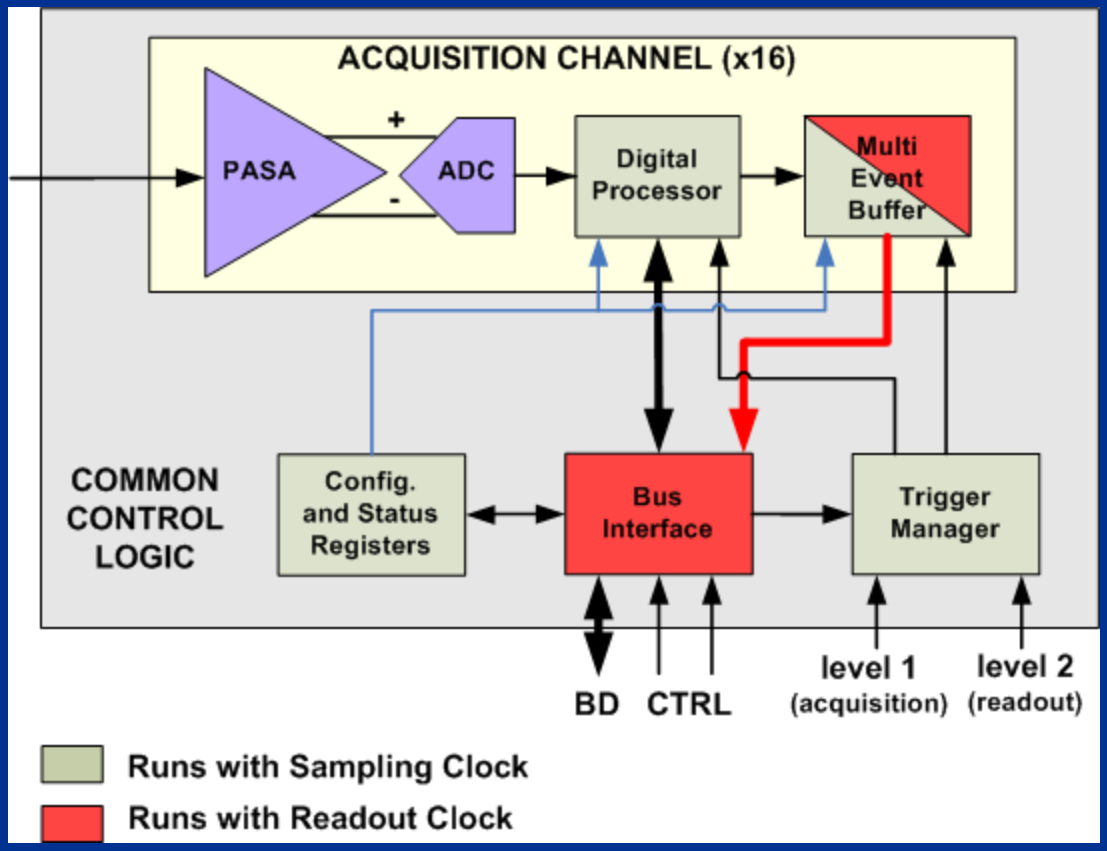
To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

Luciano Musa …… S-Altro Specifications and Architecture
Paul Aspell …….. Coordinator of demonstrator ASIC design.
Massimiliano De Gaspari ……. Front-end + ADC
Hugo França-Santos ……... ADC core
Eduardo Garcia …… Data Processing & Control

SAltro Demonstrator Architecture



- 16 Channels.
- Sampling rate 10, 20, 40MHz.
- ADC : 10 bits per sample.
- Level 1 commences sampling of a data-stream.
- 1008 (max) samples per data-stream.
- DSP for zero suppression.
- 40 bit word data packets containing timestamp and length.
- Possibility to by-pass DSP to have raw data.
- MEB (1024*40 RAM).
- Max. storage of 4 non-zero suppressed data-streams.

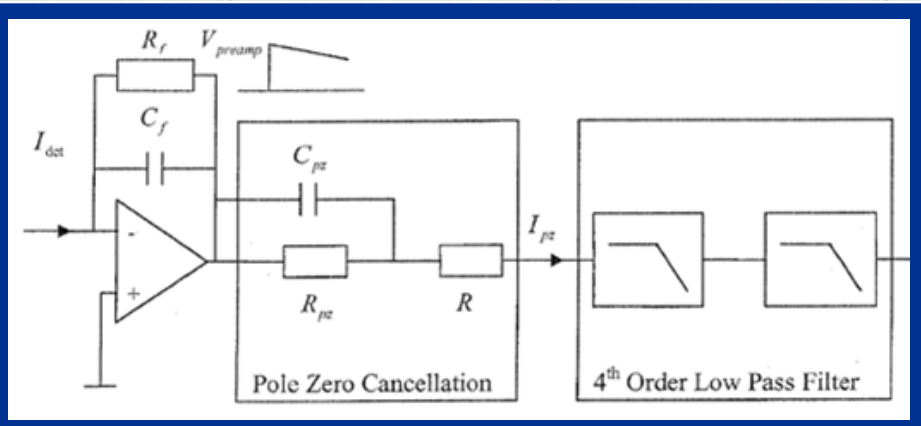
or

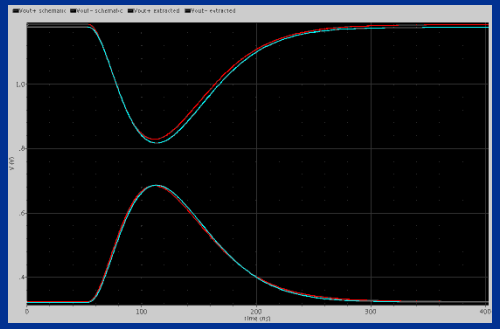
- Max. storage of 8 zero suppressed data-streams and/or with reduced data-stream length.
- Level 2 must arrive before next Level 1 in order to keep the data.
- <80 MHz readout on 40 bit CMOS bus.

Technology :
IBM 130nm CMOS 8RFDM

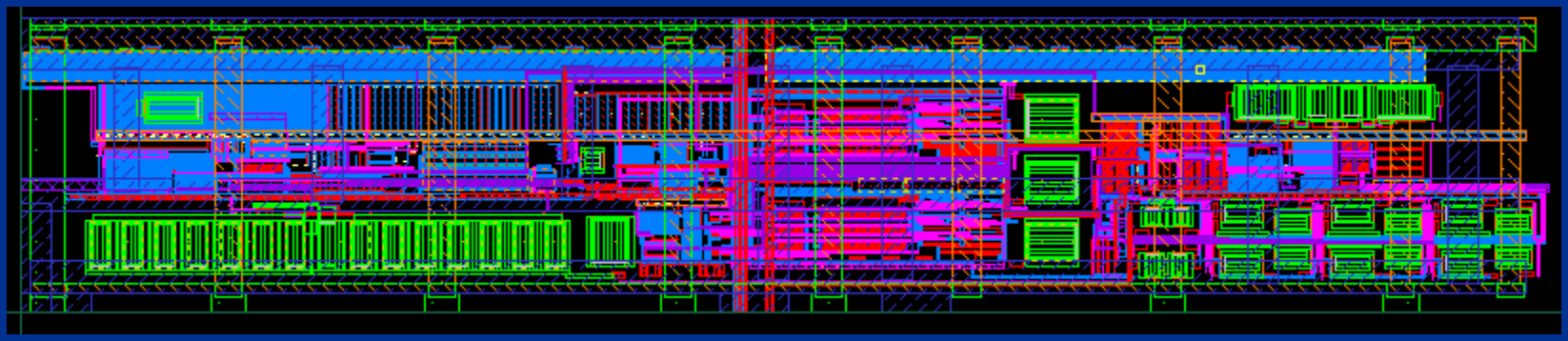
Saltro demonstrator Preamplifier/Shaper

- Single-ended input, differential output
  - Dual polarity
  - 4 Gain options : 12, 15, 19 & 27mV/fC
  - 4 Shaping times : 30, 60, 90 & 120ns.
  - Linearity <1% to 150 fC
  - Shutdown mode (for power pulsing via a duty cycle clock)
  - Preamplifier enable (bypass shaper)



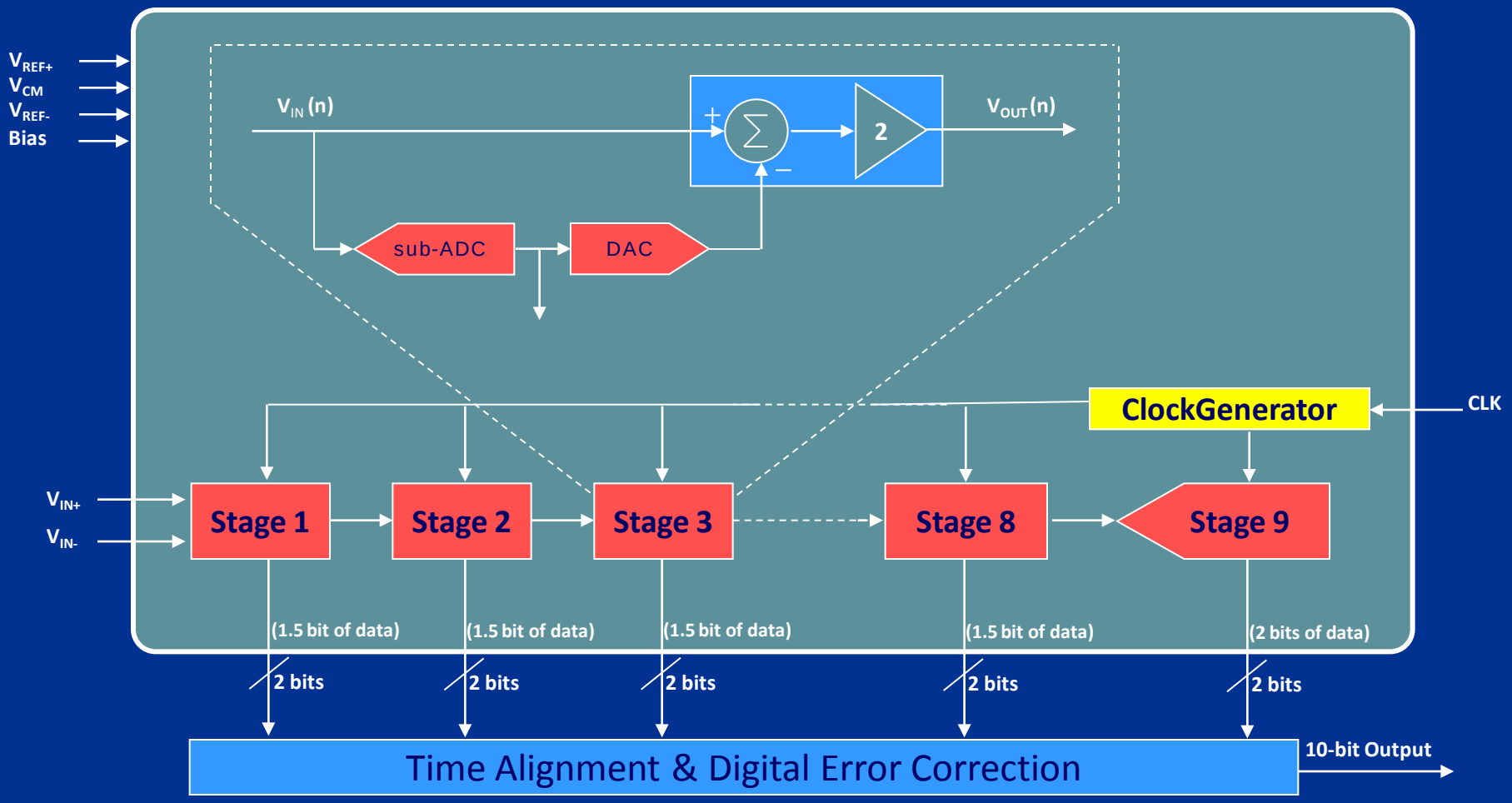


Size: 1100um X 210um Power: 8.4mW/channel Supply: 1.5V



Massimiliano De Gaspari

Pipeline ADC

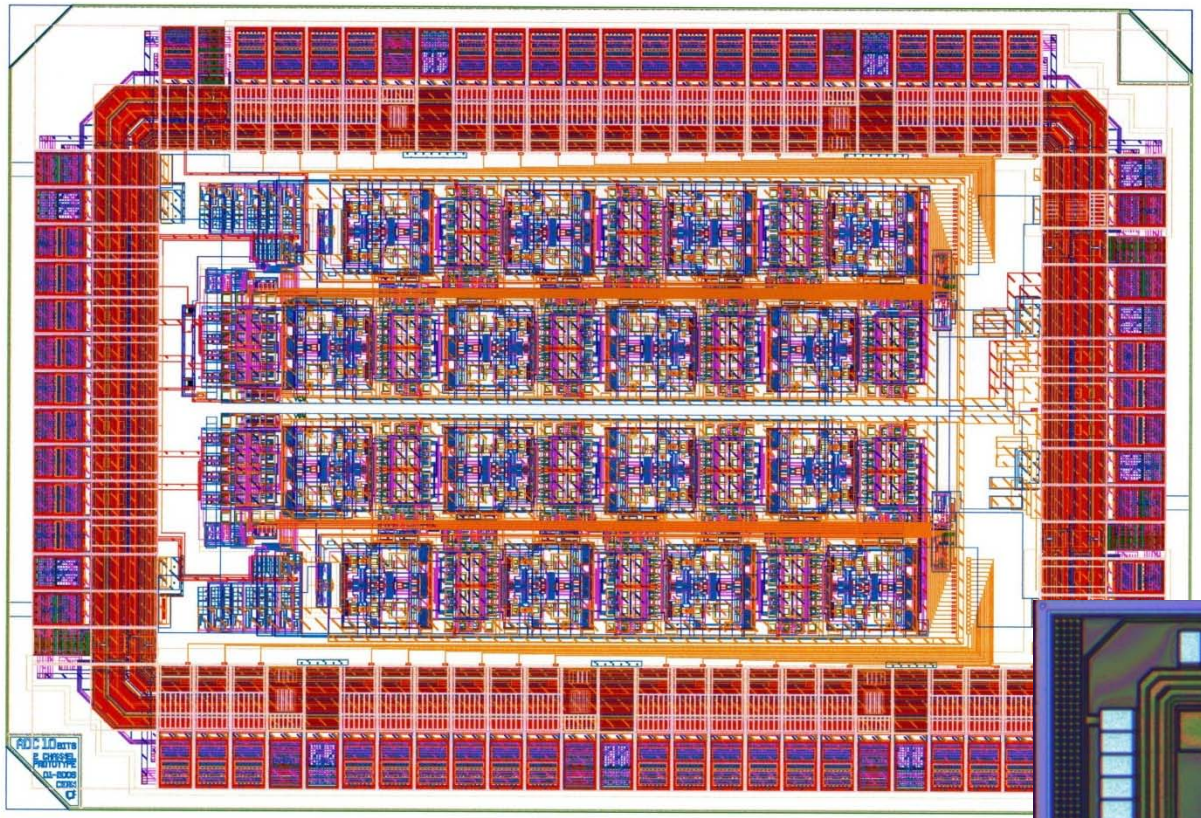


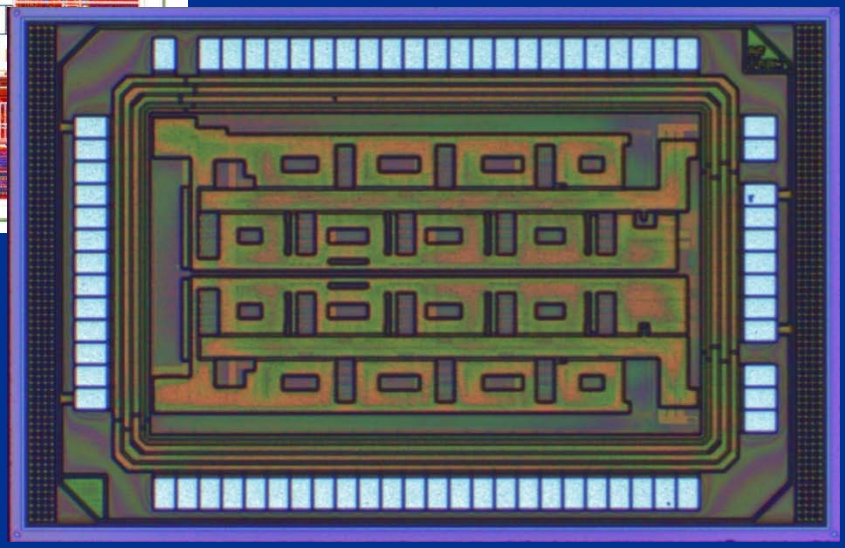
Hugo Franca-Santos, Massimiliano De Gaspari

10bit, 40MHz, 1.5V supply, 34mW power , 0.7mm^2 area

Power pulsing possible through bias pin.

Pipelined ADC: 2-Channel Prototype Layout





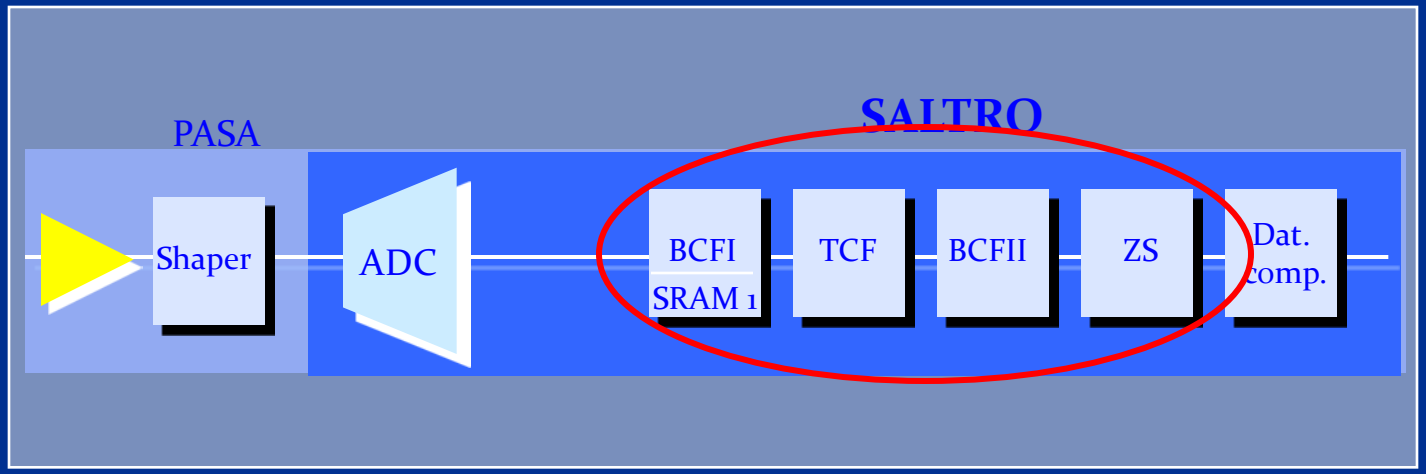
Single ADC area **1.57 X 0.45 = 0.7 mm²**
Prototype area **2.35 X 1.6 = 3.76 mm²**

A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process – TWEPP 2009

ENOB = ~9 FOM = 1.56pJ

Hugo França-Santos

DP functions

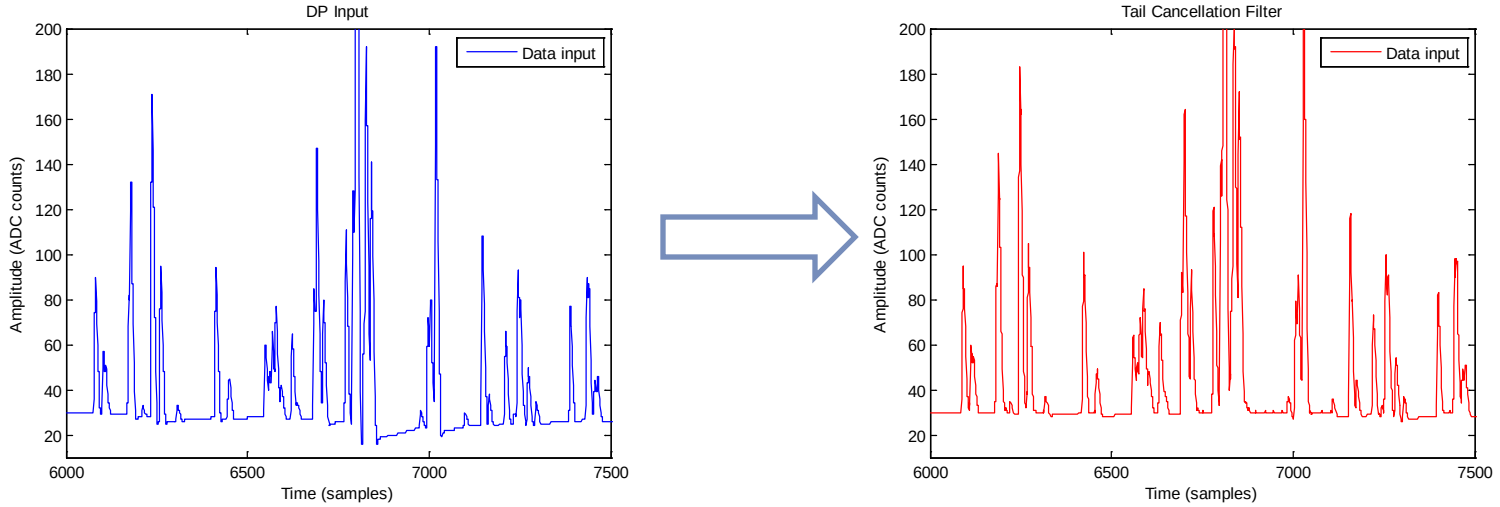


Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to very long ion tails.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.

Eduardo Garcia

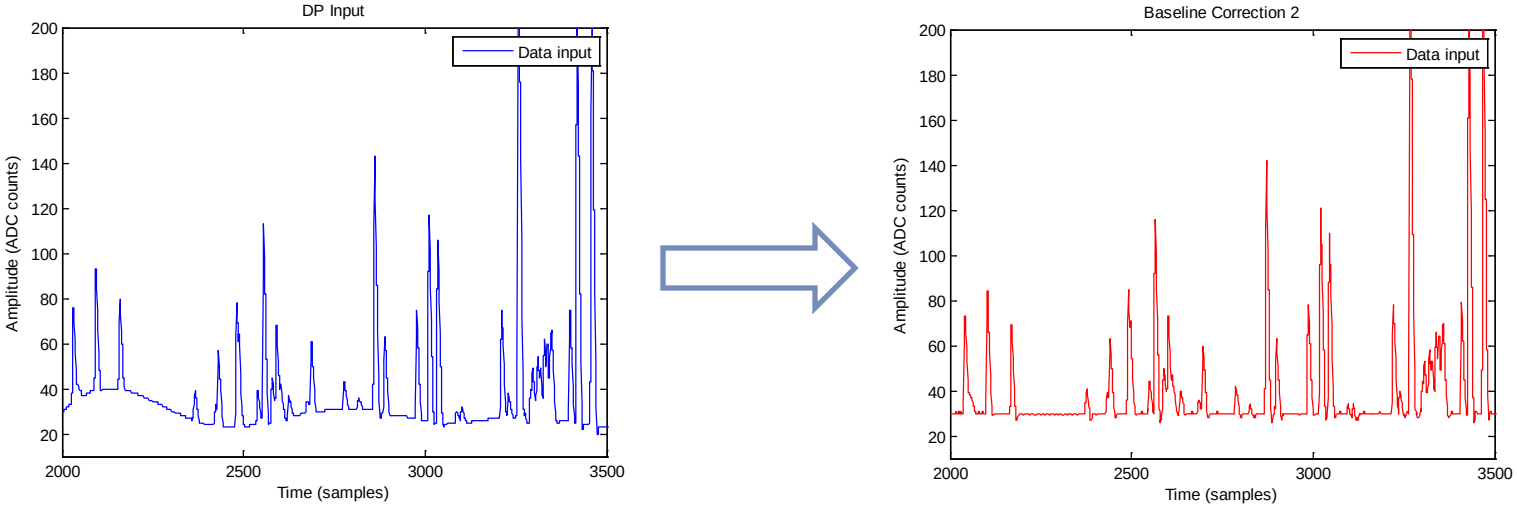
DP simulation results

- TCF example test: rest of the filters are disabled.

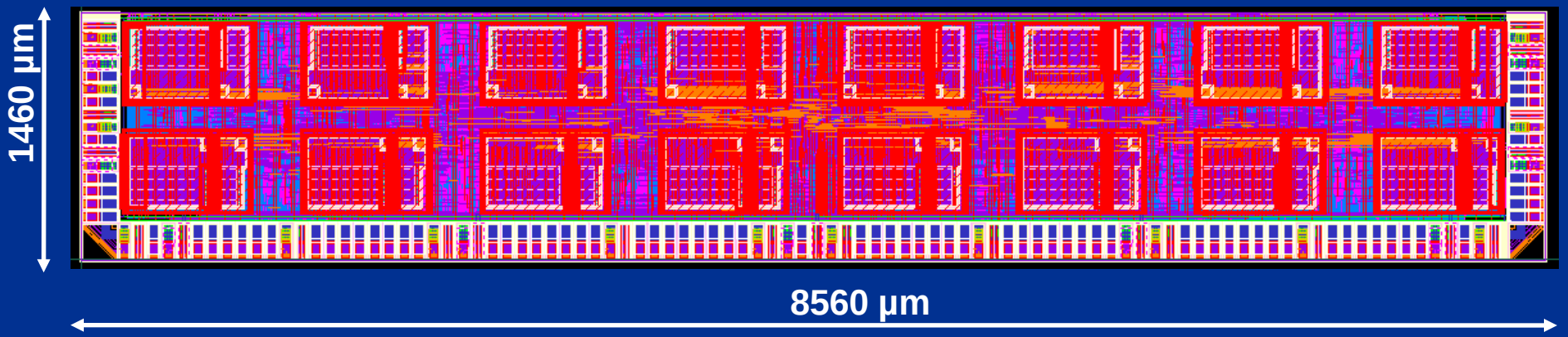


- BC2 example test: rest of the filters are disabled.

Eduardo Garcia



DSP, memories and data-formatter



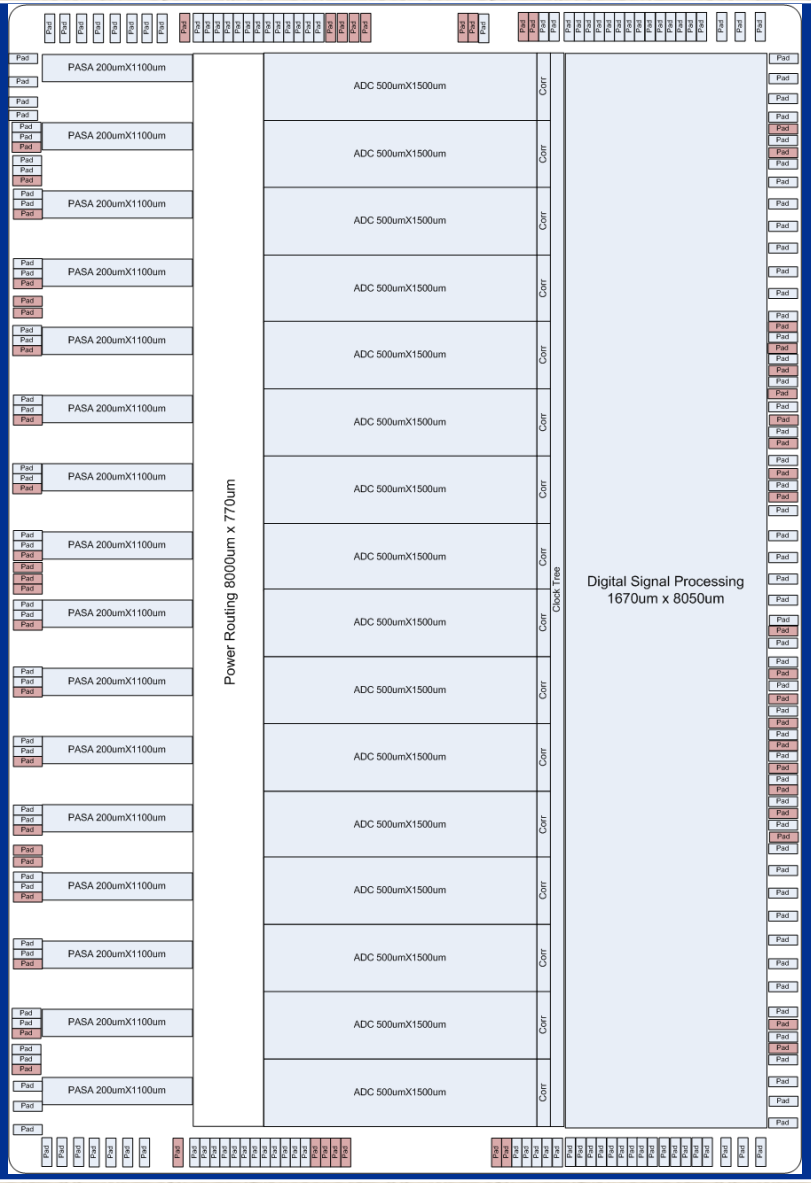
Conditions:

Static Analysis	Toggle probability: 0.3
VDD = 1.5V	Temperature: 25 C
Sclk = 50MHz	Voltage variation: 10%
Rdoclk = 90Mhz	Signoff verification

Encounter Statistical Power Analysis:

- Average power (considered in rail analysis): **118.62 mW**

S-ALTRO Demonstrator Floorplan



16-channels:

PASA **210um X 1100um**

ADC **500um X 1500um**

Digital Signal Processing
1670um X 8050um

The wide power routing ensures low IR power supply drop (10mV for the ADC)

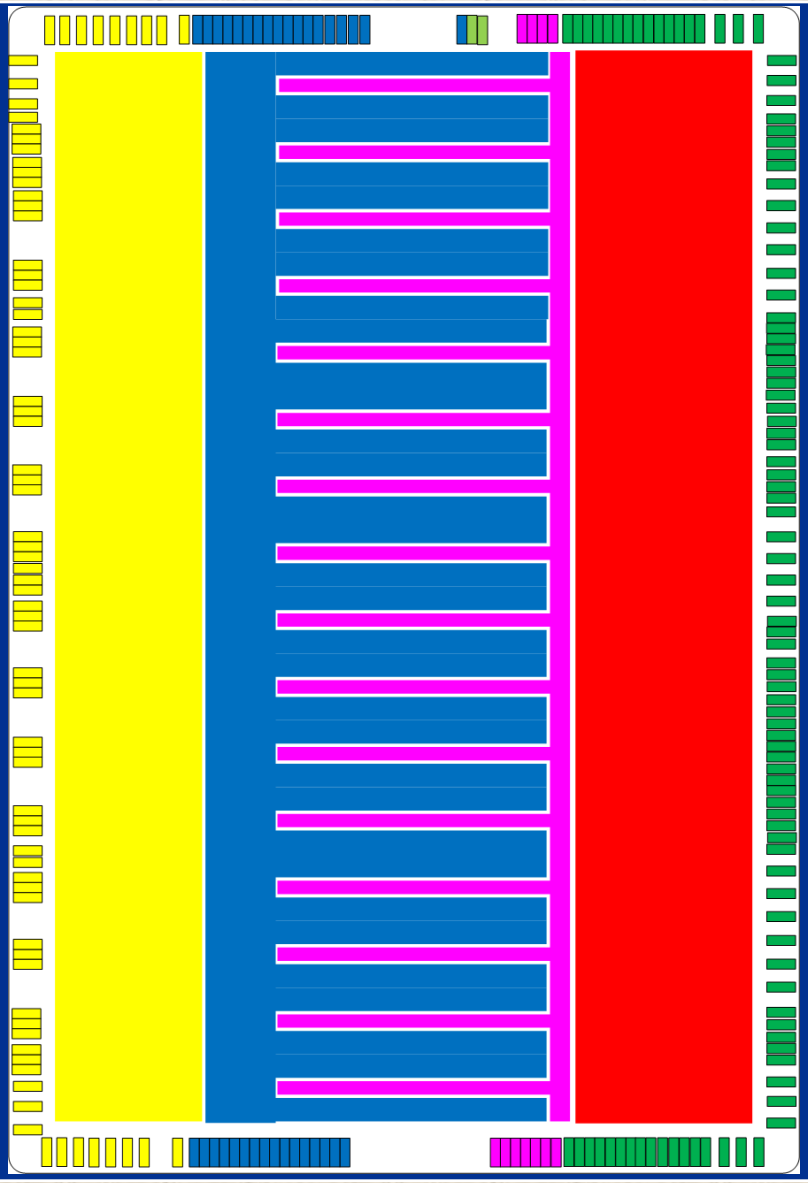
PASA ~8mW/ch,

ADC 32mW/ch @40MHz

Digital functions ~114mW

Total power ~ 750mW

Power domains



Power domains:

PASA analog

ADC analog

ADC digital

Digital core

Digital Pads

Power supply decoupling capacitors:

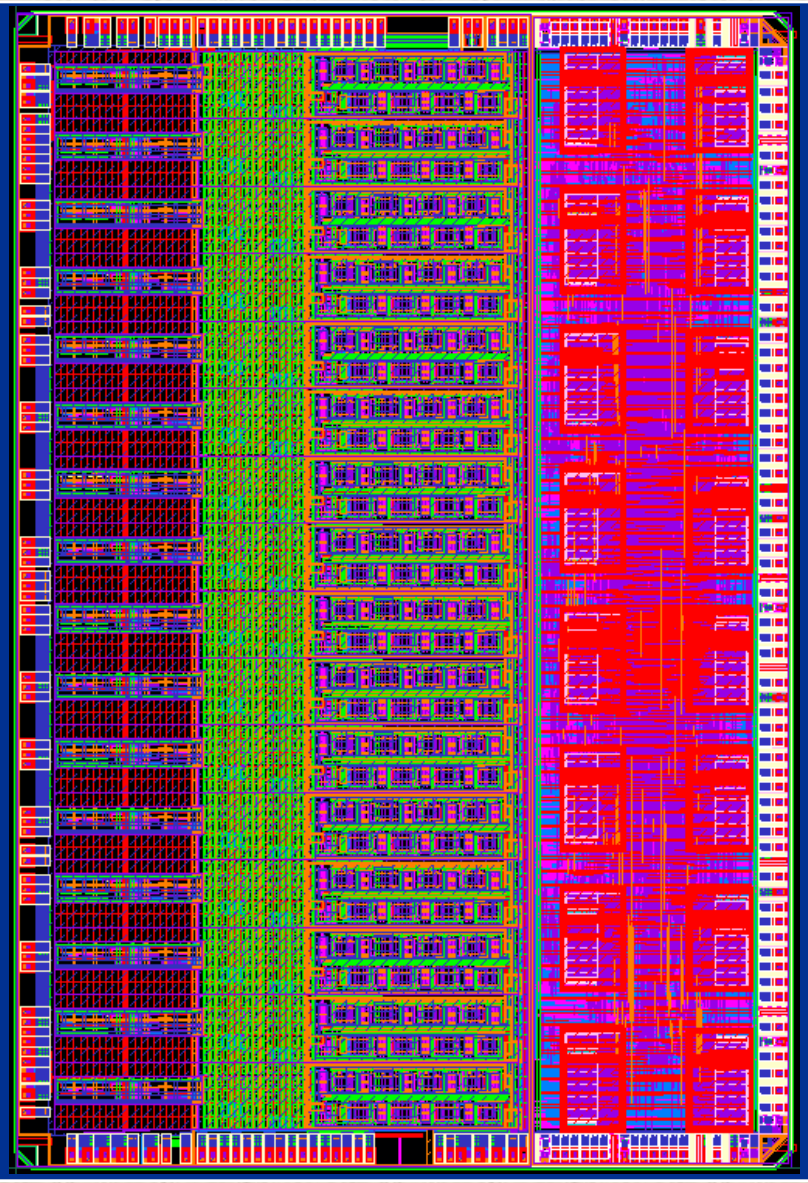
600pF /channel PASA

600pF /channel ADC analog

40pF /channel ADC reference voltages

80pF/channel ADC digital

Layout



Size: 5750um x 8560um
(49.22mm^2)

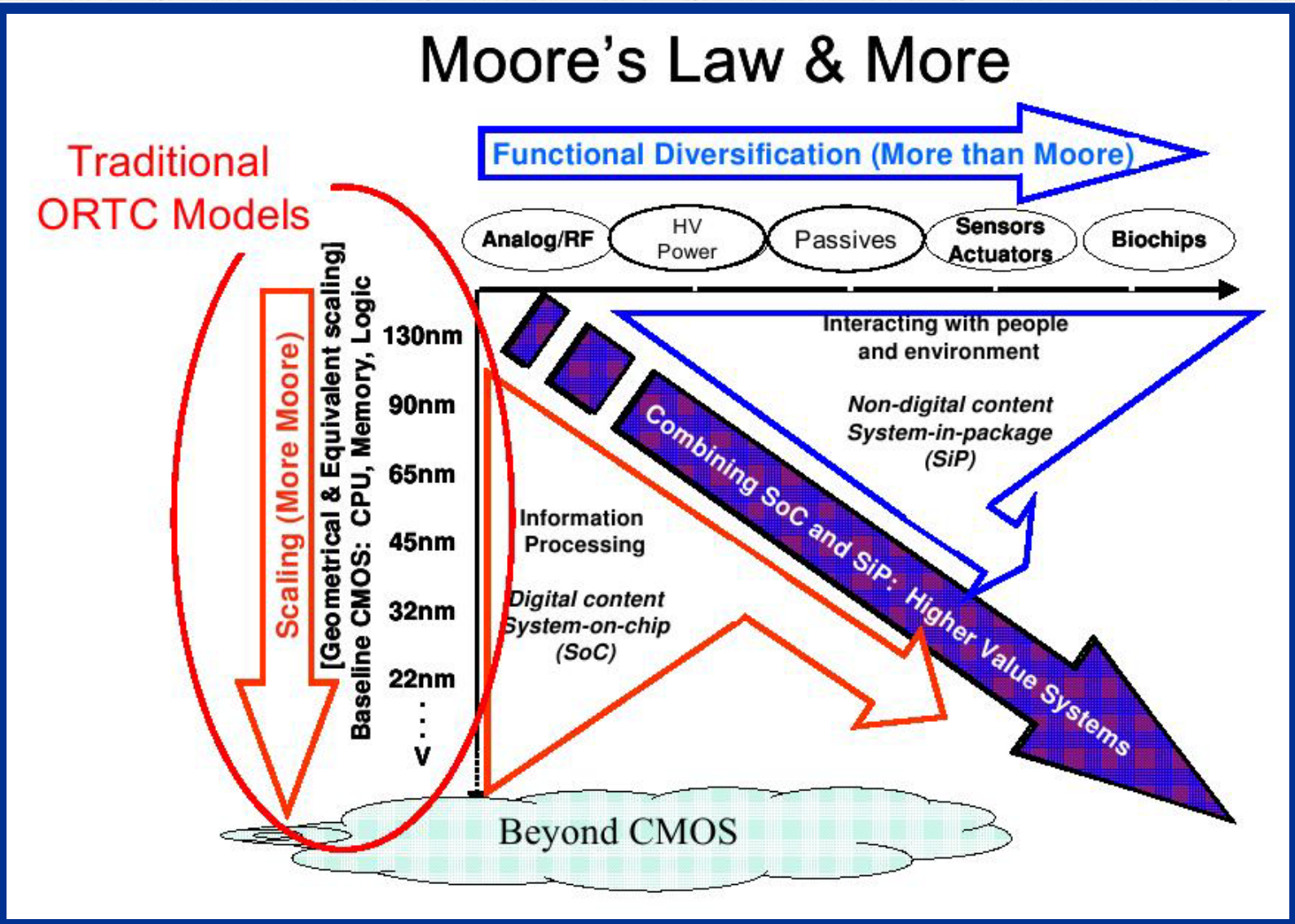
MPW organised by CERN.

Chip submitted in August 2010

Expected back at the end of 2010.

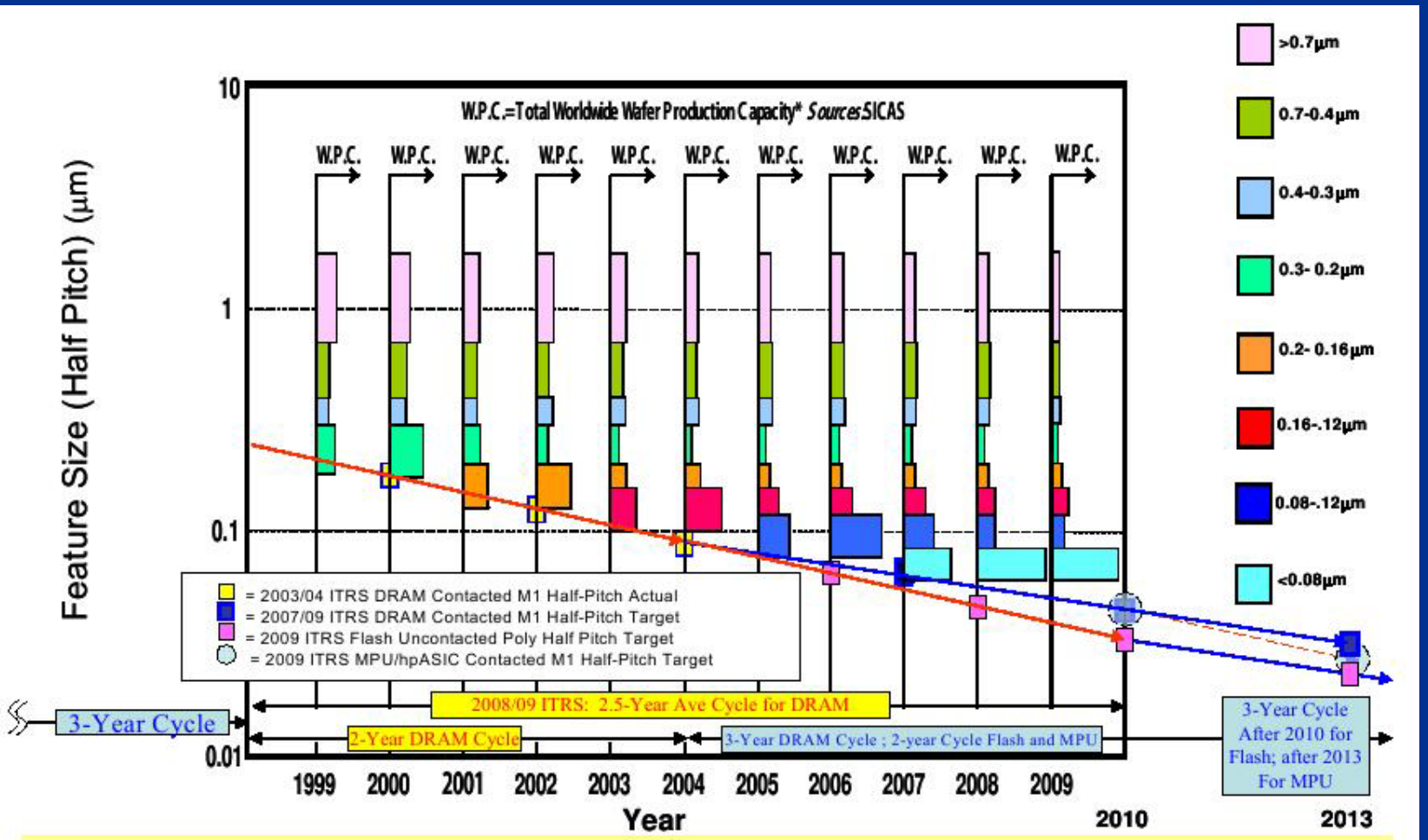
The pad placement has been optimised for packaging within a TQFP 176 pin package.

The Future & Technology Trends



Source : ITRS roadmap 2009

Technology Trends



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2009. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Source : ITRS roadmap 2009

Technology : CERN microelectronics group

- In addition to our current use of 0.25µm, 0.13µm and 90nm CMOS technologies CERN are now investigating 65nm CMOS technology.

- 12” wafers
- <10 Metal layers
- Vdd = 0.9V to 1.2V
- 840k gates/mm^2

- Regular MPWs.

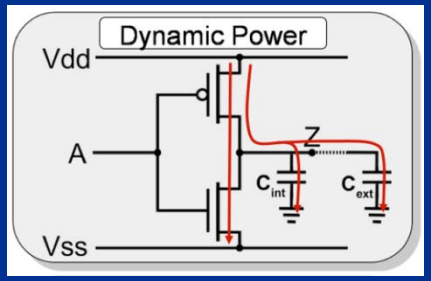
- LP process uses thicker gate oxide to GP to reduce leakage.

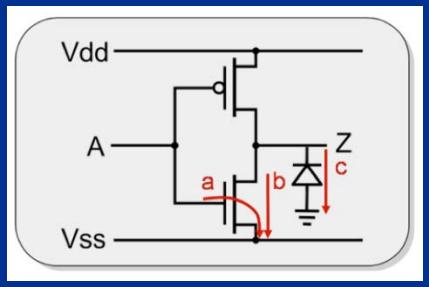
Standard Offering		65GP	65LP	65LPG	
				G	LP
Vt	Low	●	●		●
	Medium Low		●		
	Standard	●	●	●	●
	High	●	●	●	●
IO	1.8V	●			
	1.8V (2.5V Under-drive)	●	●		●
	2.5V	●	●		●
	3.3V (2.5V Over-drive)	●	●		●
	3.3V	●	●		
SRAM	Ultra High Density (0.499)	●			
	High Density (0.525)	●	●		●
	High Current (0.62)	●	●	●	●
	Dual Port (0.97)	●	●	●	●
	Dual Port (1.158)	●	●		●

- CERN are now evaluating several 65nm design kits.
- Test structure submission planned for early 2011. To be followed by radiation studies.
- Standard cell libraries are available. They will probably need modification to be compatible with our needs.

Digital

Scaling reduces source/drain capacitances and reduces power supply levels.



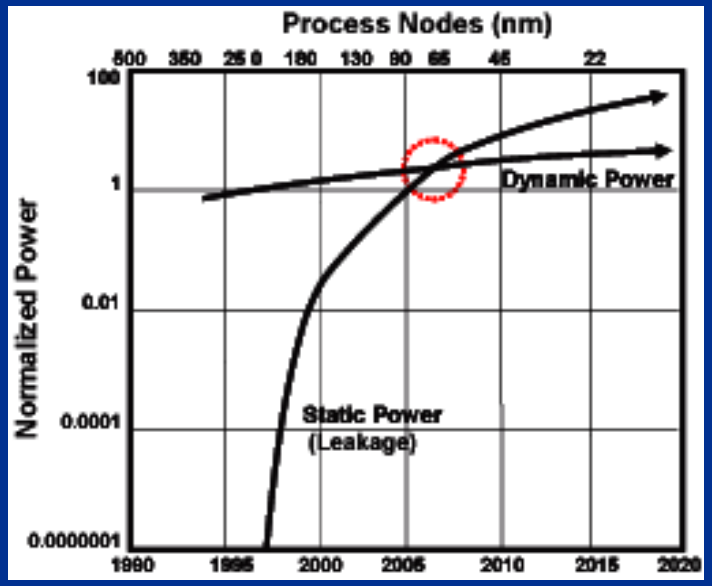


- Dynamic power goes down.
- $P_{dyn} = (C.Vdd^2 + Q_{short\_circuit}\ Vdd)\ f\ .$ activity

- However static power increases even in CMOS:
- Leakage currents increase including gate leakage current.

- Multiple power domains possible (vdd= 0.9V to 1.2V) depending on operating frequency required.
  - » Very high speed : Lowest Vt and max Vdd
  - » Moderate and Low Speed : higher Vt and reduced Vdd.

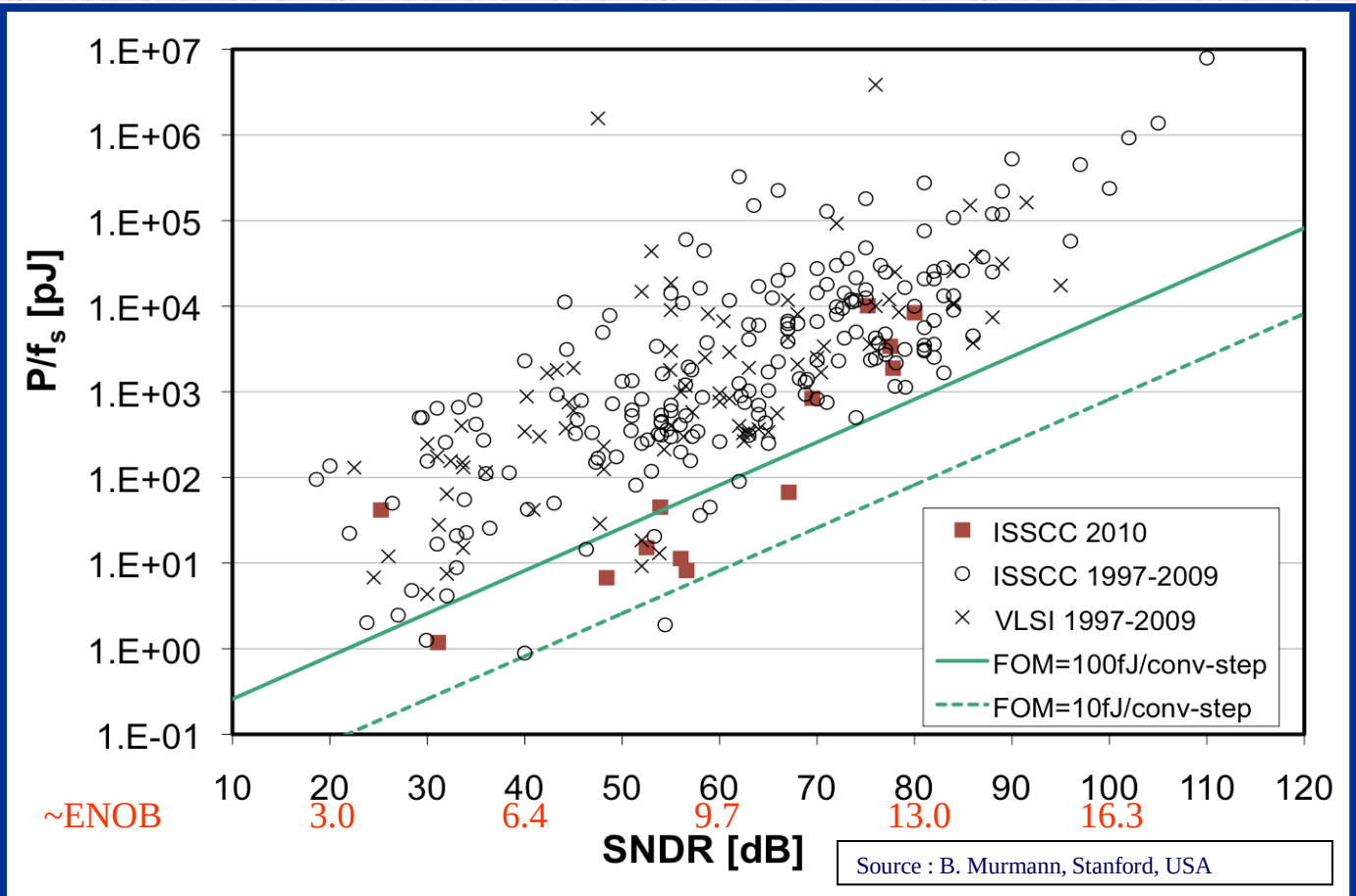
- The digital power consumption will take a larger % of total chip power in future designs compared to previous chips.



Source : Altera on TSMC 65nm

ADC Trends

- FOM ~ P / (2^{ENOB}. 2BW)
- 1pJ is high
- (~40mW @ ENOB 9, 40MS/s)
- 100fJ is good
- (~4mW @ ENOB 9, 40MS/s)
- 50fJ excellent
- (~2mW @ ENOB 9, 40MS/s)



State of the art :

A 30fJ/conversion 8b 0 to 10MS/s Asynchronous SAR ADC in 90nm CMOS. P. Harp et. al. IMEC ISSCC 2010
[They measured 69uW at 10MS/s,]

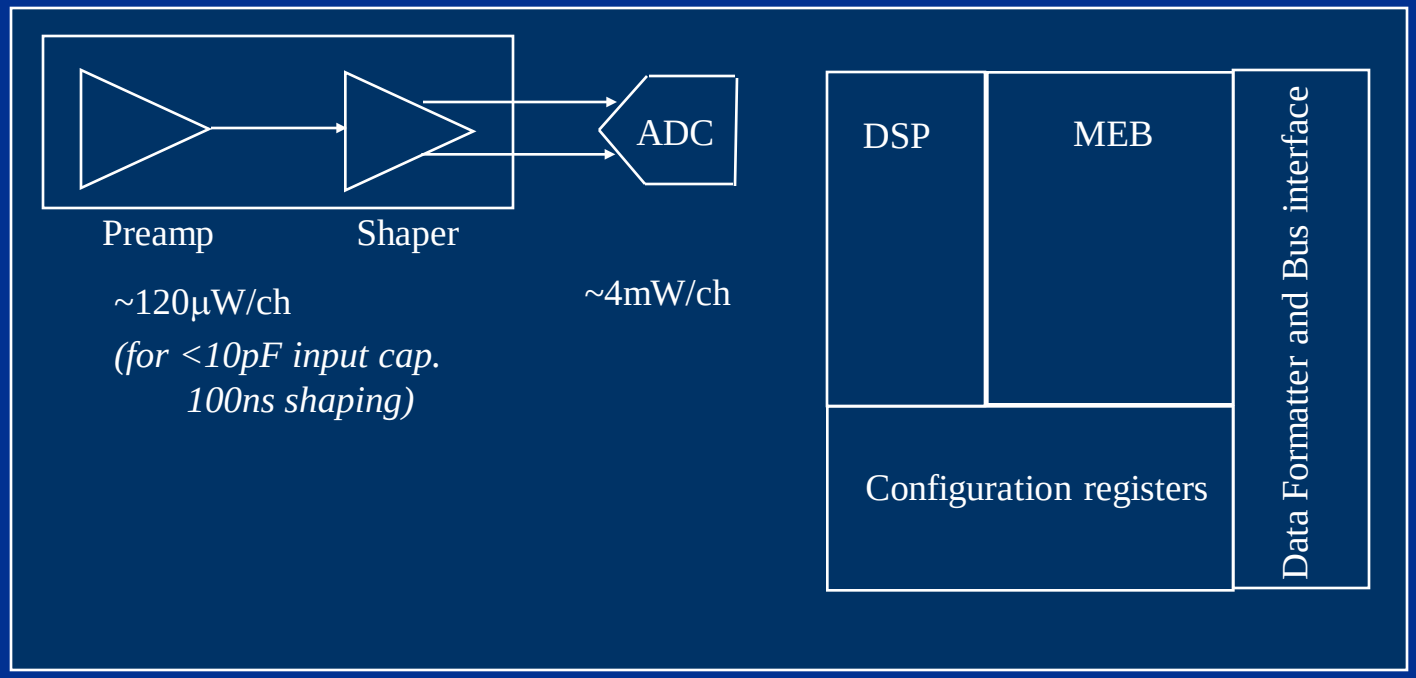
A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.*
CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

Front-ends

- Front-end power can be very finely tuned but requires detailed knowledge of the sensor characteristics.
  - » Total input capacitance (sensor + coupling to neighbours + board) is required to optimise the input transistor current.
  - » Charge collection properties are required to make the correct choice of shaping time. If the shaping time is too small ballistic deficit will degrade S/N.
- Input transistor current scales with detector capacitance and charge collection time. Approx. 10μA/pF for 25ns shaping and ~ 2.5μA/pF for 100ns shaping .

Rough estimate of front-end power budgets		
Electrode capacitance	for 100ns shaping	for 25ns shaping
1pF	12μW ??	48μW
10pF	120μW	480μW
20pF	240μW	1.6mW
50pF	800μW	3.2mW

Estimate for future power (static)



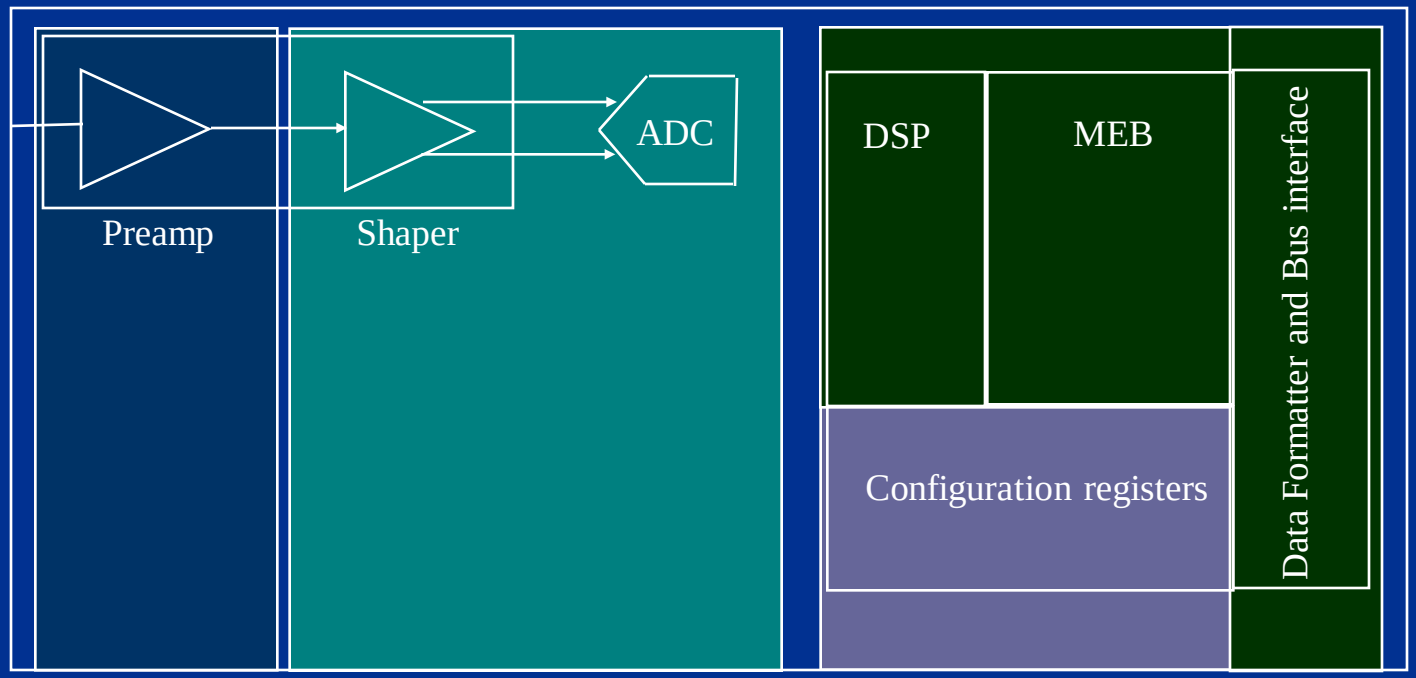
64 channels = Analog power ~ 263mW + Digital power ~ a few hundred mW.
Approx. 400-500mW / chip.

128 channels = Analog power 526mW + Digital power ~ some hundreds mW.
Approx. ~800-900mW / chip.

Should be possible to get < 7mW/ch for everything on a 128 ch chip.

Power management & pulsing may then be applied to reduce power further.

Power management : Power domains for reducing power further during "down" time (dynamic).



Preamp > Reduce current via bias control, important to maintain a low impedance on the electrode.

Shaper > Reduce current to approx. zero via bias control. Vdd could be maintained.

ADC > Stop clock and reduce current to approx. zero via bias control. Vdd could be maintained.

Configuration reg.s > Reduce Vdd to minimum voltage necessary to hold data. Current consumption limited to leakage currents.

Digital logic > Switched off by reducing Vdd to 0V.

Duty cycle of UP/DOWN time determined by a clock.

Summary

- The SAltro architecture is derived from the Altro architecture currently used for TPC readout in ALICE.

- The SAltro demonstrator chip has been designed and submitted.
  - » Comprises 16 channels of Front-end + ADC + DSP on the same chip.
  - » Chip return back from foundry for beginning of 2011.
  - » Many things can be studied using the SAltro demonstrator :
    - – GEM properties : capacitance, charge collection time, optimal shaping, channel to channel coupling etc.
    - – Internal power pulsing on front-end and ADC via clock and bias control.
    - – The power consumption of the present 16 channel chip is about the same absolute value as future chips with more channels. This makes the demonstrator useful for groups studying external power pulsing.

- The future looks favourably on the SAltro architecture.
  - » The industrial trend is with us continually looking for ways to reduce power.
  - » The ADC remains the critical element w.r.t. power, however state of the art ADCs are becoming more and more power efficient.
  - » Front-end power optimisation requires detailed knowledge of the sensor characteristics.
  - » Power management within a chip is now common place in modern industrial chips and could be a useful tool for power pulsing.