Tracking with Monolithic Pixel Sensors in SOI Technology

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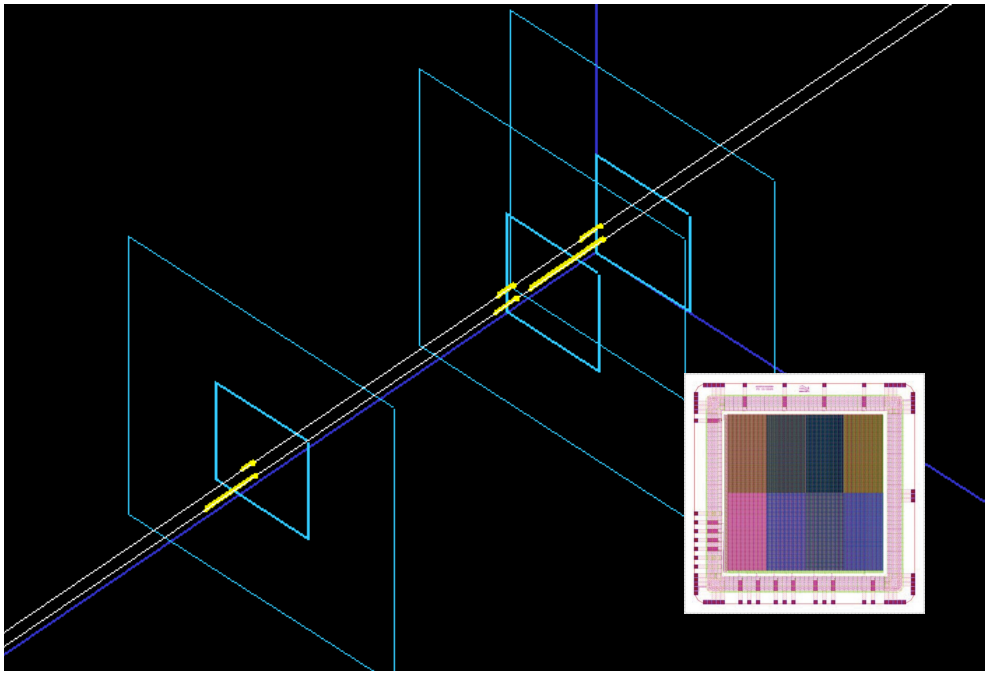
and the SOIPIX Collaboration



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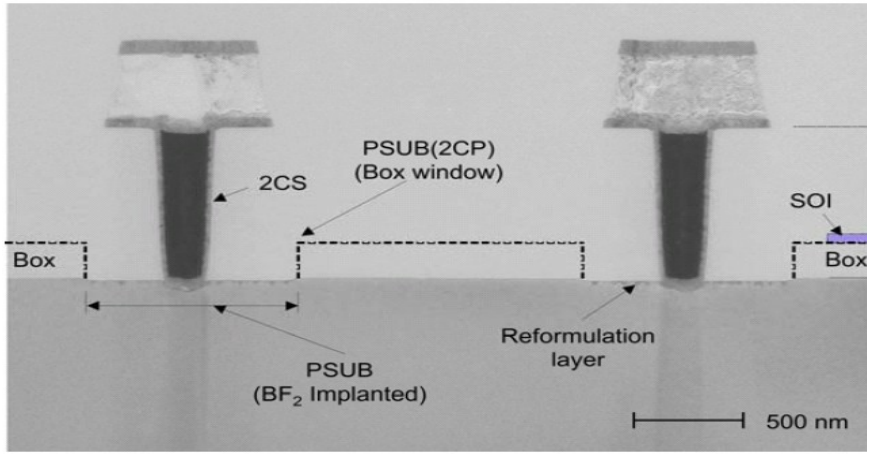
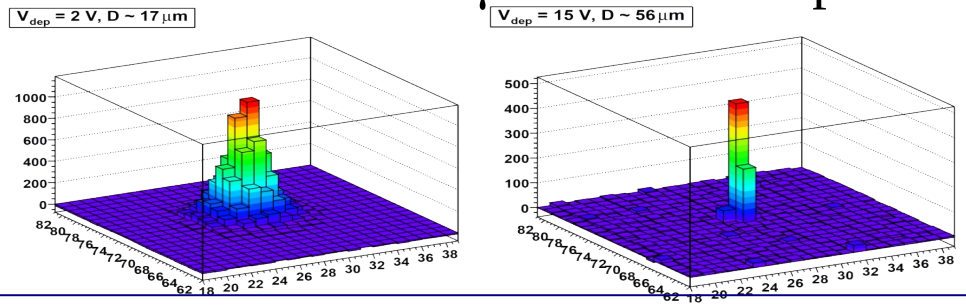
Monolithic SOI Pixel Sensors

Silicon-On-Insulator technology isolates CMOS from high-res charge collection volume offering full CMOS capabilities, low junction capacitance,potentially radiation tolerant: KEK-OKI offer 0.2µm FD-SOI process with vias through BOX to contact high-res substrate:

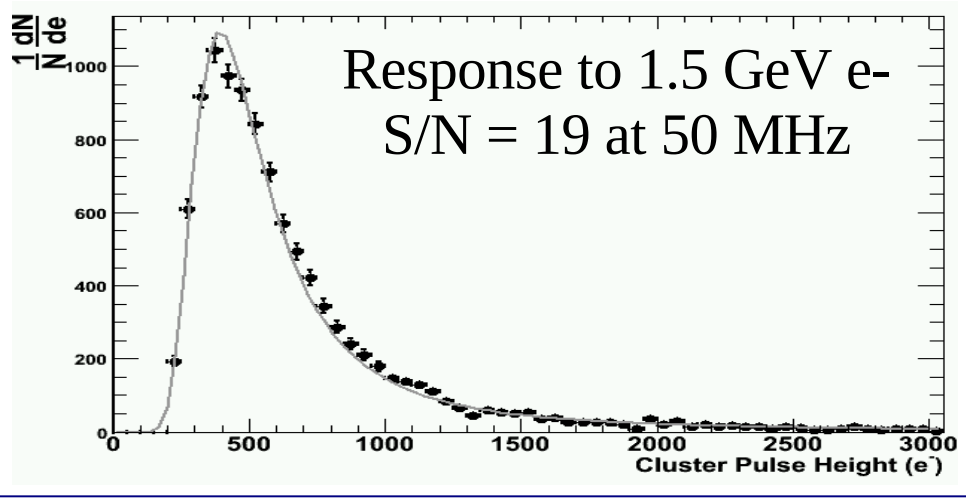


Thick fully depleted substrate gives large collected charge, faster collection time and small charge spread compared to conventional CMOS APS on low-res epi:

Response to 850nm laser on back-illuminated 50µm-thick SOI pixels

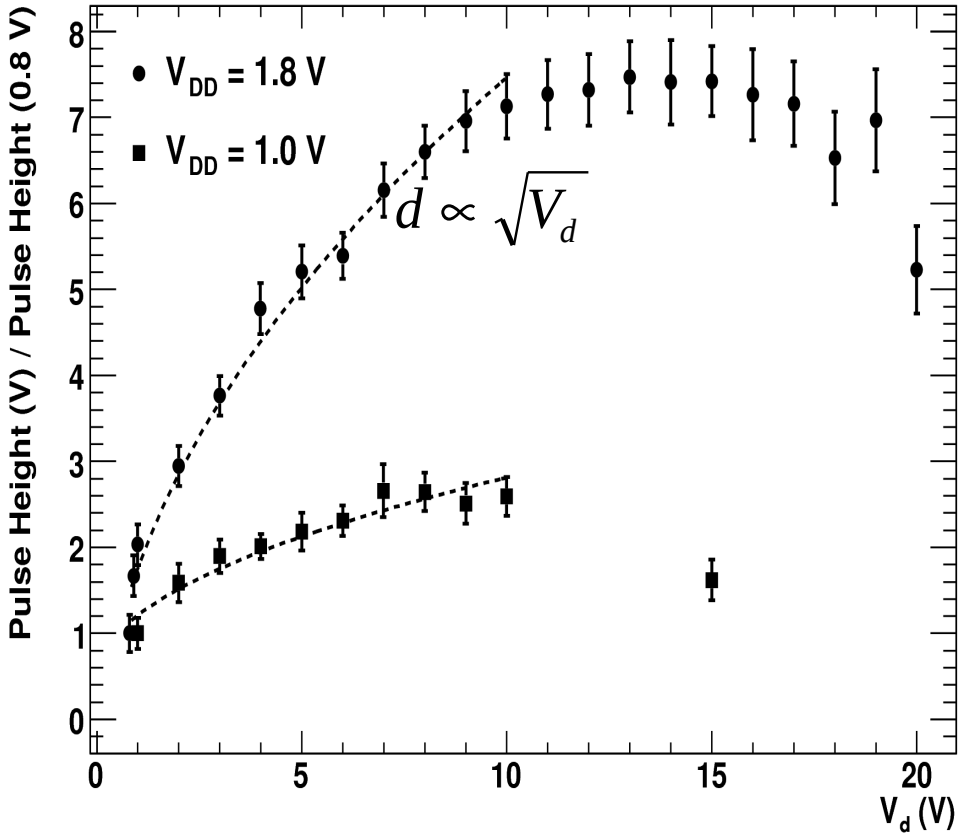


Results of first pixel detector test structures in OKI SOI technology encouraging but two main issues emerged: transistor back-gating and charge trapped in thick BOX

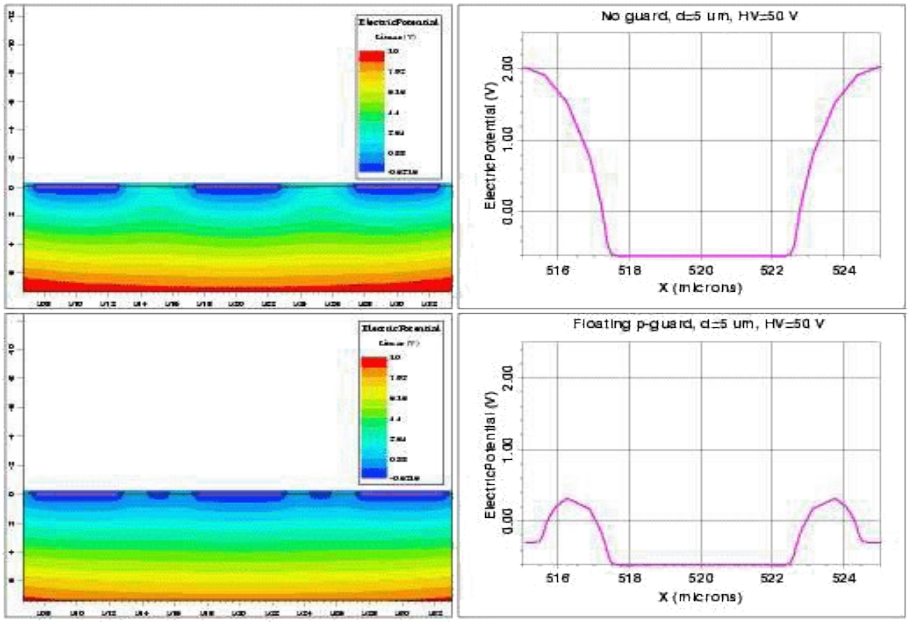


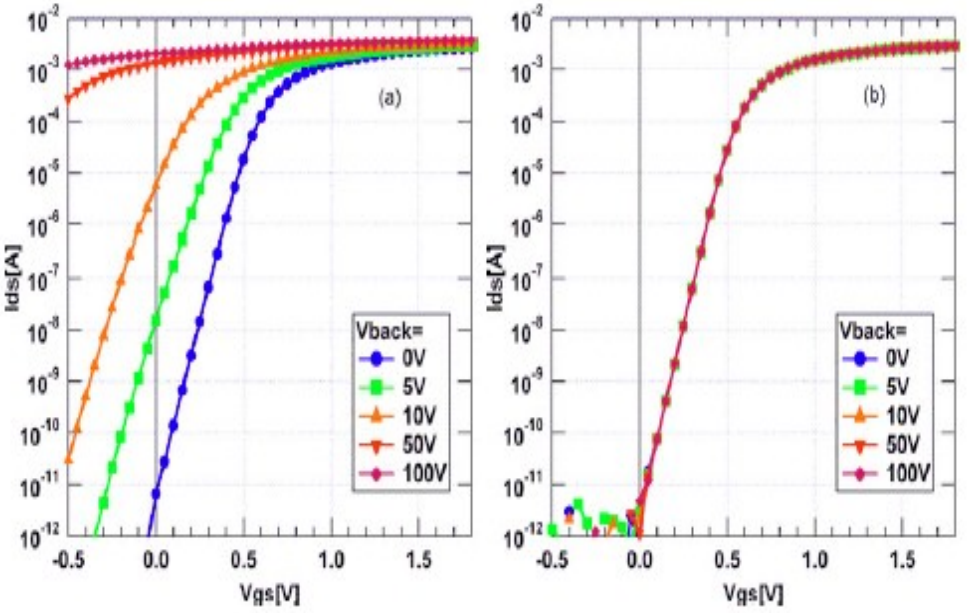
Transistor back-gating

Substrate potential acts as back-gate shifting transistor threshold and increasing leakage current:



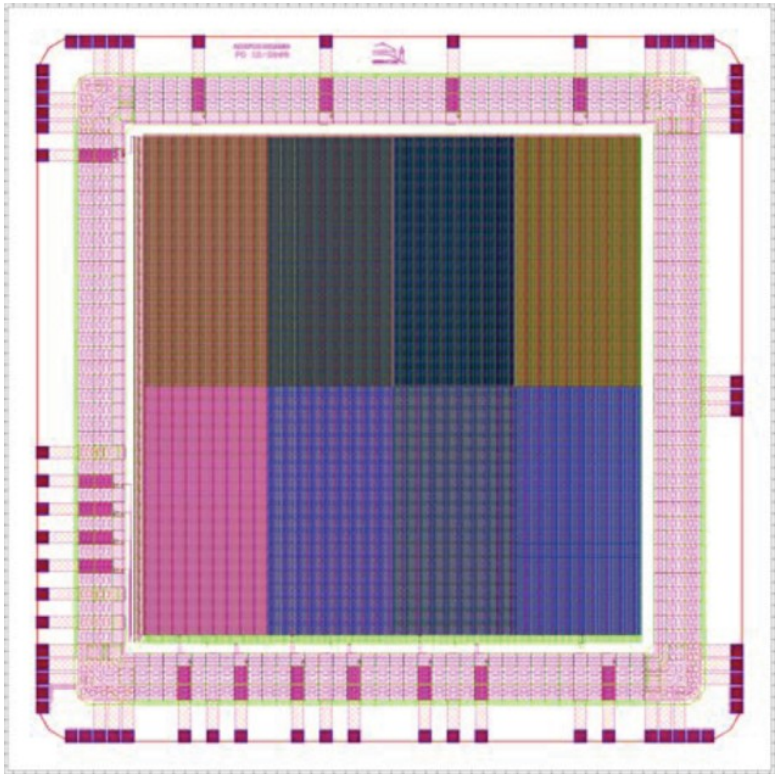
- Floating p-type guard-ring around pixel
- Buried p-well
- SOI-3D: vertical integration of r/o electronics





Arai et al., to appear on NIM A (2010)

SOImager2 Pixel Sensor

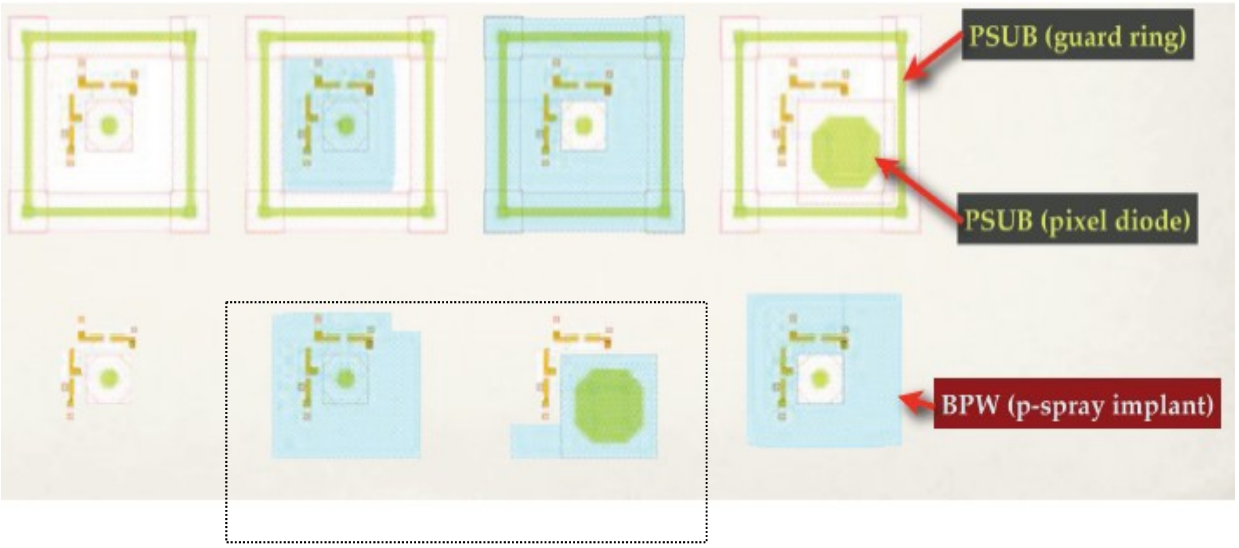


Test chip to optimise pixel cell for charge collection and back-gating effect mitigation;

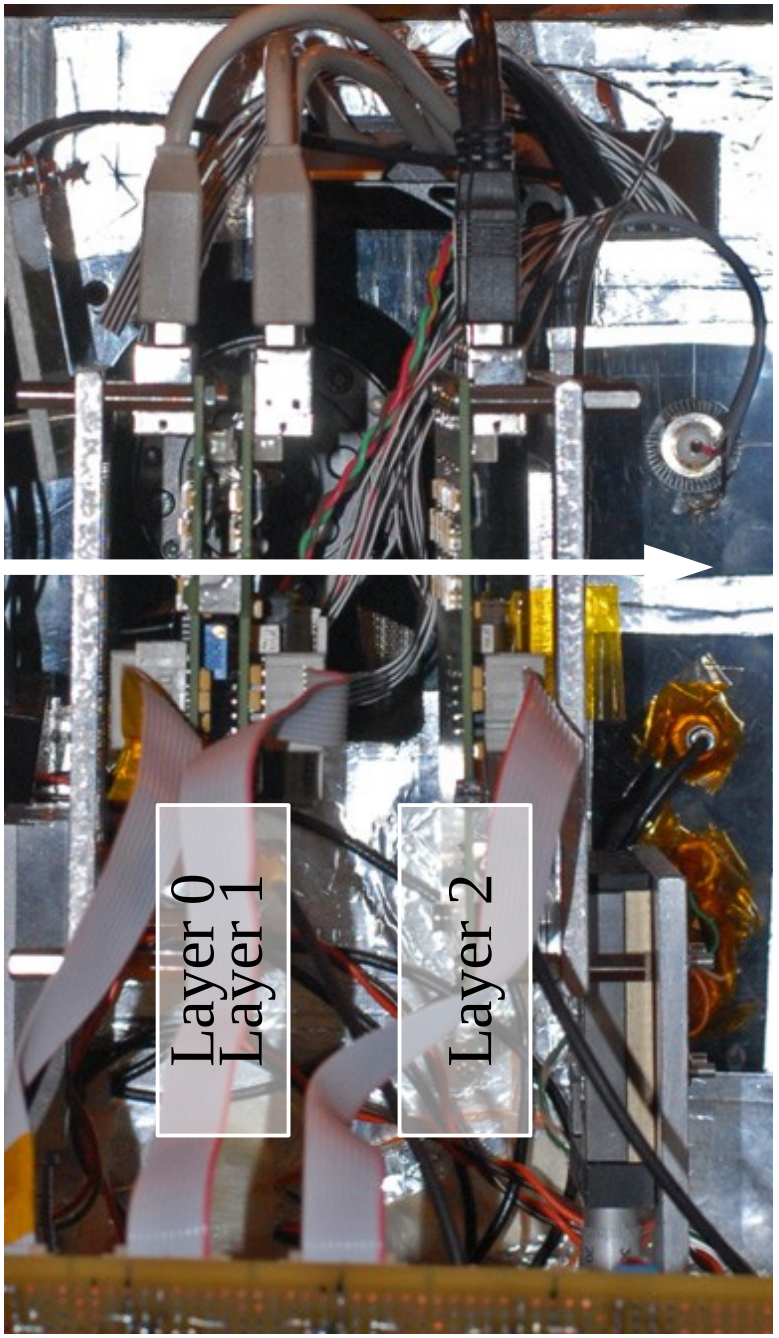
Study performance of various pixel designs with guard ring and light-doped p implant (BPW);

256x256 (3T) pixels arrayed on a 13.75 µm pitch;

Designed at LBNL and produced at OKI in 0.2µm FD-SOI process in Spring 2010 as part of US-Japan collaboration on SOI pixel R&D.



CERN Beam Test Setup



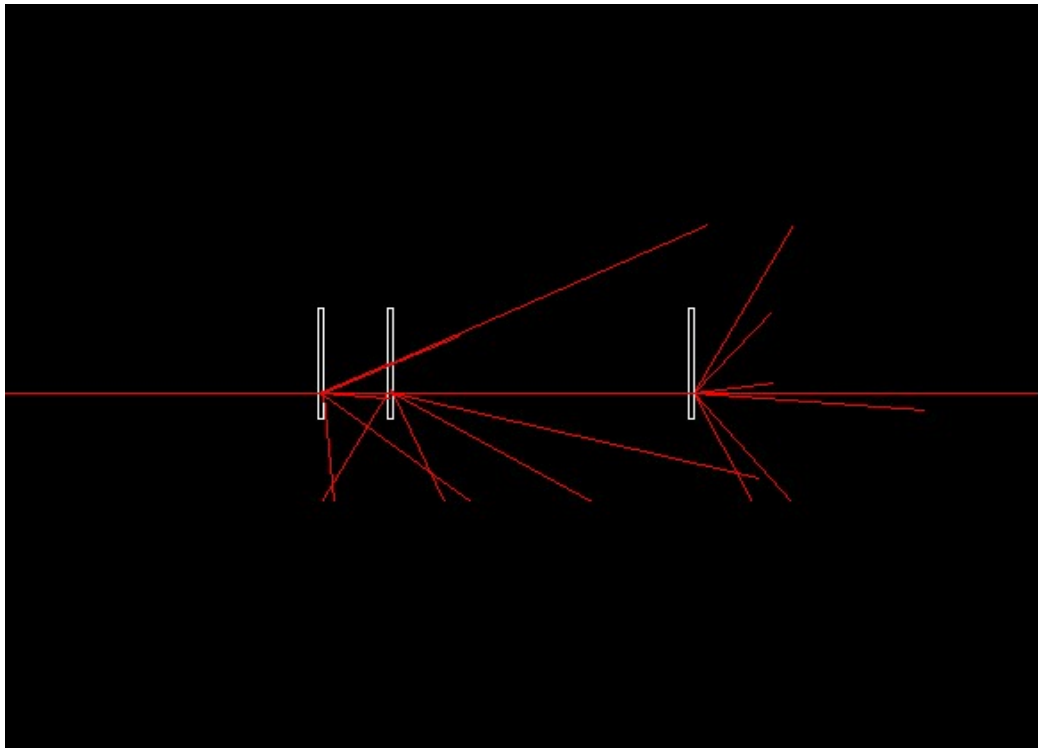
Beam test at SPS on H4 with 200 GeV π- at beginning of September 2010;

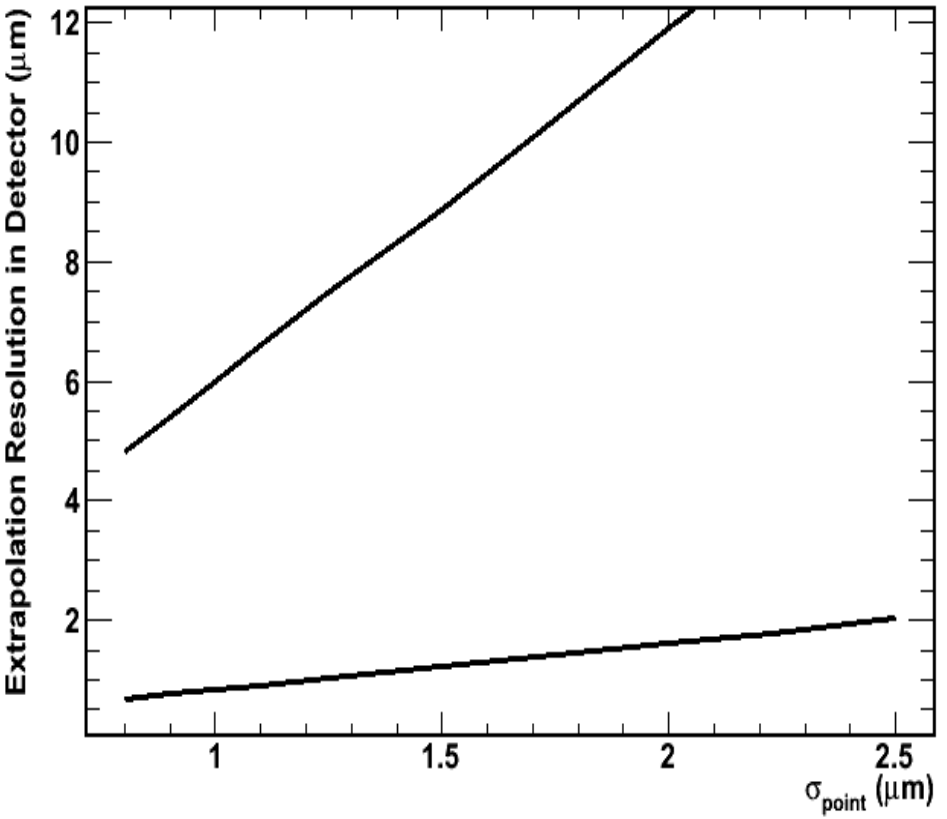
Small telescope made of three planes of SOImager2 to study charge collection, single point resolution and efficiency as function of depletion voltage, one plane mounted on motorised rotation stage to study charge collection for inclined tracks;

Data acquisition performed using custom ADC+FPGA board, online cluster search using ROOT-based COOL program, tuple output converted to lcio, offline analysis performed with custom processors in Marlin;

Readout at 12.5 MHz corresponding to ~1500 frames/spill, operation at constant temperature (20+/-1)^{o}

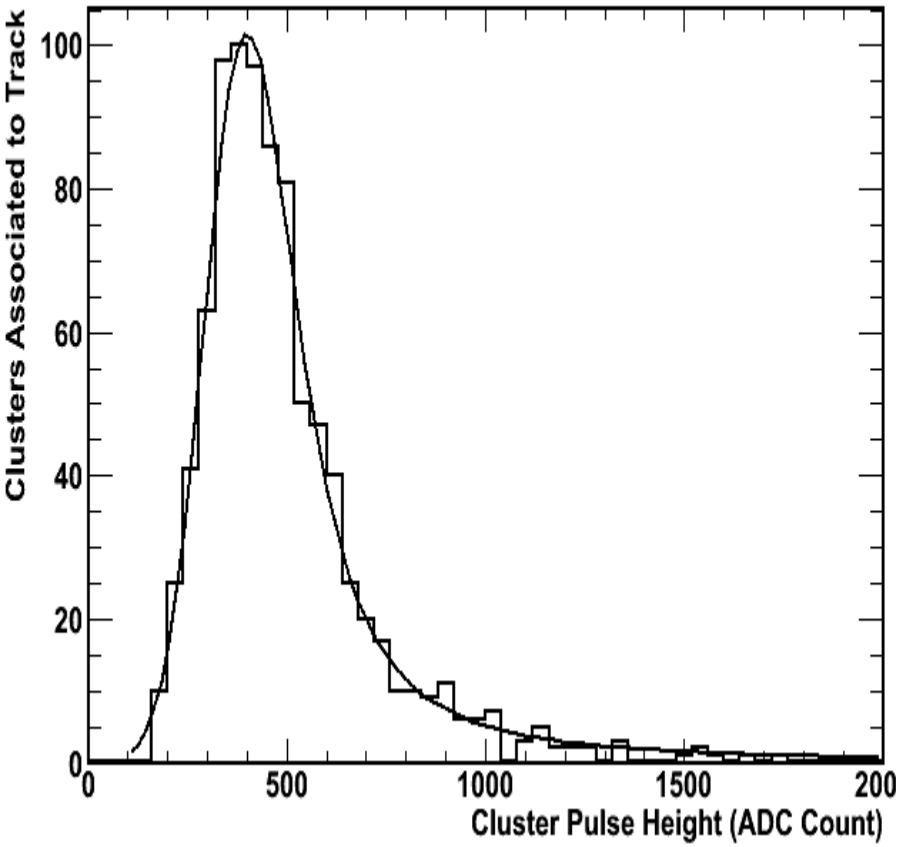
Beam Test Setup G4 Simulation

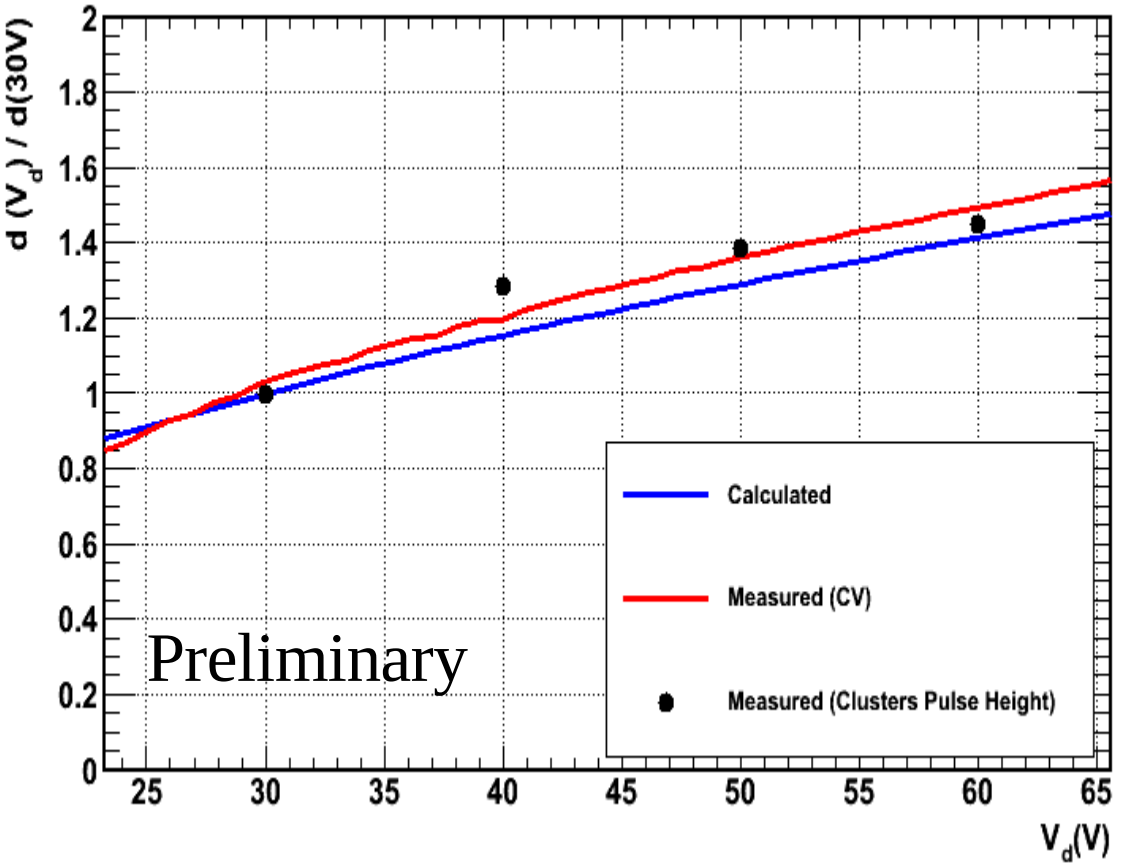




Generate lcio files of simulated SimTrackerHits and MCParticles to test reconstruction and extrapolation resolution;

Beam Test Results:
Charge Collection and Depletion Voltage

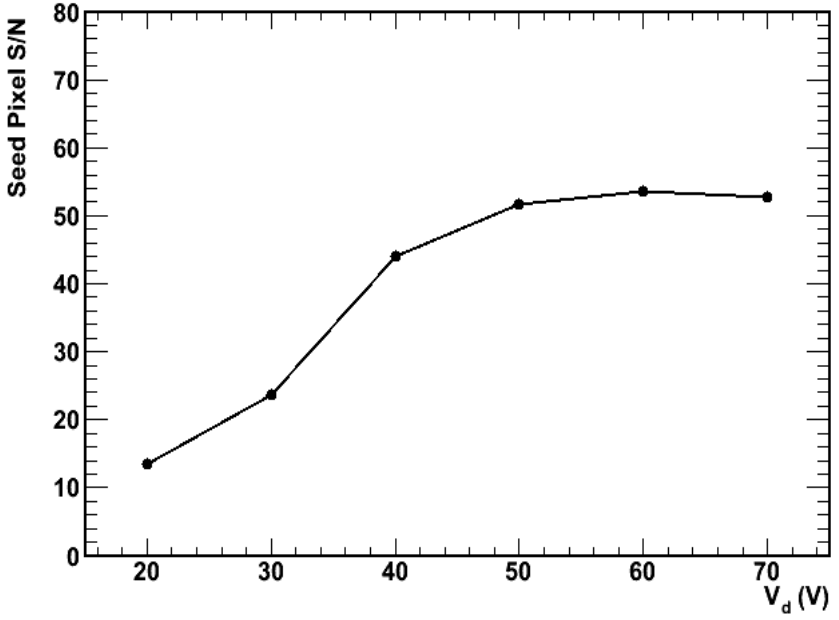


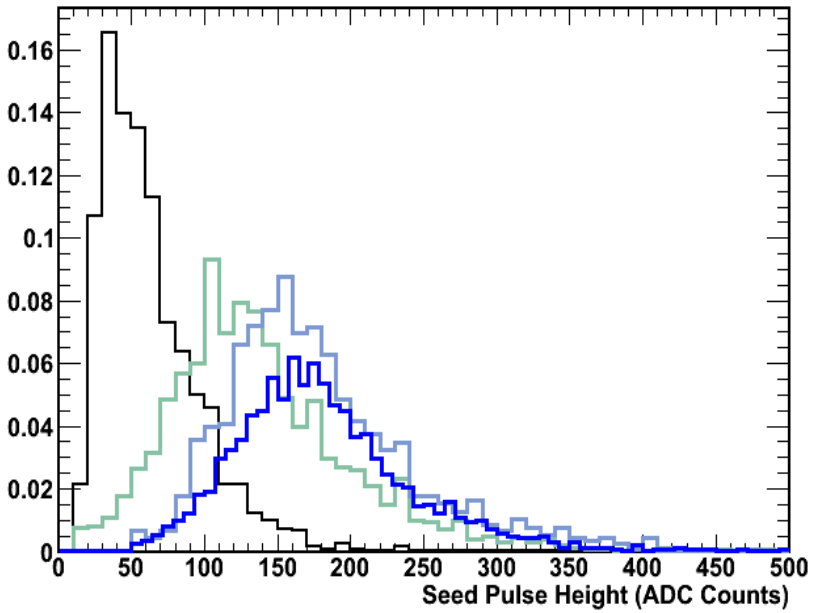


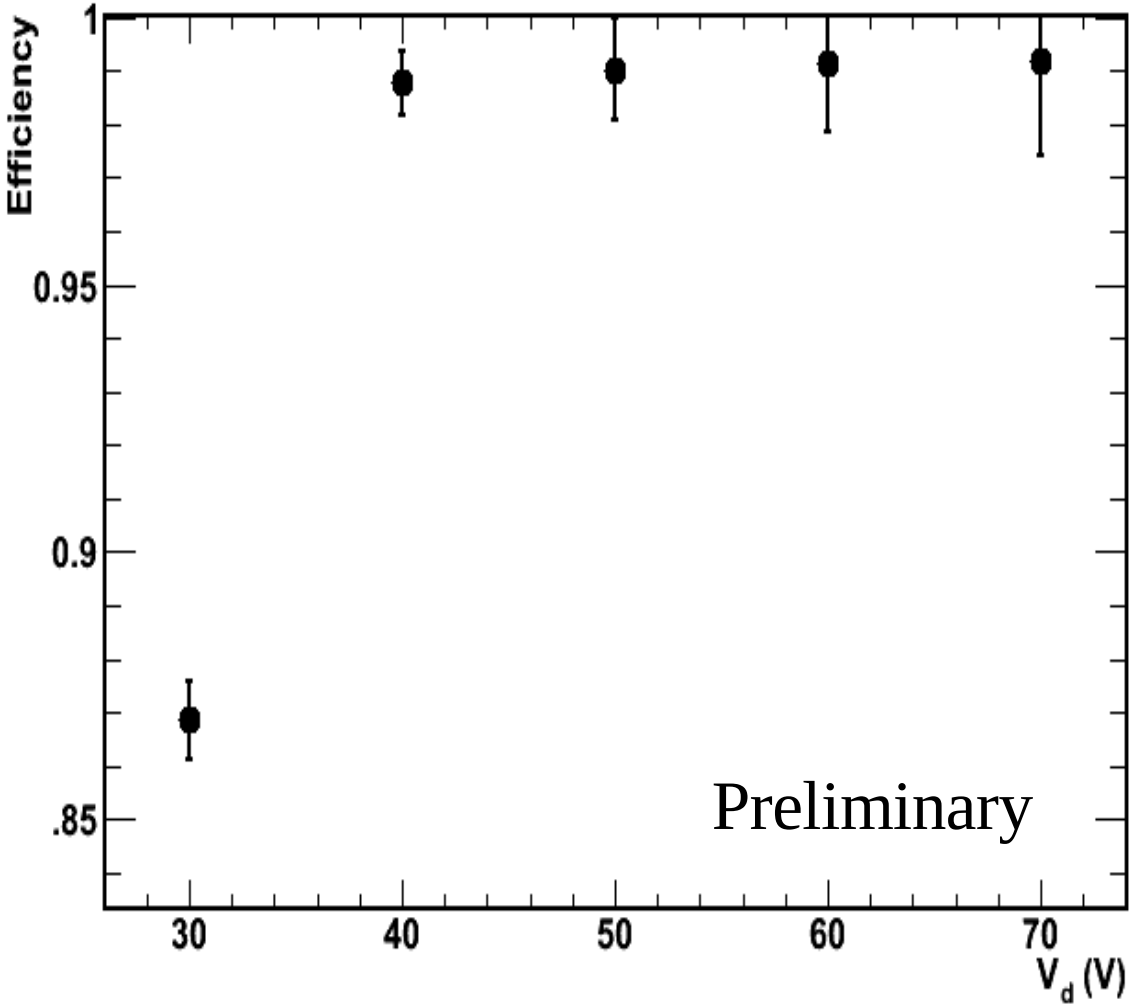
Cluster reconstruction using double S/N threshold (seed and neighbouring pixels) (seed S/N > 10 and N_{pixels} > 1)

Calculated depletion from nominal resistivity (200 Ω cm);
Measured (CV) from CV measurement of the substrate using pixel guard ring as electrode
Measured (PH) from signal in cluster pulse height for hits associated to reconstructed track

Beam Test results:
Sensor Efficiency and Depletion Voltage

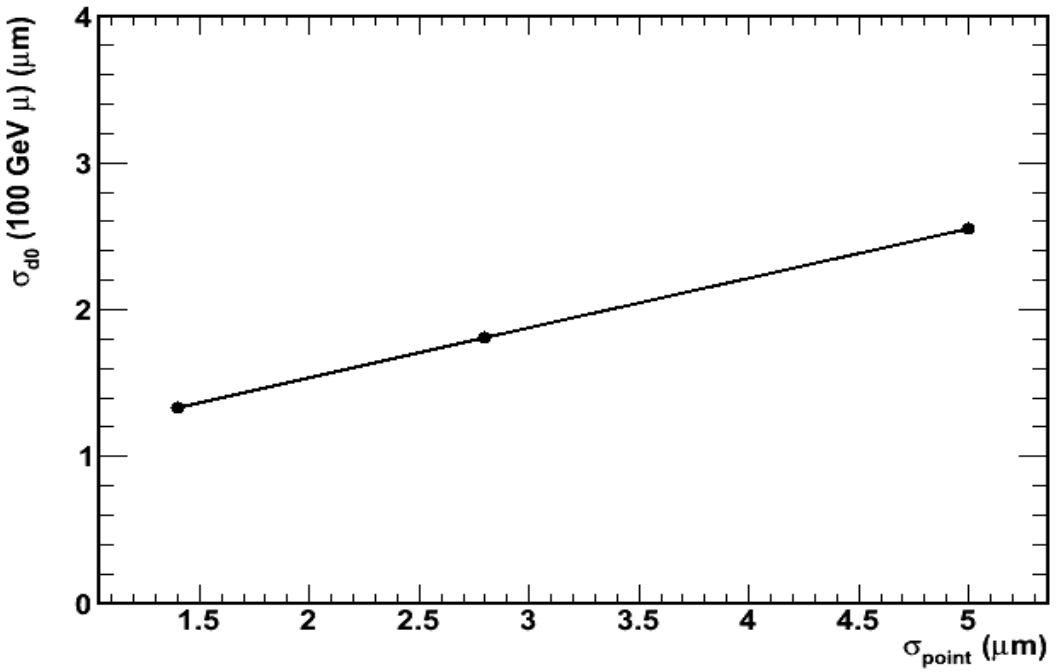




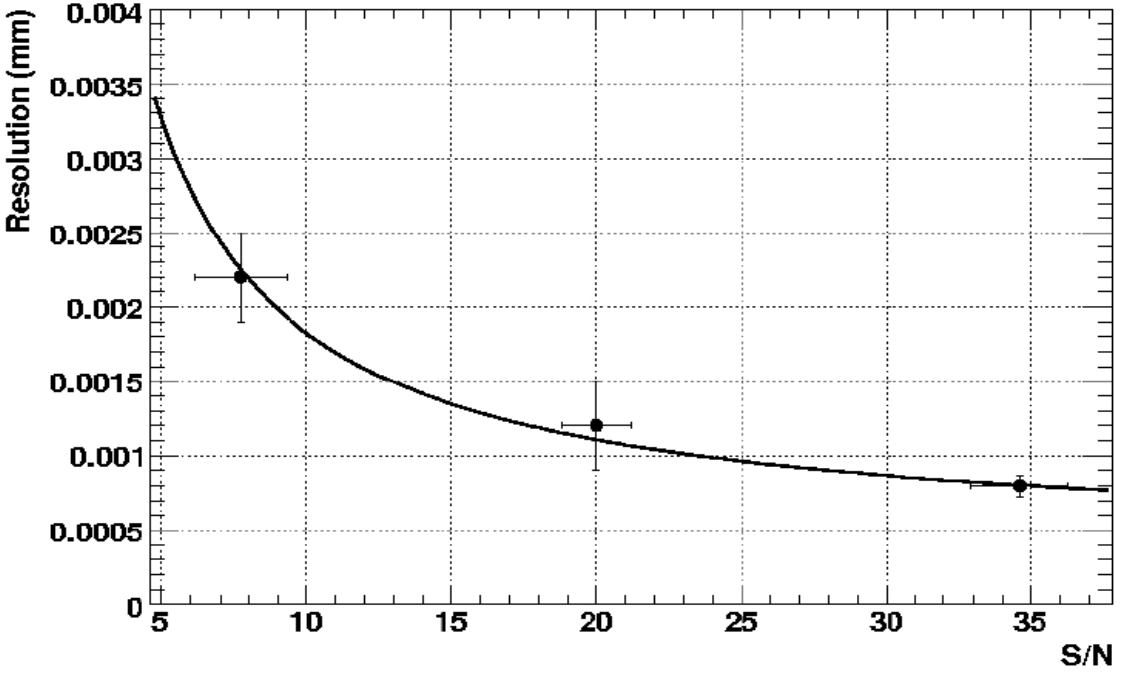


Compute hit efficiency from probability to find an hit on one layer for extrapolated tracks reconstructed on other two layers.

Single Point Resolution

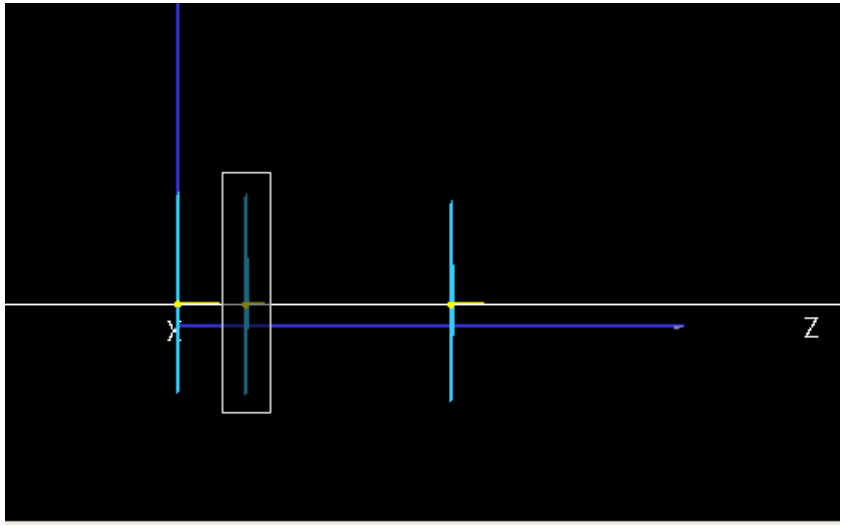


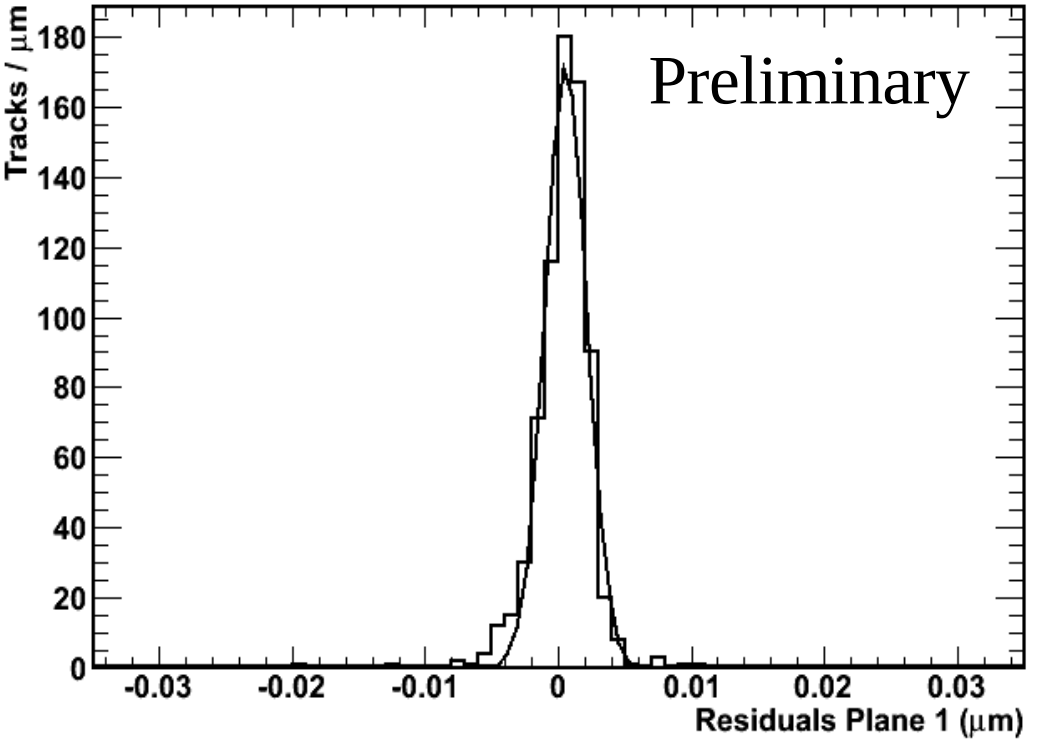
Scaling of asymptotic R-Φ impact parameter resolution (a) with single point resolution for a three double-layered barrel VXD in the CLIC geometry (100 GeV single muons with Mokka+MarlinReco);

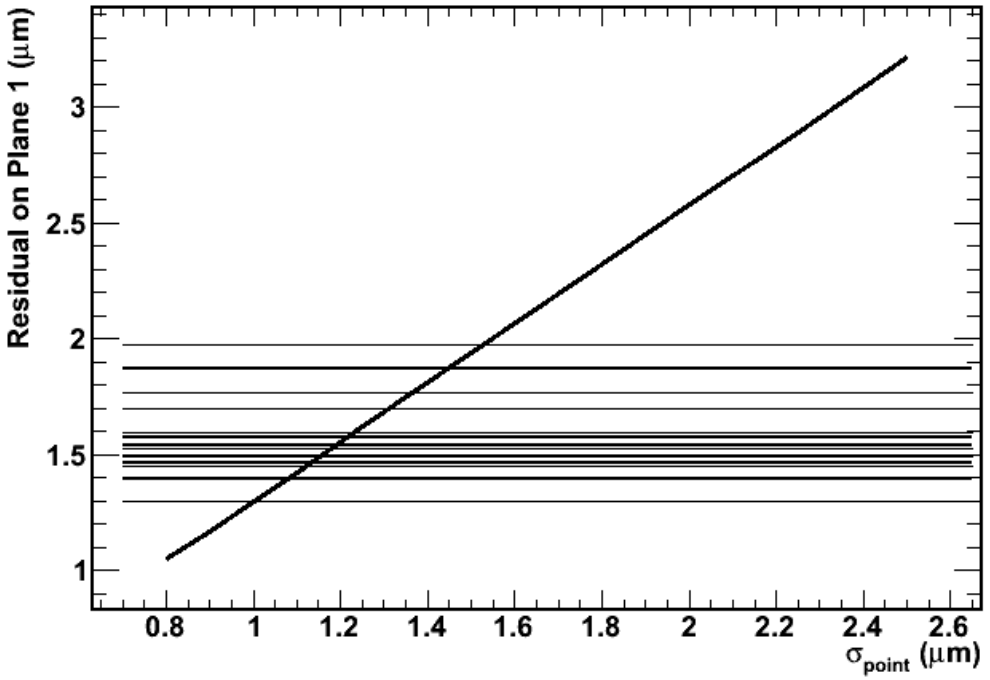


First estimate single point resolution by performing pixel scans on SOImager chip with 1060 nm laser focused to ~5 μm spot at various intensities to simulate m.i.p. charge deposition;

Beam Test Results:
Single Point Resolution

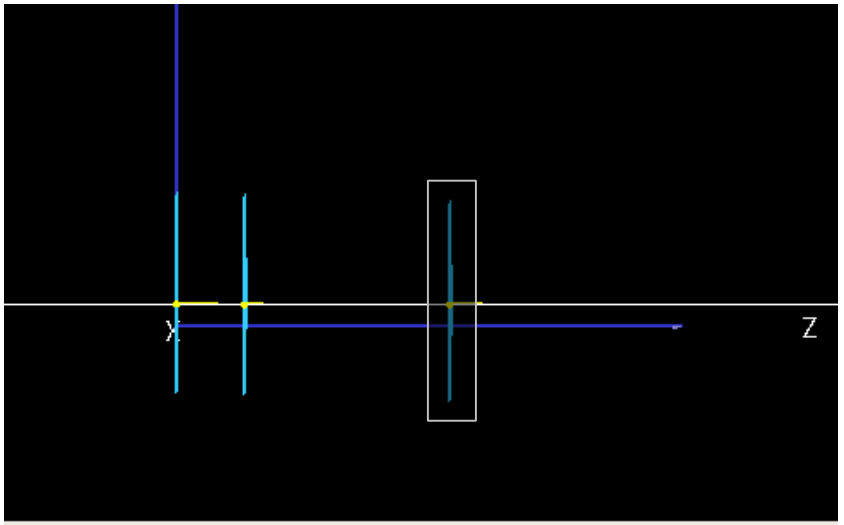


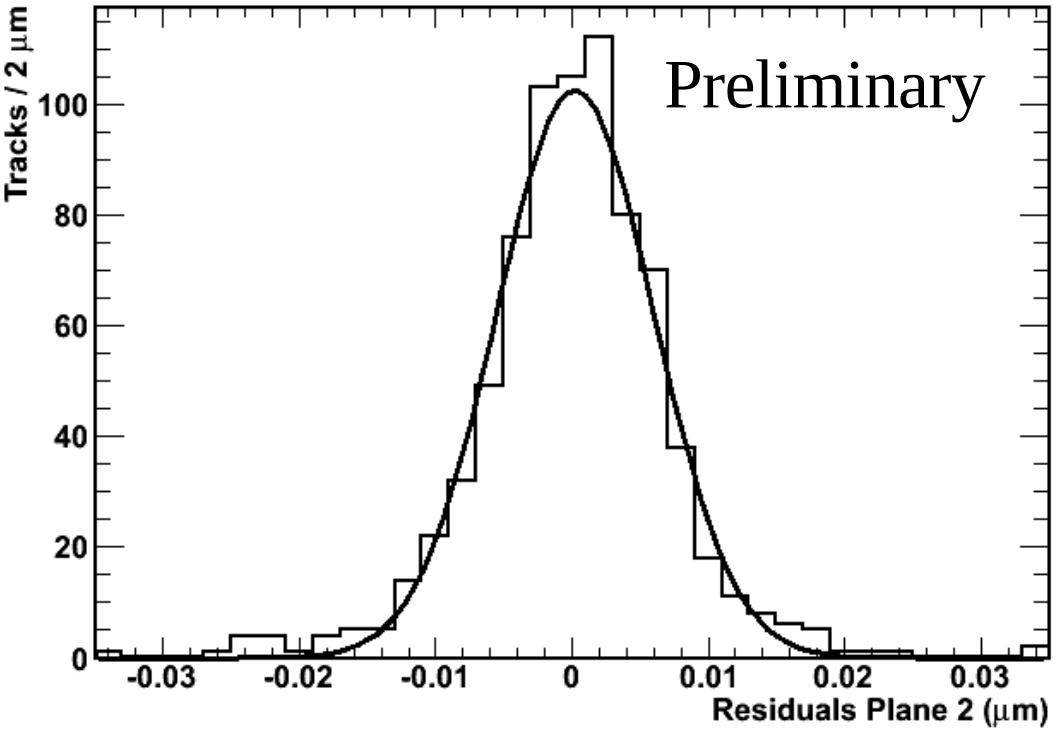


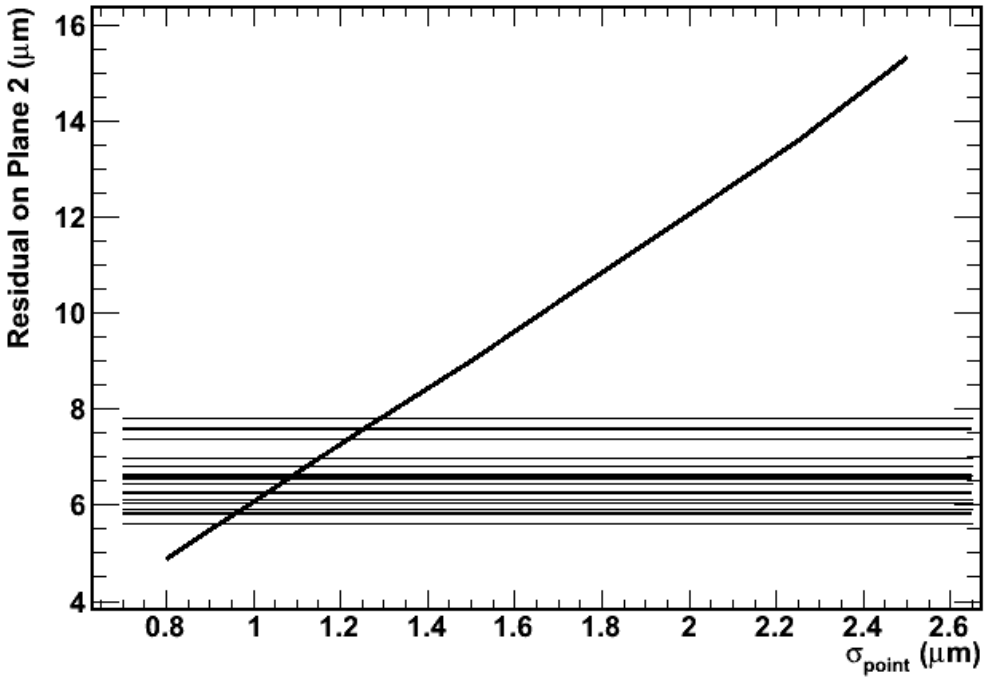


V_d (V)	σ_{point} (μm)
30	1.45+/-0.06
50-70	1.18+/-0.04

Beam Test Results:
Single Point Resolution

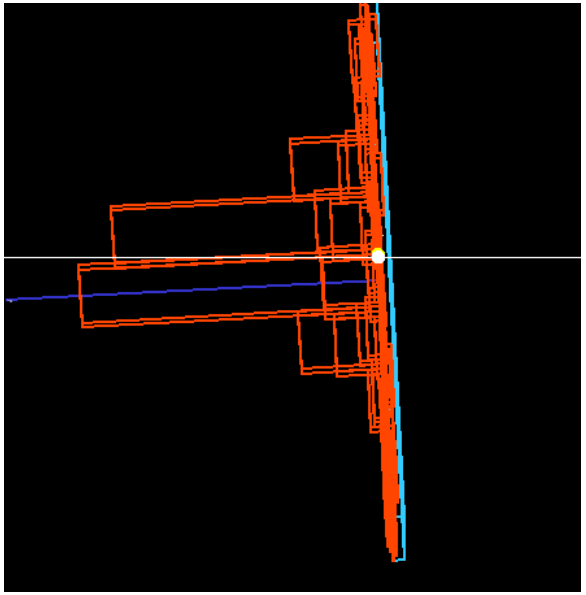


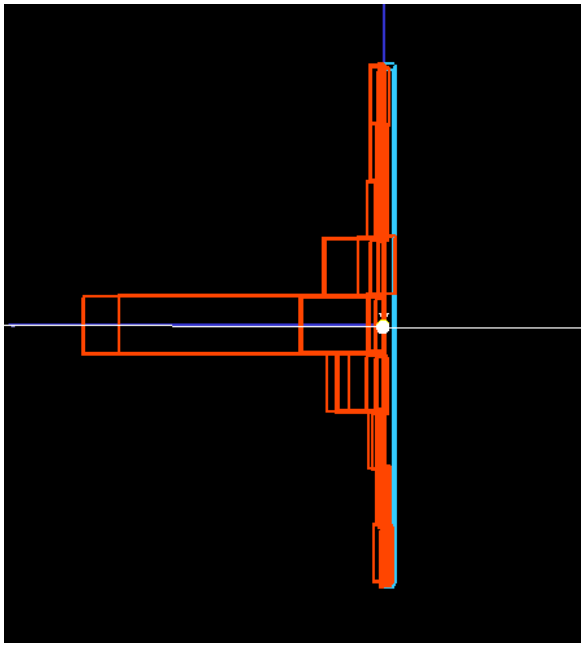


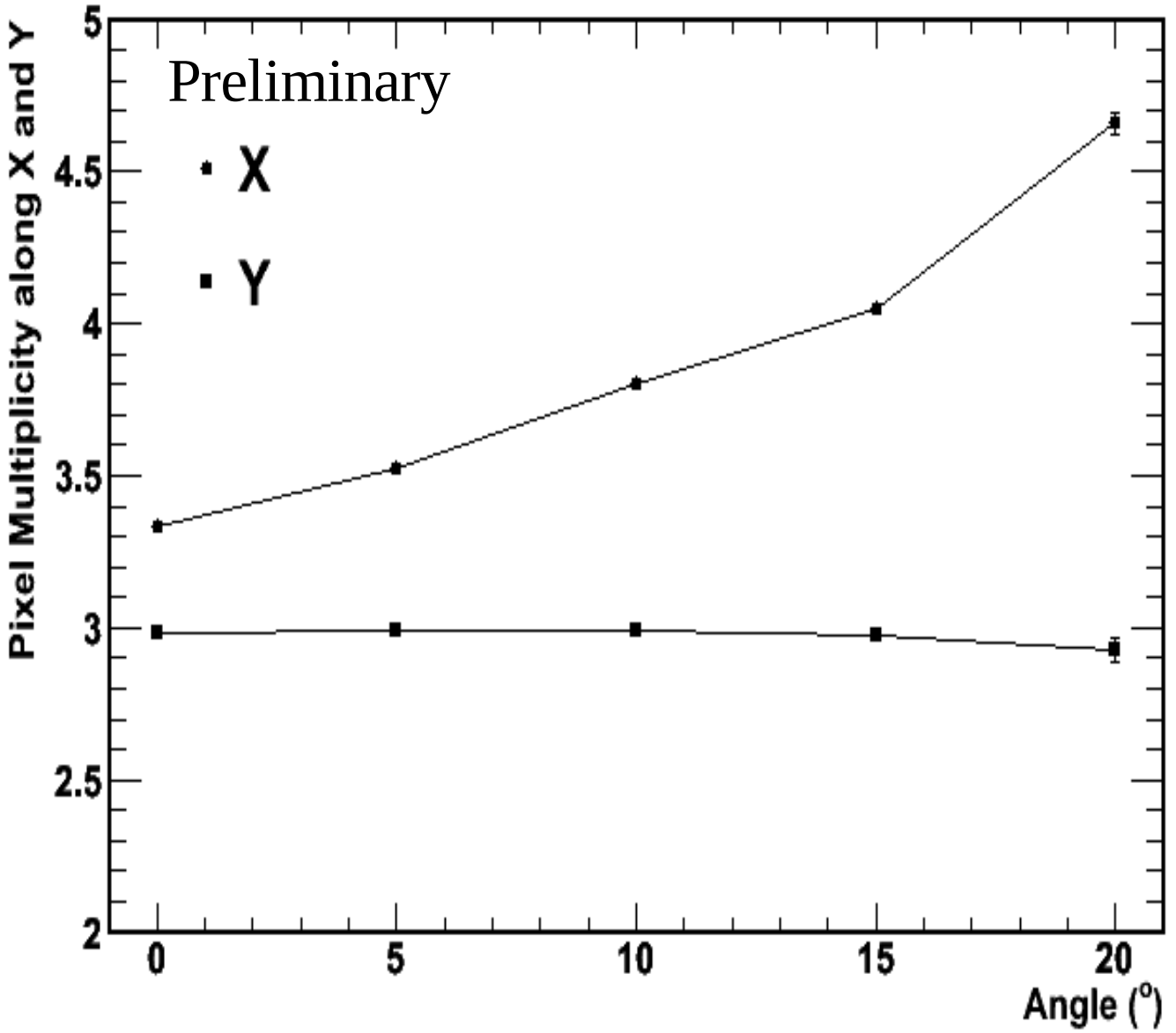


V_d (V)	σ_{point} (μm)
30	1.26+/-0.05
50-70	1.06+/-0.04

Beam Test Results:
Cluster Size for Inclined Tracks







Conclusions

The fourth in the series of test chips in OKI SOI technology has been designed at LBNL and tested by a collaboration including LBNL, INFN, Padova and UCSC;

Several pixel cell designs adopting both guard ring and buried-p-well have been implemented and evaluated;

Three sensors installed on the SPS H4 beam line and tested with 200 GeV π^- to study charge collection, efficiency and resolution vs. depletion voltage;

Efficiency > 98% and single point resolution ~1.2 μm obtained for $40 < V_d < 70$ V

Study of charge collected on pixels as a function of point of impact of particles for straight and inclined tracks in progress;

Encouraging results motivate next steps towards implementing in-pixel and on-chip functionality;

Role, advantanges and limitations of SOI technology compared to CMOS on high-res sensitive volume and 3D vertical integration sensors to be assessed as part of this R&D.