Particle pixel detectors in high-voltage CMOS technology

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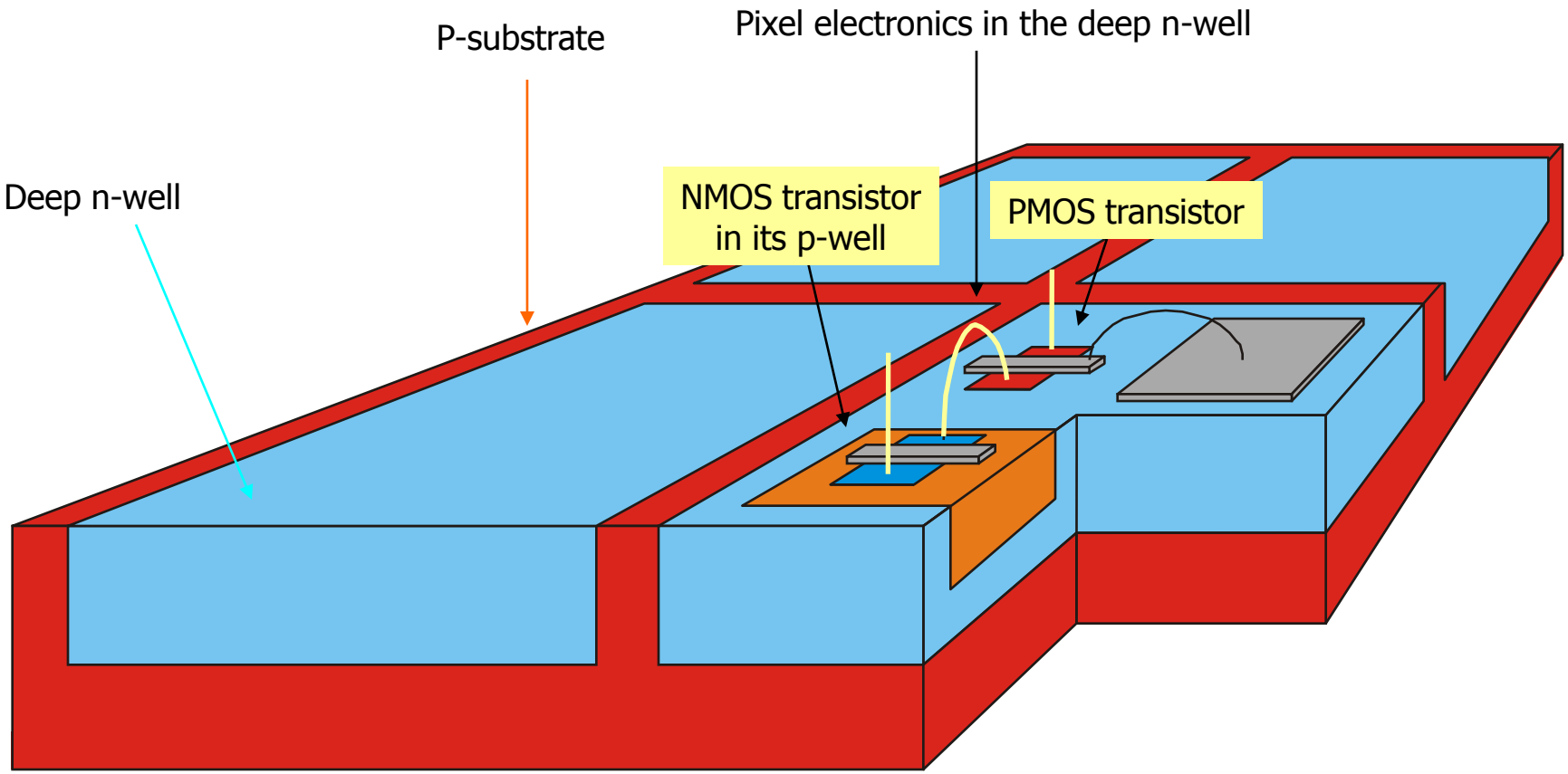
Pixel detector in HV CMOS technology

- Monolithic pixel sensor
- 100% fill-factor
- In-pixel CMOS signal processing
- Excellent SNR (seed 21 μm-pixel SNR for high energy betas > 80)
- Allows thinning below 50 μm without signal decrease
- Good timing properties (theoretically 40 ps signal collection time)
- Radiation hard (tested to 50 MRad (x-rays) and 10^{15} n_{eq} (protons))
- Not expensive (standard technology used, wafer run costs 98 k€)

The detecor stucture

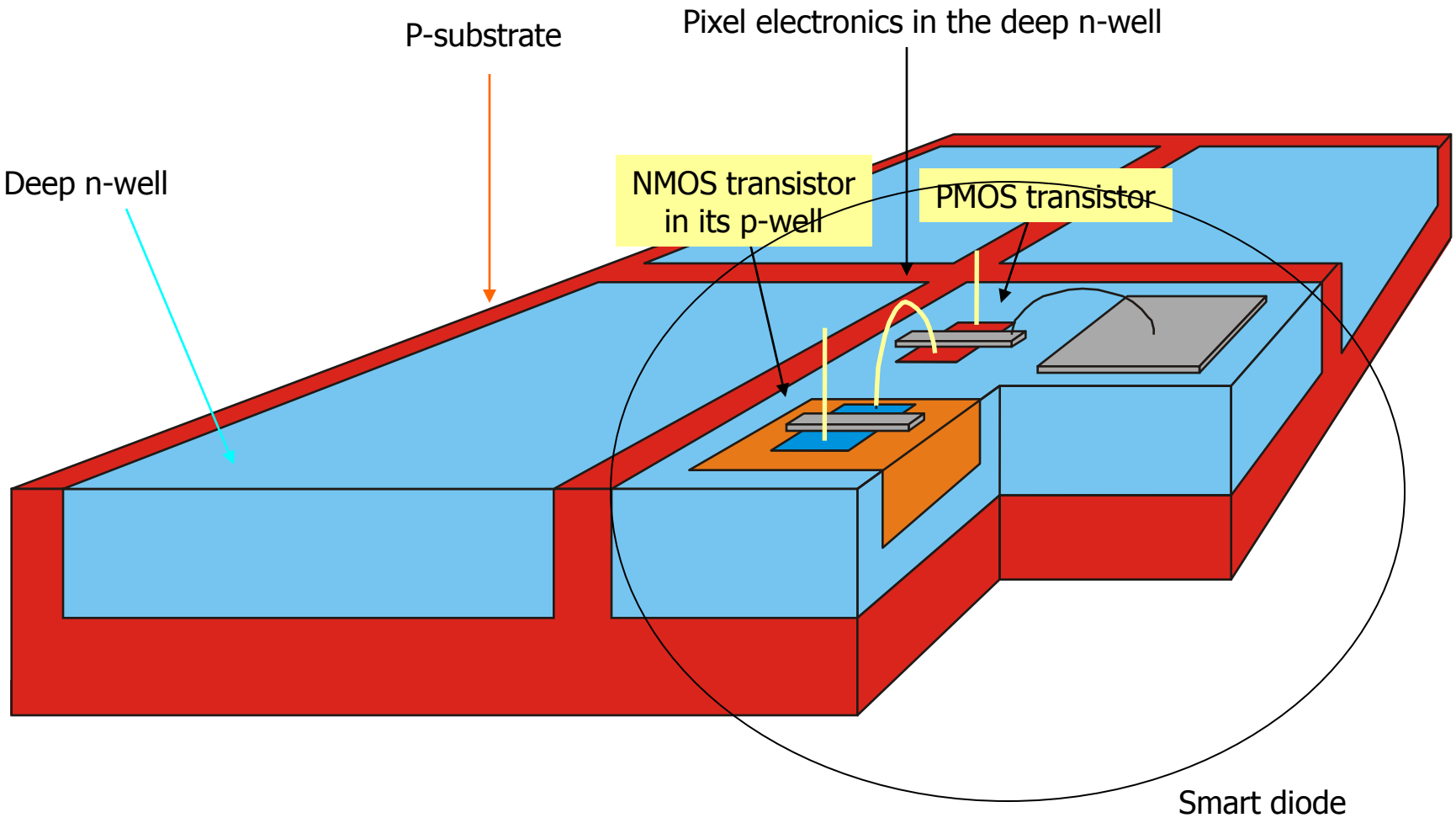
Based on twin-well structure



The CMOS signal processing electronics are placed inside the deep-n-well. PMOS are placed **directly inside n-well**, NMOS transistors are situated in their **p-wells** that are embedded in the n-well as well.

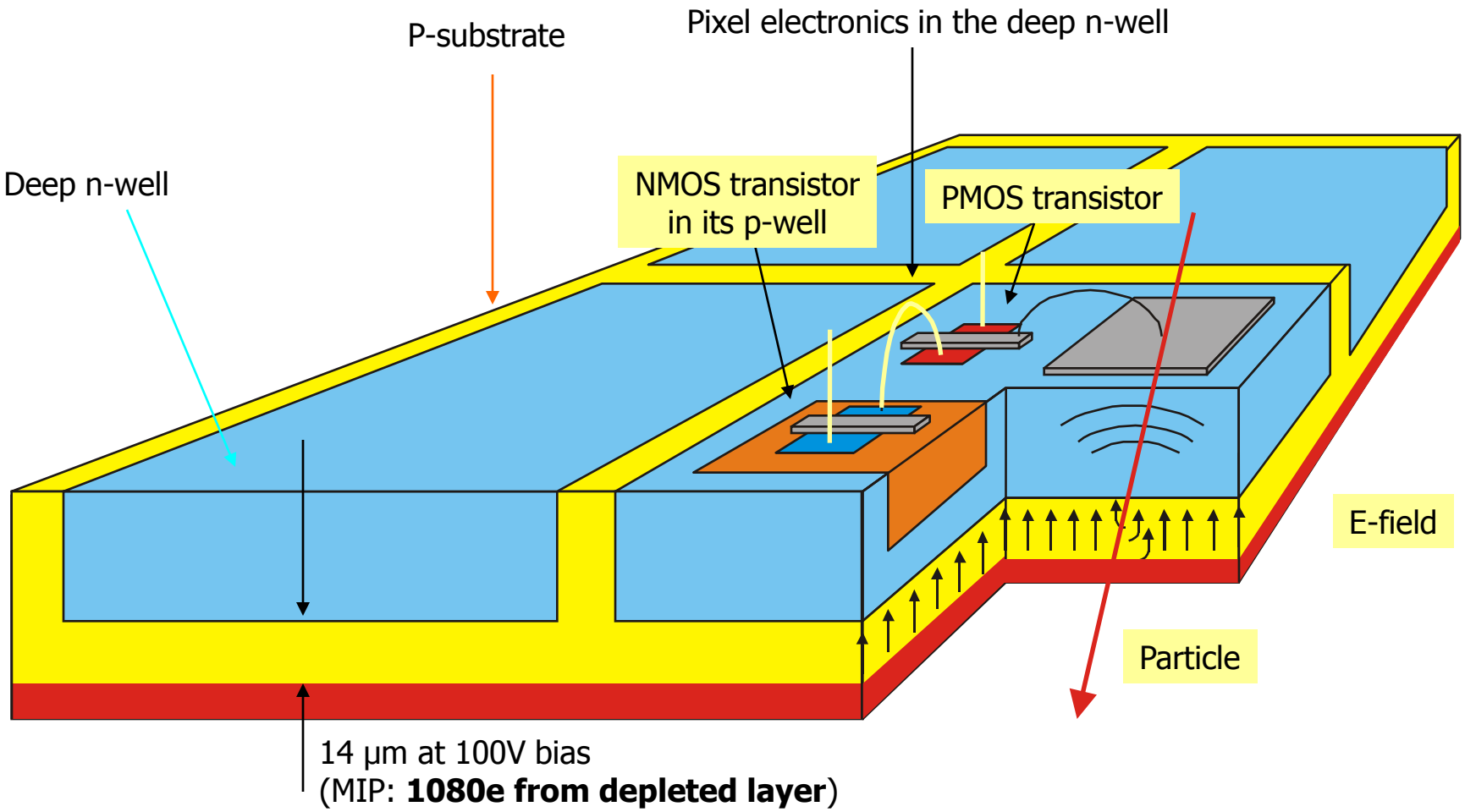
“Smart” diode array

Based on twin-well structure

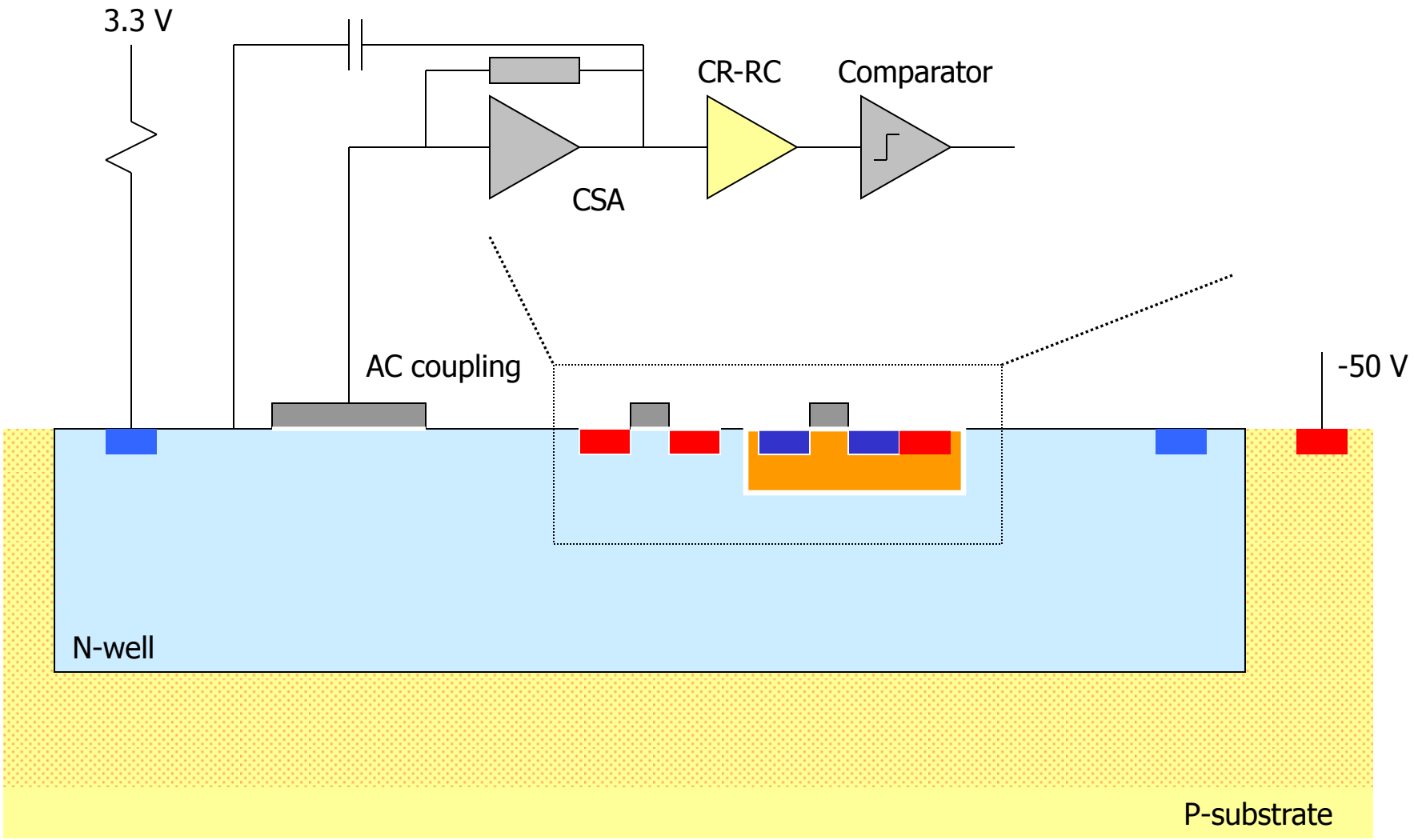


“Smart” diode array in HV CMOS technology

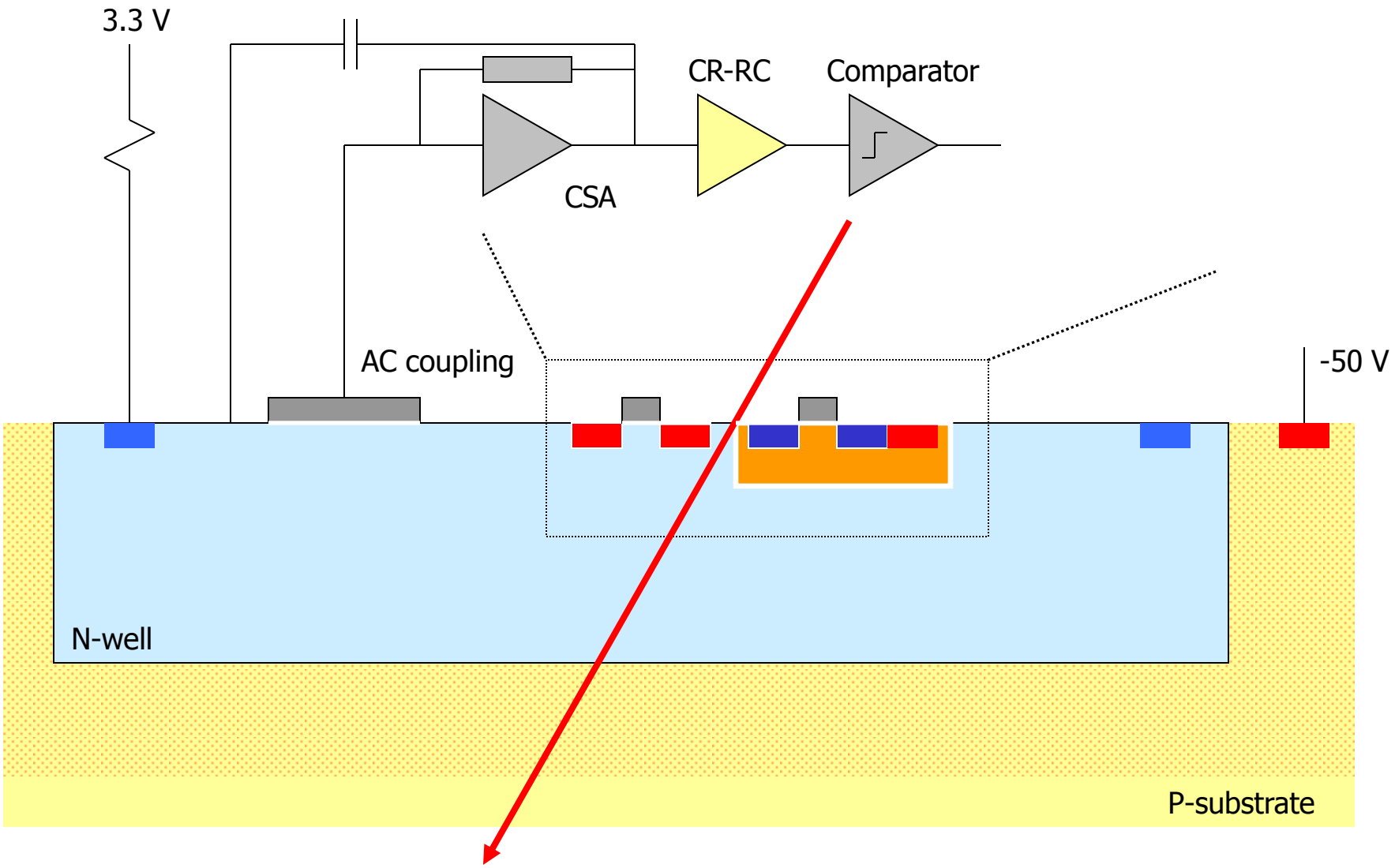
High voltage deep n-well used



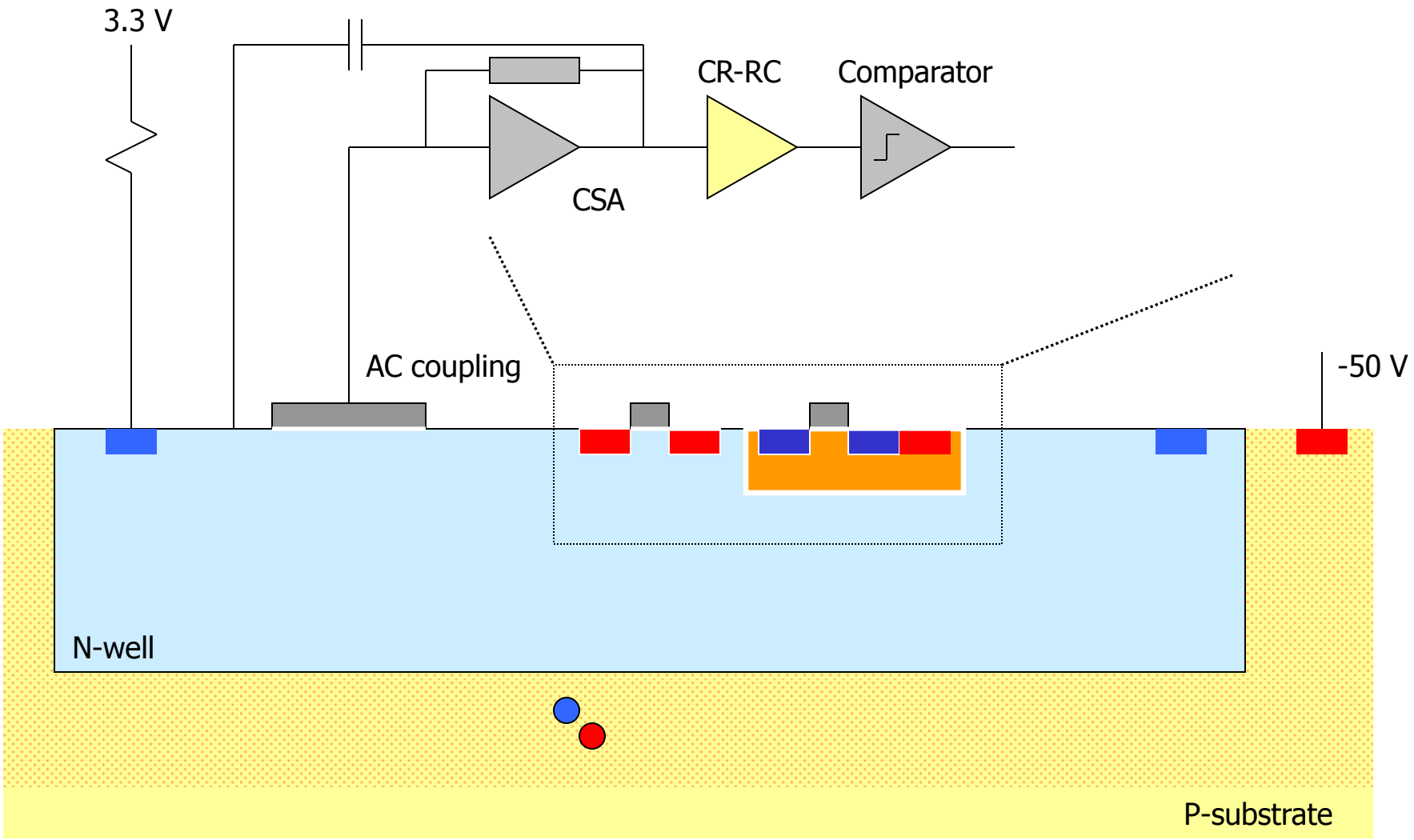
Signal detection



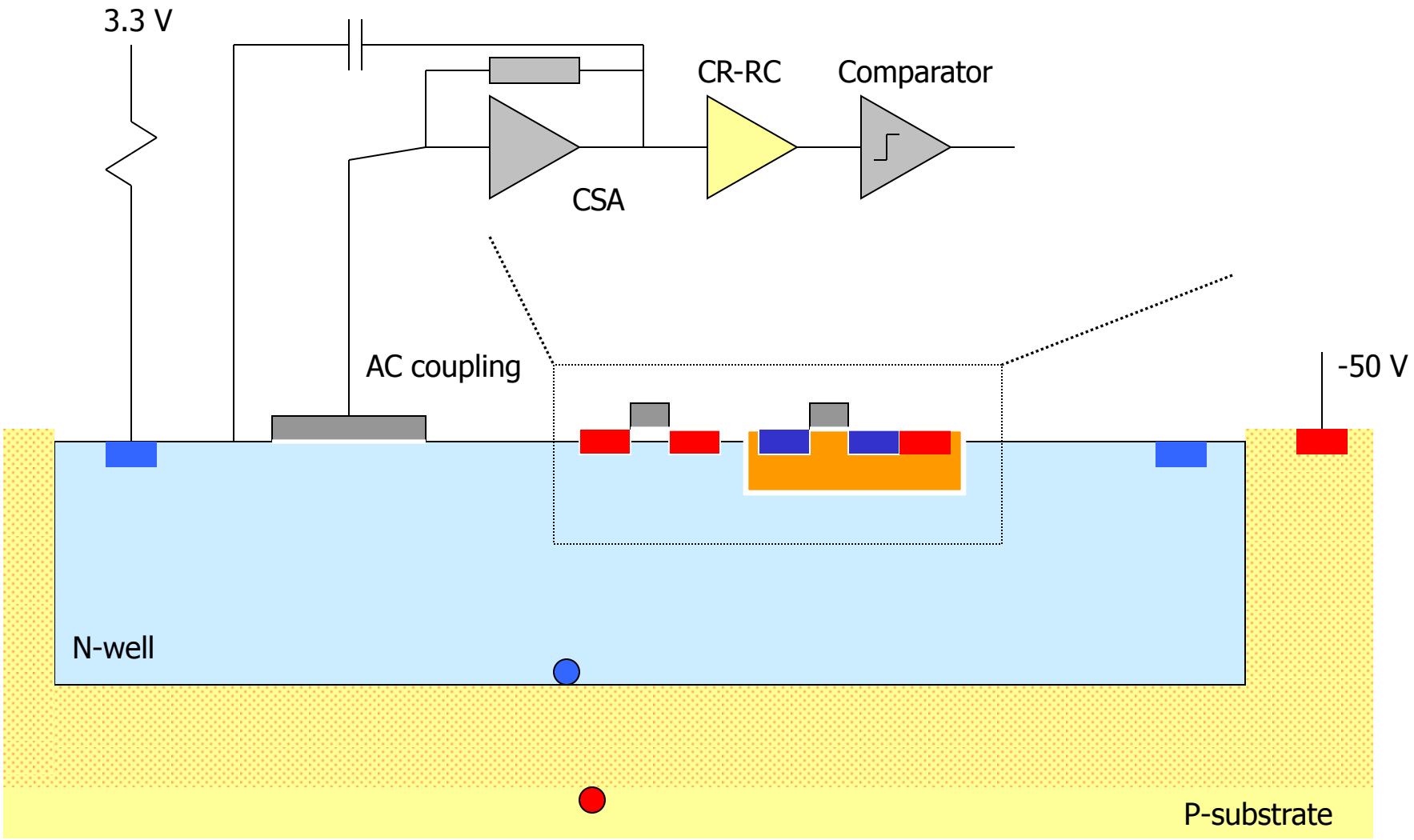
Signal detection



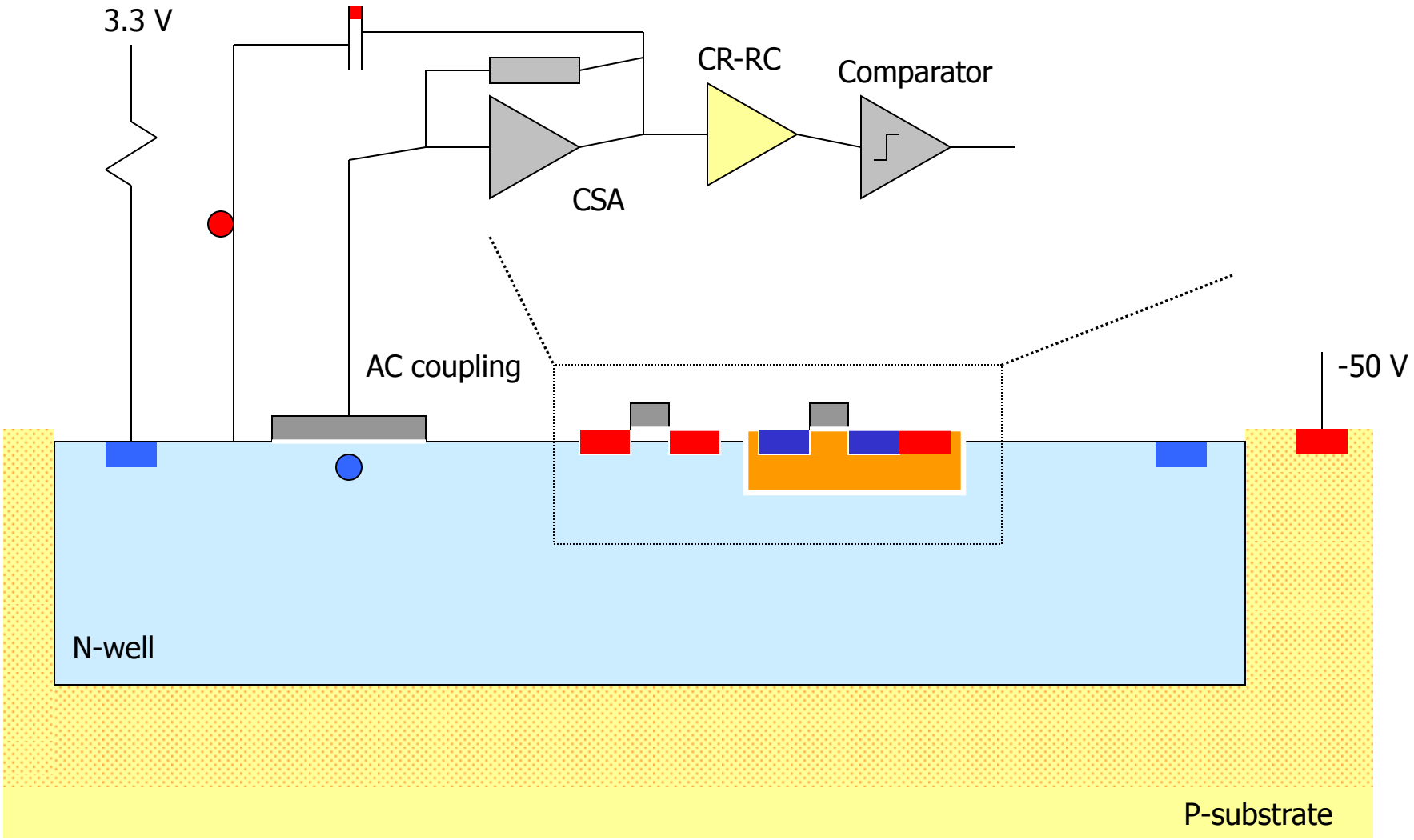
Signal detection



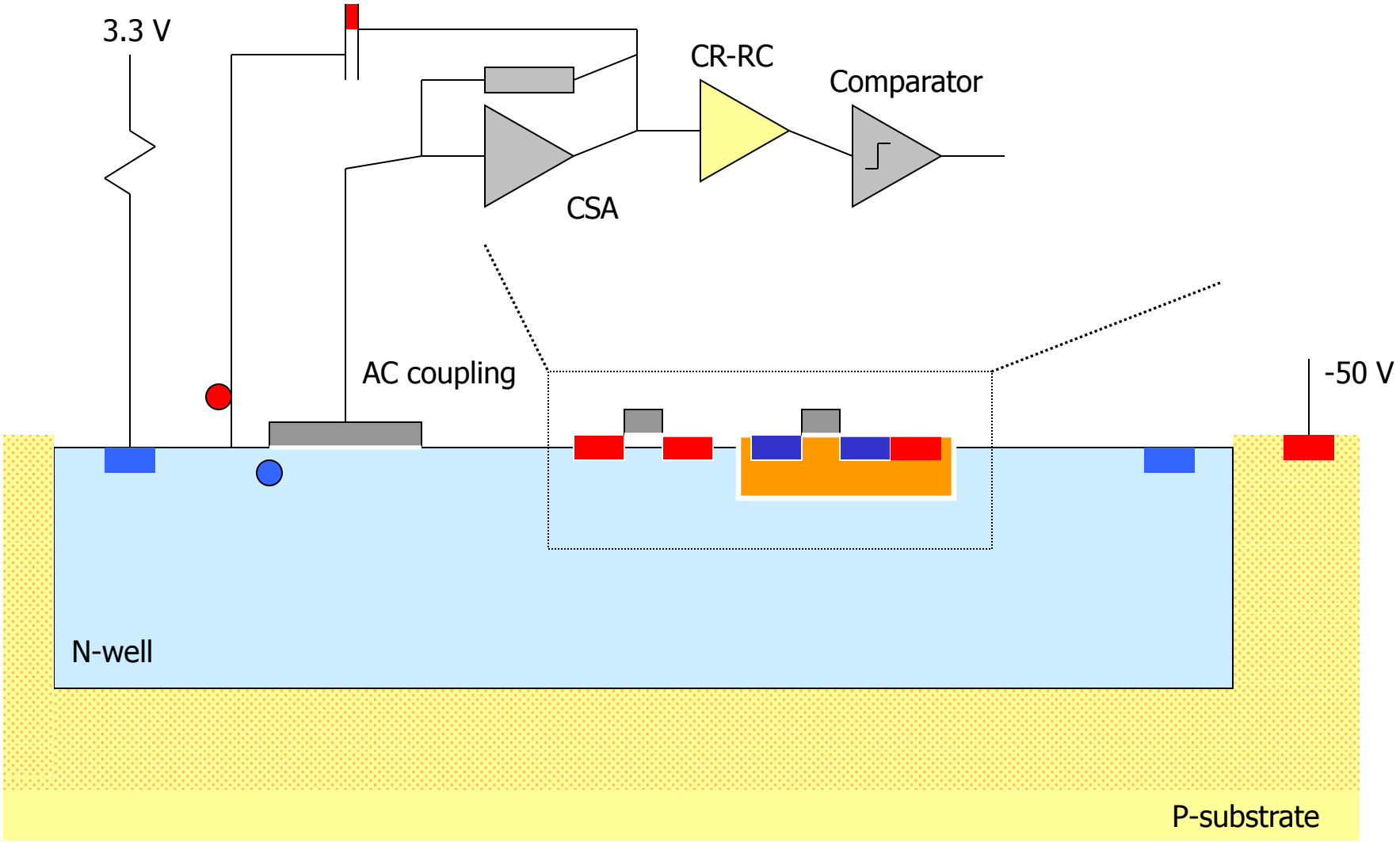
Signal detection



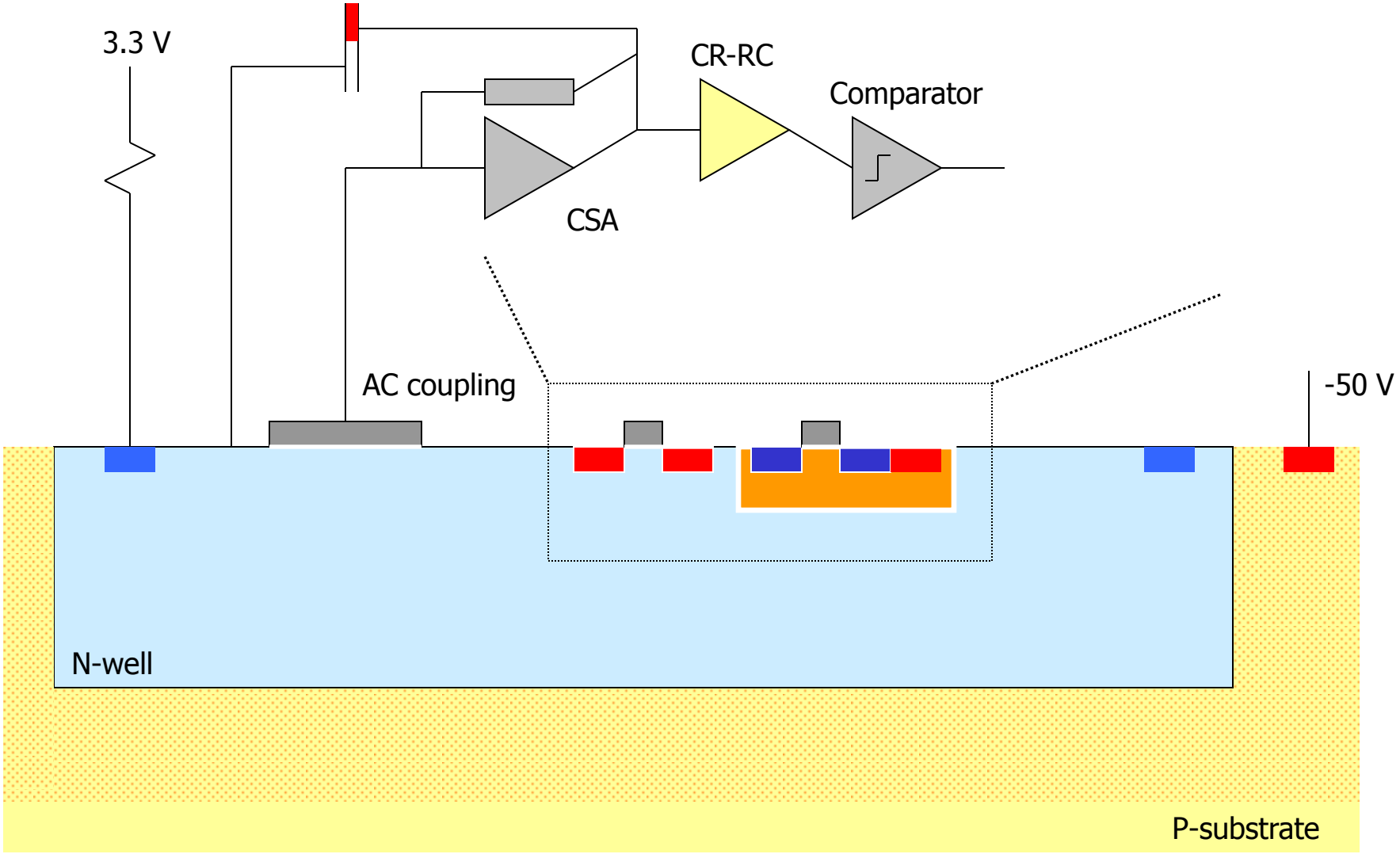
Signal detection



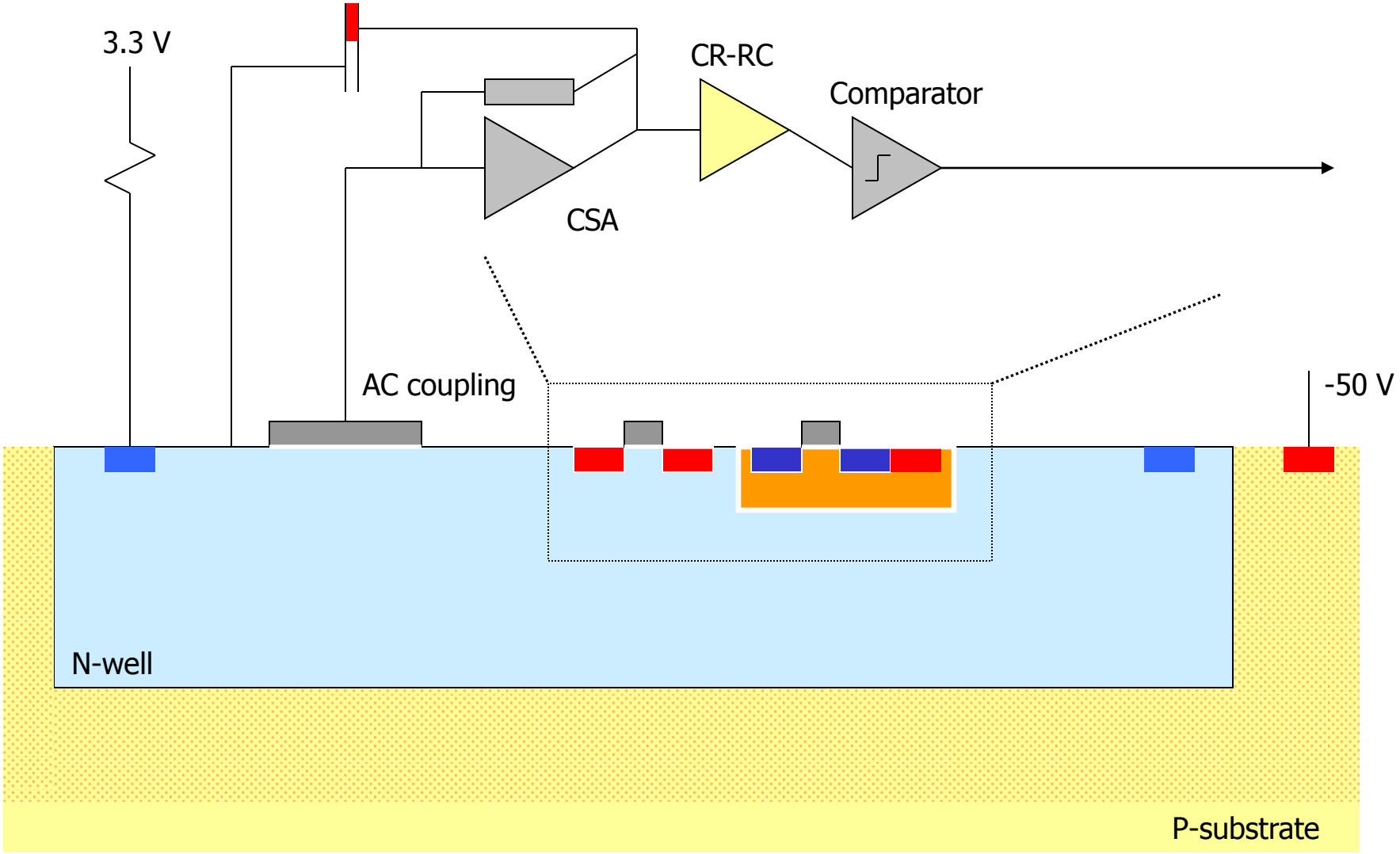
Signal detection



Signal detection



Signal detection

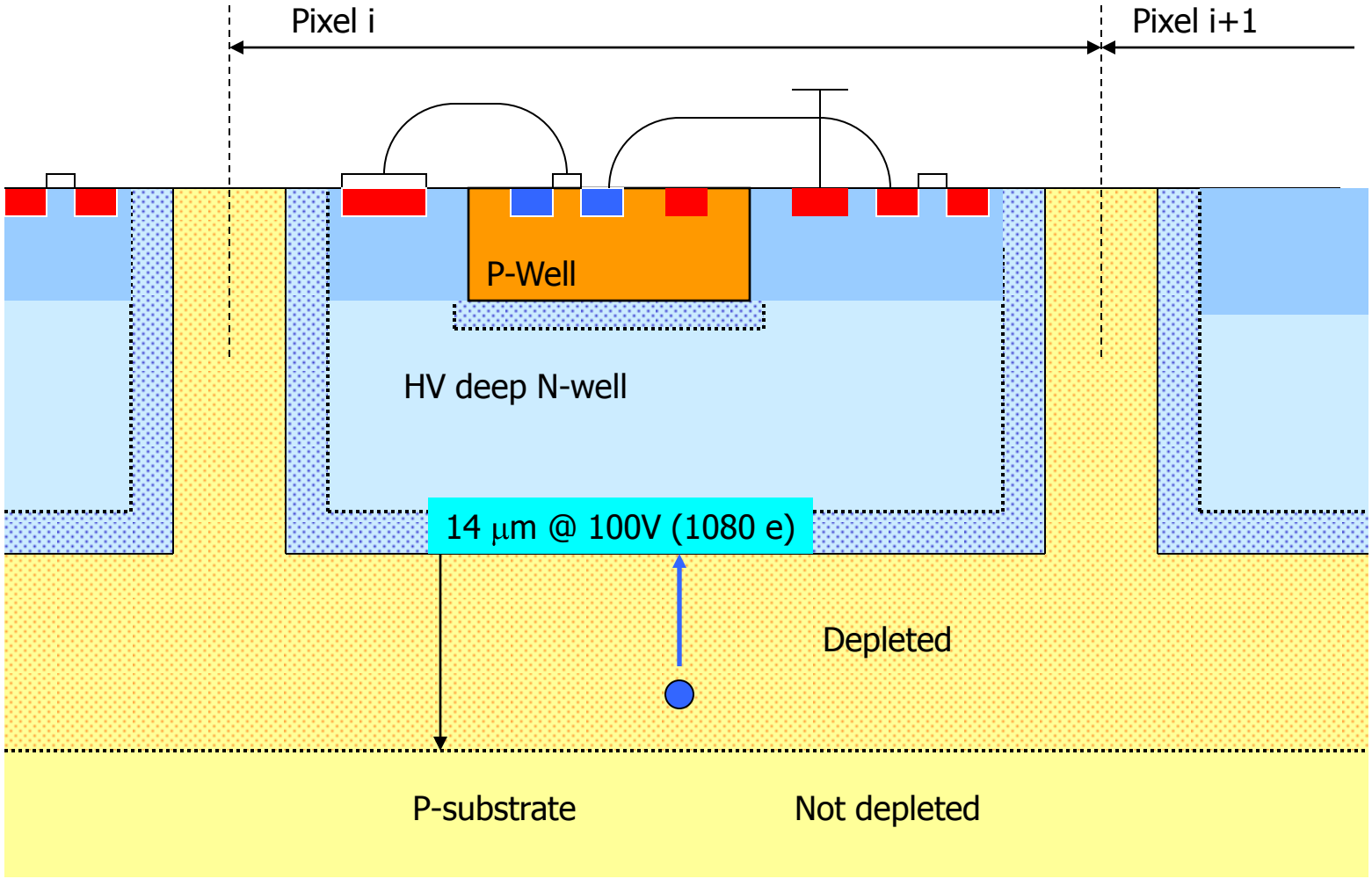


Strong points

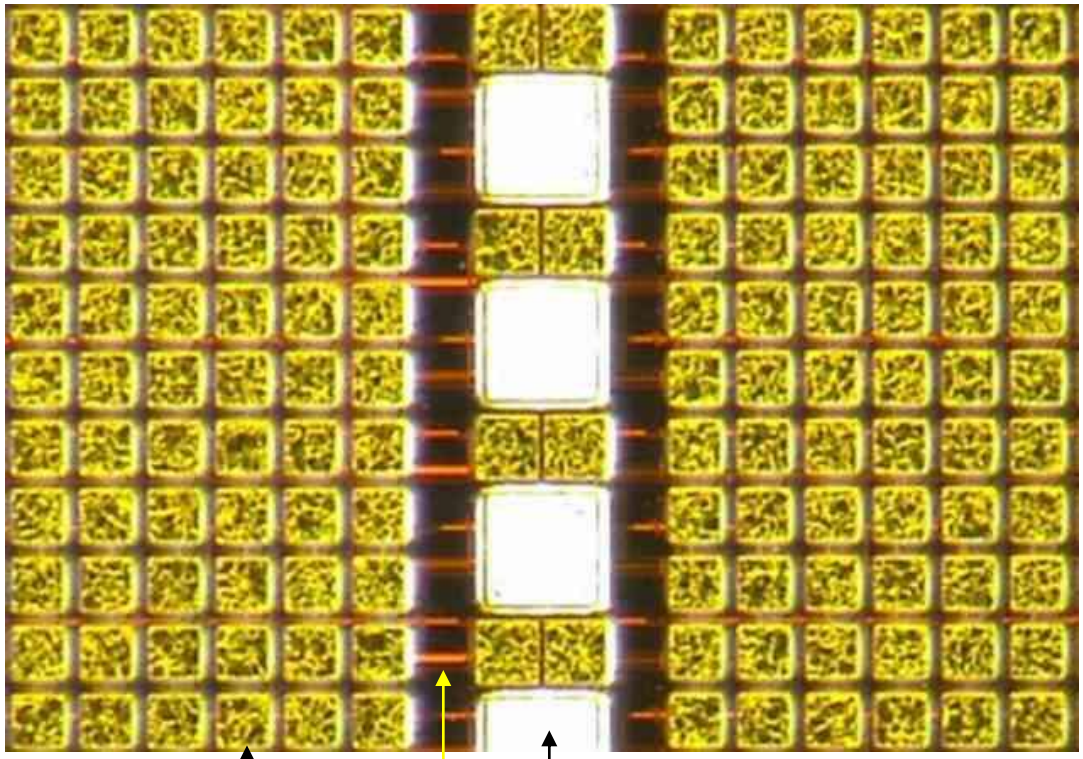
- 1) CMOS in-pixel electronics
- 2) Good SNR
- 3) Fast signal collection
  - Theoretically 40ps
- 4) Thinning possible
  - Since the charge **collection is limited to the chip surface**, the **sensors can be thinned**
- 5) Price and technology availability
  - Standard technology without any adjustment is used
  - Many industry relevant applications of HV CMOS technologies assure their long tern availability
- 6) High tolerance to non-ionizing radiation damage
  - High drift speed
  - Short drift path
- 7) High tolerance to ionizing radiation
  - Deep submicron technology
  - Radiation tolerant design can be used
  - Radiation tolerant PMOS transistors can be used (in contrast to MAPS with high-resistance substrate)

Drawbacks

- 1) Capacitive feedback
  - must be taken into account when the pixels are designed and simulated.
  - In some cases the capacitive feedback can be of use, for instance if provides a feedback capacitance for the charge sensitive amplifier.
  - **Despite some limitations**, we can implement the majority of important pixel circuits in CMOS, like the **charge sensitive amplifier**, shaper, tune DAC, SRAM…
  - **CMOS logic gates in pixels should be avoided – current mode logic can be used instead**
- 2) Relatively large size of the collecting electrode
  - However the high voltage deep n-well has relatively **small area capacitance**.
  - Typical values for the total n-well capacitance are from 10fF (small pixels and simple pixel electronics) to 100fF larger CMOS pixels.
  - Despite of the capacitance, we achieve excellent SNR values.

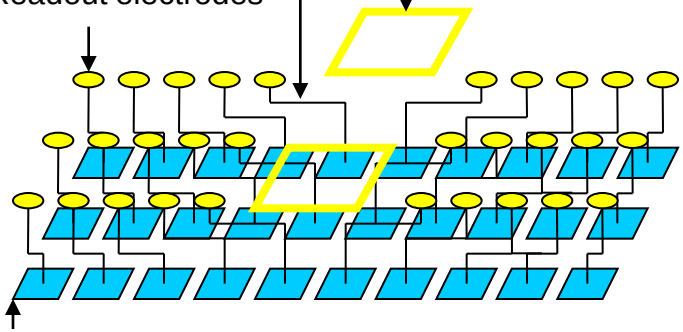

Pixel i
Pixel i+1
P-Well
HV deep N-well
14 μm @ 100V (1080 e)
Depleted
P-substrate
Not depleted

Tes

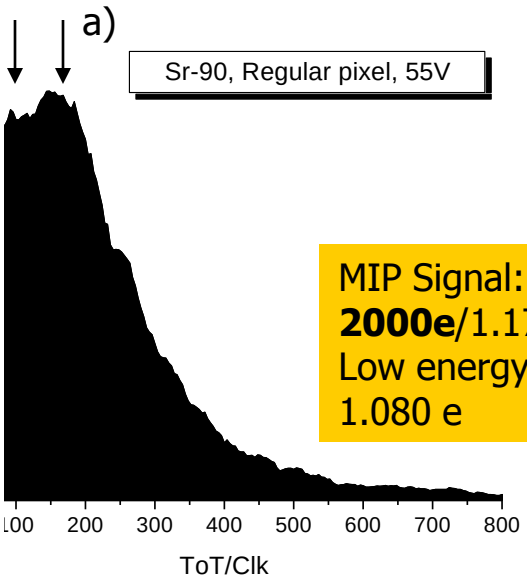


Pads for power and signals

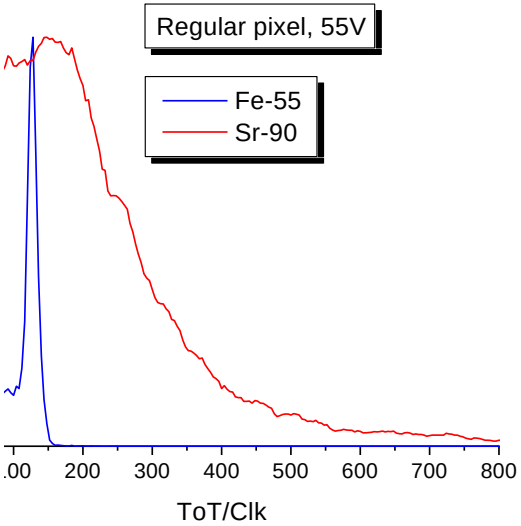
Readout electrodes



Sensor pixels



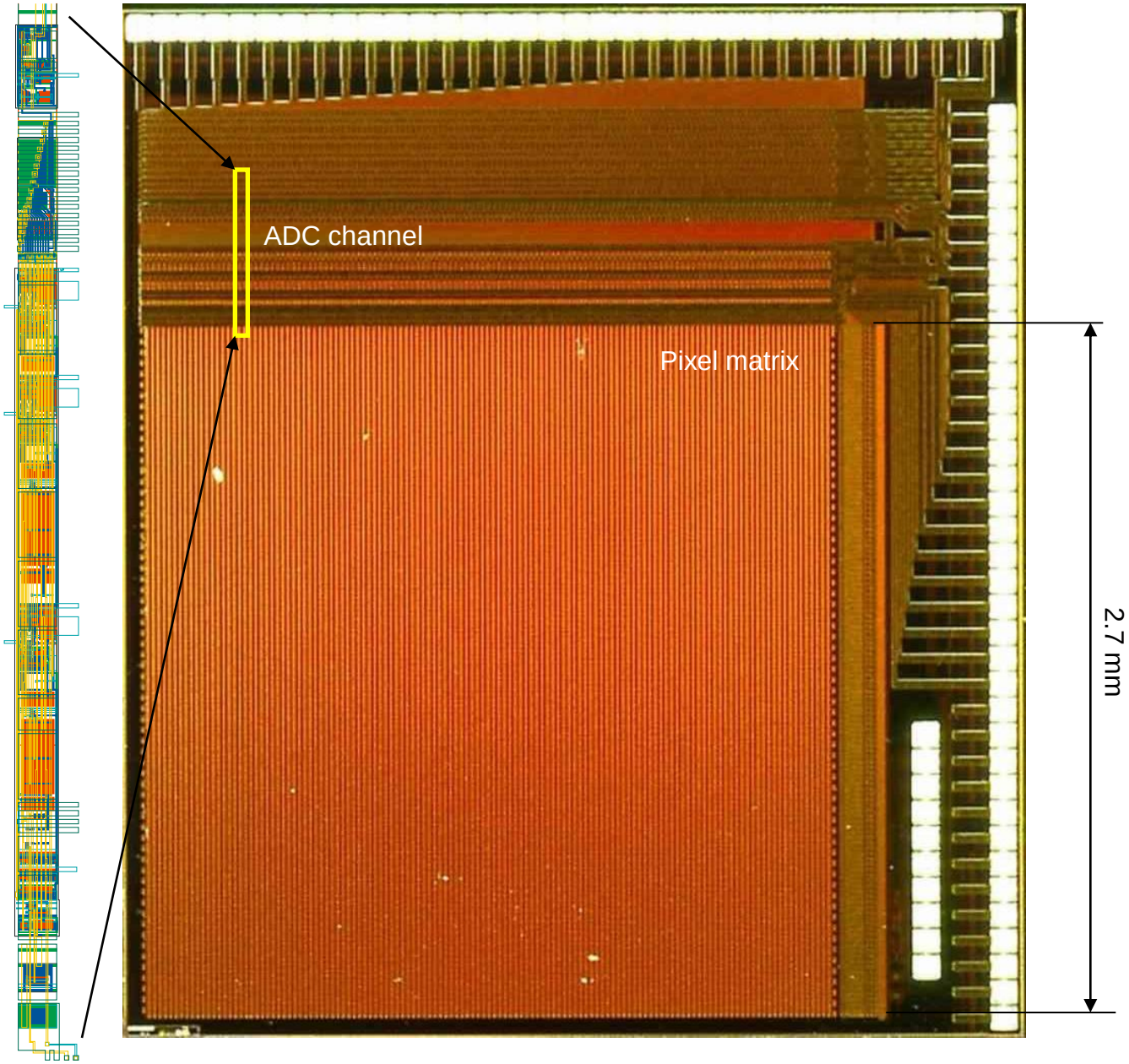
MIP Signal:
2000e/1.17 = **1710 e**
Low energy peak:
1.080 e



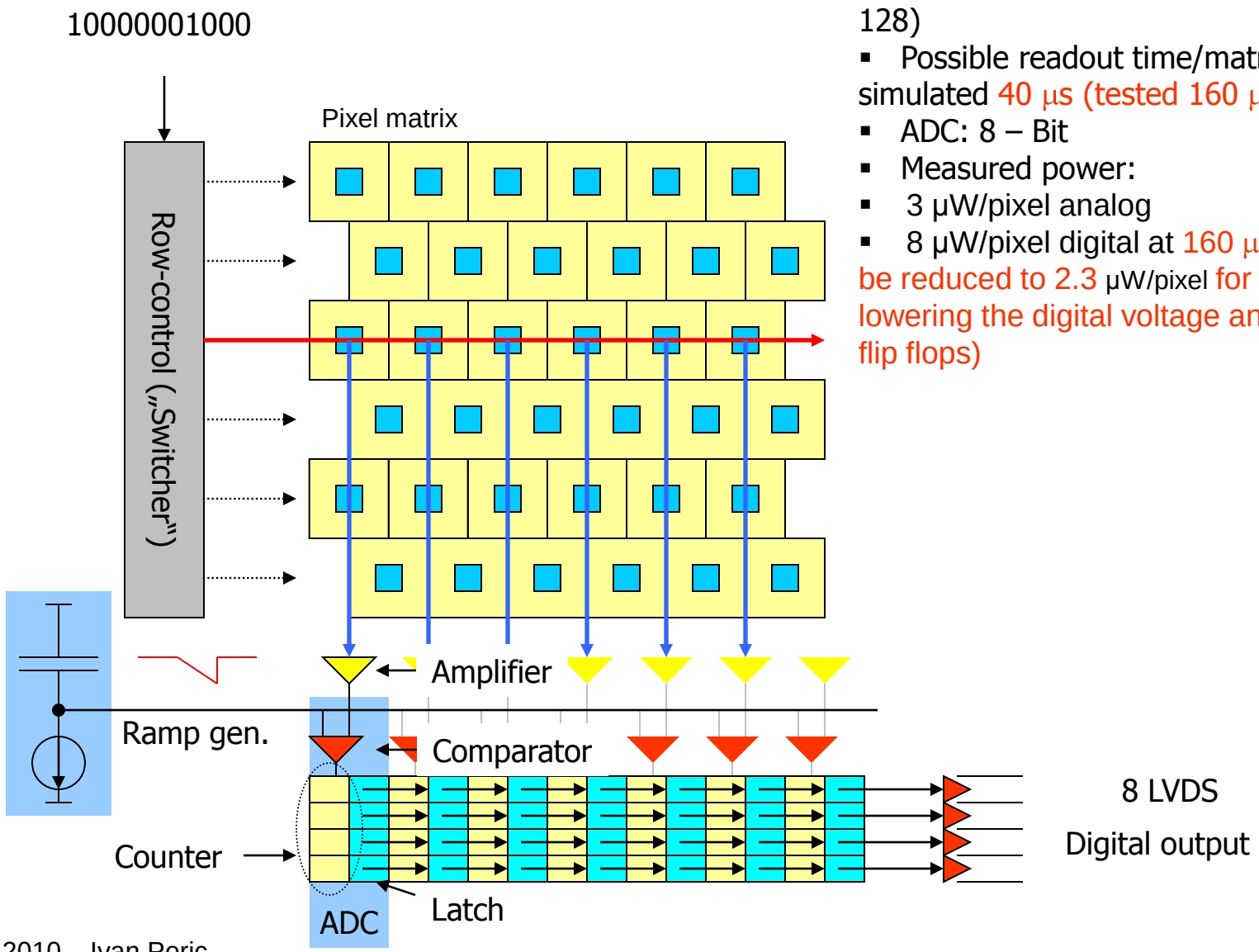
Experimental results

- Measurements with HVPixelM2

HVPixelM2 chip

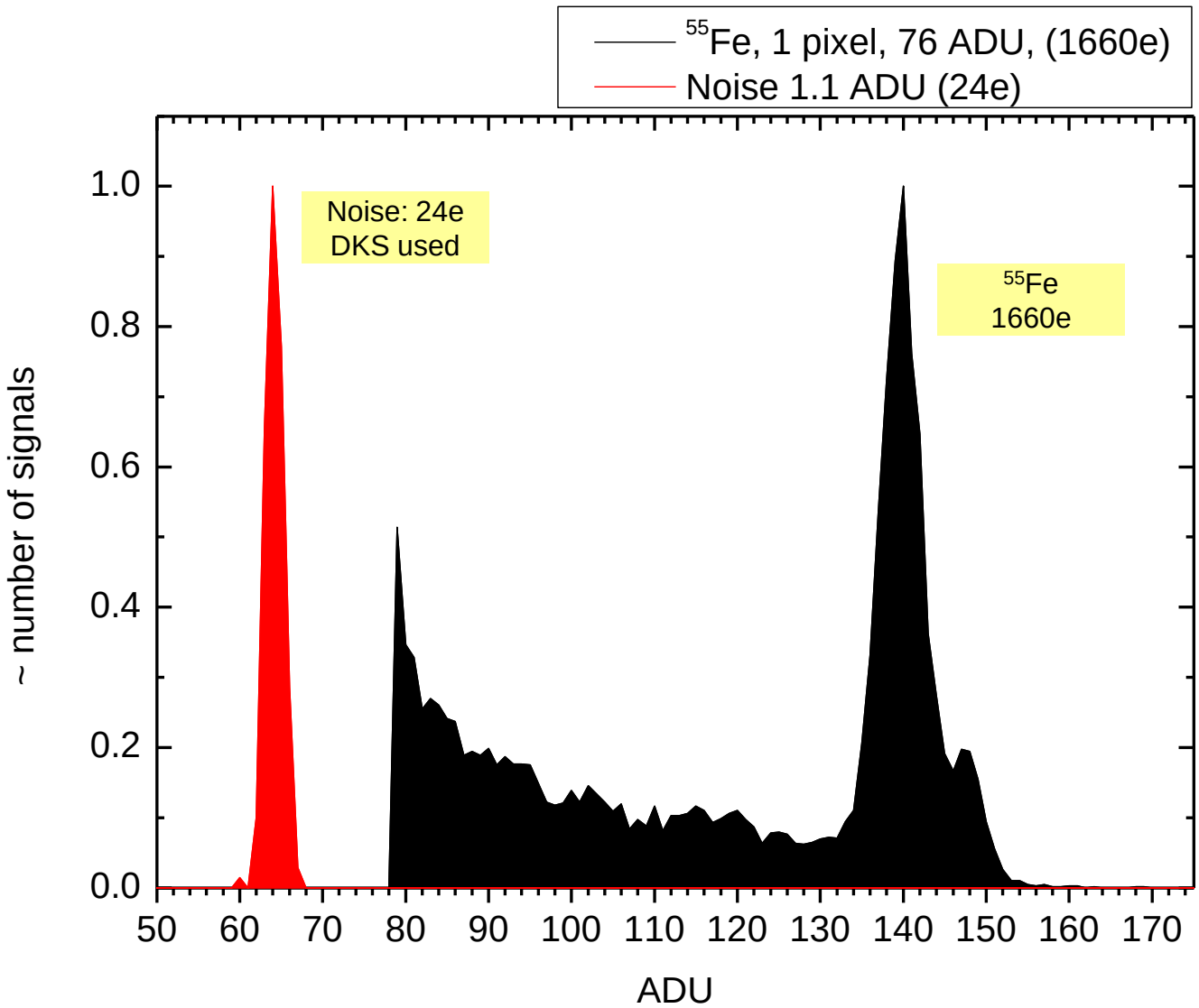


HVPixelM2 chip



- Pixel size: 21 X 21 μm
- Matrix size: 2.69 X 2.69 mm (128 X 128)
- Possible readout time/matrix: ~ simulated 40 μs (tested 160 μs/matrix)
- ADC: 8 – Bit
- Measured power:
- 3 μW/pixel analog
- 8 μW/pixel digital at 160 μs/matrix (can be reduced to 2.3 μW/pixel for 40 μs/matrix by lowering the digital voltage and resizing the flip flops)

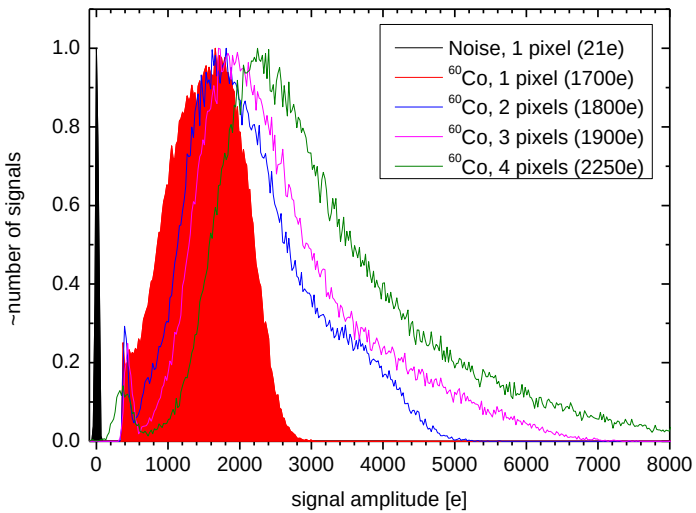
Noise measurement and ^{55}Fe spectrum (HVPixelM2)

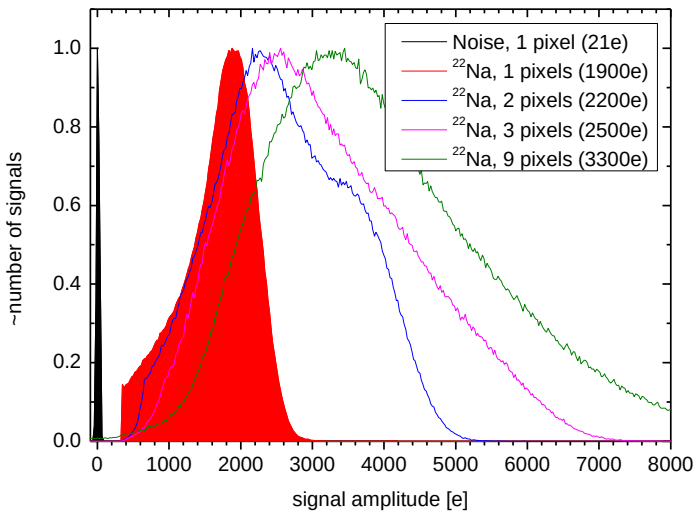


High-energy beta spectra (HVPixelM2)

^{60}Co betas (about 10% higher signals than MIPs)
Seed signal: 1700e
Cluster signal: 2250e
Noise: 21e
Seed SNR: 81
Cluster signal/seed noise: 107

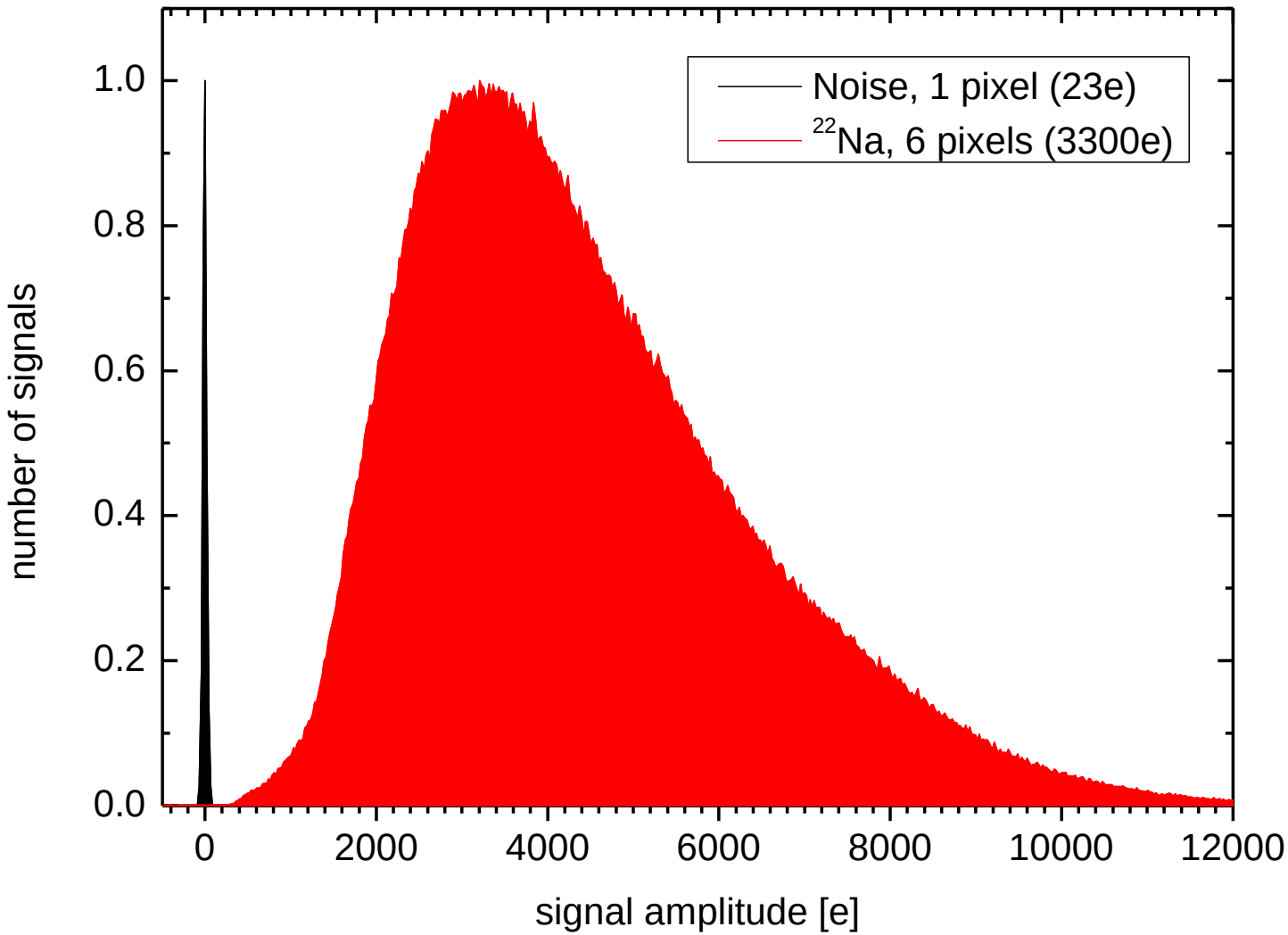
^{55}Na betas
Seed signal: 1900e
Cluster signal: 3300e
Noise: 21e
Seed SNR: 90
Cluster signal/seed noise: 157





Estimated MIP seep pixel SNR 70

High-energy beta spectra (HVPixelM2)

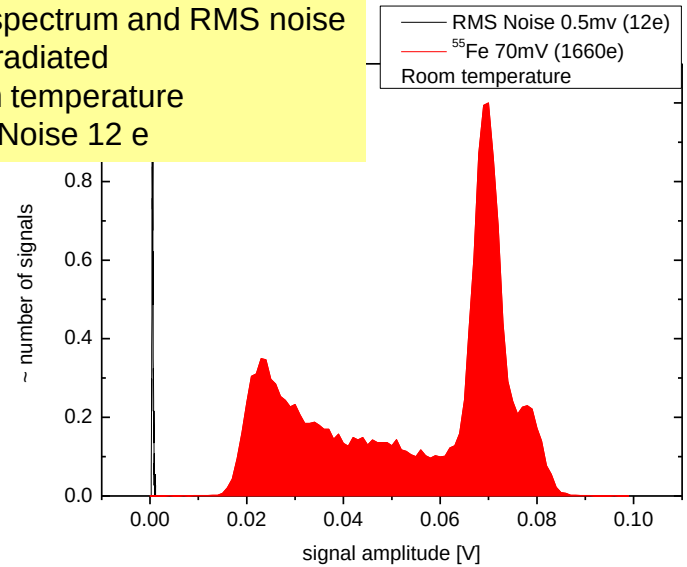


Radiation tolerance

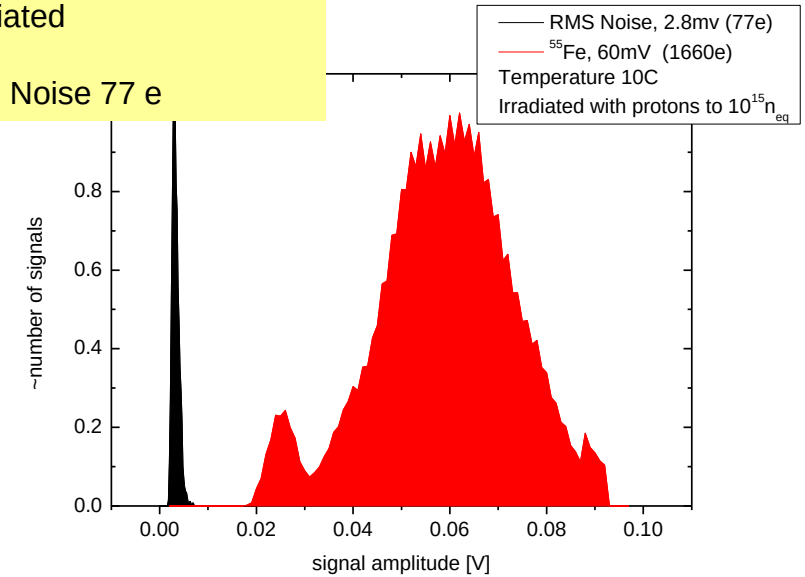
- We expect a good tolerance to non-ionizing damage thanks to the small drift distance and high drift speed in the depleted area. Due to high dopant density the type inversion should occur at higher fluencies.
- Concerning the ionizing damage, we can benefit from the properties of the used deep submicron CMOS technology. In contrast to the most of the MAPS, we can rely on PMOS transistors inside pixels that are more radiation tolerant than NMOST.

Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

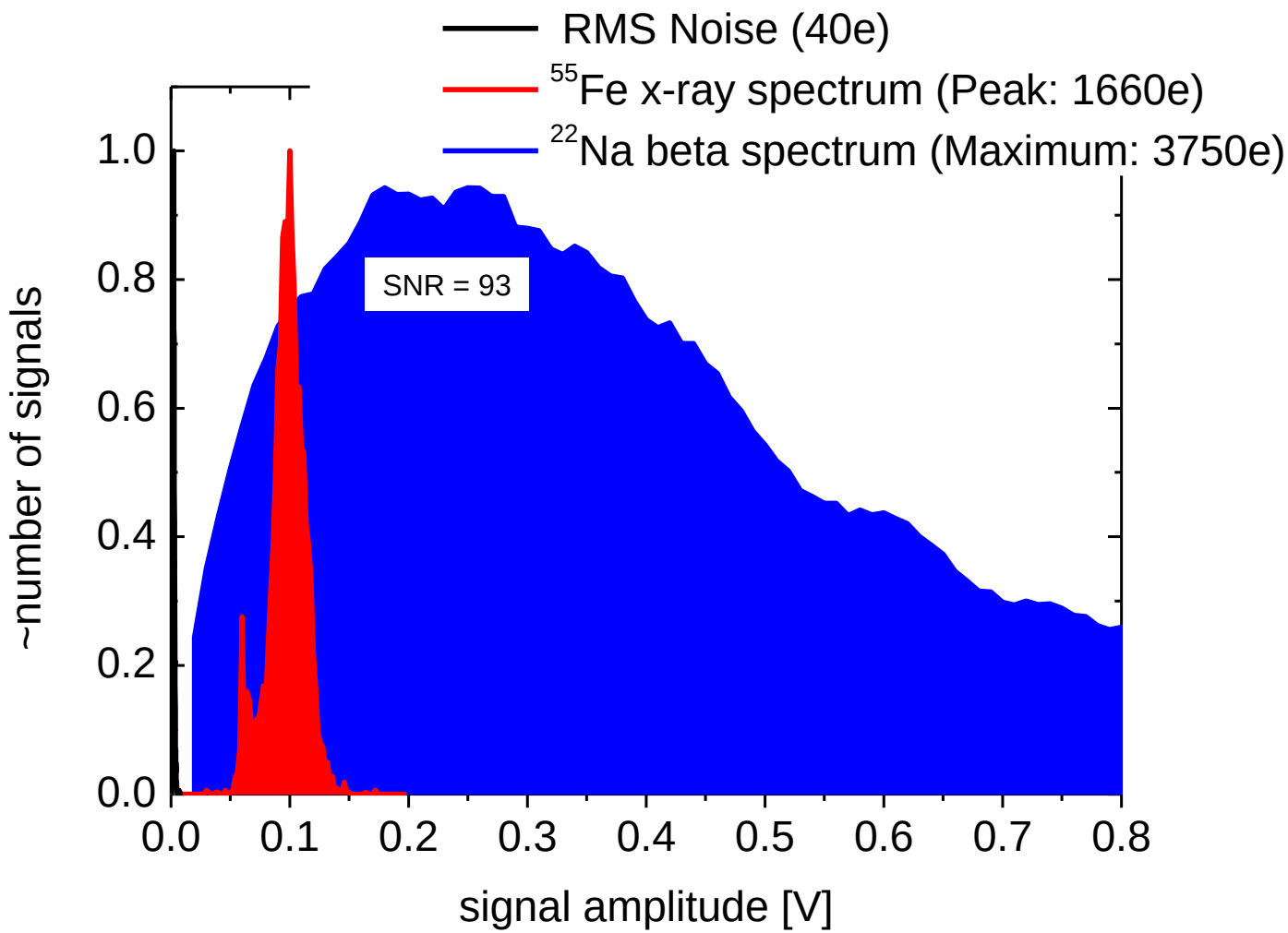
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e



Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)



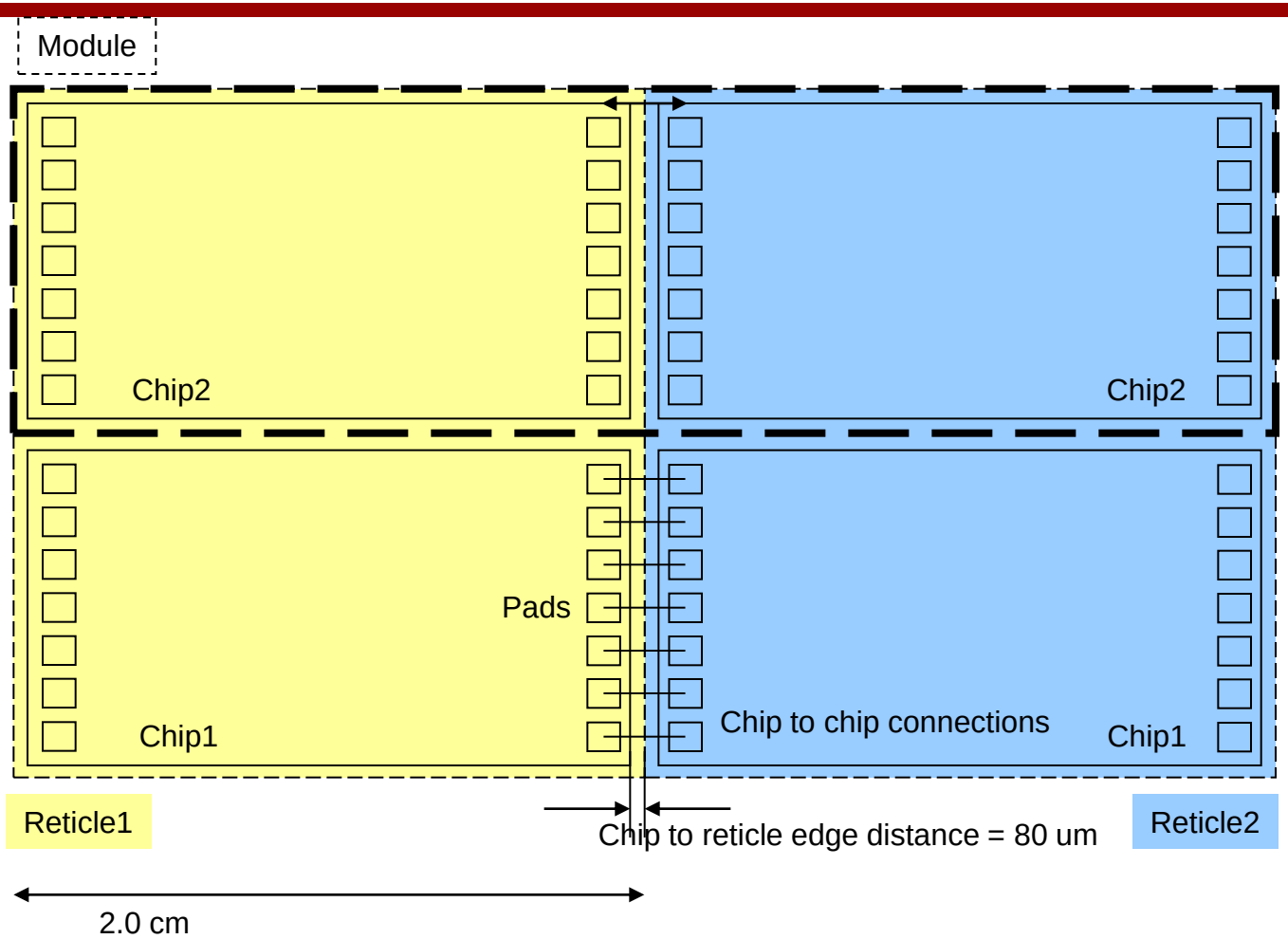
Summary

- We have developed a new pixel sensor structure (smart diode array) for high energy physics that can be implemented in a high voltage CMOS technology.
- The sensor has 100% fill-factor and can have in-pixel electronics implemented with p- and n-channel transistors.
- We have implemented the sensor structure in various variants:
- 1) Sensor with in-pixel hit detection and sparse readout,
- 2) Sensor with fast rolling-shutter readout and simple pixel electronics,
- 3) Hybrid sensor based on capacitive chip to chip signal transfer.
- We measure excellent SNR in all three cases.
- We have done a test-beam measurement with the first version of the frame readout detector with good results.
- The SNR of the second chip version is four times better.
- Excellent seed pixel SNR of almost 100 has been achieved.
- We have irradiated the chips with neutrons, protons and x-rays to test radiation tolerance.
- After irradiation with protons up to very high fluence 10^{15} n_{eq}/cm^2 and dose 300MRad, we have still very large SNR (>40) for high energy beta particles at nearly room temperatures (10C).

Outlook

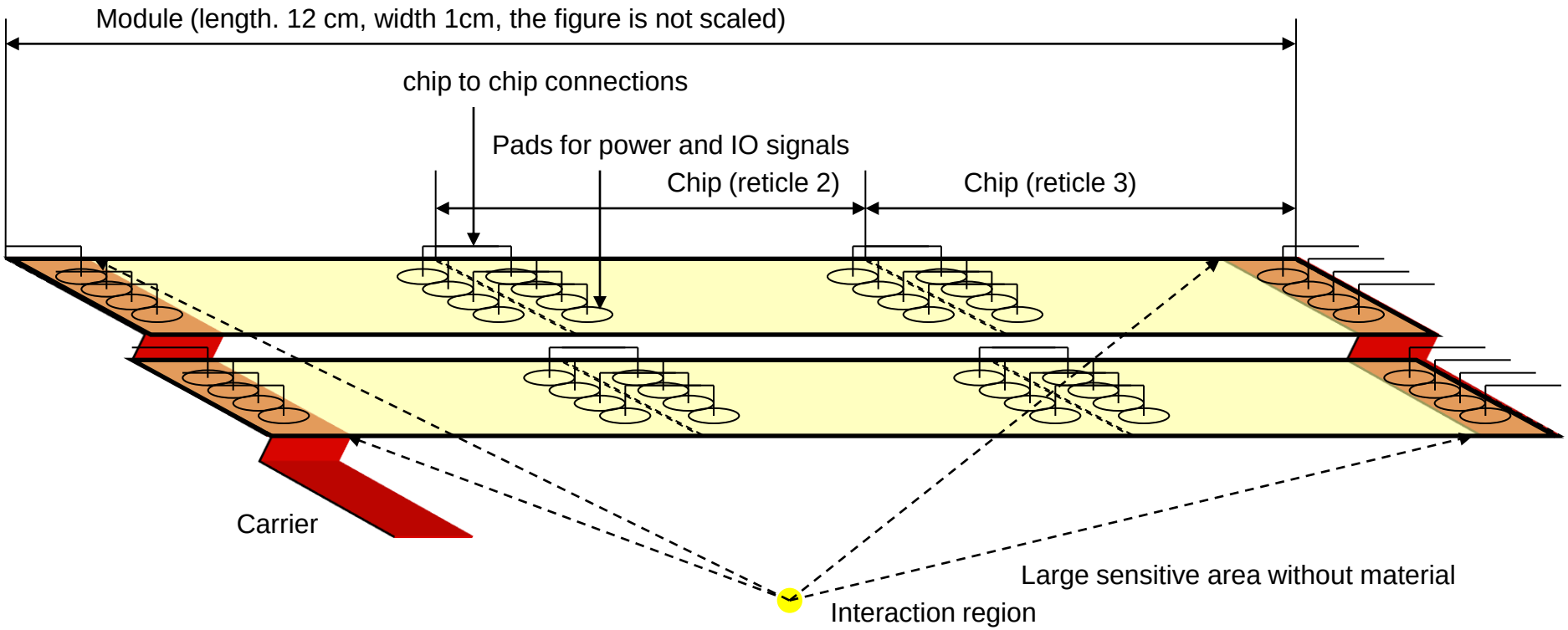
- The engineering run in the used technology costs only 98k €
- By proper arrangement of the dices, we can obtain long monolithic multi-reticle sensors with 12cm length and 1cm width
- We would have 8 such modules per wafer and one engineering run could give us up to 48 modules
- We are confident that the sensor technology has achieved such a degree of maturity so that it can be considered as a good candidate for future particle physics experiments

Multi-reticle module



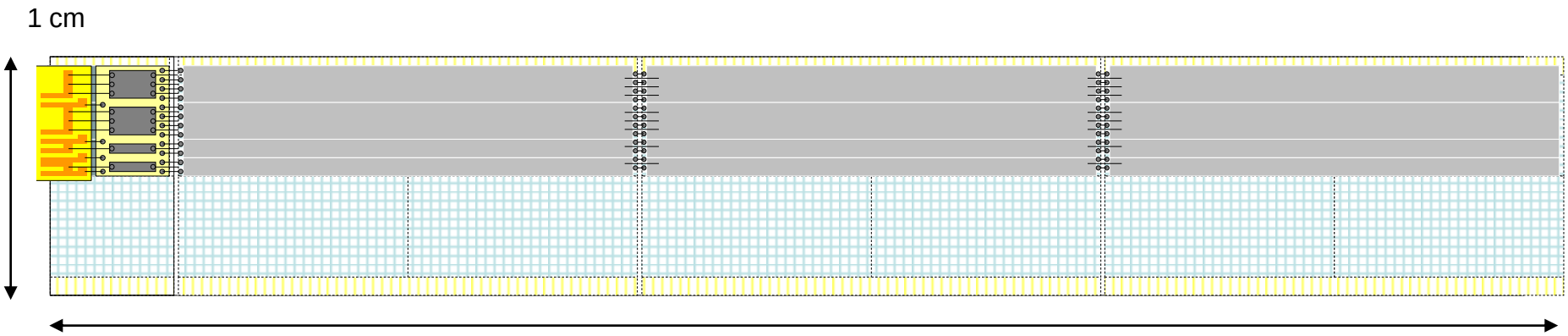
Very long low-cost pixel modules with (almost) no insensitive area can be produced
Reticle-reticle connections can be made easily by wire bonding
Instead of wire-bonding, an extra metal layer can be used as well

Multi-reticle module



Very low-mass only silicon modules are possible as well (similar to DEPFET module for Belle II)

SDA long module



Sensor types

- Frame RO type 1: (for ILC)
  (Scaling of the existing PM design)

  Half module size 1x6cm
  Pixel size 40x40µm
  Pixels 250x1500
  RO time 80µs/matrix
  Resolution 8bit/pixel
  Power 900mW/module (150mW/cm^2)
  Data output width 96 bits @ 400Mbit

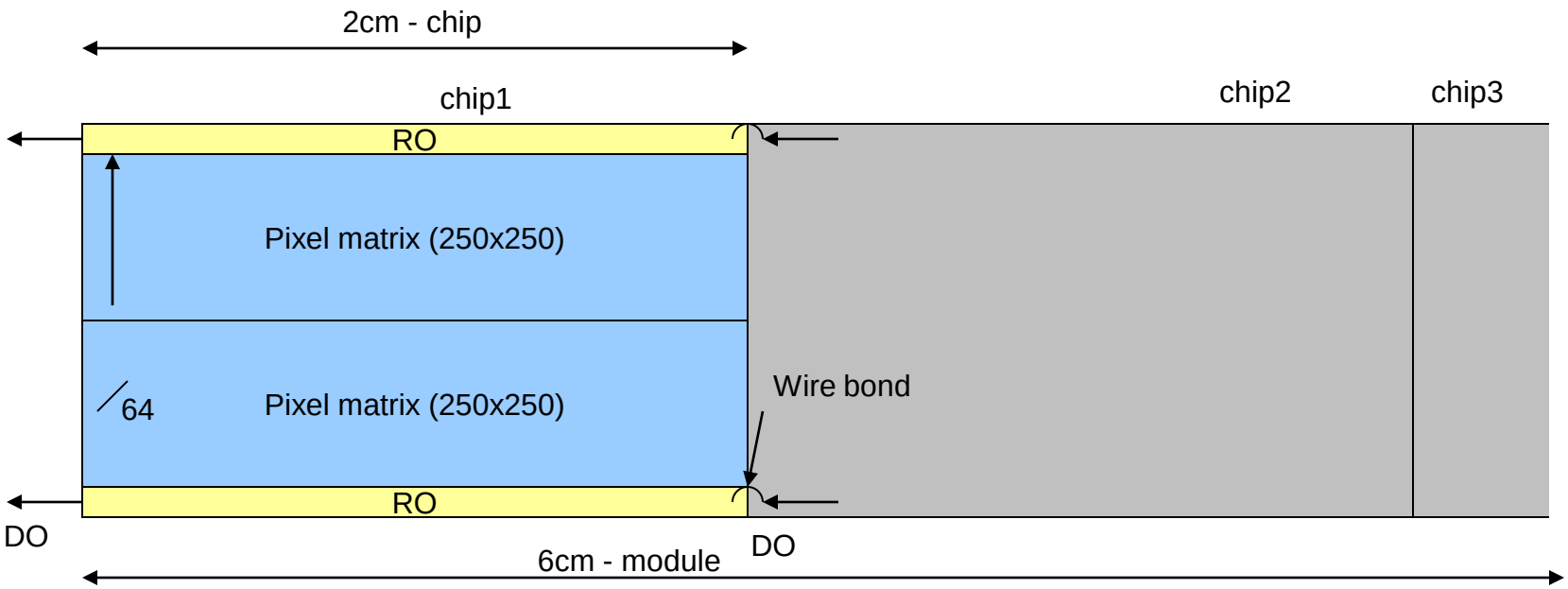
- Frame RO type 2 (in-pixel DKS and binary readout): (for Belle II, ILC...)
  (new Design)

  Half module size 1x6cm
  Pixel size 40x40µm
  Pixels 250x1500
  RO time 10µs/matrix
  Resolution 1bit/pixel
  Power 900mW/module (150mW/cm^2)
  Data output width 96 bits @ 400Mbit

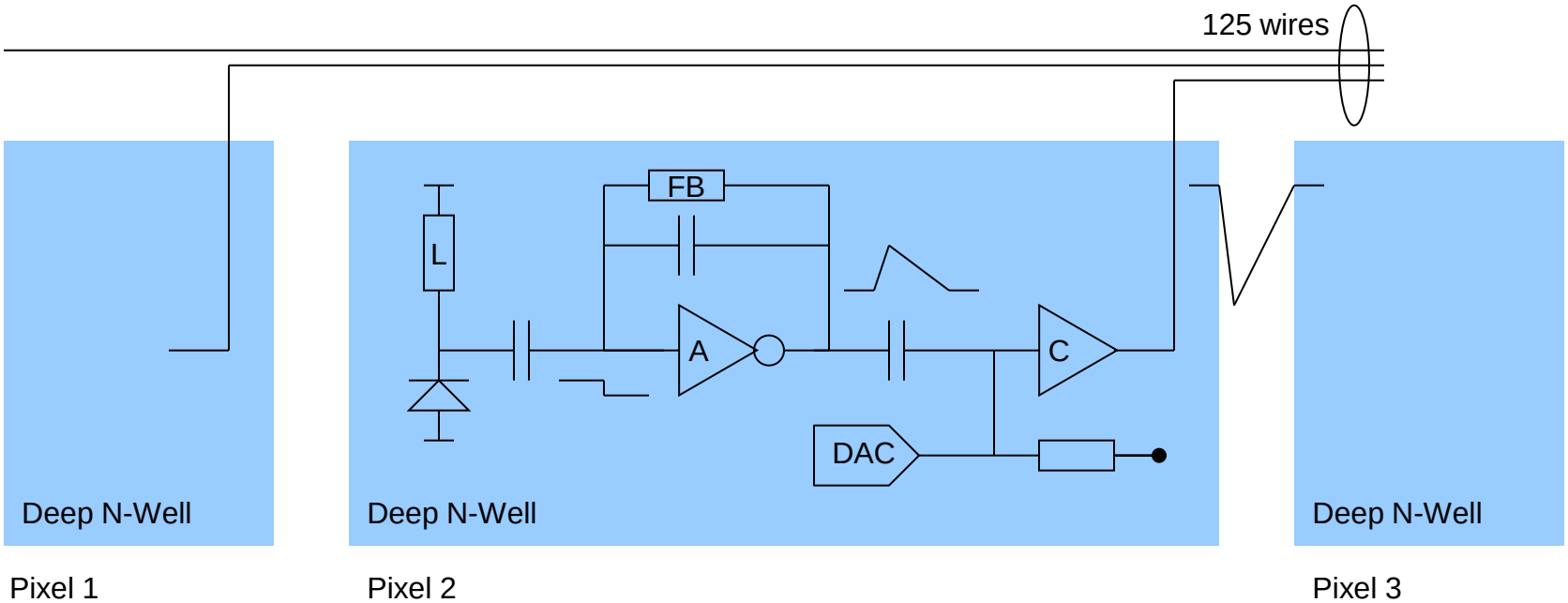
- Continuous RO type (in-pixel hit-detection): (for LHC, Belle II...)
  (Scaling of the existing design plus new readout periphery block)

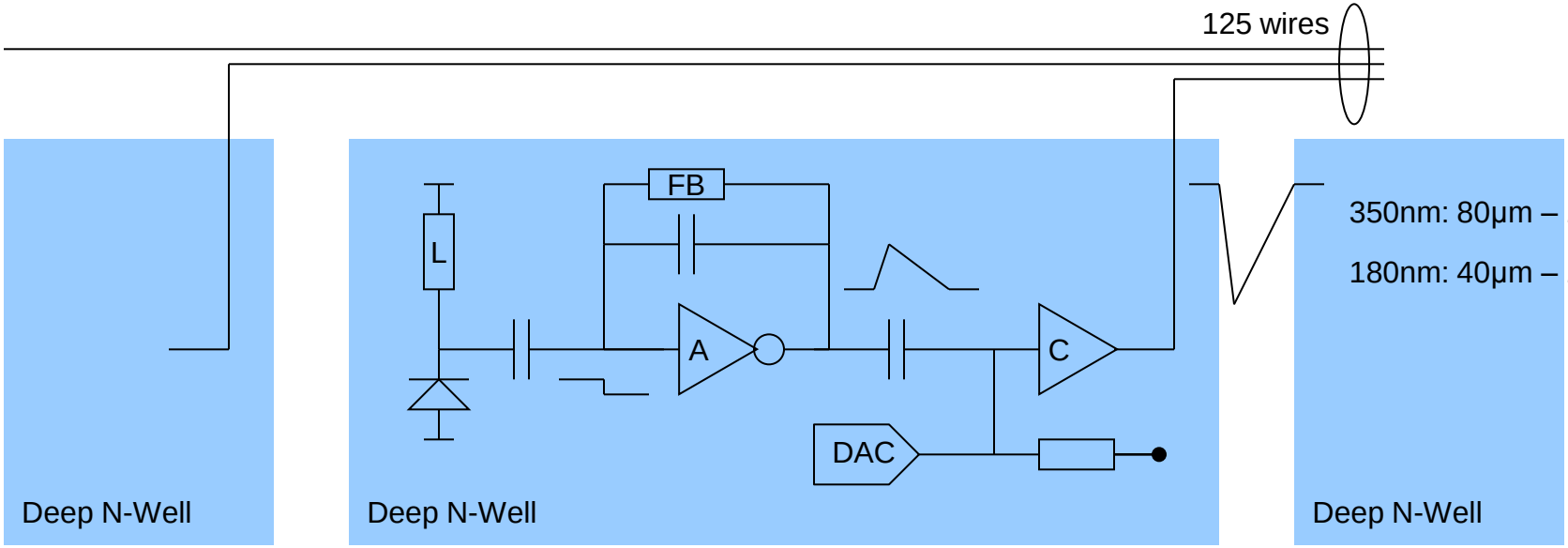
  Half module size 1x6cm
  Pixel size 40x80µm
  Pixels 250x750
  Time resolution: 50-100ns
  Power 1000mW/module (167mW/cm^2)

Sparse RO typ



Sparse RO typ

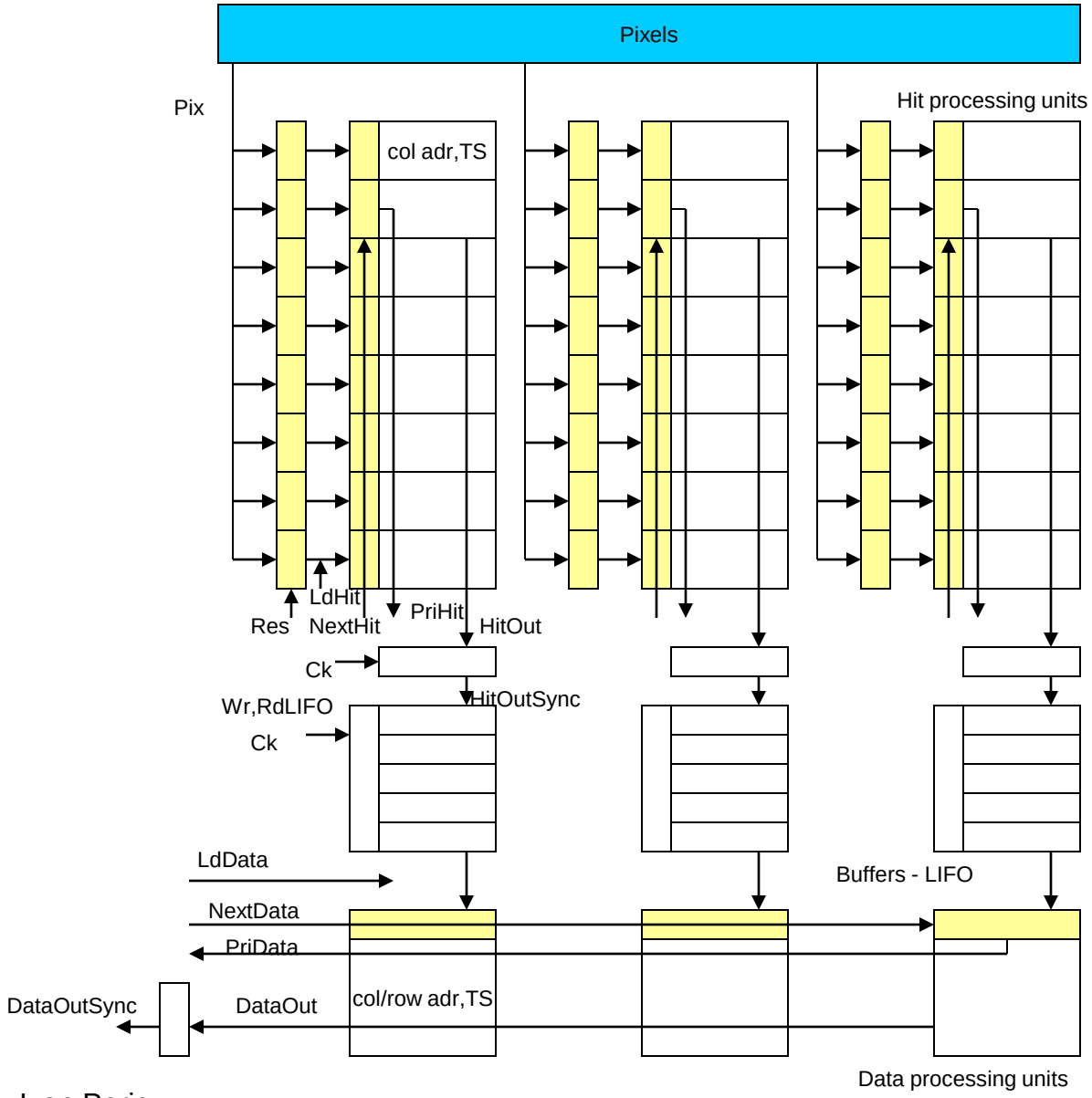




350nm: 80µm – 125 lines

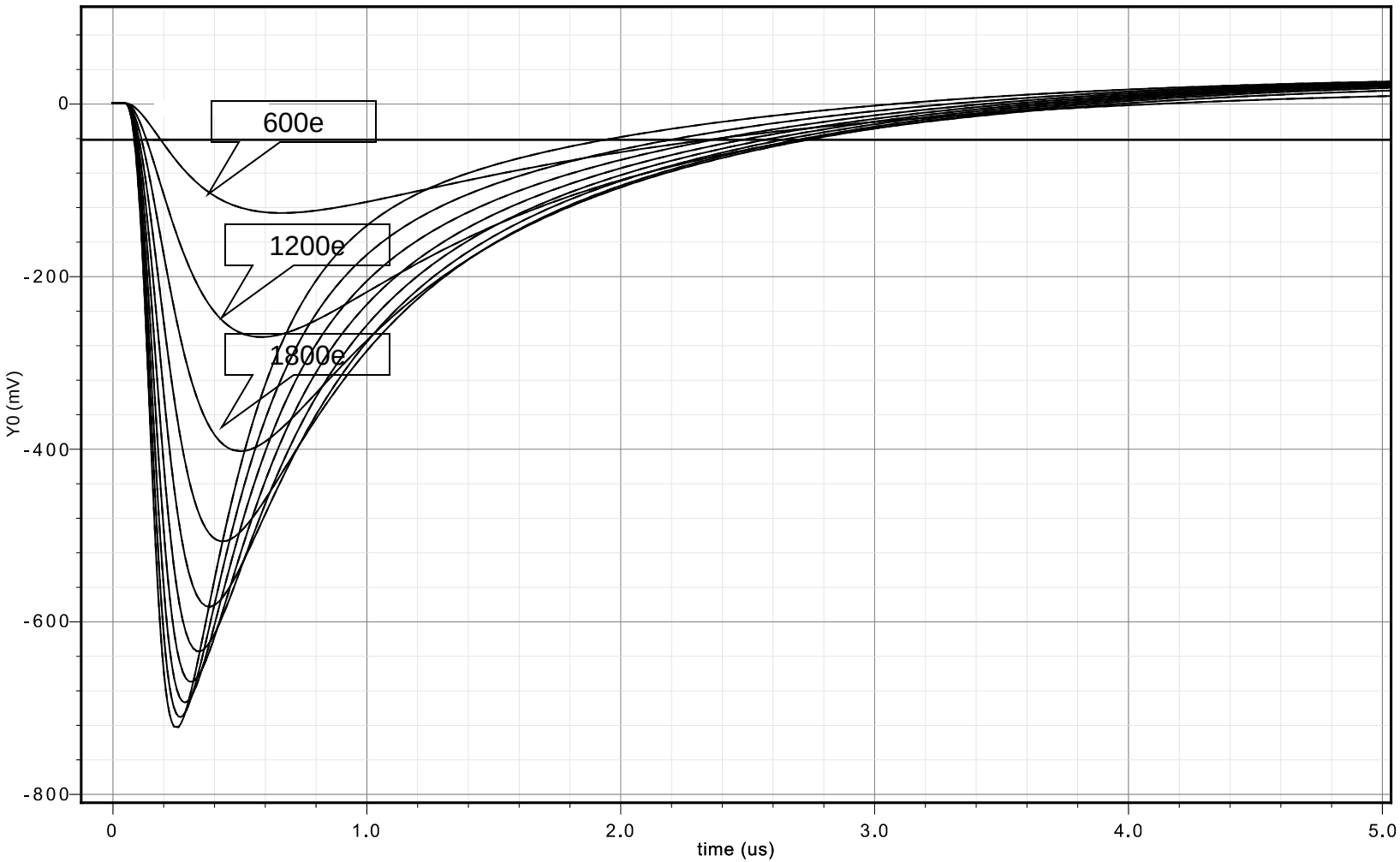
180nm: 40µm – 125 lines

Sparse RO typ



Time walk for 5μW pixel amplifier

Output of the Pixel amplifier



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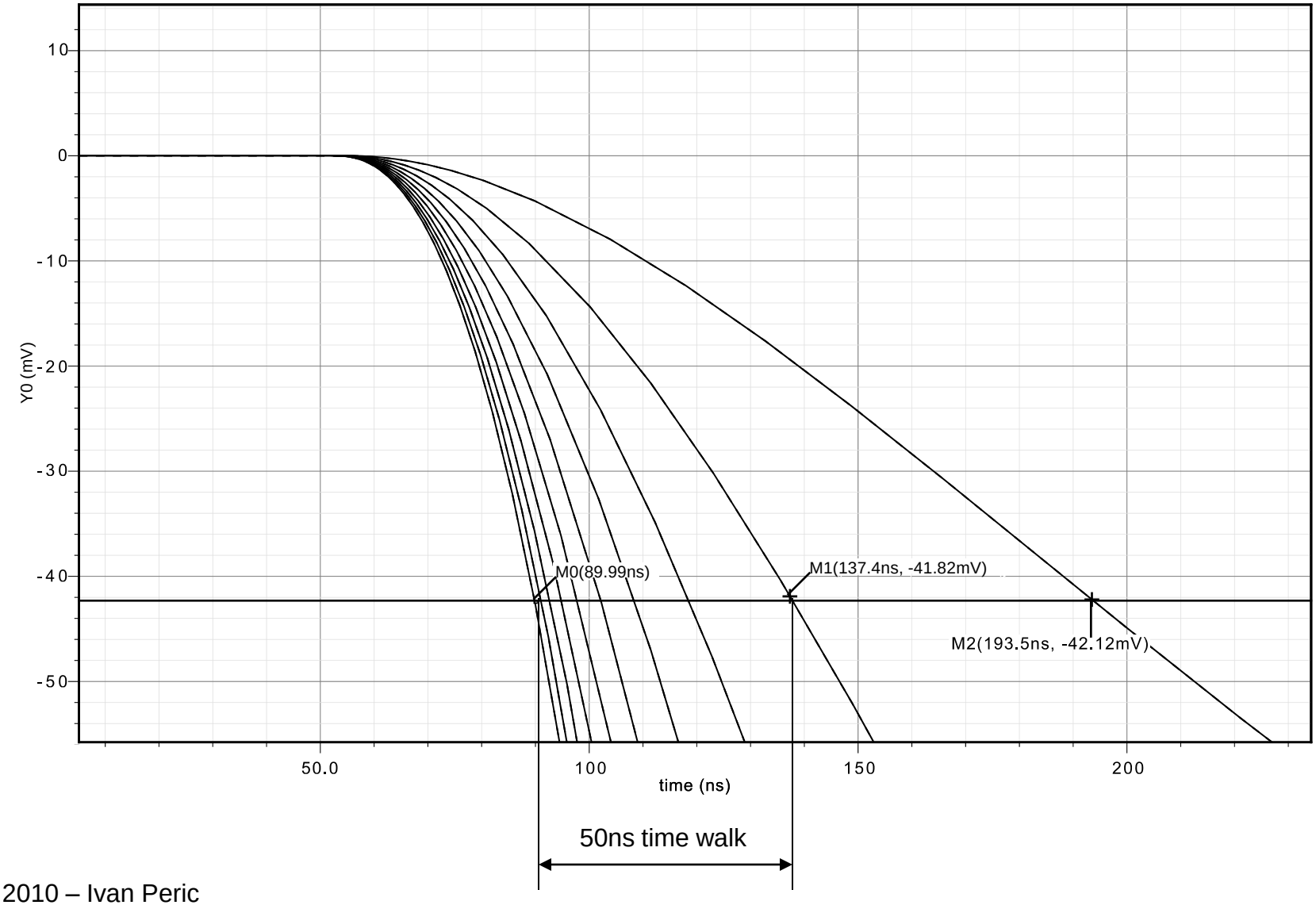

- Thank you!