Development of CMOS pixel sensors for an ILC vertex detector

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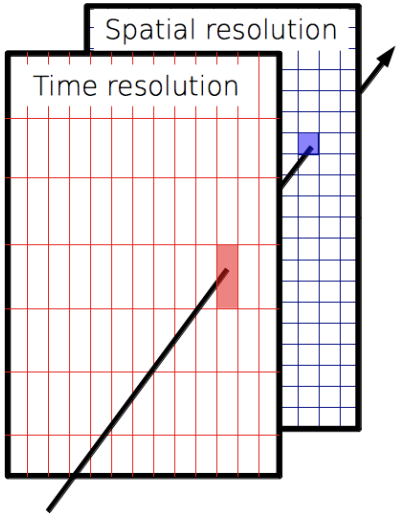
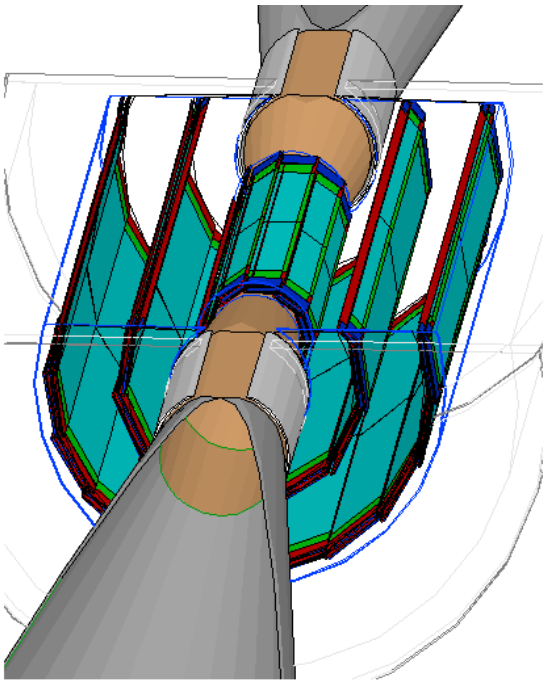
- **A dedicated design**
  - Inner & outer sensors
- **Current prototypes**
  - Generic architecture for granular, fast pixels
  - Assessment of radiation tolerance
  - Integration studies
- **Next steps for DBD 2012**
  - Benefits of smaller feature size
  - final sensor architectures
- **Developments not directly related to DBD**
  - First CMOS pixel sensor vertex detector for HEP
  - New technologies for improved performances

A dedicated design

- **The inner double-sided layer**
  - Granularity ← pointing resolution $\sigma_{s.p.} \leq 3$ µm
  - Readout speed ← occupancy from beam background
  - Separate spatial resolution & time resolution on each layer



- **The two outer double-sided layers**
  - Granularity ← track to VXD hit association
  - "Reduced" readout speed ← Power dissipation
  - Lower #pixels but good charge estimation/pixel

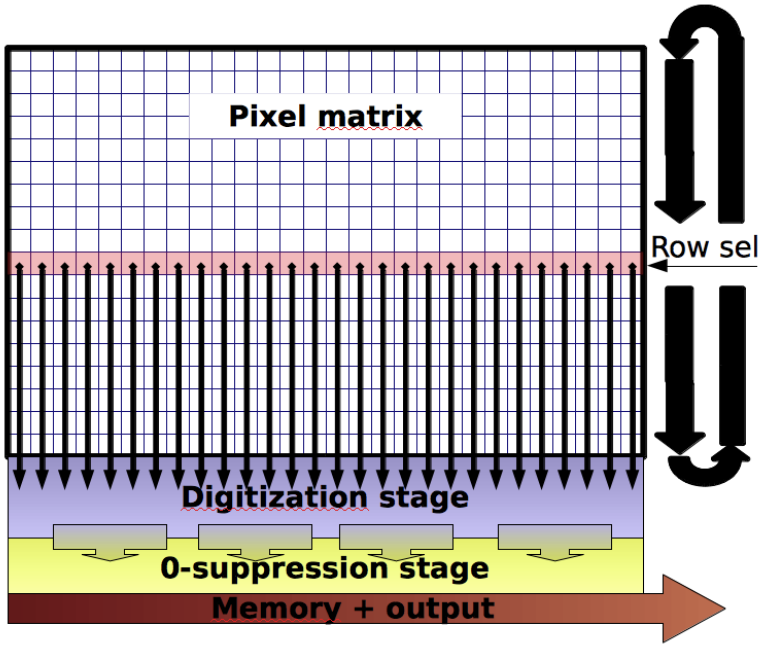


- **Other constraints**
  - Material budget ≤ 0.16 % X0 / layer
  - Radiation tolerance

A generic achitecture

- **Speed = sparsification**
  - Include CDS (correlated double sampling) in pixel
  - Discriminate pixel output
  - Suppress zeros

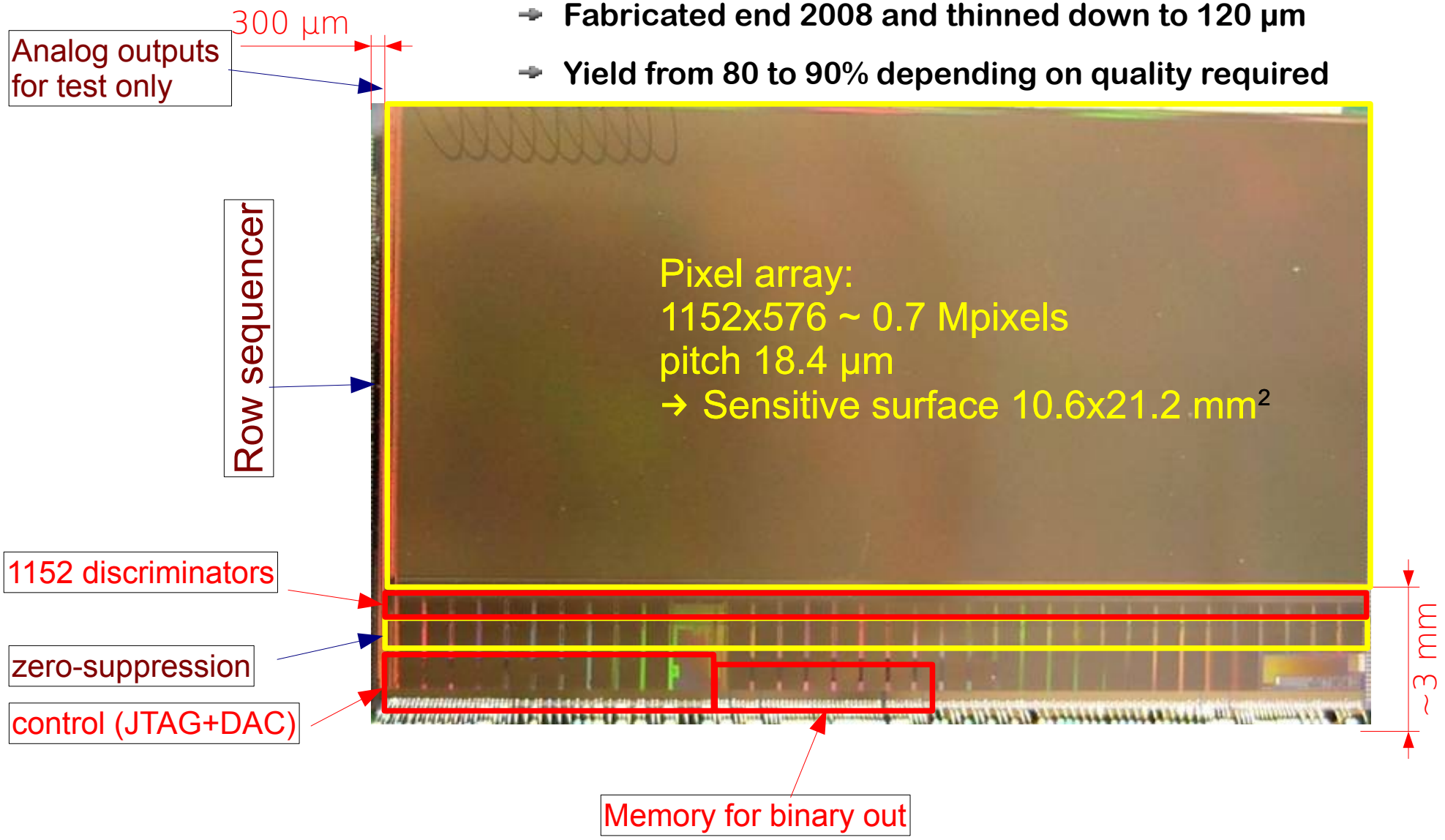
    ⇒ column parallel binary output
  - Very few rows powered at a time
    → Low power dissipation



- **Spatial resol. (inner layer, side 1)**
  - Pixel pitch 16x16 μm², binary output
  - 1.9 cm² of sensitive area
    2x320 rows of 1152 columns
  - Two-sided readout @ clock(100MHz)
  - $\sigma_{s.p.} \leq 3$ μm, integration time ≤ 50 μs
- **Time resol. (inner layer, side 2)**
  - Pixel pitch 16x64-80 μm², binary output
  - 1.9 cm² of sensitive area
    160 rows of 1152 columns
  - Single-sided readout
  - $\sigma_{s.p.} \sim O(5)$ μm, integration time ≤ 10 μs
- **For power dissipation (outer layers)**
  - Pixel pitch 35x35 μm², 4-bits ADC output
  - 4 cm² of sensitive area
    576 rows of 576 columns
  - $\sigma_{s.p.} \sim 4$ μm, integration time ≤ 100 μs

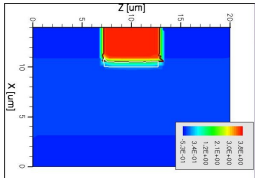
Generic architecture validation

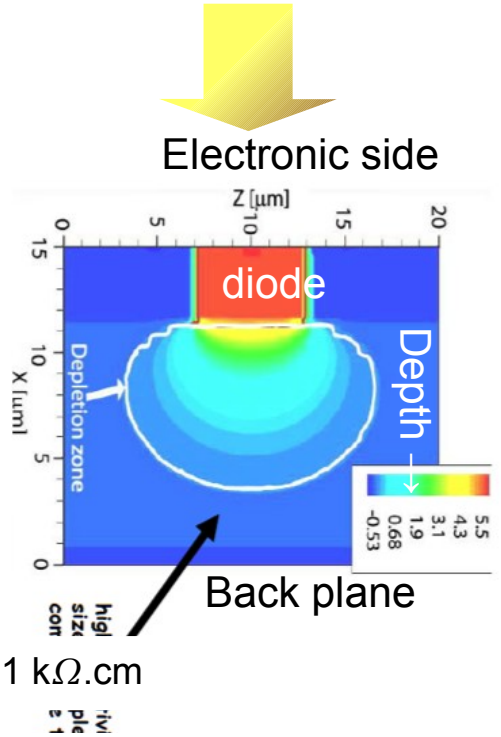
- **Full size : MIMOSA 26 (EUDET final sensor)**
  - **Process AMS 0.35 µm OPTO**
  - **Fabricated end 2008 and thinned down to 120 µm**
  - **Yield from 80 to 90% depending on quality required**



Radiation tolerance improvement

- **For a better charge collection**
  - Standard process epitaxial layer
    - resistivity ~10 Ohm.cm → charges drift ONLY thermally
  - Low-doped epitaxial layer
    - resistivity ≫100 Ohm.cm "HR" grade → deeper depletion
    - Note: depletion level depends on diode voltage
  - Expected shorter collection time & charges more spatially focused

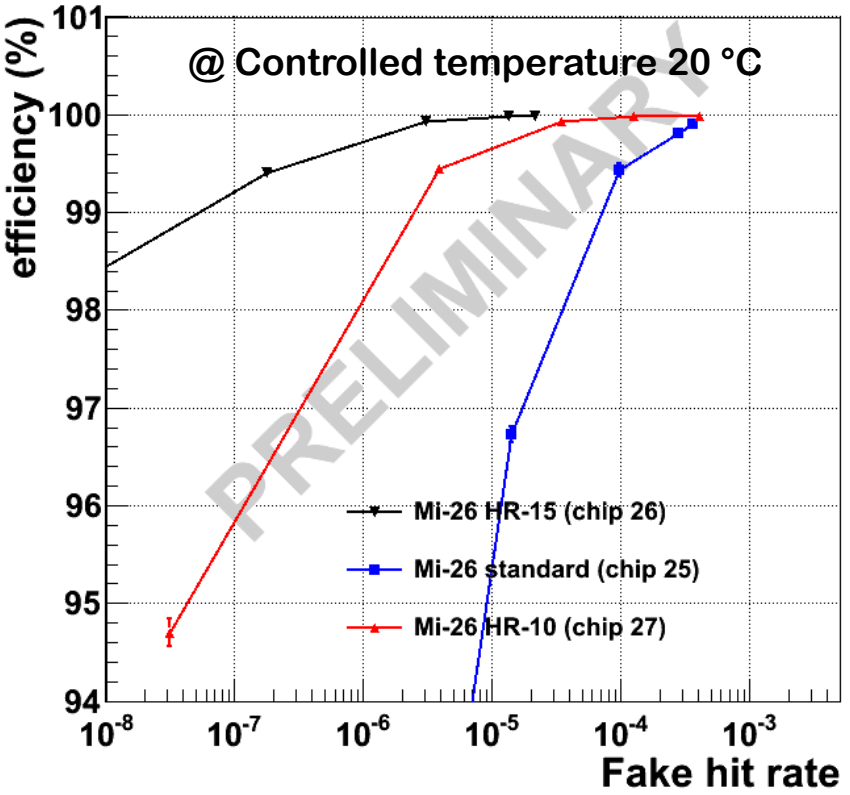




- **Prototype: MIMOSA 26-AHR**
  - Process AMS 0.35 µm OPTO with 400 Ohm.cm epi. layer
  - Exact same layout / MIMOSA 26
  - Fabricated in 2009 with 3 composite epi.: 10, 15 & 20 µm thick
  - Yield at least as good as std. Epi. Layer
  - Test in lab with Ru source (MIP-like β)
    S/N x 1.5 to 2 from std to HR epi.
    (depending on epi. thickness)

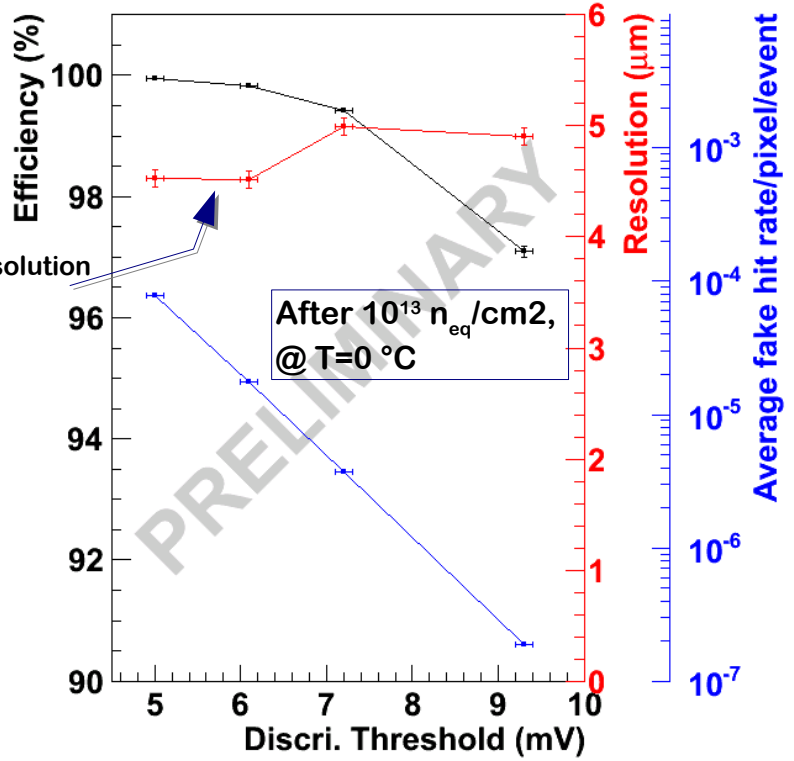
- **Irradiated sensors at**
  - 150, 300, 500, 1000 kRad
  - 3., 6., 10., 30. 10^{12} n_{eq}/cm^2

MIMOSA 26 performances



! shift of .5 µm in resolution
(due to alignment)

High resistivity (400 Ω.cm), 15 µm thick epitaxial layer

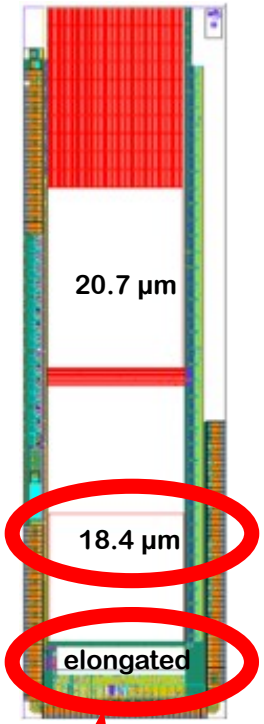


- **120 GeV π⁻ beam tests**
  - With High Resistivity layer
  - With typical threshold ~6 x noise: Effi ~ 99.5 %, fake ~ 10^{-5} hits/pixel, $\sigma_{s.p.}$ ~ 3.5 µm
  - Readout speed with 80 MHz clock: 115 µs
  - Performances checked to hold up to 10^{13} n_{eq}/cm^2

Optimized pixel for HR epi. layer

MIMOSA 22-AHR = pixels + discri. only

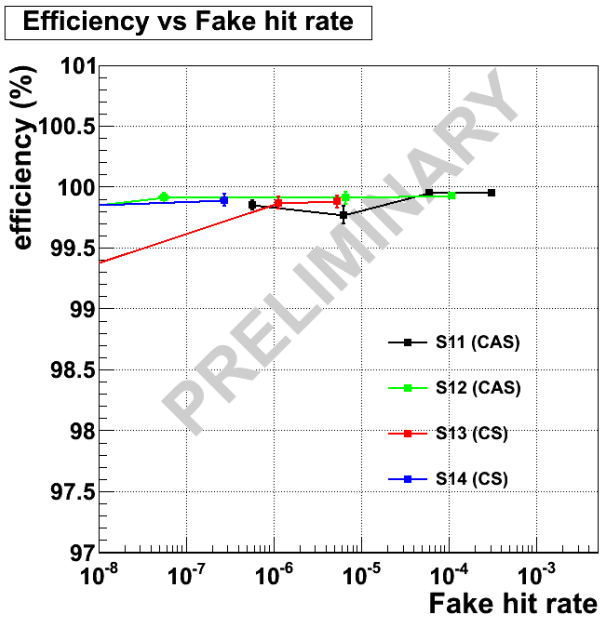
- Process AMS 0.35 µm OPTO with 400 Ohm.cm resistivity
- Digital part: 128 columns x 576 rows
  Analog part: 8 columns x 576 rows
- Fabricated 2010 with 3 epi: 10, 15 & 20 µm thick
- New pixel designs
  - Different amplification schemes & diode biasing
  - Different pitch 18.4, 20.7 µm & elongated pixels
- Irradiated sensors at
  - 150 kRad or 3., 6.10^{12} neq/cm^2
  - Combined 150 Krad + 3.10^{12} n_{eq}/cm^2
- Operation $t_{r.o.}$ = 92.5 µs (80 MHz), T=20 °C
- Beam test in late summer 2010 with 120 GeV π^-

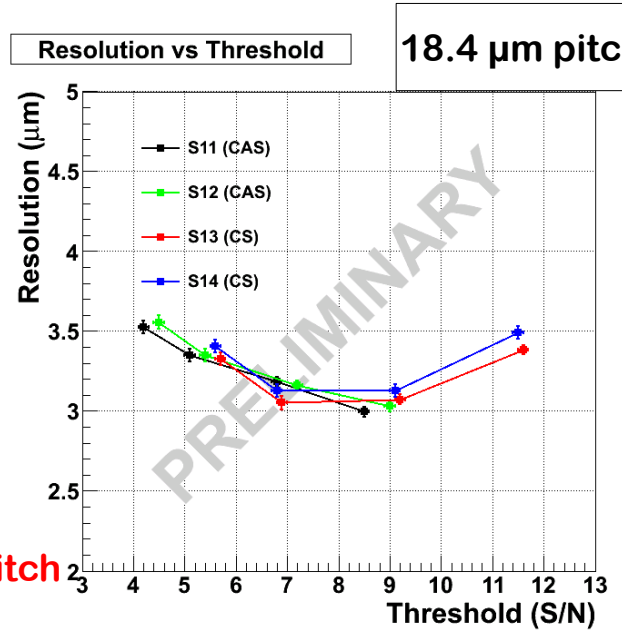


Discussed later

Improvements observed

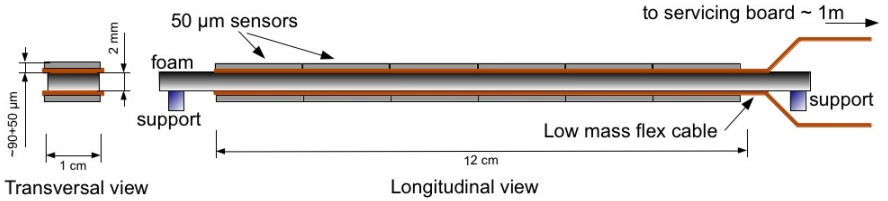
- Lower fake hit rate achievable @ ~100% efficiency
  below 1 hit/frame on the full matrix
- Spatial resolution reaches 3µm: -0.5 µm with same pixel pitch
- Performances stability with irradiation under study



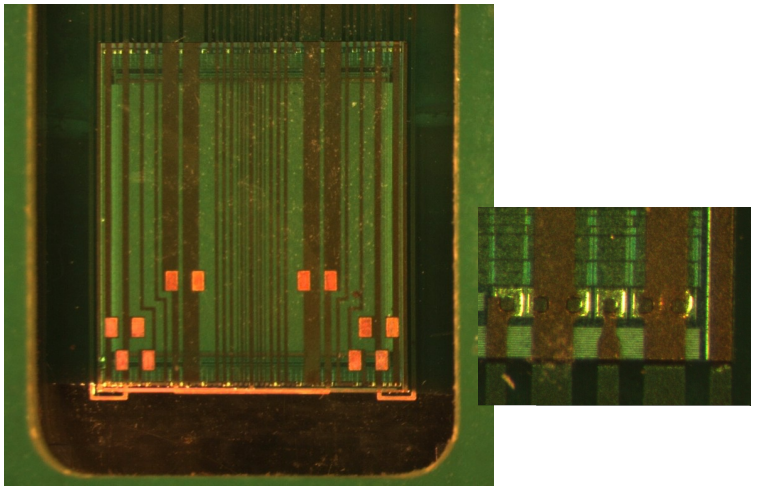


Integration studies

- **The PLUME project (see Ingrid Gregor's talk)**
  - **Double sided ladder (2x6 Mimosa 26) @ 0.3% X0**
  - **Passive cooling: air flow**
  - **Power pulsing**
  - **Collab.: Bristol U., DESY, Oxford U., IPHC**
  - **Several iterations over 2009-2012 (Current proto @ 0.6%X0)**
    - **Classical "secured" sandwich: separated parts bonded together**



- **An "aggressive" alternative: SERWIETE**
  - **Embed an ultra-thin sensor in a custom made flex cable**
    - **cable+sensor sheet ≤ 0.15 % X0**
    - **"single" operation**
  - **Collab.: IKF-Frankfurt, GSI-Darmstadt, IPHC**
  - **Technology provided by IMEC-Belgium**
  - **First trial with an analog sensor of ~0.5 cm² ongoing**

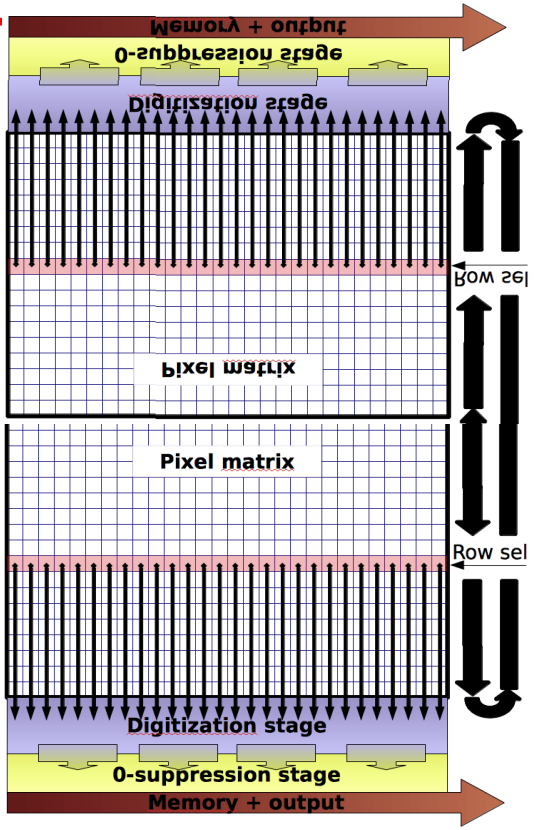


MIMOSA 18 embedded on a 50µm kapton, 1µm Cu cable

- **Other alternative with stitching: all-silicon ladder**

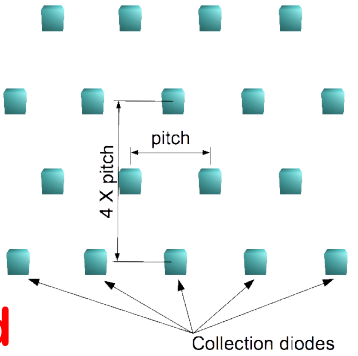
Next step 1: final architectures

- **Two-sided readout with small pitch sensor**
  - MIMOSA 29, AMS 0.35 µm OPTO
  - Pitch 16x16 µm²
  - Two-sided readout → 50 µs readout time
  - Submission in 2011



- **4-bits digital sensor**
  - MIMOSA 30, AMS 0.35 µm OPTO
  - Several ADC prototypes already studied (low power & area)
  - Readout time ≤ 100 µs
  - Studies on analog sensor with off-line digitization : $\sigma_{s.p.}$ ~ 2 µm with a 20 µ
  - Submission in 2011

- **Elongated pixel sensor**
  - Already studied with MIMOSA 22 AHR (2010)
  - Pitch 18.4 µm x 73.6 µm tested (last week) with 120 GeV π-
    → 100 % efficiency, $\sigma_{s.p.}$ ~ 6 µm



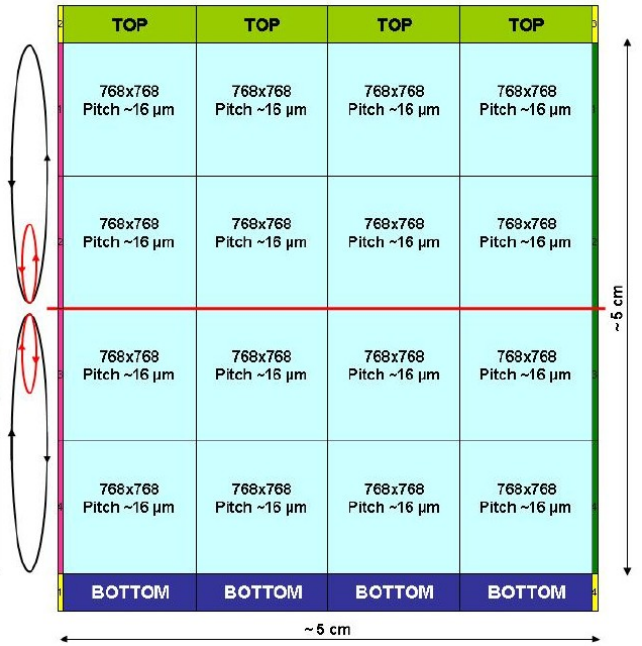
⇨ large pitch validated

  - Final version: pitch 16 µm x 64 to 80 µm for $t_{r.o.}$ ~ 10 µs

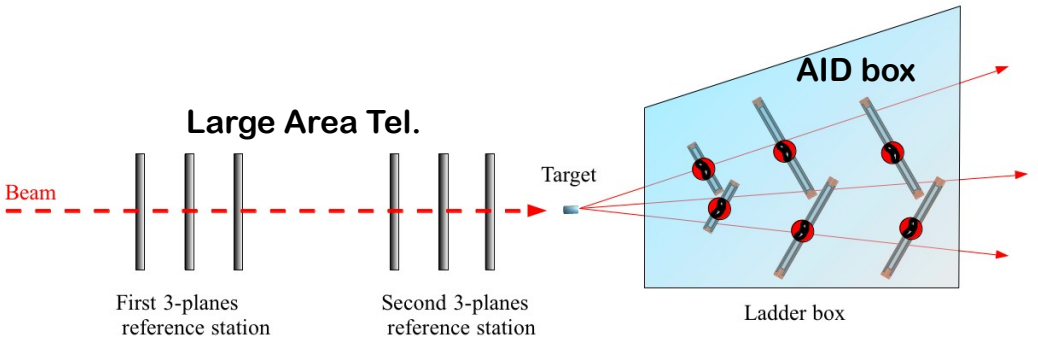
Next step 2: bigger systems

- **Within the AIDA FP7 project (2011-2014)**

- **Large Area Telescope**
  - Provide a facility for beam test with 5x5 cm² sensitive area
  - Produce stitched sensors (could be interesting for ladder integration)
  - Operation of final architecture sensors (inner layer)



- **Alignment Investigation Device: AID box**
  - Performance assessment of double ladders in "real" environment
    - Power pulsing operation
    - Air cooling
  - Alignment strategy development
  - Use PLUME ladders



AIDA setup

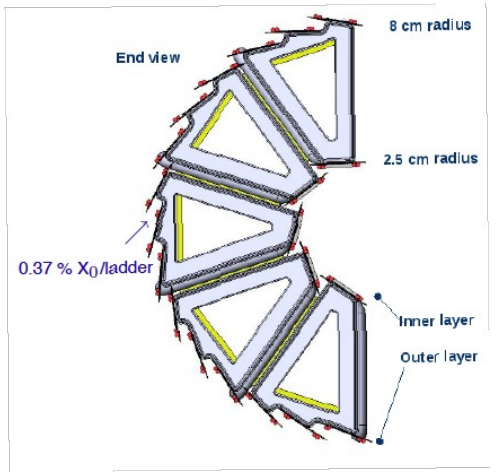
Next step 3: VDSM process

- **Motivations for Very Deep Sub-Micrometer processes**
  - Smaller pitch → Better spatial resolution
  - Higher number of metal layers + smaller feature size → Smaller insensitive area
  - Lower line capacitance → Higher clock freq. (+15 to 20%) → increased readout speed
  - Thinner gate oxyde → Higher ionizing radiation
- **2010**
  - Design analog sensor **MIMOSA 27 in XFAB 0.18 µm OPTO**
    - 16.4 kPixels over 10 mm^2 with **16 different pixel options**
- **2011 & 2012**
  - In-beam tests of MIMOSA 27
  - Design of building blocks for column // binary readout
    - In-pixel CDS matrix + discriminator
    - Zero suppression logic and readout memomries
- **2013**
  - **Submission of full size, complete functionalities, prototype**

Non-DBD activities

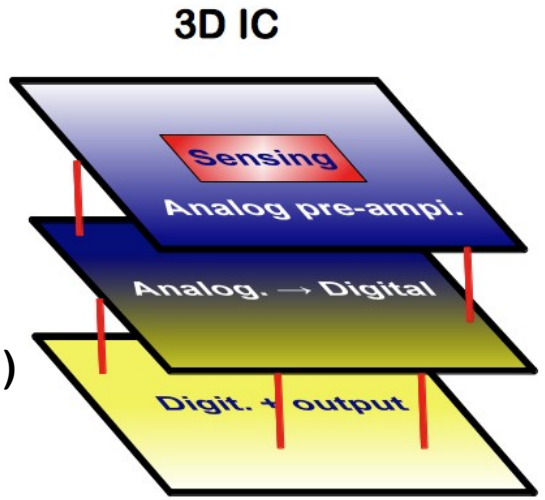
The first vertex detector with CMOS sensor

- STAR @ RHIC: heavy ion collisions
- With LBNL
- ULTIMATE sensor ~2x2 cm^2 @ $t_{r.o.}$ ~ 200 µs
  based on MIMOSA 26
- Single material budget ~0.37 % X0
- Submission 2010, physics by 2013
- Other VXD following (CBM@SIS, ALICE@LHC, …)



Exploiting the full CMOS technological potential

- 3D integration technologies → 1 functionality per tier
- From "standard" CMOS pixel (granular, thin & fast)
  To "intelligent sensors" (granular, thin, ultra-fast, ultra-rad.tol.)
- Targets: ILC 1TeV, CLIC (5-10 ns)
- CAIRN series, started in 2009 within international HEP consortium



SUMMARY

NOW

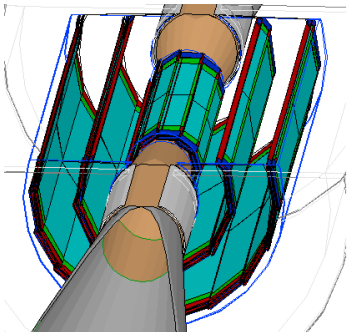
- Fast binary architecture validated on full scale sensor
- $t_{r.o.}$ = 85 µs (for 576 rows), $\sigma_{s.p.}$ ~ 3 µm @ 18.4 µm pitch
- ≥ 99.5 % efficiency for ≤ 10^{-6} fake hit/pixel @ 3.10^{12} n_{eq}/cm^2 + 150 kRad

ILD-DBD 2012

- Prototypes for each layer validated
- 16x16 µm² @ 50 µs / 16x64 µm² @ 10 µs / 16x16 µm² + 4bits-ADC
- Ladder demonstrator at ~0.3 % X0

Besides ILD-DBD

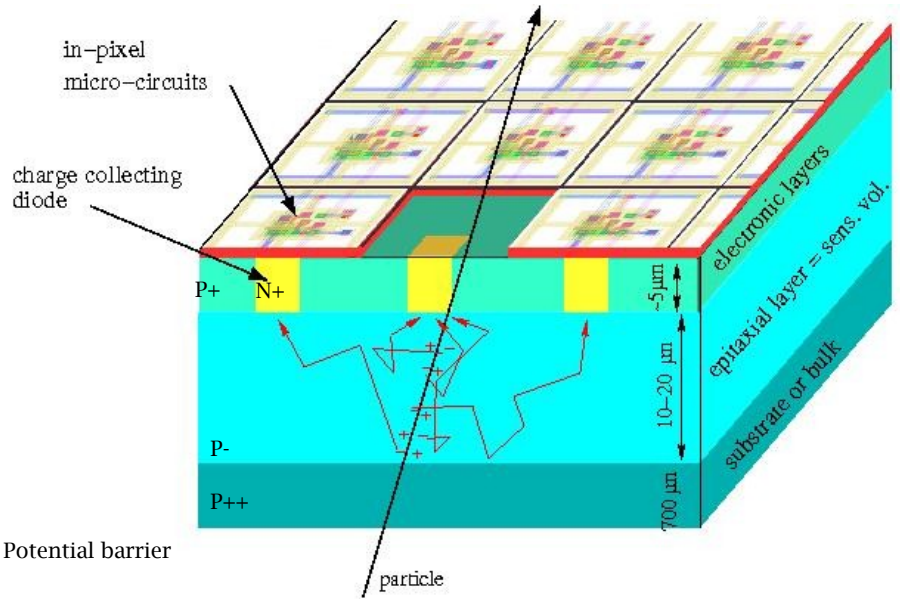
- From 2012: real physics with CMOS pixels (c-tagging, …)
- 3D sensors
  - Road to CLIC requirements
- Large surface with large pitch
  - Road to larger tracker



BACKUPs

MAPS, the basics

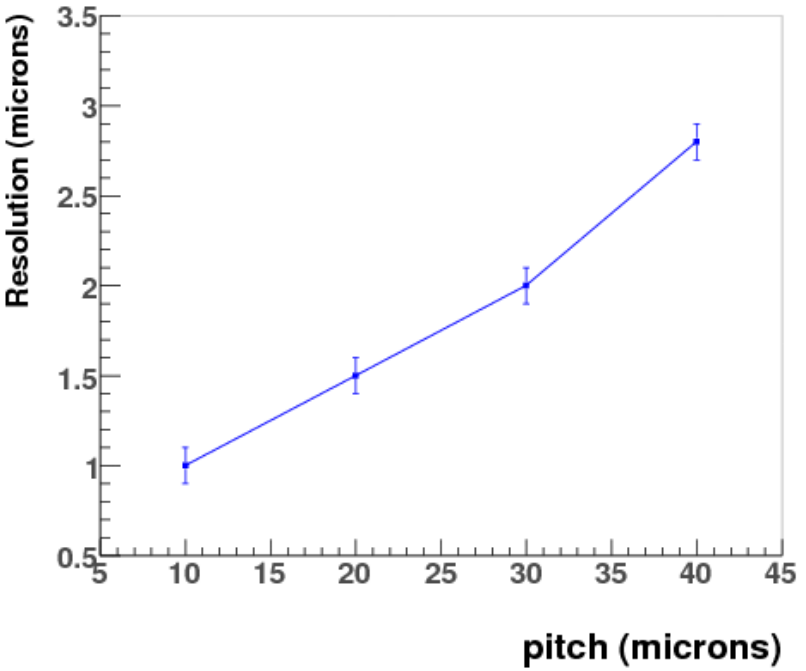
- **Technology**
  - Industry standard for ICs
  - All processes not optimized
    - Epitaxial layer thickness
    - # metal layers
    - Nwell – Psubstrate junction



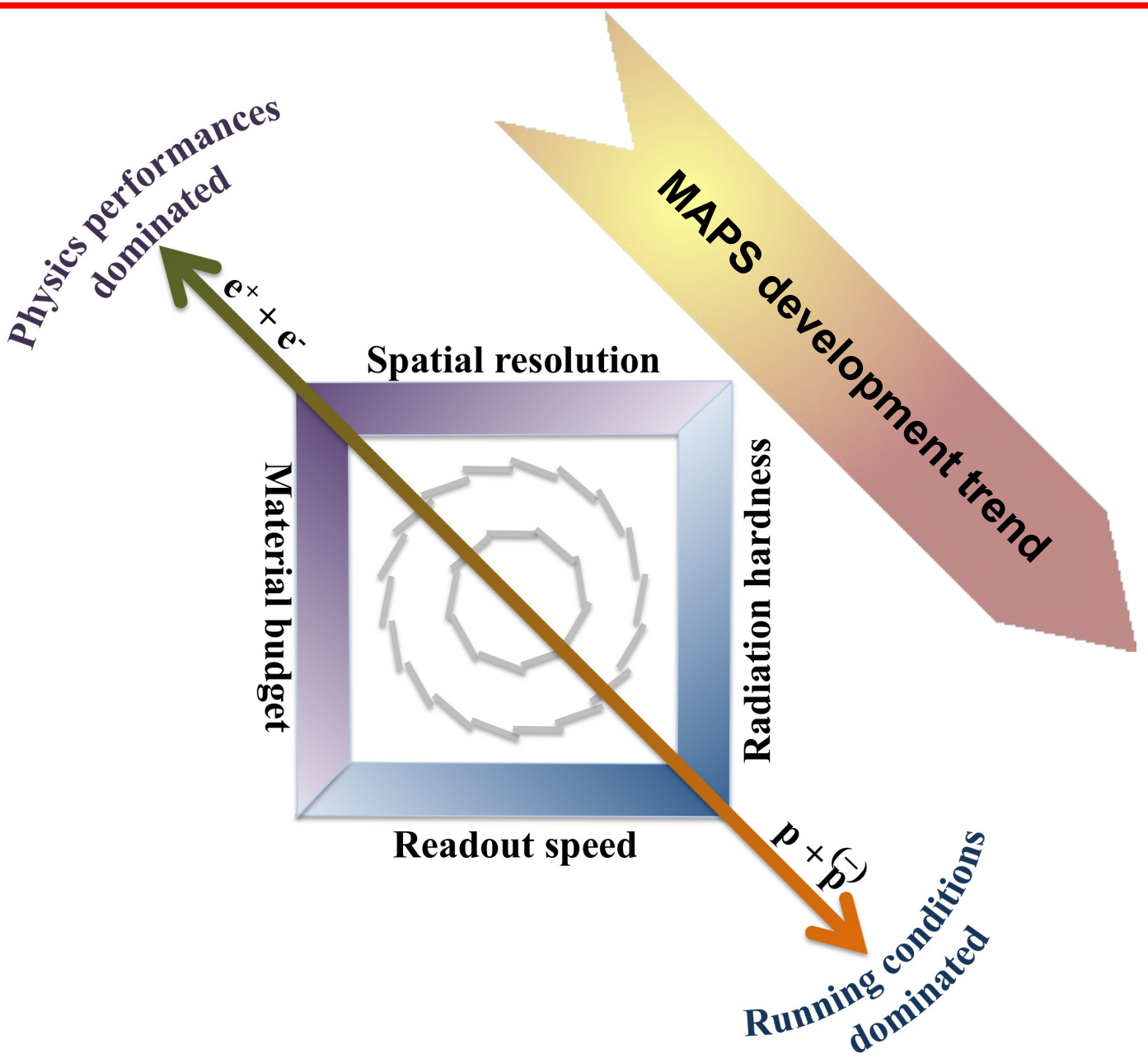
- **Intrinsically thin sensors**
  - sensitive layer ~10-20 µm
    - Small MIP signal, few 100 e- per pixel → **requires low pixel noise *O*(10 e-)**
  - Substrate almost useless
    - Few µm enough, total thickness could reach 20 µm
  - Monolithic & active
    - No external IC required in vicinity

MAPS, standard performances

- **From the MIMOSA family**
  - Developed at IPHC-Strasbourg
  - AMS 0.35 µm process, ~11 µm epitaxial layer
  - 3 transistors pixel - Sequential analogue readout
  - Performances assessed also @ **50 µm thickness**
    - Thinning routinely achieve by industry
- **Hit rate**
  - With parallel **analog outputs**
  - 1Mpixels **~ 1ms r.o, time**
- **Radiation tolerance**
  - Ionizing: **~Mrad**
  - Non-ionizing: **few 10^{12} n_{eq}/cm^2**
  - Integration time and temperature dependant



Vertex detector figures of merit

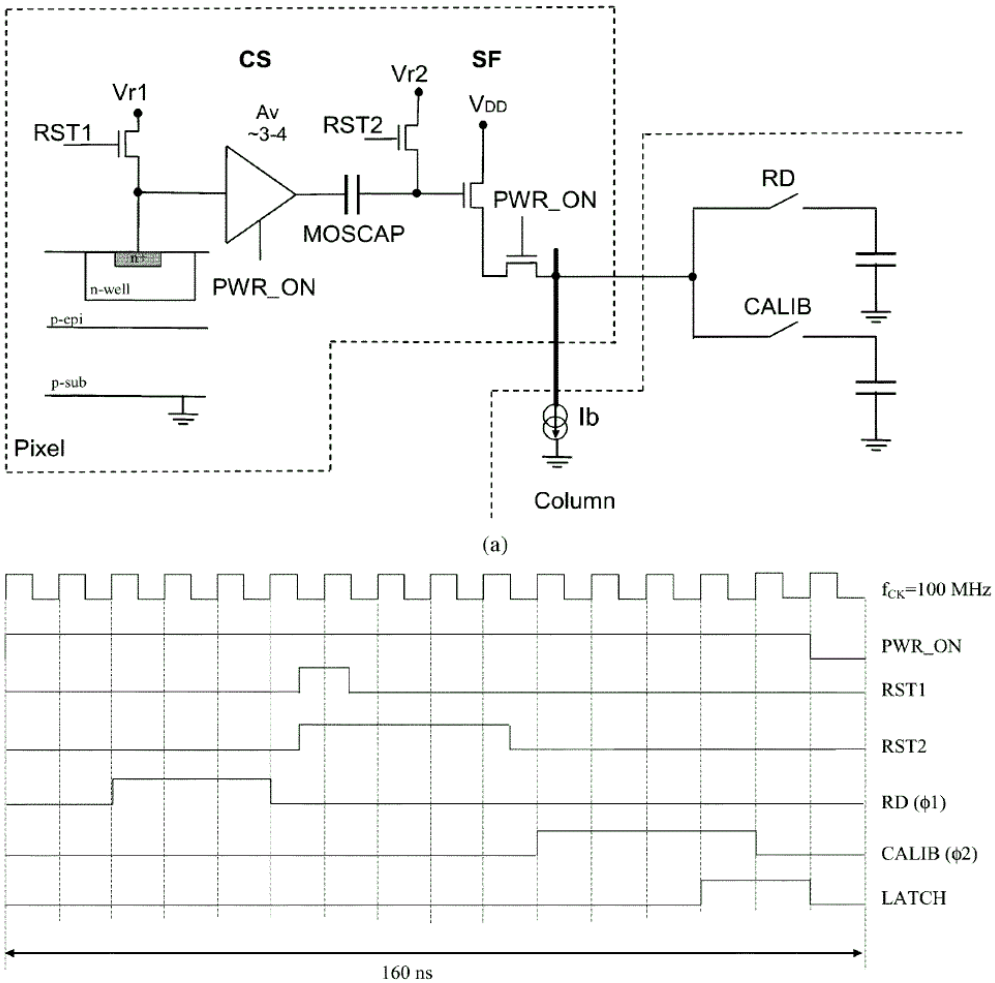


Chronogram of column // readout

- **Parameters driving**

  the readout time of a single row

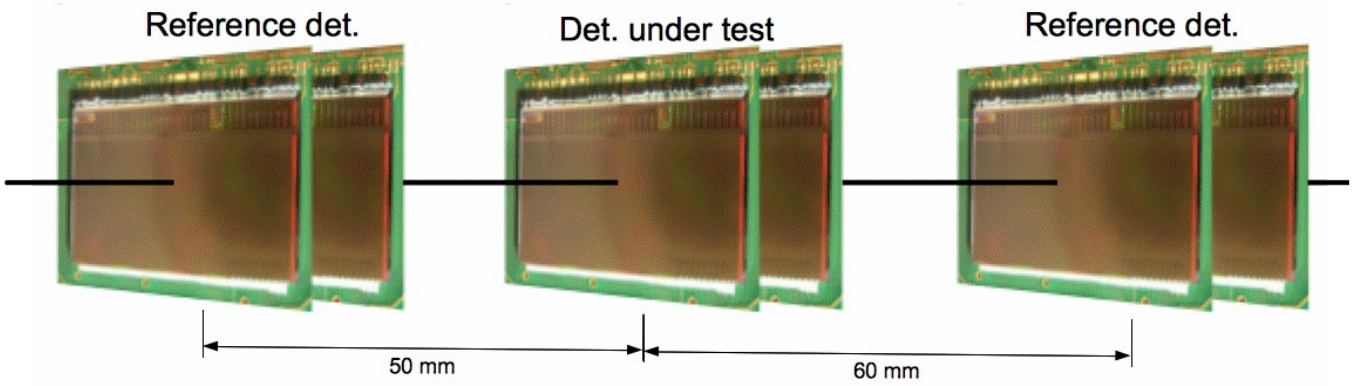
  - Clock frequency
  - Duration of each control signal, the latter is impacted by
    - Column length
    - Process feature size



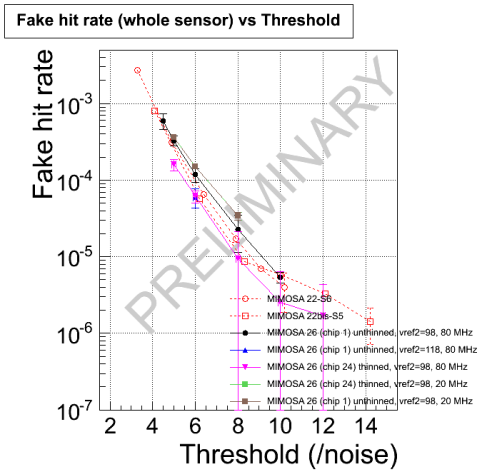
MIMOSA 26 performances

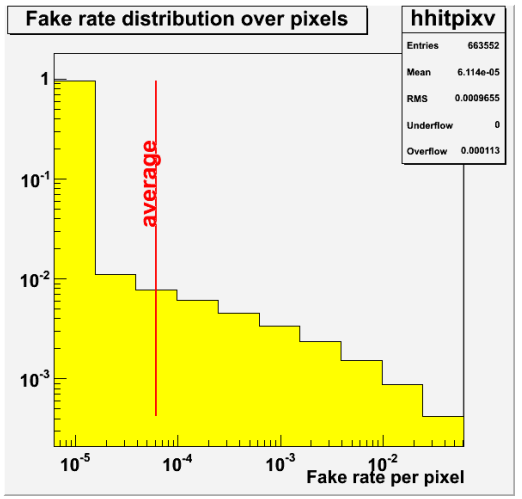
Beam test setup

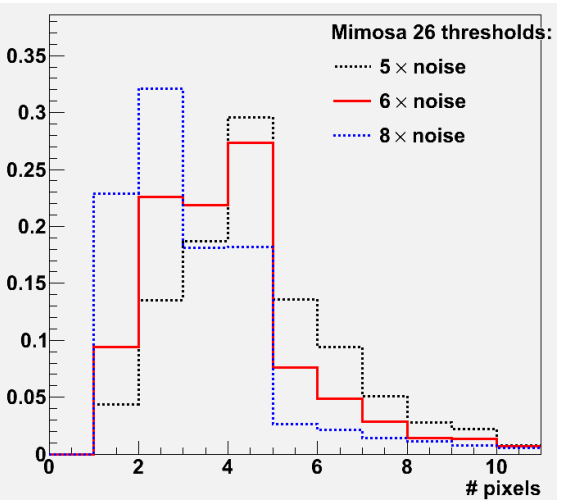
- 2009 & 2010 campaigns at CERN SPS with 120 GeV π-
- Using IPHC DAS based on NI-PXI digital IO board → event rate ~ kHz
- Operating at 80 MHz ($t_{r.o.}$ = 115 µs) and T=20 °C (80 Mbits/s @ output)



Thresholding strategy validation







Time resolution in rolling-shutter