AHCAL electronics integration status

Mark Terwort

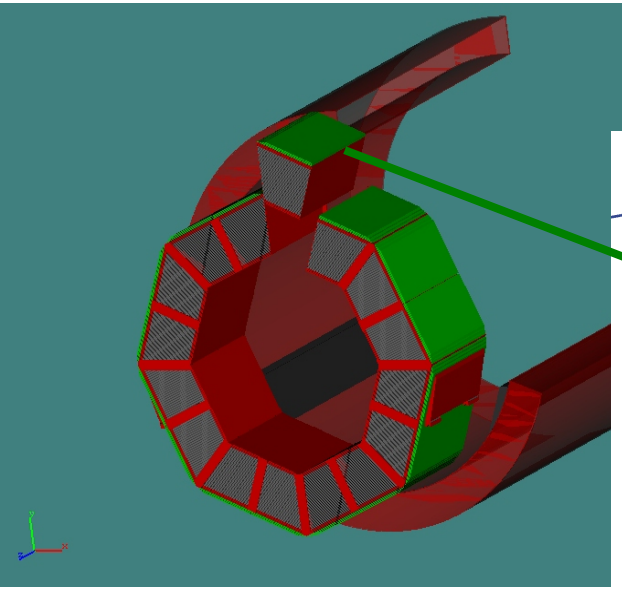
ECFA meeting

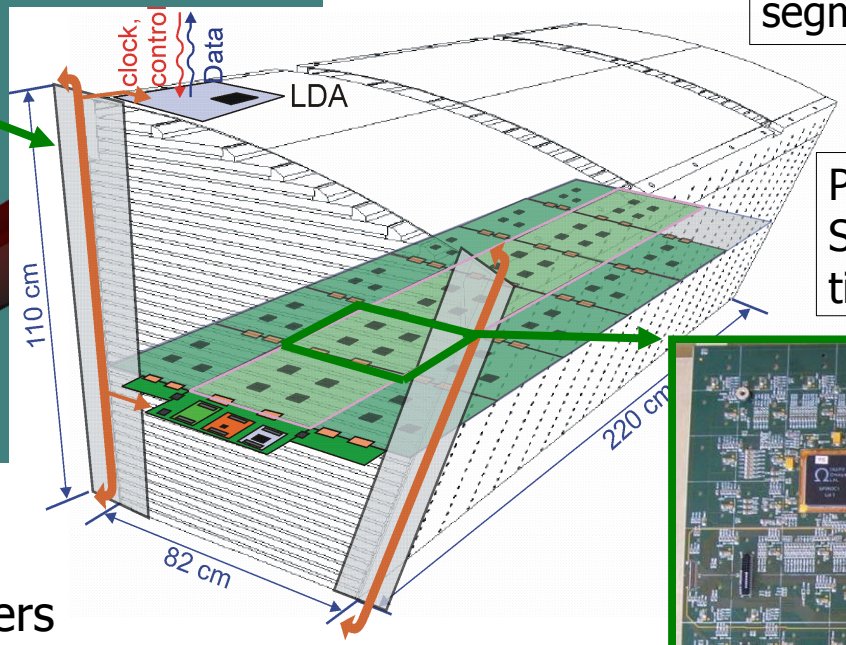
21.10.2010

- Status of electronics/DESY activities
  - Next generation electronics status
  - Testbeam and charge injection setups and results
  - LED calibration systems
- Summary and outlook

The technological AHCAL prototype

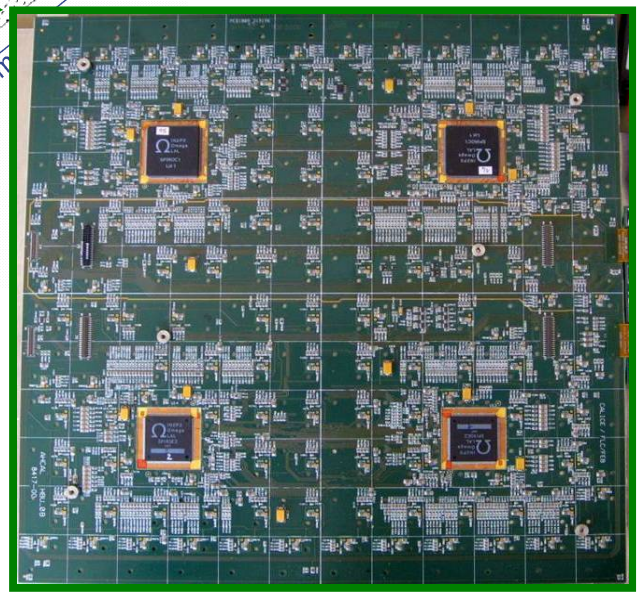
Development of scalable LC detector based on successful experience with physics prototype





Octagonal shape, 16 equivalent wedges, segmented in two along z

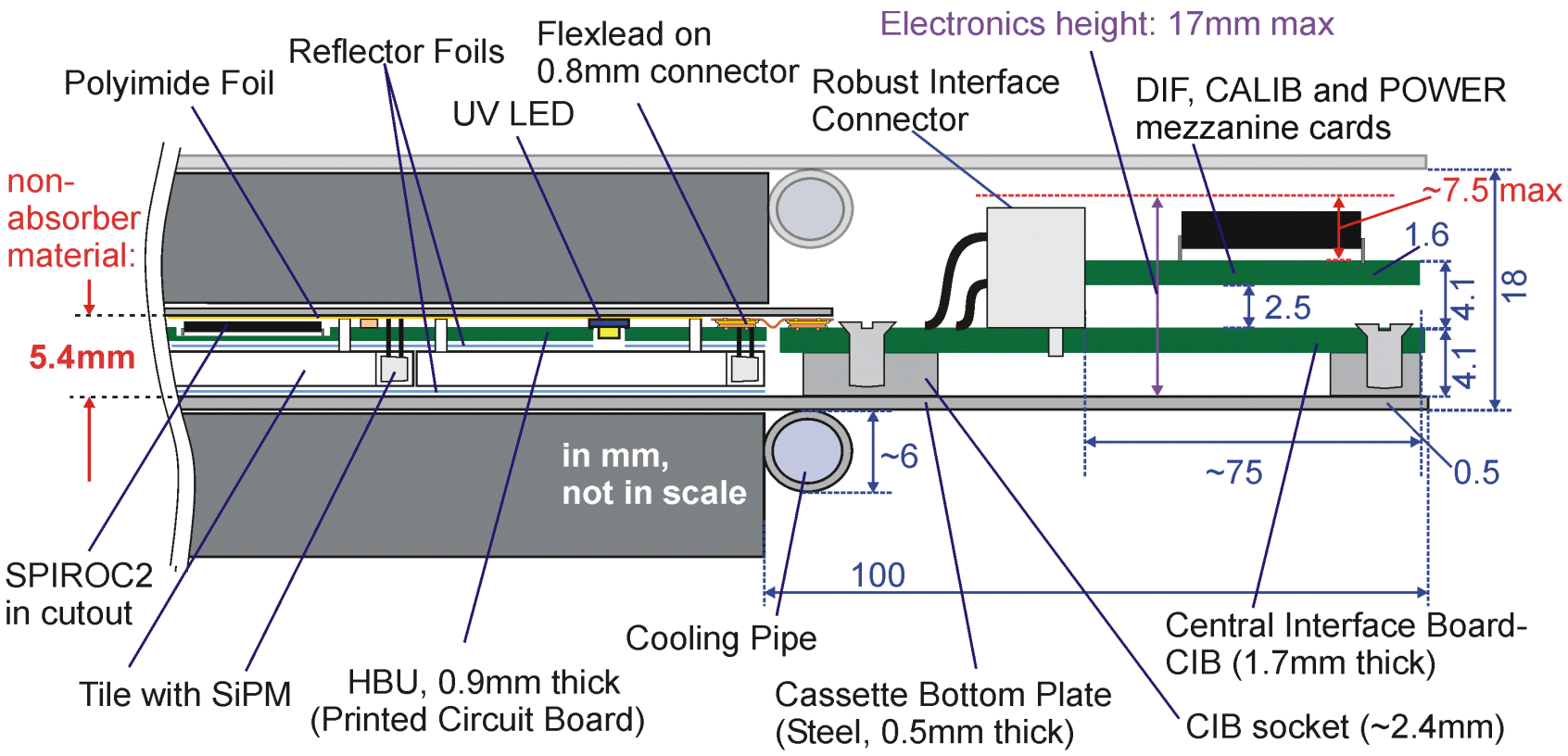
PCB board with 4 SPIROCs, 144 scintillator tiles, SiPM readout



- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

→ Integrated readout electronics

AHCAL layer – cross section



- Redesign and production of subcomponents ongoing or finished (DIF, CALIB2, POWER2, HBU2, CIB, Flexleads (SIB not needed yet))
- Compliant with steel and tungsten options

The SPIROC2

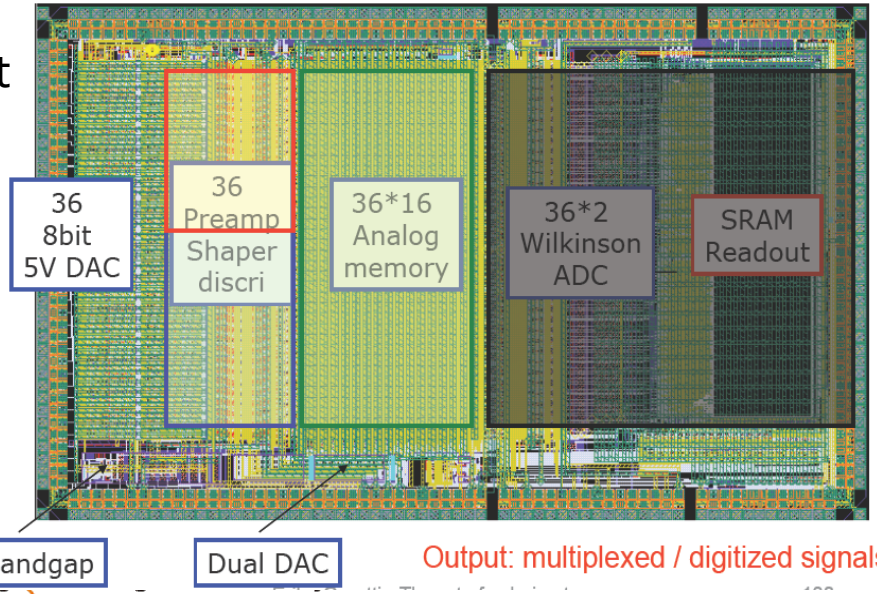
Specific chip for SiPM readout:

- Input DAC for channel-wise bias adjustment

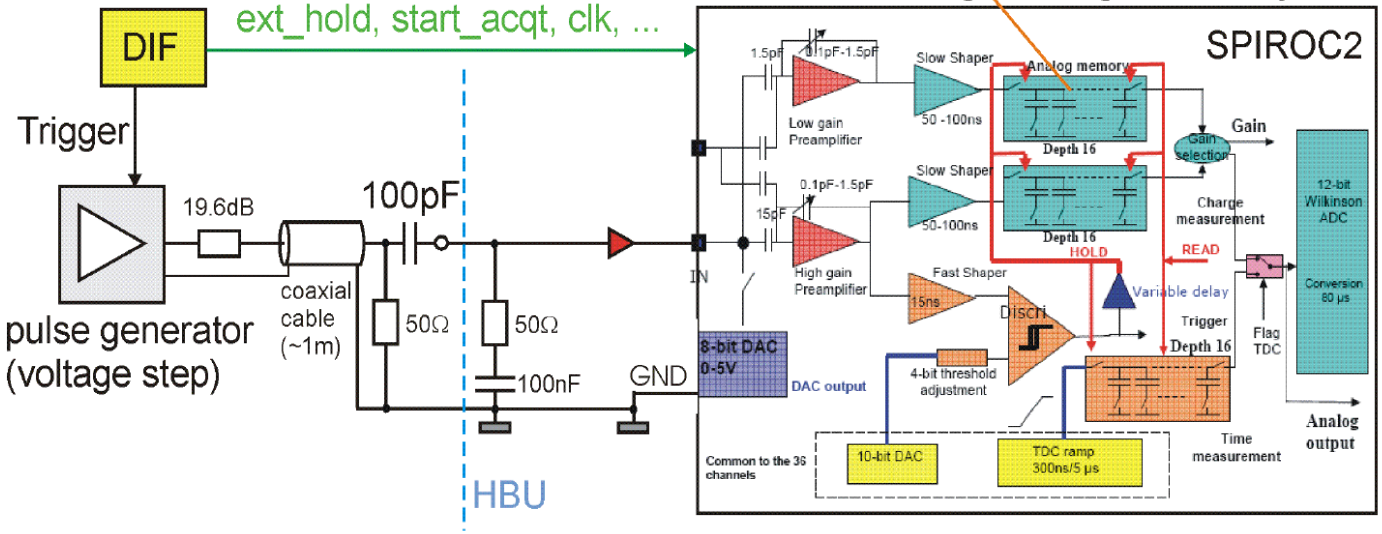
Designed for ILC operation:

- Power pulsing → 25µW/ch
- Dynamic Range 1-2000pe with dual-gain setup per channel
- Internal ADC
- Autotrigger mode
- Time stamp (~100ps)

SPIROC layout (CALICE chip for Analog HCAL readout)



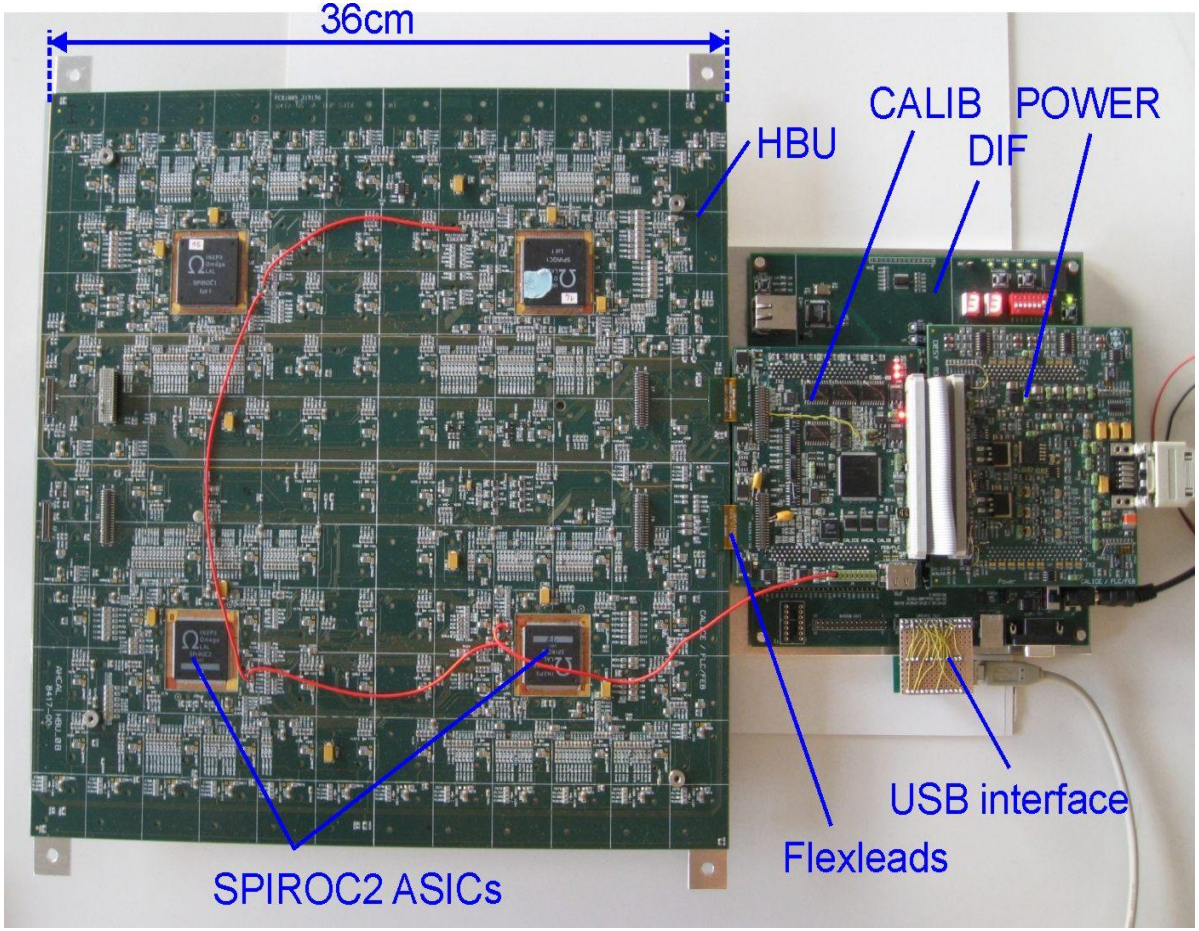
Output: multiplexed / digitized signals



Charge injection setup

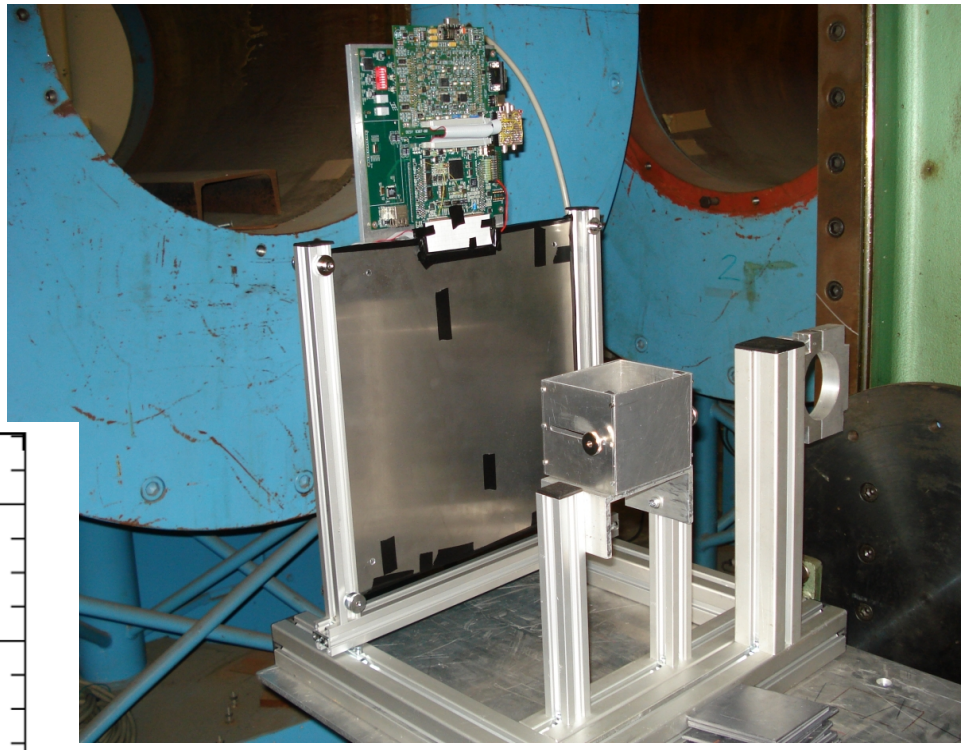
Current AHCAL electronics setup

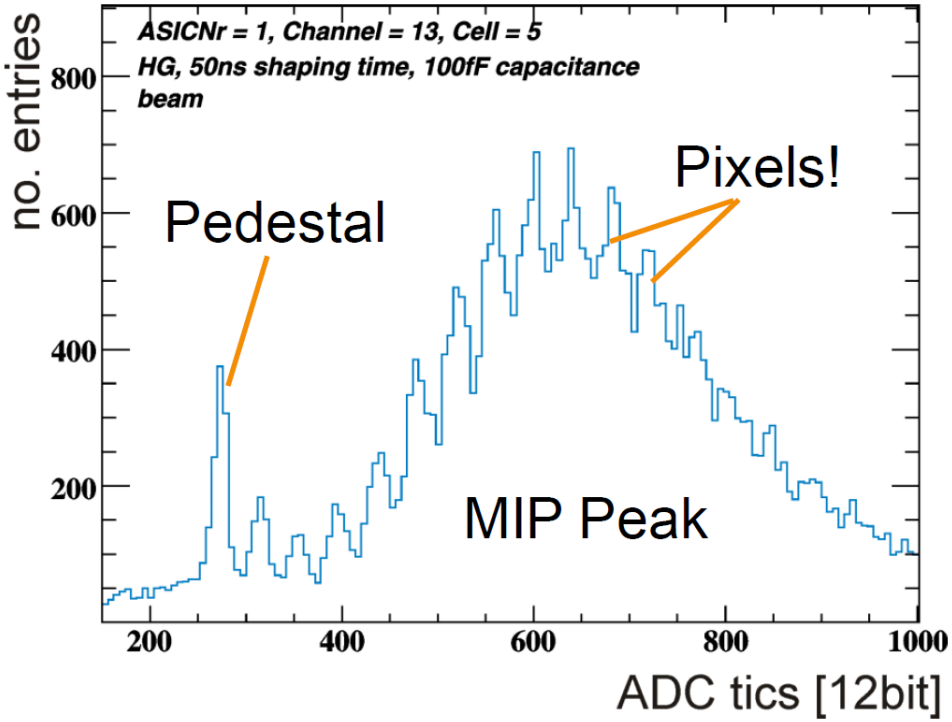
- At DESY 2 setups (HBUs) available
- 1 for charge injection and LED calibration tests
- 1 for testbeam operation with 2GeV electron beam
- Multiple tests performed and issues discussed with Omega
  - SPIROC2a/2b just arrived at LAL
  - SPIROC3 design ongoing
- Redesigns of boards currently ongoing



DESY testbeam setup

- Setup optimization, channel-wise calibration with MIPs
- MIP level: S/N ~ 45
- Single pixel level: S/N ~ 5.5
- SiPM gain: $G_{LED} = G_{MIP}$ ~ 30 ADC ch.

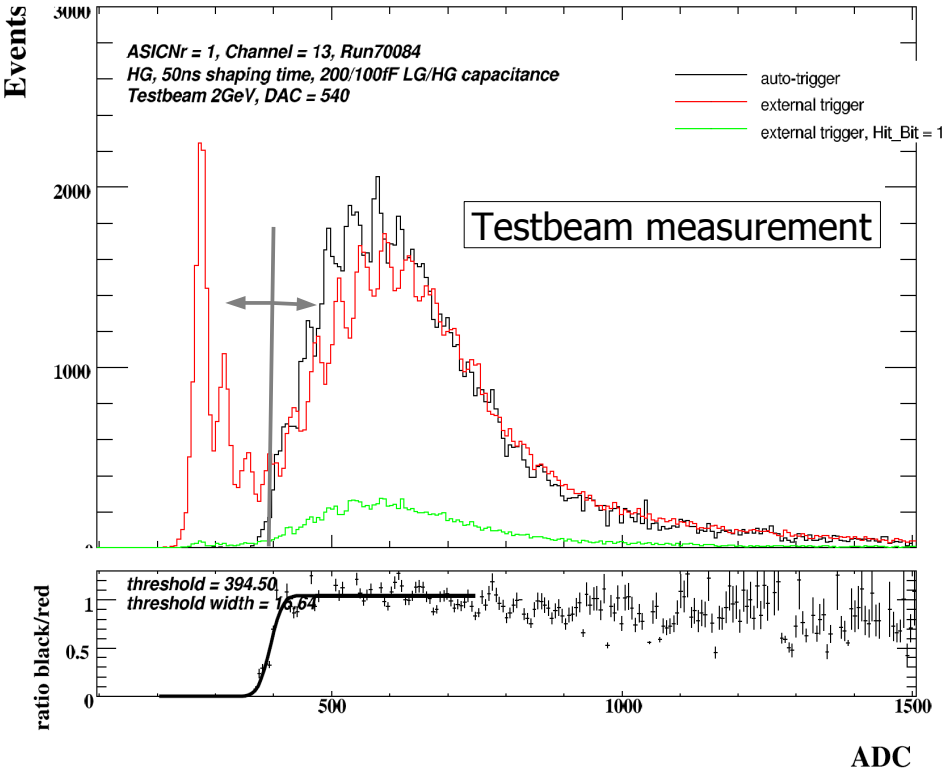


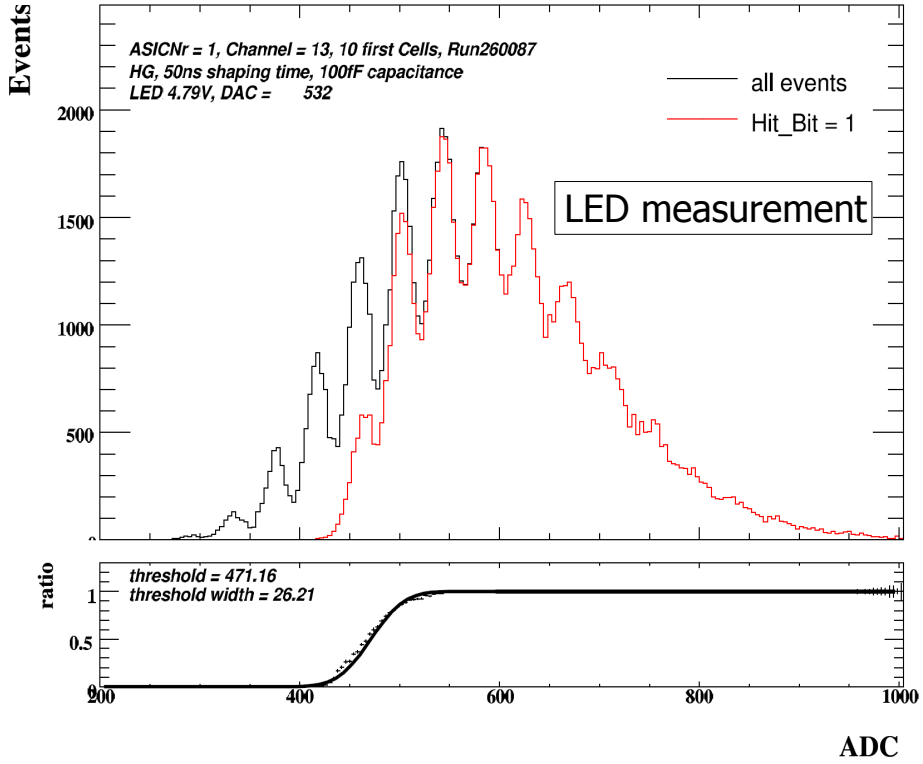


→ Very clear MIP signal with visible single pixels!

Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Efficiency studied with external trigger





Set threshold to

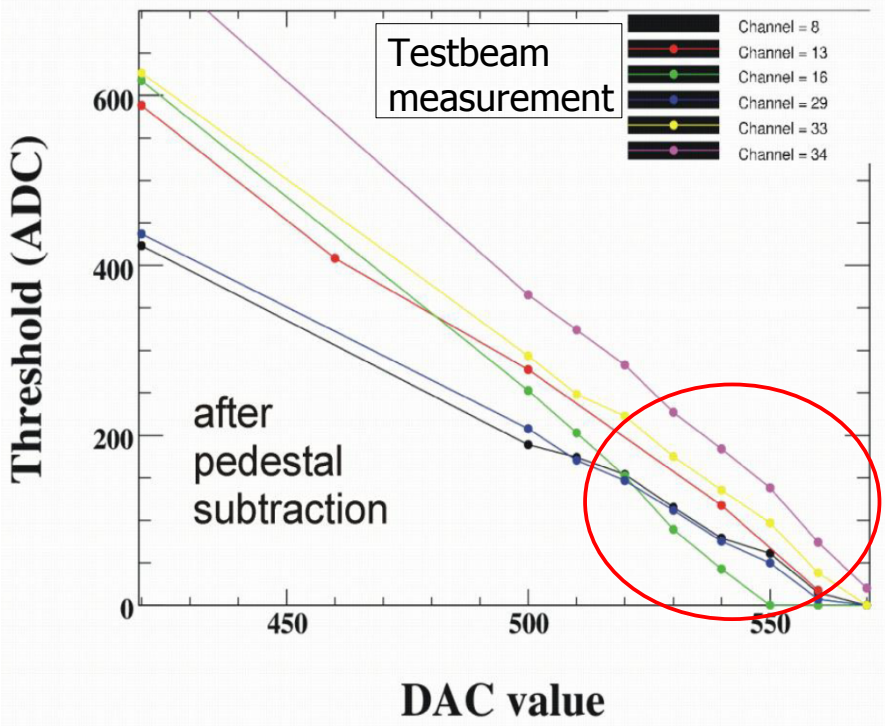
→ minimize noise hits (10^{-4})

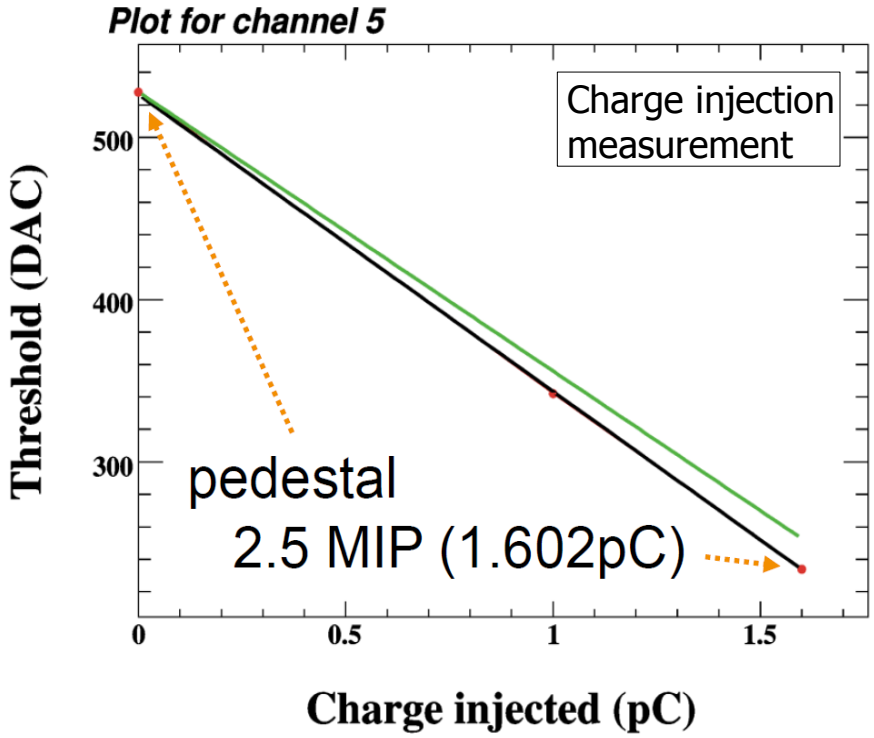
→ maximize MIP efficiency

Autotrigger threshold behaviour

- Characterisation of threshold behaviour
- Example:
  - Charge injection: ~182 DACtics/pC
  - Testbeam: ~191 DACtics/pC

    (8 pix, 350 ADC/MIP, gain $5*10^5$)





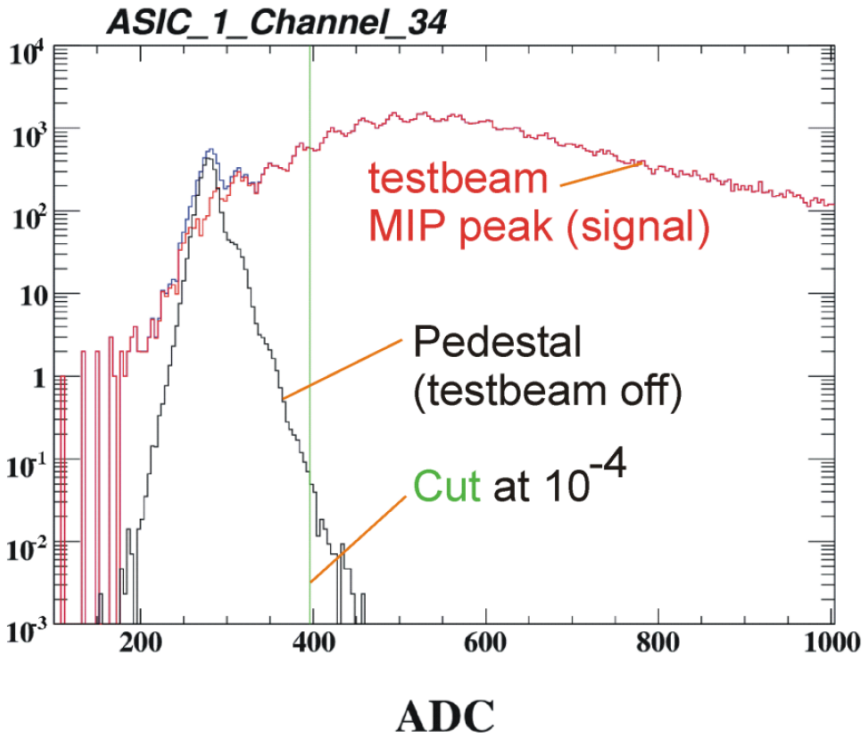
Large spread between channels

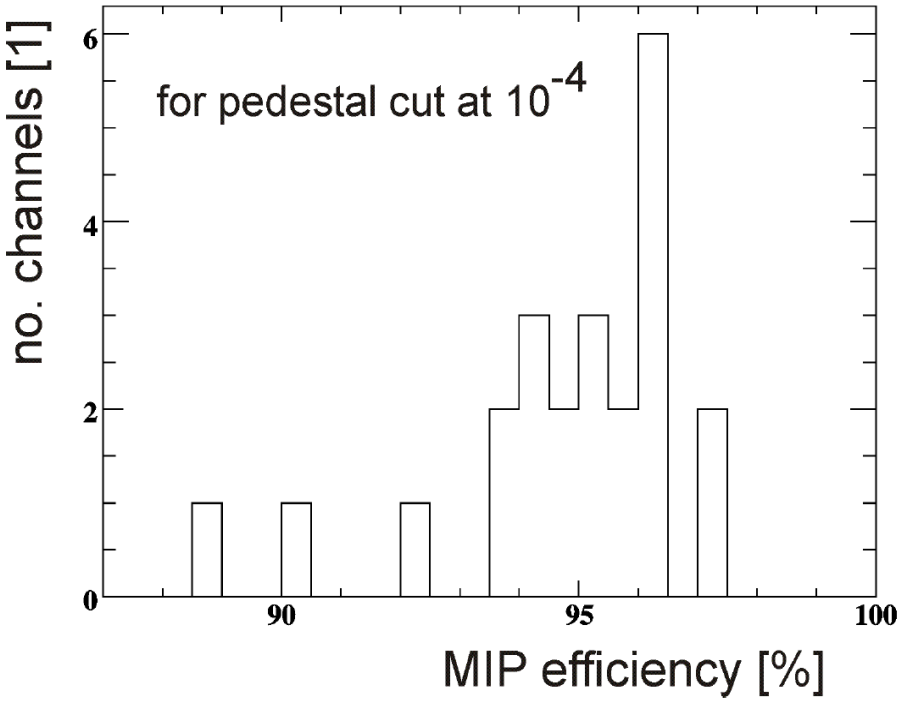
→ Channel-wise adjustment in SPIROC3

Autotrigger MIP efficiency

How noisy is the system?

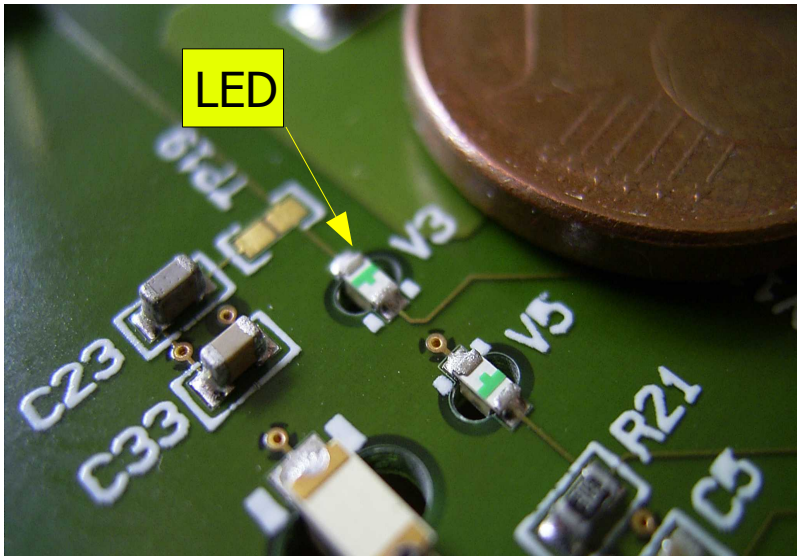
- Is the MIP efficiency high enough?
- Autotrigger threshold calculated channel-wise for 10^{-4} cut
- Keep in mind width of threshold!





→ MIP efficiency of ~95% achieved for pedestal cut at 10^{-4} for most channels

Wuppertal LED calibration system

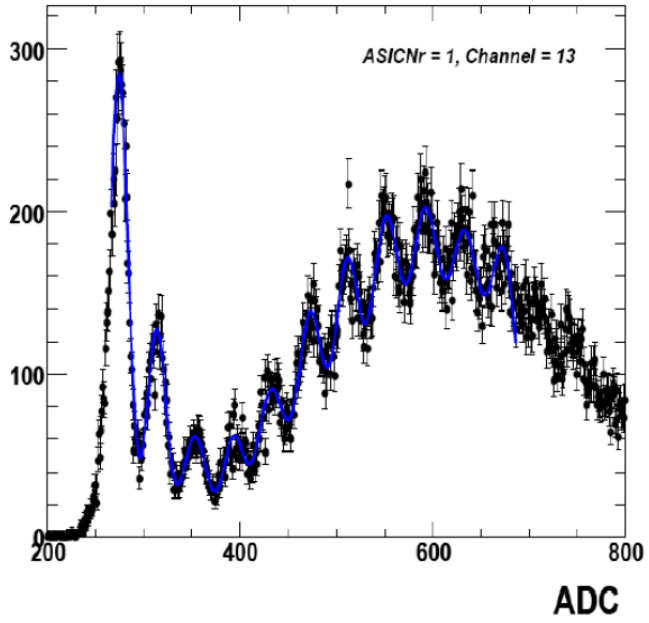


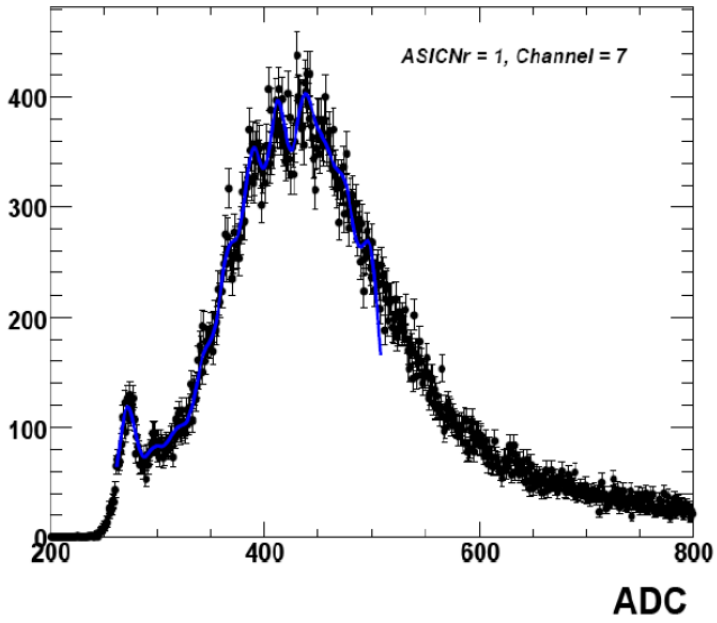
System task:

- SiPM gain calibration via single pixel spectra
- SiPM saturation curves

Wuppertal solution:

- Light directly coupled into the tile by 1 integrated LED per channel
- Multiple tests performed: uniformity, shifts...



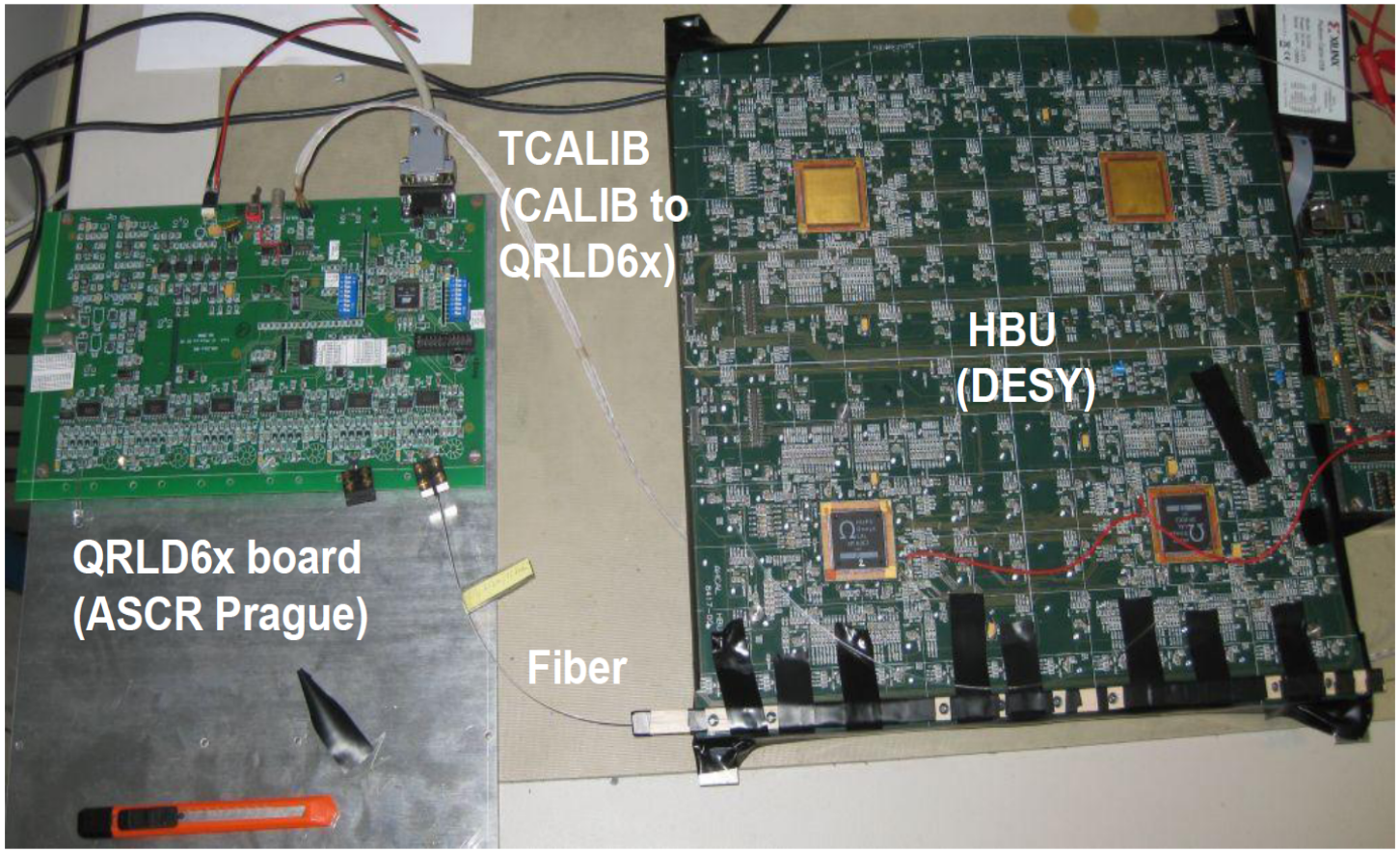


Development of automatic fit and gain extraction routines (here for testbeam MIP signals)

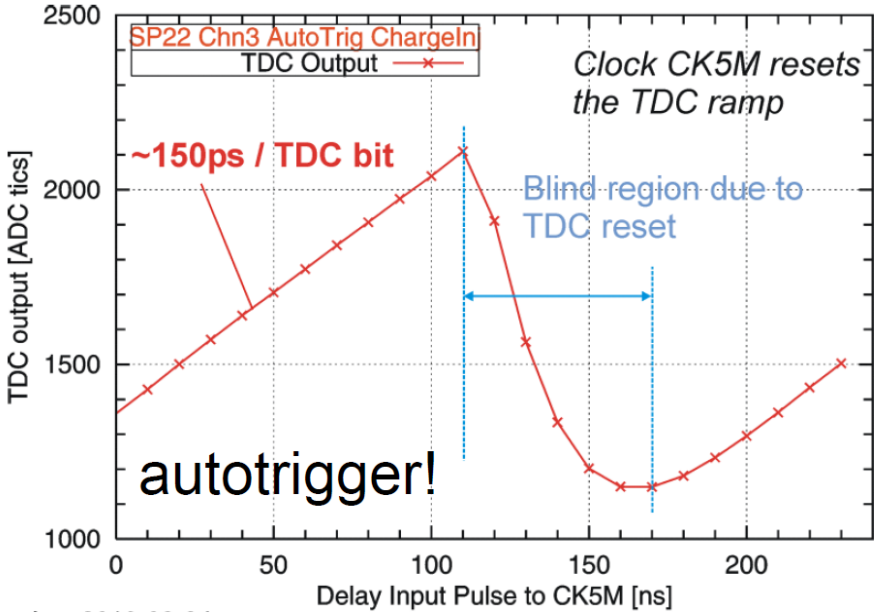
Prague LED calibration system

Second option for LED system (Prague solution):

- Light distributed by notched fibers
- First tests (including lab and testbeam measurements) promising



Next important steps

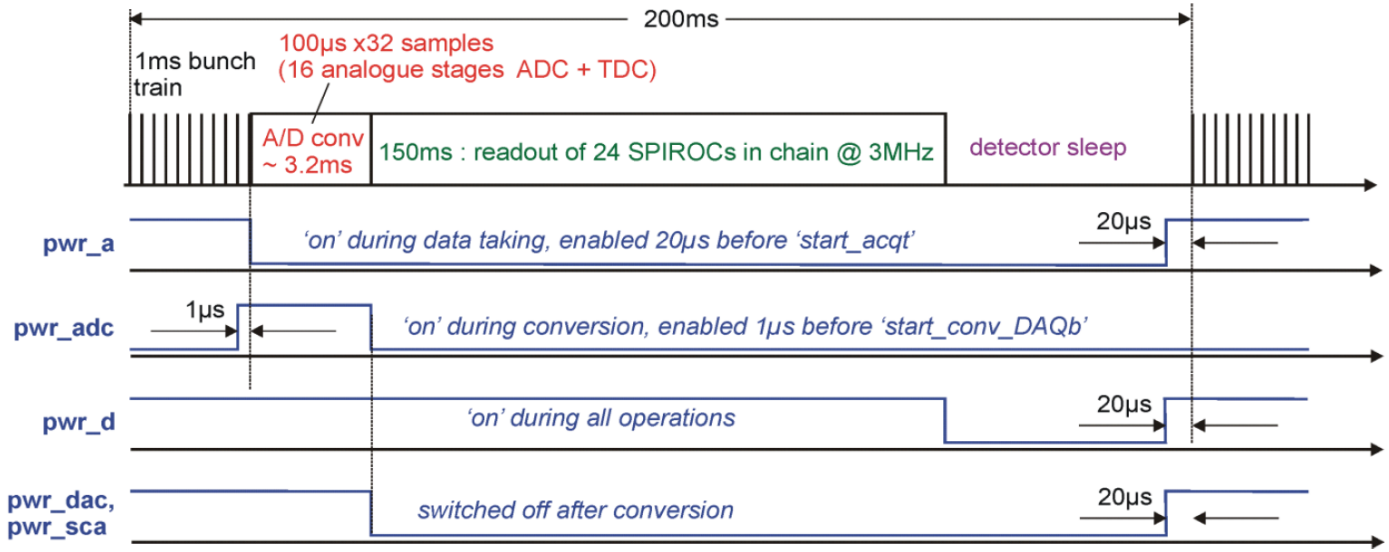


SPIROC2 TDC characterisation

- Just starting...
- First results already there...

SPIROC2 power pulsing

- To be started...
- No results yet...



Summary and outlook

- New technological AHCAL prototype under development
- 2 setups running in Hamburg
  - Successful testbeam operation and MIP calibration
  - Tests of SPIROC2 with charge injection
- Redesigns ongoing and partially finished
- LED calibration system development ongoing with 2 options

To do

- Test of TDC and power pulsing
- CALICE DAQ integration
- Start of SPIROC2a/b tests soon
- Integration to full slab (2.2m calorimeter layer)

Status redesigns

	DIF	CALIB2	POWER2	HBU2	CIB	SIB	Flexleads
concept dev., circuit design	X	X	X	X	X	X	X
schematic entry	NIU X	X	X	X	X	X	X
Layout	NIU X	X	X	X	X	X	X
Production	NIU X	X	X	X	X	X	X

X done

X in preparation

X not started yet