The second generation of the CALICE DAQ

Vincent Boudry
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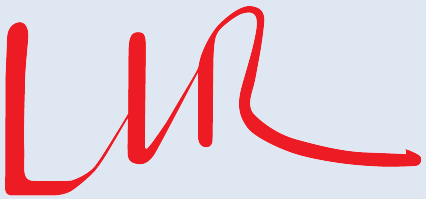
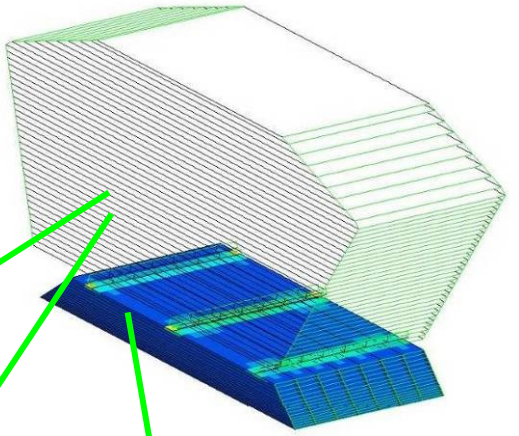


IWLC'2010
CICG, Geneva
20/10/2010

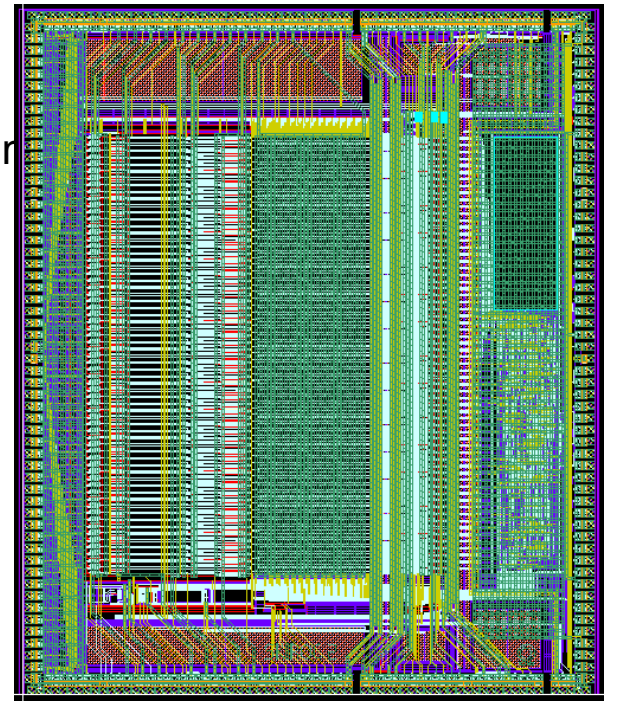
Second generation ASICs

FE electronics adapted for the ILC:

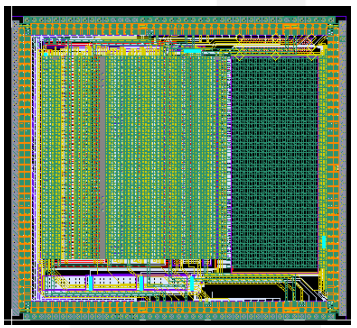
- Add **auto-trigger**, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)



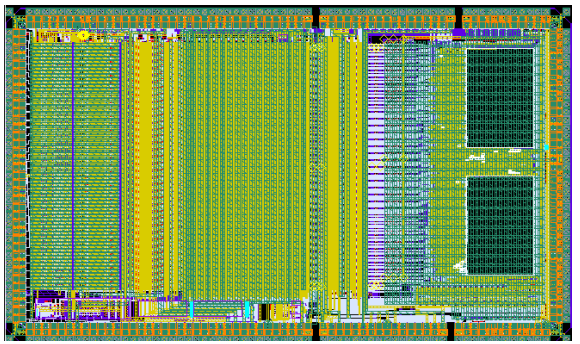
SKIROC2
ECAL Si
64 ch 70 mm



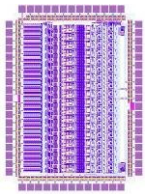
HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²



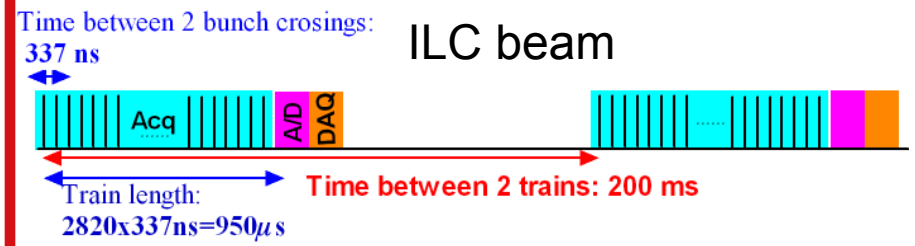
FLC_PHY3 (2003)

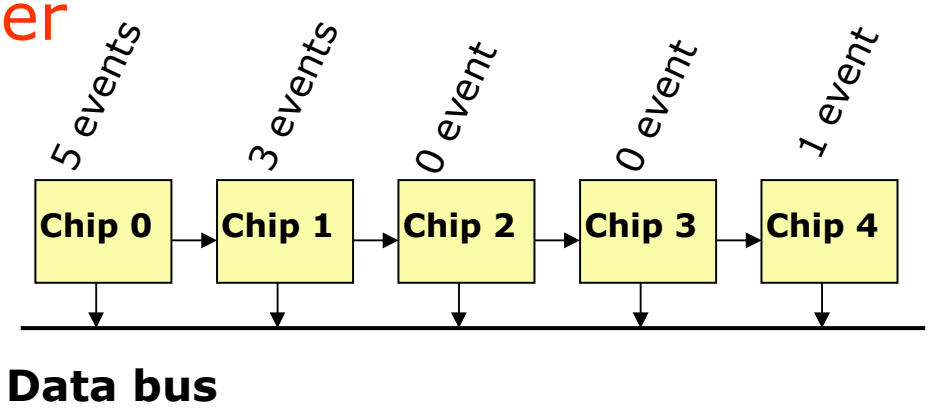


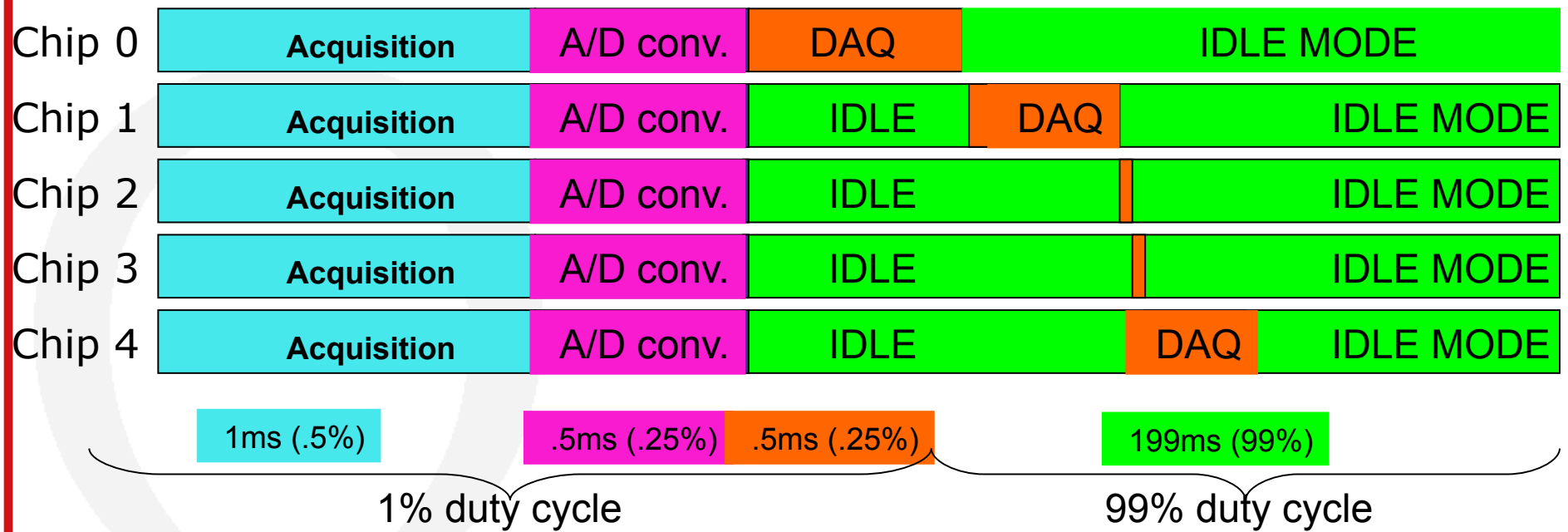
Slide from Ch. de la Taille

Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power







Slide from Ch. de la Taille

ECAL DAQ : data volume and rate

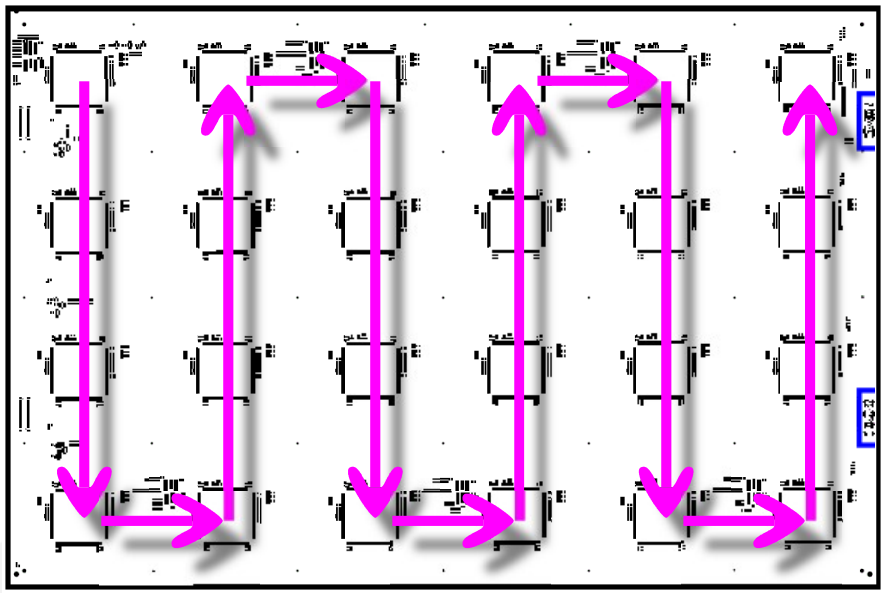
- Raw Data volume
  - 2 Bytes of Energy data/Channel, 20 Million channels
  - Raw data per bunch train ~ 20M ch ×5000 BX × 2B
    ⇒ 200 GBytes ECAL
  - No way to digitize inside the ~ ms train
  - 10 kbytes/channel/train ~ 50 kbytes/ch/s
  - Physics data rate : 90 MBytes/train = ~20 Bytes/ch/s

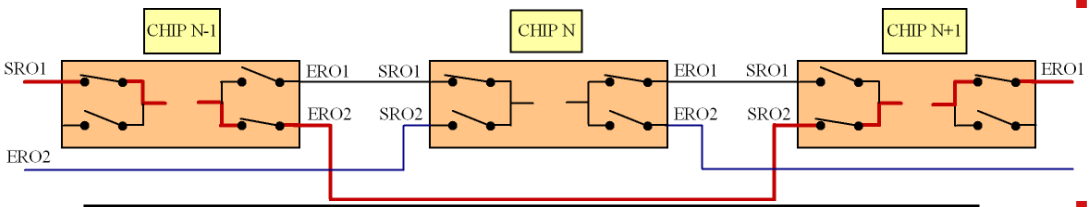
- Auto-trigger + Zero suppression mandatory
  - 10^3 rate reduction => drastic for power dissipation
  - Digitize only signals over ½ MIP with noise < MIP/10
  - Allow storage in front-end ASIC
    - Noise MUST be tamed

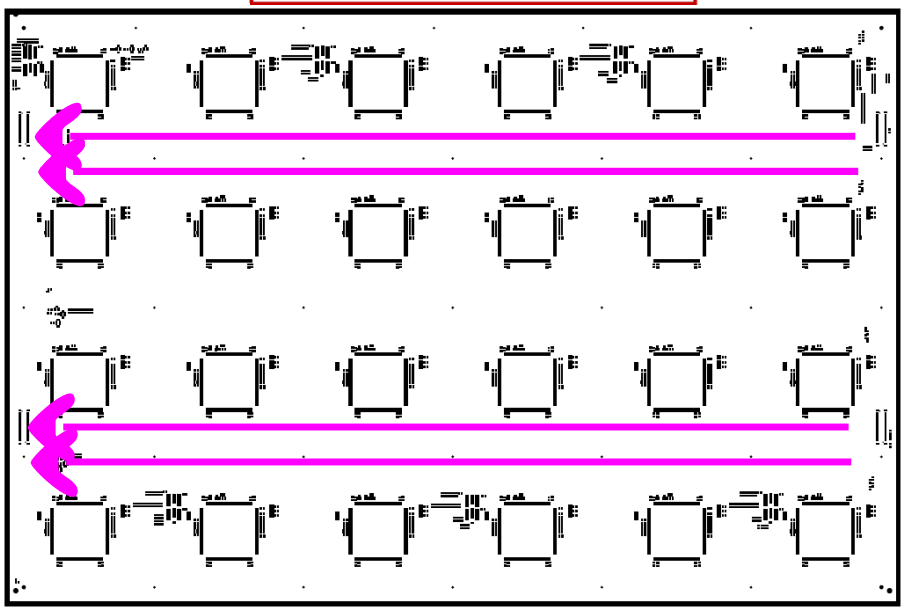
Slide from Ch. de la Taille

The ASU board: clock lines

- Clocks : 2 lines, drive every other chip, terminated at the end,
- 100 ohm resistance in series inside the chip
- **Clock switched off inside the chip when not used**







- Data : 4 lines : 2, doubled for redundancy
- Each chip has 2 data outputs that can be removed from each line by slow control

Slide adapted from Ch. de la Taille

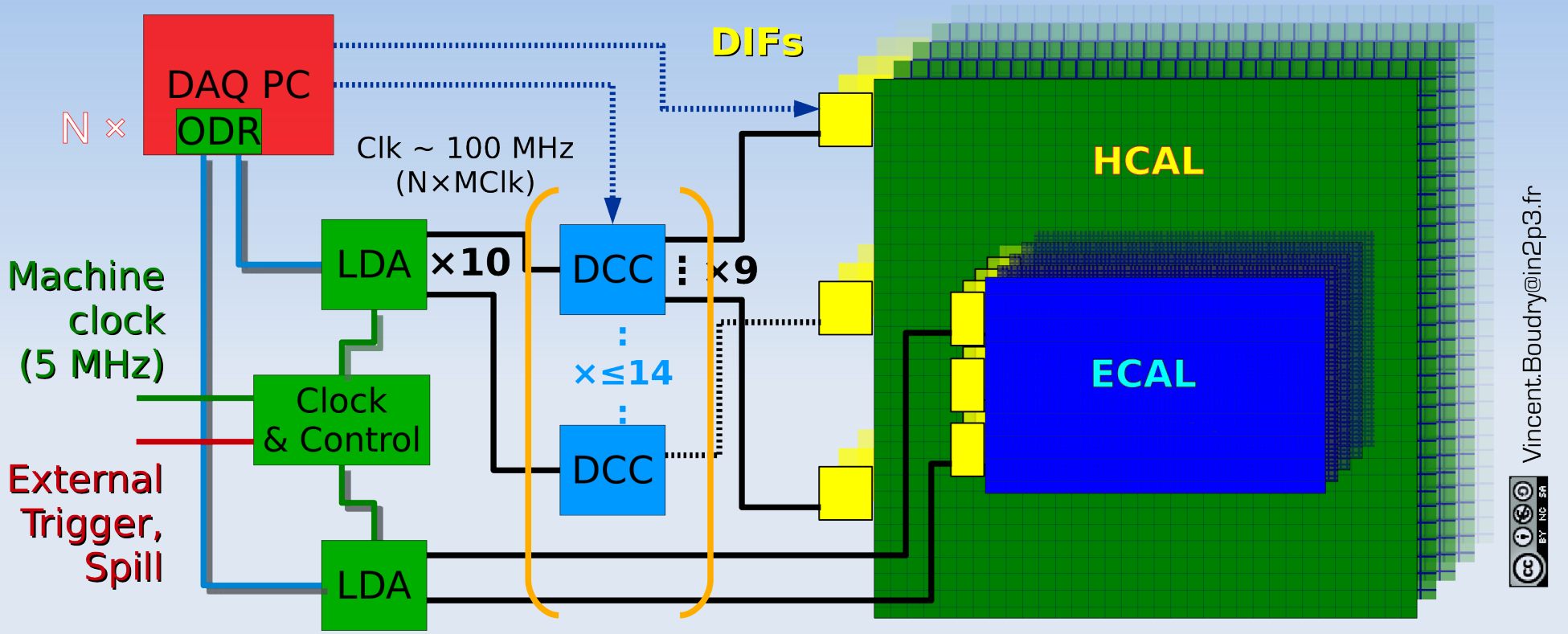
DAQ Task goal

Original ideas and R&D from CALICE-UK (UCL, Cambridge U., Manchester U., RHUL)

- "Generic" DAQ based AMAP on commercial boards
  - **Extensible** for Large Detectors + redundancy
  - **Flexible** → FPGA based : various acquisition modes (triggered, ILC-like)
- Provide the **digital** readout of CALICE embedded front end (*ROC chips) [1st gen was analogue]
  - All calorimeters seen through CALICE **standard** Detector **InterFace** board (**DIF**)
    - **Sends** configuration; fast commands; clocks; Triggers
    - **Receives** Data; Busy
  - 1 (opt. 2) **Concentrator** cards level
  - 1 **Clock and Control Card** (CCC) for the fast signal distribution and collection
  - Advanced Off-Detector Receiver (FPGA based event builder)
  - **All signals on 1 cables**; add-hoc **secure communication** protocol
    - "low speed" 8b/10b coding

- 3 CALICE prototypes en route:
  - SDHCAL : ~400.000 ch; Digital (2b/ch → 2.5 with BC information & fmt)
  - ECAL : ~ 22.000 ch; Energy (12b → 32.2)
  - AHCAL : ~ 52.000 ch: Energy & time (2×12 b → 32.3)

CALICE DAQ2 scheme



LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)

Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)

Optique (alt. Cable) GigE

Debug USB

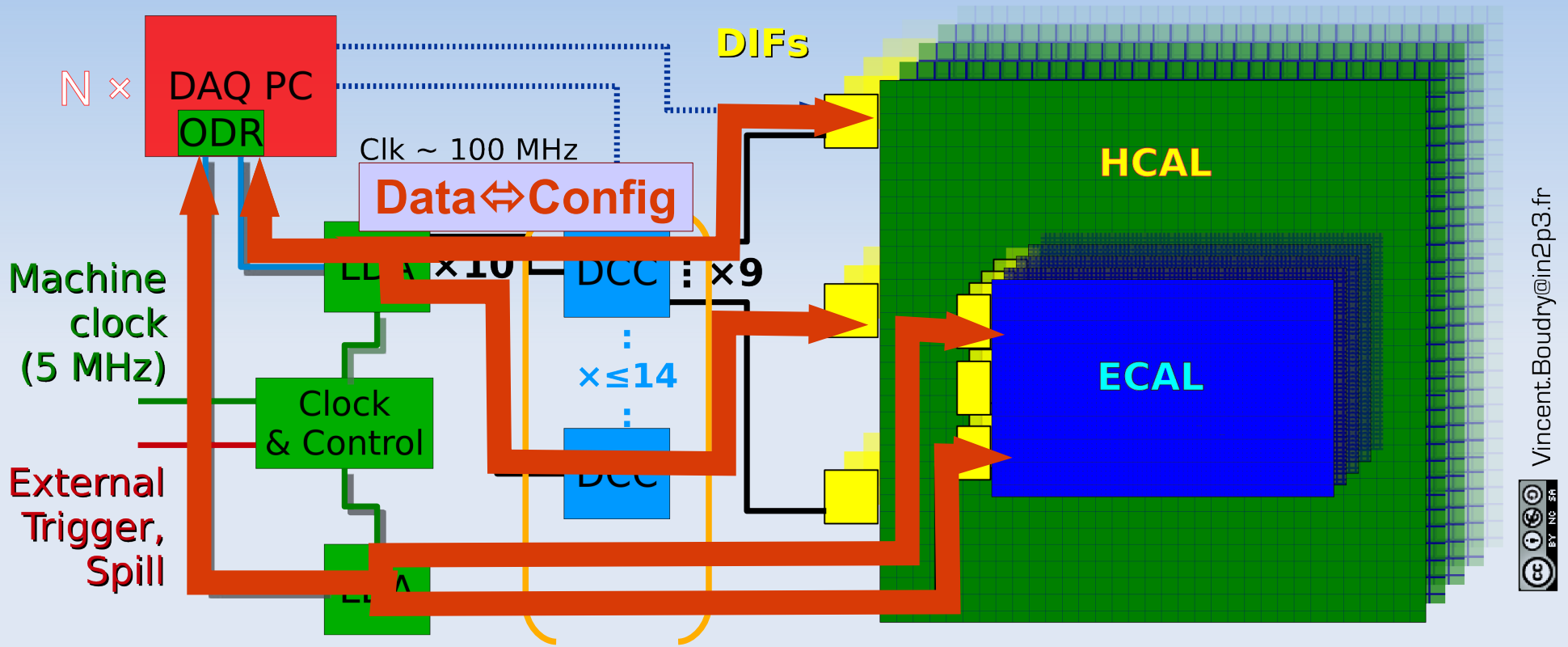
External Trigger

ODR = Off Detector Receiver
LDA = Link Data Agregator

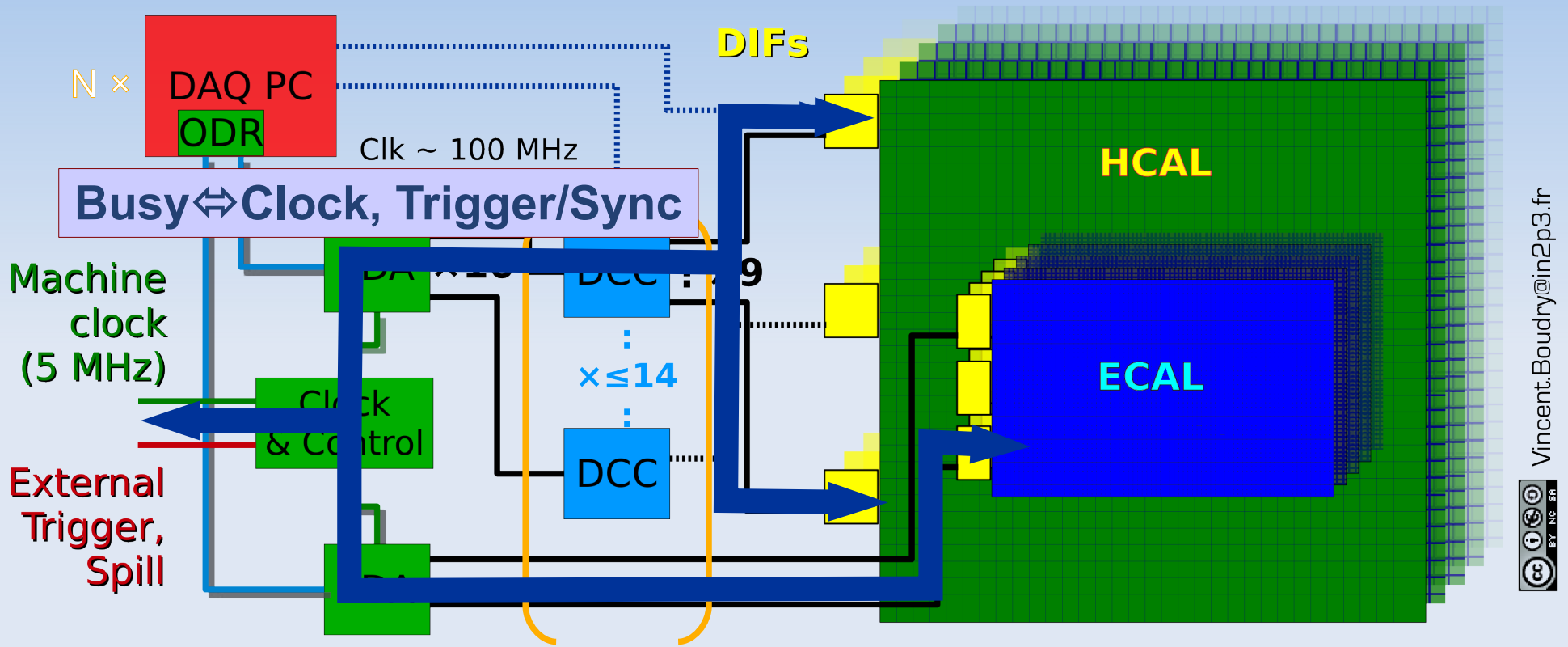
DCC = Data Concentrator Card
DIF = Detetcor InterFace

CCC = Clock & Control Card

CALICE DAQ2 scheme



CALICE DAQ2 scheme



LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)

Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)

Optique (alt. Cable) GigE

Debug USB

External Trigger

Detector InterFace (DIF) board

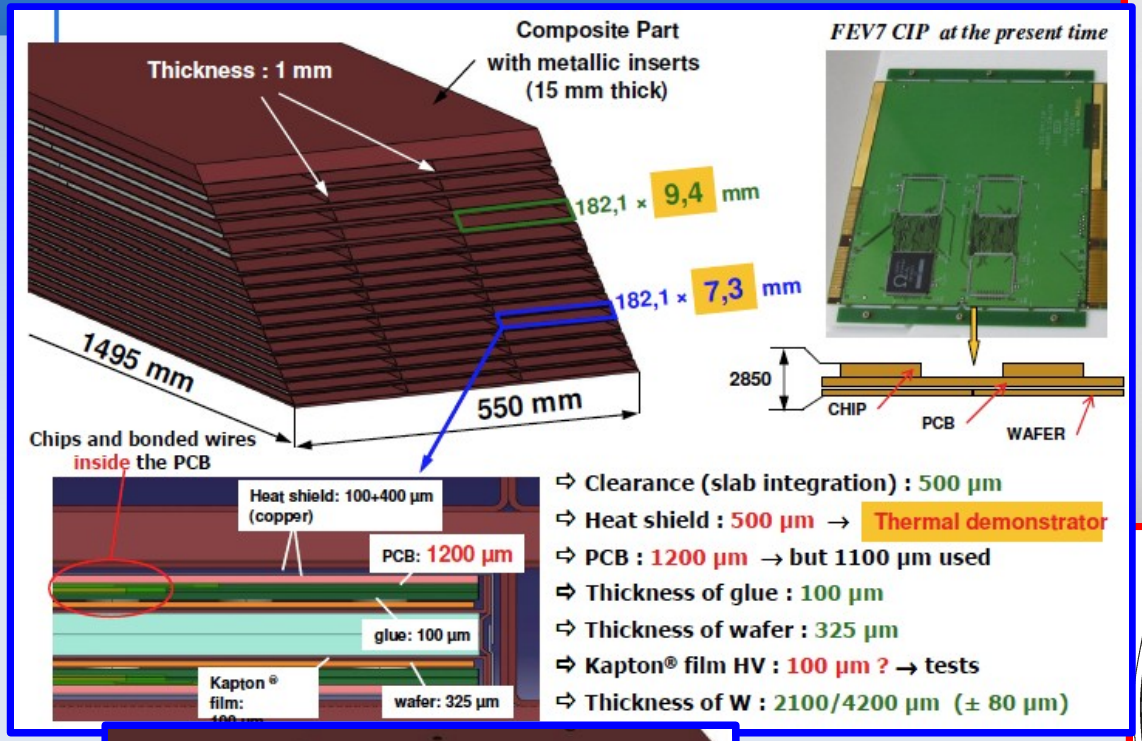
- Can use the same hardware for every detector
  - Same connectors & interfaces
  - Compact : credit card and below
- Customizable anyway
  - Size
  - Test beam/calibration features (add exttrig, clk, RAM, …)
  - Debug (test of single detector module)
- Functionalities are simple
  - VFE chip management (power pulsing, SC, DAQ) with a common interface
  - Local storage of SC data
  - Protocol conversion (8b/10b to VFE)
  - Based on low cost fpga
- DIF task force (4 persons)
  - LLR, DESY, LAPP, Cambridge
  - Specifications
  - Common firmware

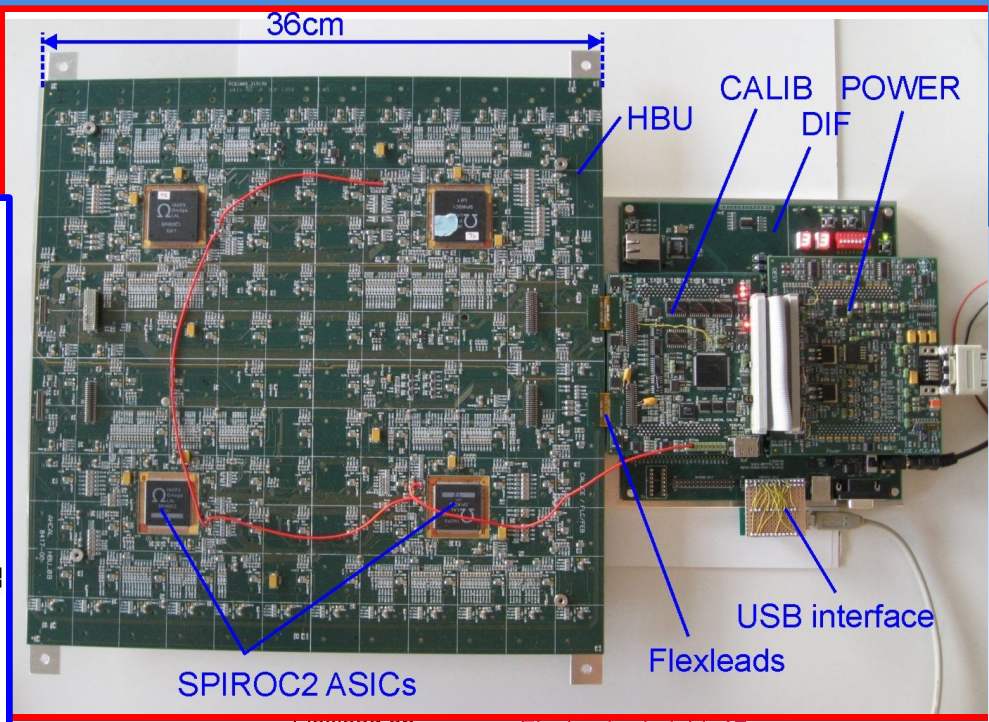
Actually 3 different hardware versions in use : ECAL, DHACAL,AHCAL but same firmware

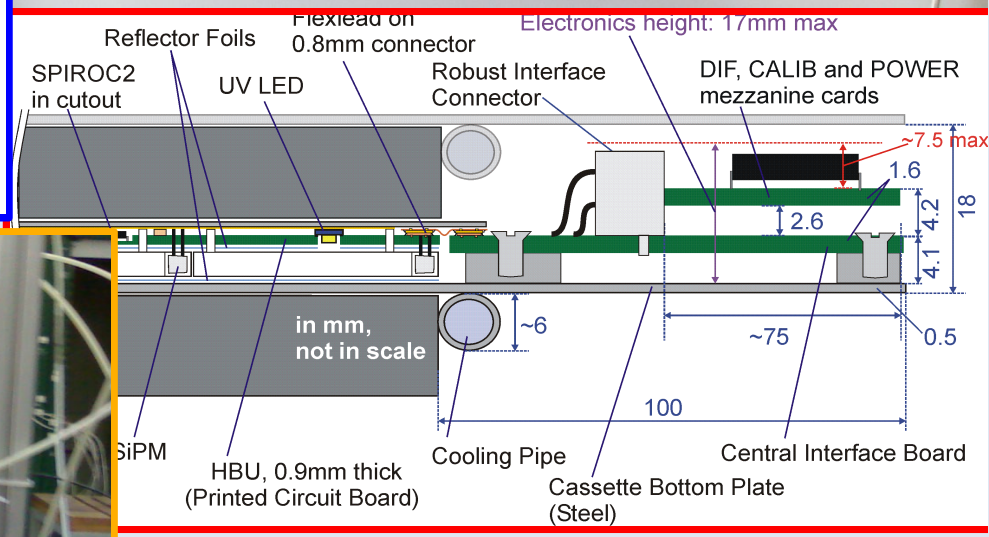
Firmware for use with 8b/10b link developed at LLR and shared (svn server)
- Used for system level tests
- Get ROC interface blocs from LAPP
- Mixing is a success : SC data generated on both DHCAL and ECAL DIFs

Slide from R. Cornat

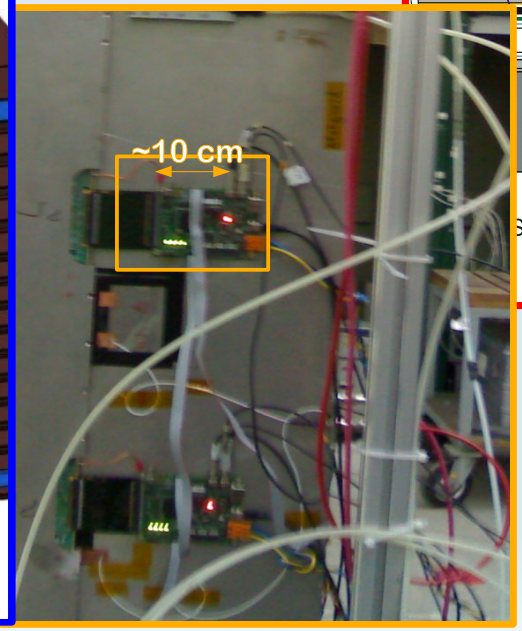
Detector interfaces





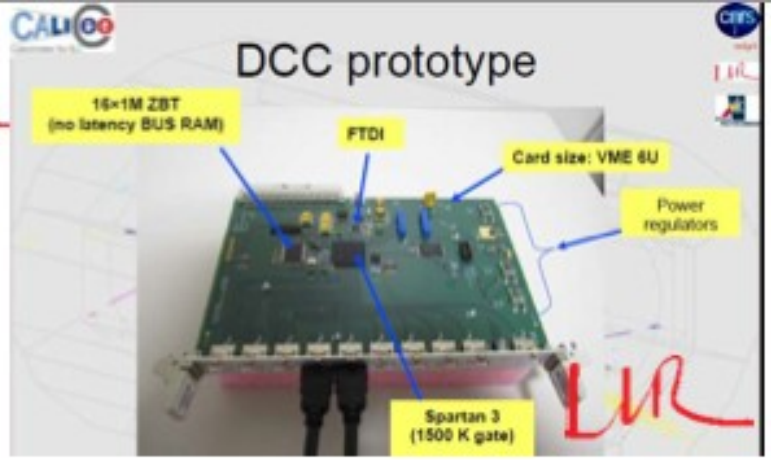


ECAL (CAM)



AHCAL (DESY)

SDHCAL (LAPP)



LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR.
- Firmware development :
  - DIF <=> LDA link running;
  - new code soon to be posted to svn;
  - same format as ODR in svn repository.

DCC and LDA are essentially similar to an ethernet switch but using a low level protocol

They both fan-out/in fast isochronous signals on a dedicated path and commands on the 8b/10b serial link

LDA has a fast link : Gb ethernet to the upper level = ODR, and can connect to 10 DIFs or DCC with the 8b/10b serial link
DCC can connect to 1 LDA and 9 DIFs using the 8b/10b serial link, data from DIF are buffered and sent to the LDA

CCC

- Overall status unchanged for a while.
- Fans out clocks, fast commands and control signals.
- Fans in busy.
- Full complement of 10 boards with power supplies tested.
- One in LLR and one in LAPP.
- CCC link to LDA still needs to be done :
  - Board designed and firmware developed for testing;
  - Soon to produce enough boards for all LDAs.

ODR

- Receive data on 4x fibre (RX).
- Write to disk FAST (>150MB)
- Send data up fibre (TX)
- Controlled from Linux driver
- DOOCs Interface

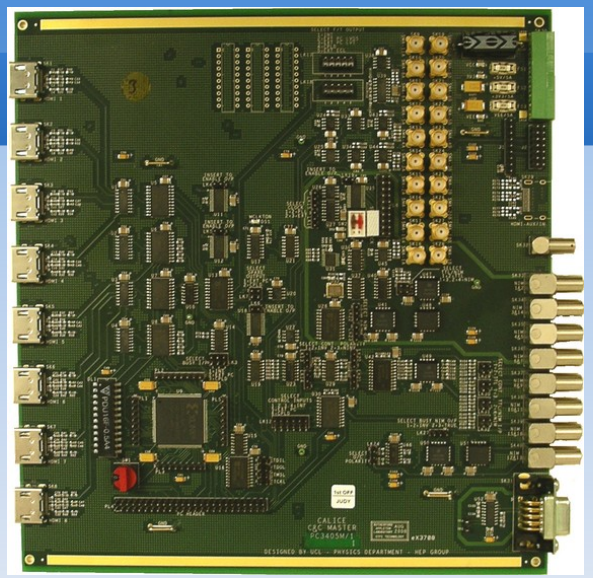
Documentation / repository

- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

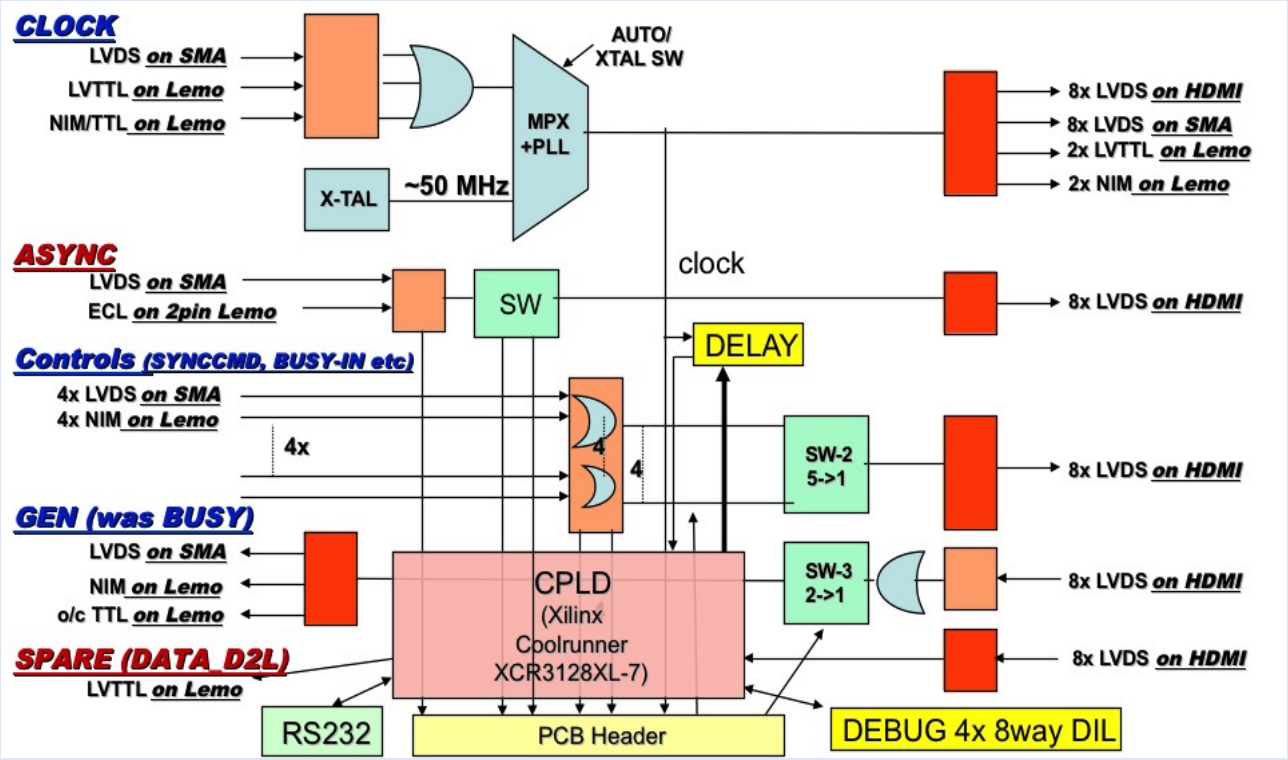
  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

Clock and Control Card



- Developed at UCL (M. Warren, M. Postranecky)
- Distributes on 8 channels (HDMI, SMAs, NIM, …) via dedicated circuitry for **low jitter**
  - Int | ext clock
  - Fast Signal (Trigger | Sync)
- Sums-up BUSY
- Performs Trigger logics
  - CPLD
- Was used as DIF-Master (dev^{t} of LAPP)
  - Aka also sending hard-coded commands to DIF directly
  - Standalone tests with USB readout



HW status

- 10 ECAL DIF ready and working; 10 in prod; mat for 40 in total (CAM)
- DHCAL DIF: 165/170 cards tested & ready (LAPP)
- AHCAL DIF: in design, prod in NIU → 4 unit
- CCC: 10 cards ready; 4 in use in 4 labs; 3 more shipped → LLR
- DCC: 3 prototypes ready; 2 cards being tested → 20 end of october
- LDA: 20 main board OK
  - 5 v1 + 15 v2 Ethernet mezzanine : ✔
  - 6 CCC mezzanine; clock OK — Busy & Trigger not yet tested (TBC)
  - 20 HDMI Mezzanine: faulty connectors on 8 → in repair
- ODR + PC
  - 8 ODR ready ; network card being used instead for debugging
  - 6 PC available: 1 in LLR ; 3 other ready; OS needs to be upgraded

~ No more basic problem with HW

FW status

	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	10 MUX on going	9	1
Fast Commands	✔	✔	✔
Block transfert	✔	✔	✔
Data[1)]	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure ✔ Adapt SDHCAL USB Code on going...

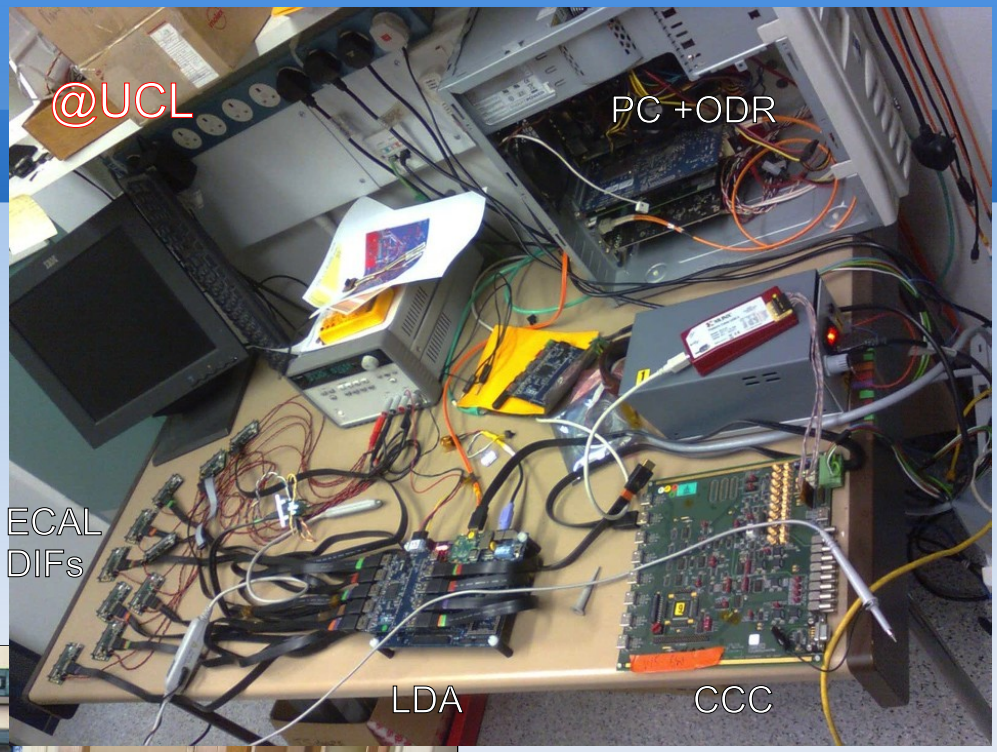
- FW have been advancing rather fast during the last 3 months

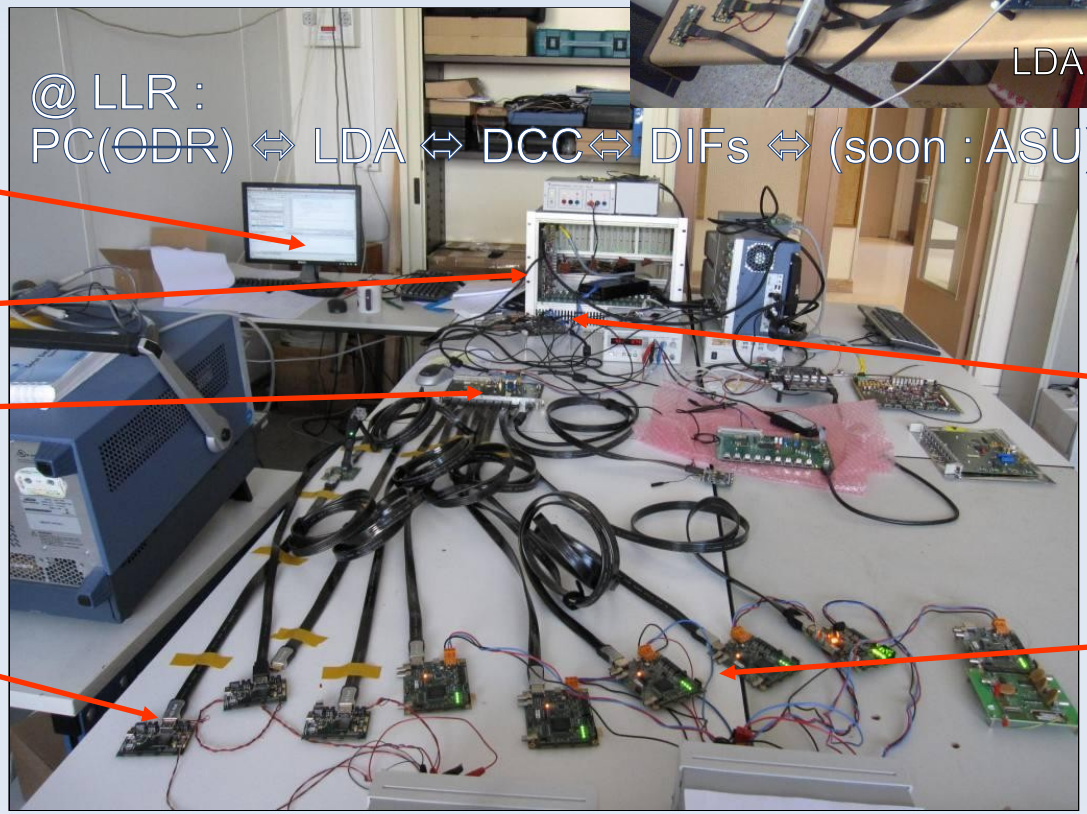
Generic code for all DIFs

Many progresses recently
End of October for first full minimal usable chain ?

Integration tests

- Systems available @ UCL, LLR and now Cambridge
- Whole chain established :
  DAQ PC with ODR ⇔ LDA ⇔ DIF and CCC source
- Multiple 10 DIF ⇔ LDA links established
- FastTrig and Busy signals functional.

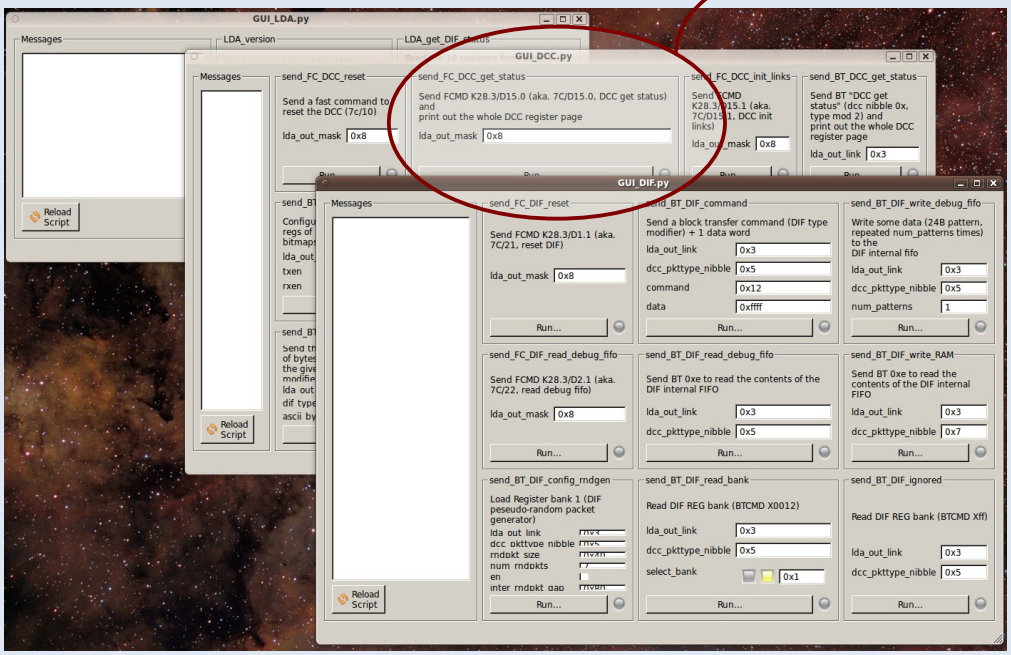




PC
UCL & RHUL (ODR)
UCL
CCC
DCC
LLR
Ecal DIF
Cambrige
LDA
Manchester
Dhcal DIF
LAPP

Python Test toolkit

- Interactive hardware test software (GUI)
  - Each HW test easily scriptable: simple user-friendly python API: each function defined ↔ 1 graphical pane with “Run” button
  - Available to anyone working with USB/RS/Ethernet devices
- C libraries implementing the complete **DIF Task force** protocole




```
File  Edit  Options  Buffers  Tools  Python  Help

def send_FC_DCC_get_status(INT0x_lda_out_mask = 0x8):
    """Send FCMD K28.3/D15.0 (aka. 7C/D15.0, DCC get status) and
    print out the whole DCC register page"""
    comma  = commons.encode_8b10b_kd(28, 3)
    data   = commons.encode_8b10b_kd(15, 0)
    ans    = LDA.do_lda_send_fastcmd(INT0x_lda_out_mask, comma, data)
    calicediag.GUI.set_statusbar_message("Get_Status FCMD sent")

    return _unpack_DCC_get_status_page(ans[16:]) is not False

--:---  DCC.py      47% (189,0)   SVN-1428  (Python)----------------------------
calicediag.register_action(DCC.send_FC_DCC_reset)
calicediag.register_action(DCC.send_FC_DCC_get_status)
calicediag.register_action(DCC.send_FC_DCC_init_links)

calicediag.register_action(DCC.send_BT_DCC_get_status)
calicediag.register_action(DCC.send_BT_DCC_config_tx_rx)
calicediag.register_action(DCC.send_BT_DCC_start_RTT)
calicediag.register_action(DCC.send_BT_DCC_stop_RTT)
calicediag.register_action(DCC.send_BT_DCC_relock_DCM)
calicediag.register_action(DCC.send_BT_DCC_register_blob)

--:---  GUI_DCC.py  Bot (7,0)     SVN-1428  (Python)----------------------------
```

https://svn.in2p3.fr/calice/online-sw/trunk/pyserdiag/

Reliability tests

Stress tests using pseudo-random generator

- 9×DIF → 1×DCC → 1×LDA → PC
  - 4 DIFs generate pseudo random data
- Results
  - Direction DIF → LDA ✔
  - Maximum DCC → LDA link occupancy (40Mbps) ✔
  - Up to 5.6 TB transferred (2 weeks), no error

End-to-end test: FIFO write/read

- PC ↔ 1×LDA ↔ 1×DCC ↔ 1×DIF
  - Tests both fast-commands and block transfer “read” requests
- Results:
  - PC ↔ LDA Ethernet OK
    - still issues when interleaving Fast Commands with configuration

Performances

- Rather low demands in term of bandwidth
  (but >> @ ILC for same vol.)
  - SDHCAL : ~ 20MB/s in Spill
  - ECAL: ~100MB/s
  - AHCAL: ~ 300 MB/s
- **Data limited by ASICs readout**
  - Modes:
    - test beam single event
    - Test beam burst (≈ ILC-like mode)
- Some code (System C, by D. Decotigny) exists for simulation of full chain
- Many other studies...

DAQv2 data flux

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	9	50	6.25	1000	125	1000	170

Detector	DHCAL	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]
		20 B	128	2.5	0.31

from LC-DET-2004-029

Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo
N ASIC/DIF	48	48	4.8	4.8	4.8
σ (NASIC)	0	0	2.6	2.6	2.6
Touched DIF/pla	3	3	1	1	1
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B
R/O time 1	*64 µ s*	*8 192 µ s*	*64 µ s*	*8 192 µ s*	*8 192 µ s*
R/O time ALL	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
DIF	960 B	122 880 B	96 B	12 288 B	12 288 B
R/O time	*154 µ s*	*19 661 µ s*	*15 µ s*	*1 966 µ s*	*1 966 µ s*
LDA w/o DCC	9 600 B	1228 800 B	320 B	40 960 B	40 960 B
R/O time	*77 µ s*	*9,830 µ s*	*3 µ s*	*328 µ s*	*328 µ s*
DCC	8,640 B	1,105,920 B	288 B	36,864 B	36,864 B
R/O time	*1 382 µ s*	*176 947 µ s*	*46 µ s*	*5 898 µ s*	*5 898 µ s*
LDA w/ DCC	86,400 B	11,059,200 B	2,880 B	368,640 B	368,640 B
R/O time	*691 µ s*	*88 474 µ s*	*23 µ s*	*2 949 µ s*	*2 949 µ s*
ODR	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
1000MB/s	*173 µ s*	*22 118 µ s*	*6 µ s*	*737 µ s*	*737 µ s*
Disk	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
170MB/s	*1 016 µ s*	*130 108 µ s*	*34 µ s*	*4 337 µ s*	*4 337 µ s*
Max R/O time	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
Min Freq	0.33 kHz	0.00 kHz	3.26 kHz	0.03 kHz	0.03 kHz
Min. evts Freq		0.33 kHz		3.26 kHz	3.26 kHz

19MB/s

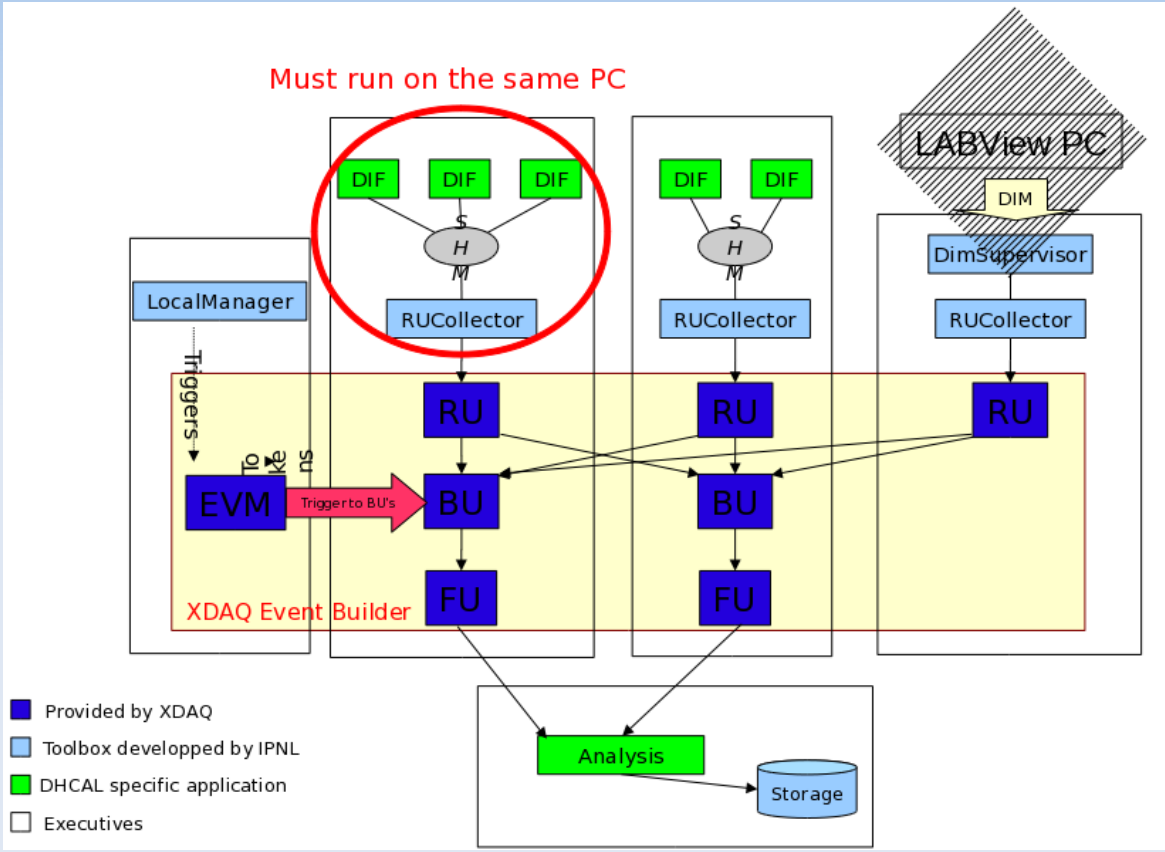
Occupancy for 100 GeV π in TB evts	
Mean	4.8
sigma	2.6
+3σ /√MemSize	5.49

Parameters codes
Hardware (~fixed)
DAQ (achievable)
Physics (occupancies)

Software: XDAQ framework

- dev[ts] started @IPNL for electronics test using XDAQ in 2008
  - Ch. Combaret (IPNL)
  - Gained (a lot of) impulsion with involvment of L. Mirabito (resp. of DAQ SW for CMS tracker)
- Ran for ≥ 1 year in TB, Cosmics & Electronics test
  - USB readout
  - Interface to old LabView program
- Recent development
  - Writing of LCIO data in RAW format
  - versatile online analysis framework (root histos)

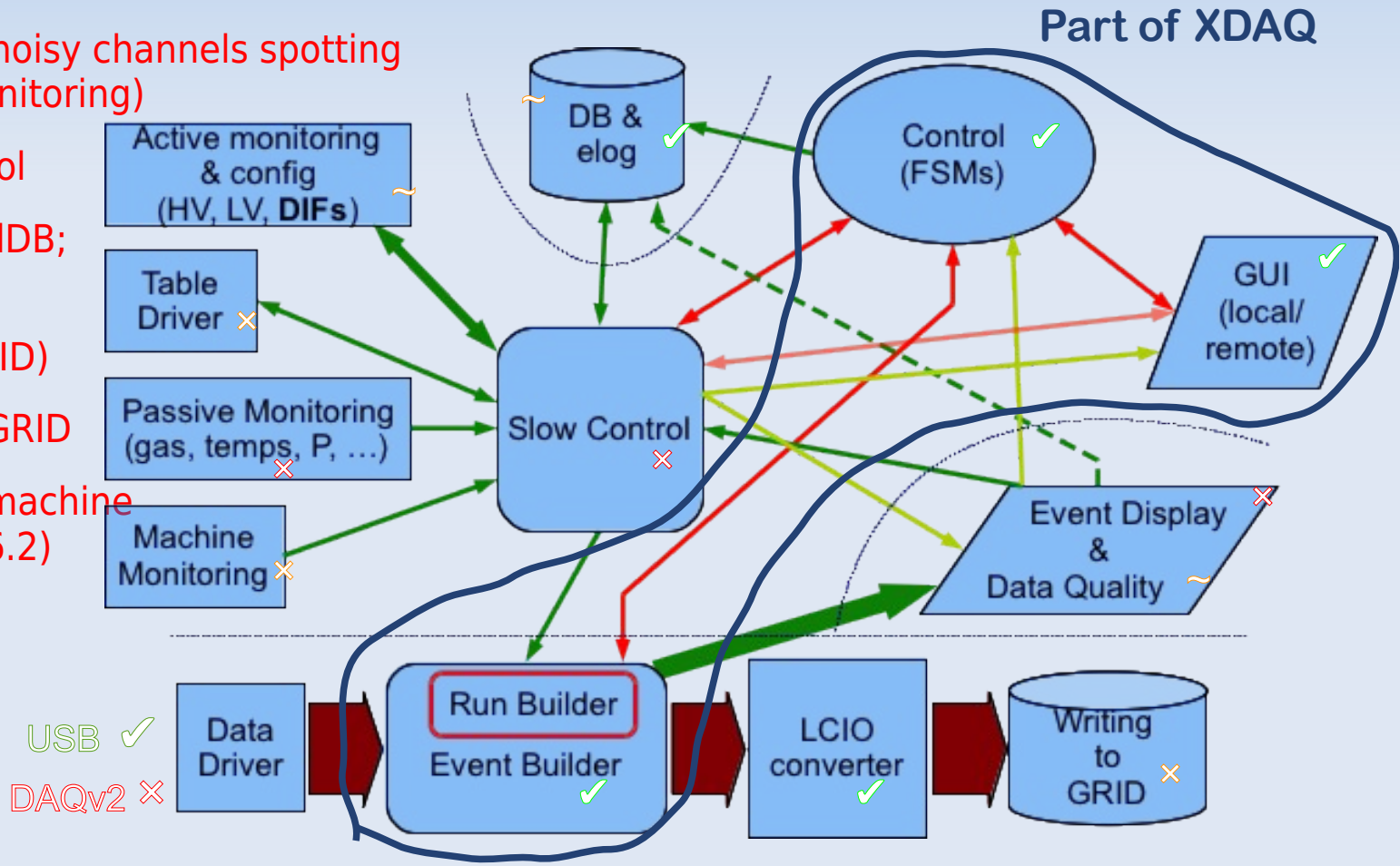
→ Marlin Based



IPN Lyon

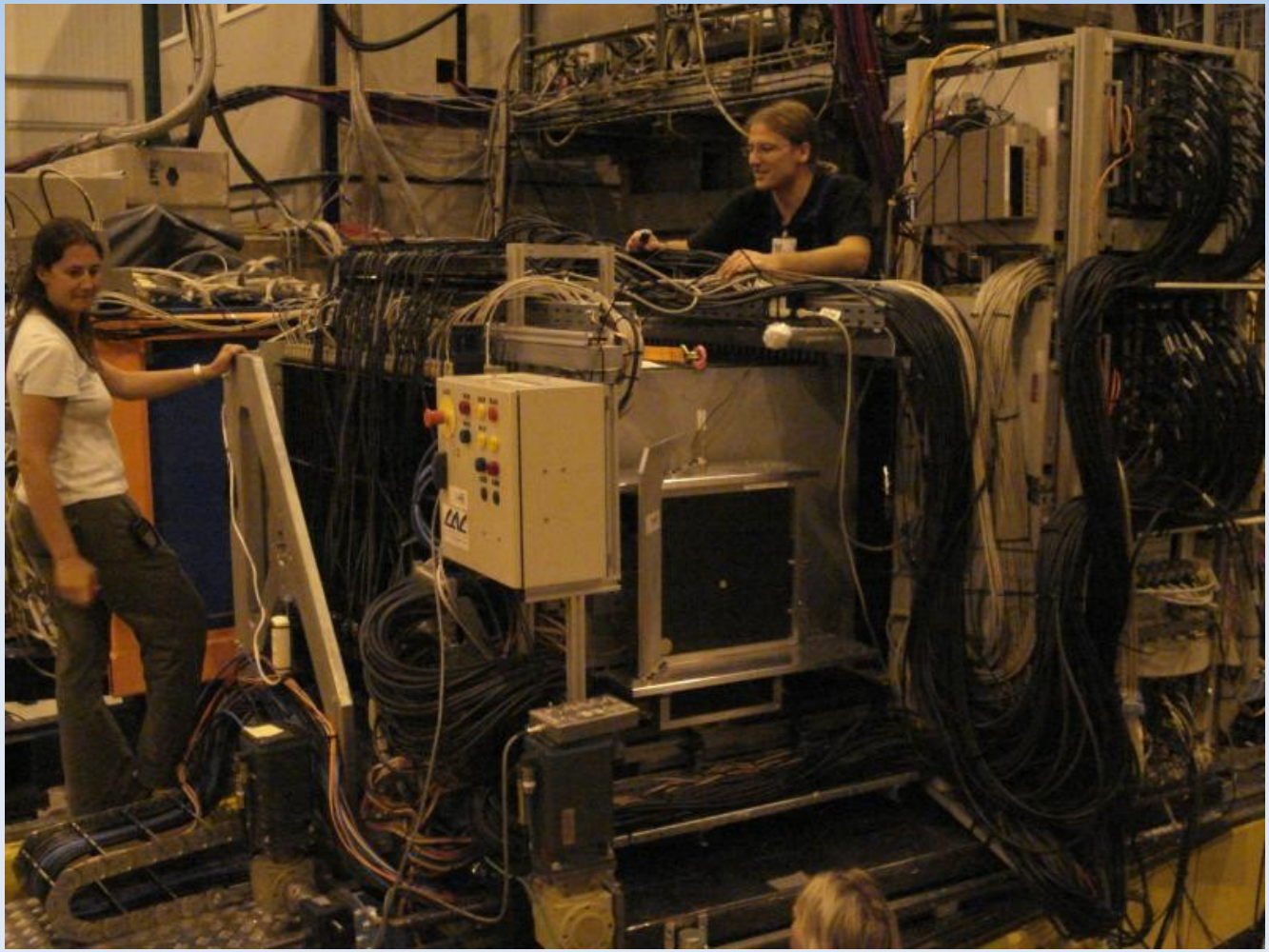
SW status

- Missing critical elements
  - Configuration DB (being worked on)
  - DAQ2 interface ↔ XDAQ being worked on
- Missing ancillaries
  - Semi-automatic noisy channels spotting & correcting (monitoring)
  - Clean Slow control
  - interface to CondDB;
  - event display (most prob^{ly} DRUID)
  - interface to the GRID
  - interface to the machine (⊃ in AIDA WP8.6.2)



Installation

- mechanics
  - mod. VME crate for
    - DCC
    - CCC
  - Special box for LDA
  - Support for cables
- Final set-up not yet known:
  - stand alone SDHCAL
  - stand alone ECAL
  - Stand alone AHCAL
  - Combined test
- → 5 m long HDMI cables
  - halogen free;



Beam InterFace card

Basis:

- CALICE chips use auto-trigger
  - Readout can be triggered by single event using external trigger (e.g. beam hodoscope)

    → “Single event” mode

    History of Chip is usable (e.g. in case of selective ext. trigger)
  - Readout triggered by environmental internal or extern trigger
    - Chip full
    - ILC-like mode (end-of-spill)
- Require some device to readout the beam line parameters
  - Scintillators; Cherenkov PM (coding of CEDAR bits)
  - Time of event (⊃ rec for wire chambers)

Implementation

- 2 solutions
  - Add-hoc card for interfaces with a CALICE ROC (SPIROC ?) + 1 DIF
  - Small adaption (buffers) card on a DIF + “simulation” of a digital ROC in the FPGA
- Both offer full compatibility with CALICE DIF for the DAQv2.
- To be implemented for 2nd version of CALICE beam test
- One of the task of AIDA (WP8.6.2)

Conclusions & Outlook

- Technological prototypes of CALICE are getting close (1st will be SDHCAL → Spring 2011)
  - 2nd version of ROC chips available
  - Being integrated in large prototypes → extensive TB in 2011
- All DAQ HW elements available
  - FW almost ready
  - Accomplishment of a long process
- SW: XDAQ took over for main stream
  - Some ancillary elements missing
- Combined (with other system) ≥ 2012
  - Prepare HW and SW beforehand
    - SW & HW ↔ TLU & EUDAQ first
    - Performances (ODR use)
  - Part of AIDA WP8.6.2

Big effort for CALICE!!
~15++ individuals from:
- UK: CAM, MAN, UCL, RHUL
- FR: LLR, LAPP, IPNL
- DE: DESY

Most of Code, Manual and HW description is available on CALICE twiki:
https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ