

LOW COST AND LOW MASS BUMP BONDING

Outline

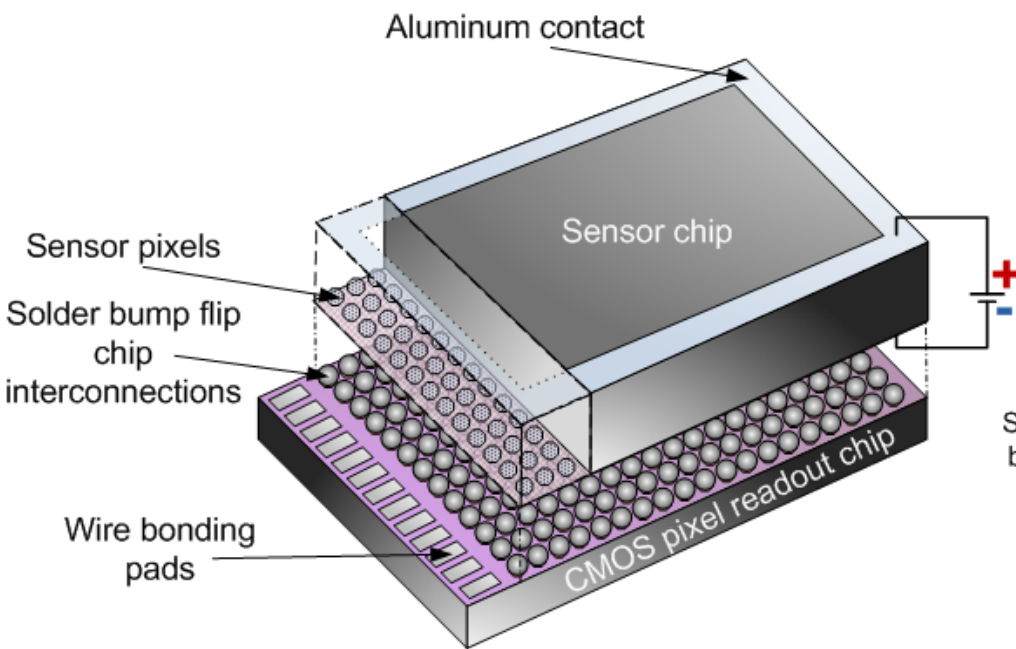
- Introduction
- Electroless Ni Under Bump Metallization (UBM) deposition process
 - Low-cost technology
- Carbon Nano Fiber (CNF) interconnection technology
 - Potential low mass interconnects
- Chip-to-wafer flip chip bonding
- Wafer thinning and thin wafer handling
- Summary

Introduction

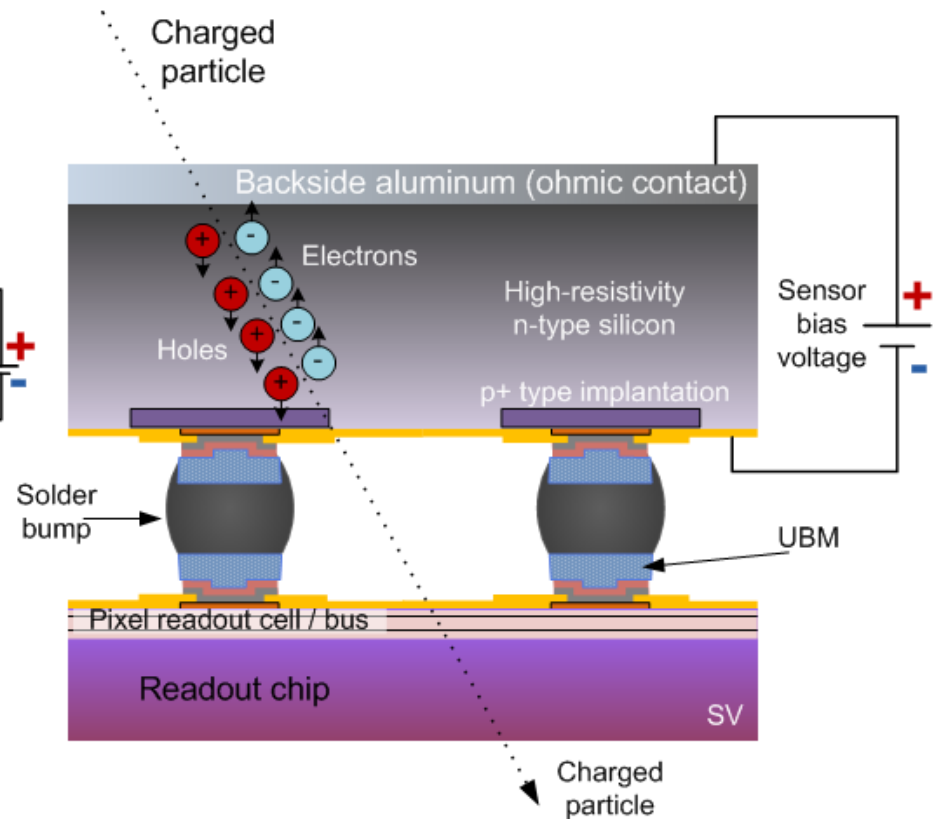
- Low-cost bump bonding solutions have been studied at CERN
 - Cost-effective method using electroless deposition of Ni/Au
 - Industrial deposition process
 - Future goal: Electroless UBM's + advanced solder transfer techniques
 - For 100 μm pitches and above
- Carbon Nano Fiber (CNF) development work for flip chip interconnections has begun.
 - Very advanced technology for making high density but ultra low mass interconnections
 - Project aims at building a handful of real Medipix2 detector assemblies
- Flip chip costs are planned to be cut using wafer-scale packaging
 - Chip-to-Wafer (C2W) technology is cost-effective way to do the flip chip
- Wafer thinning is very important to minimize the mass of the innermost layers in the vertex detector constructions.
 - New carrier wafer technologies facilitate the thinning and handling of wafers

Flip Chip in Pixel Detectors

- Pixel detector consists of a sensor chip and readout chip which are connected with flip chip bumps (picture below).
- Because each pixel represents is visible in the radiation image, a high bump bonding yield is required to avoid visible defects.
- Solder bumps have been typically used as connecting the chips electrically and mechanically together.



Generic pixel detector

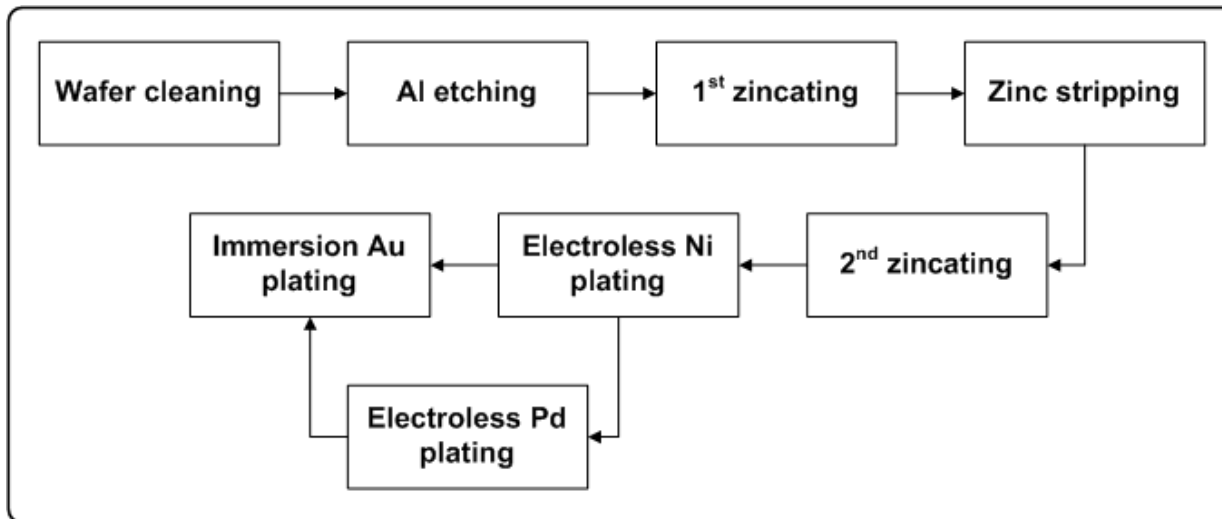


Cross-sectional cut

Elements in Solder Alloys

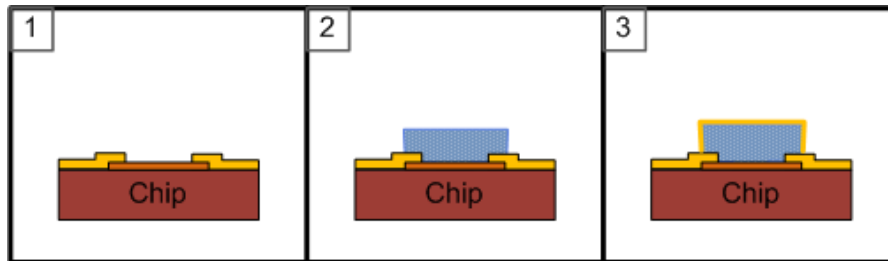
- Elements and their masses used in typical solder joints (atomic weights):
 - Ni 58.7, Cu 63.5, In 114.8, Sn 118.7, Pb 207.2, (Si 28.1)
- Solder bump volumes are typically small in pixel detectors ($d = 30\ \mu\text{m}$) and the area-coverage is relatively small (5% - 30%)*
 - Thin solder joints have relative low mass despite using heavy elements.
- Restriction of hazardous substances (RoHs) directive is limiting the use of lead in interconnections:
 - Concentration of lead in an alloy should be less than 1000 PPM ($< 0.1\%$)
 - Exemptions for flip chip / BGA solder joints
- Flip chip joints in pixel detectors are not affected by RoHs directives, but less solder bumping processes are available with lead alloys.*
- Tin-lead solder has been replaced mainly by pure tin or SnAgCu (SAC) or SnAg alloys.
- Lead free solder alloys have usually higher melting temperatures than eut. SnPb alloy.

ELECTROLESS NI TECHNOLOGY

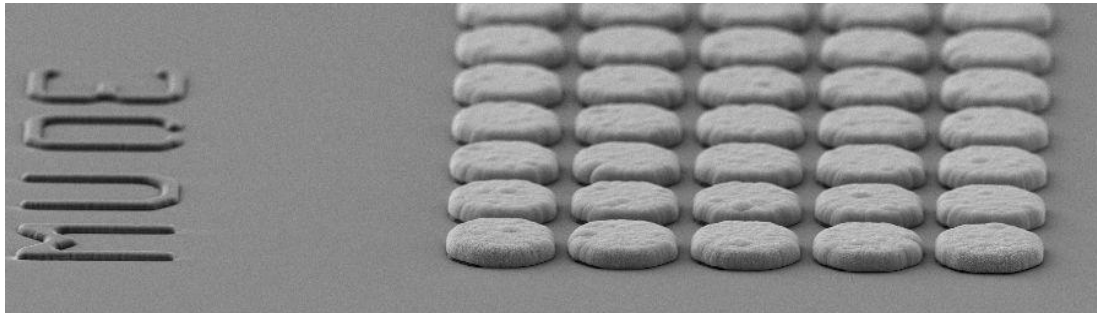


Electroless Under Bump Metallization (UBM)

- In electroless Ni UBM process, the Ni is chemically grown on Al on the bump pads.
- Photolithography can be avoided.
- The most common used electroless Ni UBM's is Electroless Nickel – Immersion Gold (ENIG).
- Strength of the UBM pads is depended on the size of passivation openings to Al on the wafers. Mechanical is contact is made only on Al – not to passivation.
- EN grows isotropically – this should be taken into account in the design phase.



Electroless process flow sketch



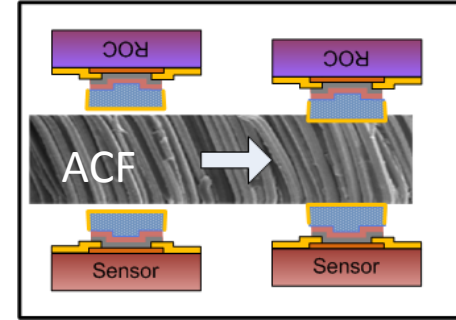
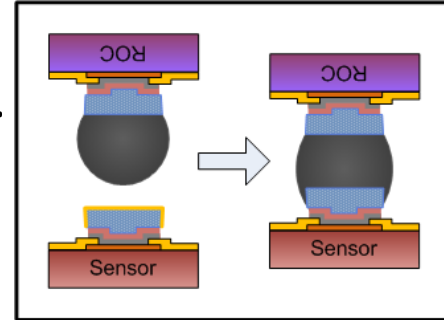
Electroless UBM's have been processed with 30 μm pitch test structures on CERN test wafers.

Electroless Under Bump Metallization (UBM)

- Electroless Ni (EN) process is a batch process, wafers are processed in cassettes.

- EN enables several flip chip scenarios.

- Soldering
- Anisotropic Conductive Films



- Wafers may be processed without a lithography step

- Lithography is possible if some areas are wished to leave without deposited metal.
- Dicing lanes, wire bonding pads, etc...

- EN is compatible with Al wedge and gold ball wire bonding.

- Technology is available for 200 mm & 300 mm wafers

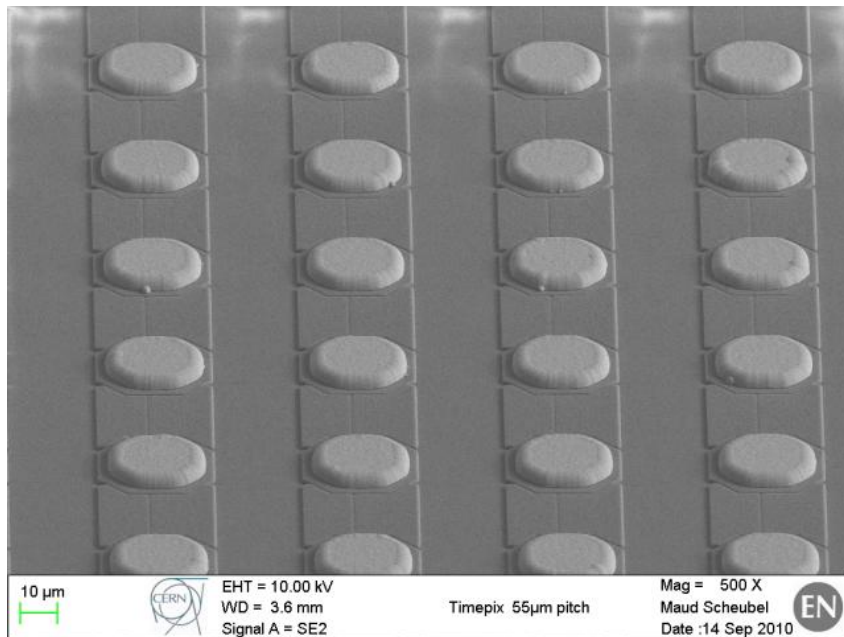
- No need for photolithography for 300 mm wafers

- EN is grown on all the exposed Al structures on the wafers

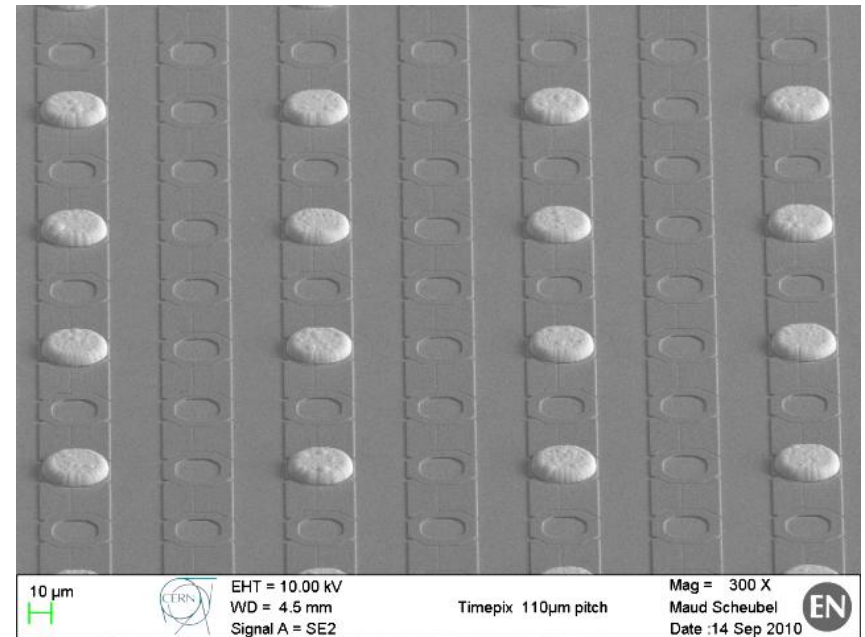
- It is very important to use Aluminum with alloyed Cu (typically 0.5 %) to produce reliable UBM structures.

Electroless Under Bump Metallization (UBM)

- Electroless Ni UBM's have been characterized on test wafers and also on real CMOS wafers
- ENEPIG UBM pads were grown on Timepix wafers with two different pitches
 - 55 μm – without photoresist mask
 - 110 μm – with photoresist masking
- Chips were electrically measured after EN process – no degradation in electrical performance
- Flip chip tests are pending



ENEPIG UBM pads on Timepix chip (55 μm pitch)



ENEPIG UBM pads on Timepix chip (110 μm pitch)

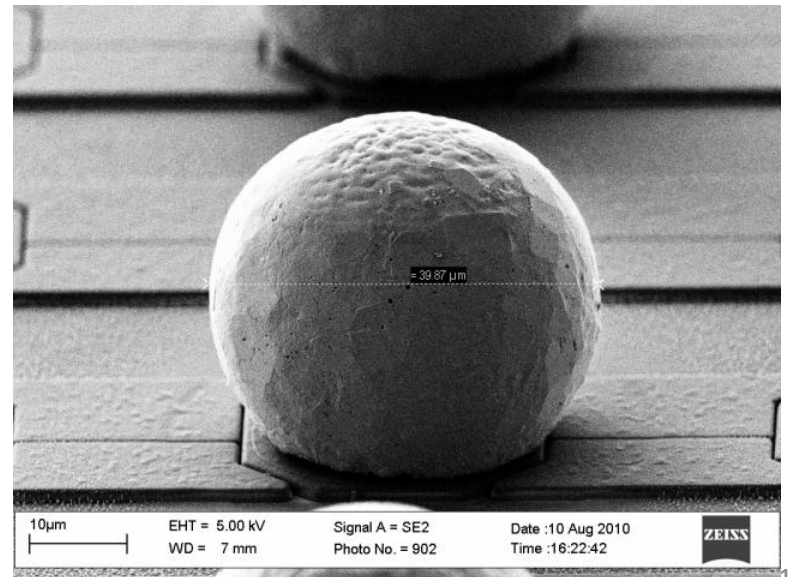
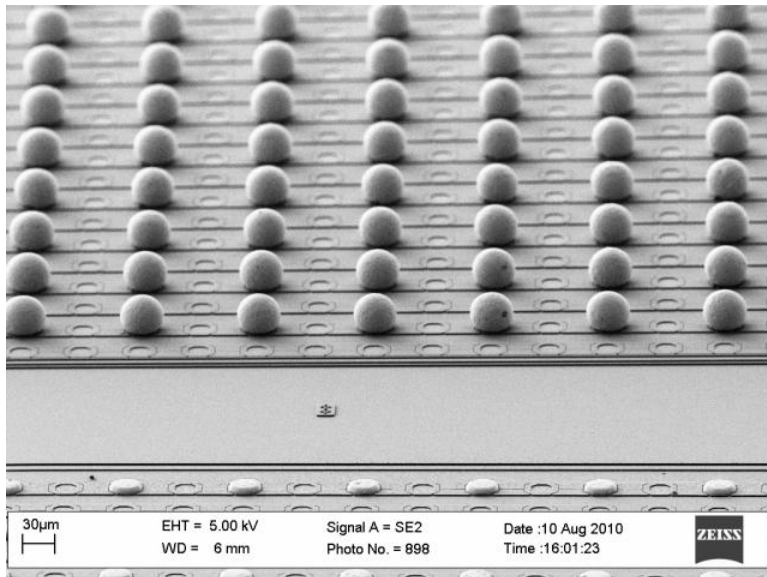
Individual Solder Ball Placement

- EN UBMs can be combined with solder transfer processes.
- Smallest solder spheres are available in 40 μm size at the moment.
 - Very interesting for outer trackers with rather coarse pitch (100 μm pitch)
 - Less stringent mass requirements
- 40 μm solder balls (very advanced) were jetted one by one on a Timepix chip with ENEPIG UBM with 110 μm pitch at Pac Tech (Germany).
- Nice way to bump of single chips from MPW runs with EN UBM



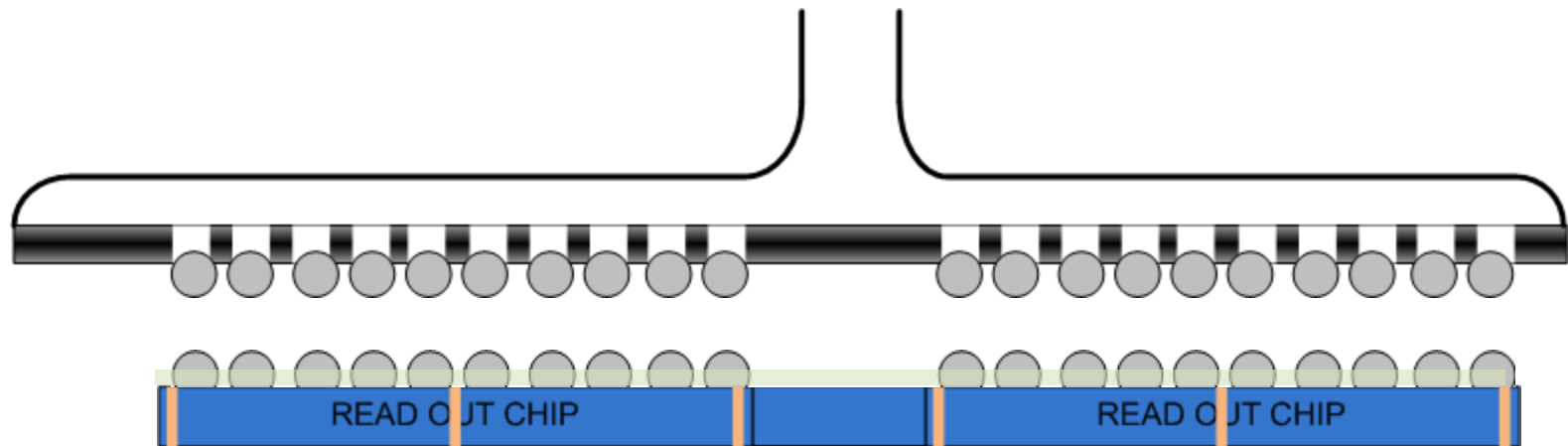
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Solder Mass Transfer Technique

- EN in combination of mass transfer of solder spheres will be the ultimate low cost solution for wafer bumping.
- Solder spheres are moved on a wafer in on single wafer-level step.
 - Stencil grid with predefined holes and vacuum is used to lift the solder sphere
 - Vibration is used to detach additional spheres
 - Solder bumping defects can be repaired with the single solder ball placement systems
 - Bumps are compressed against the EN UBM's
 - Solder reflow.
- Solder transfer takes less than 6 minutes per wafer.
- Limited by ball size, minimum 60 μm at present - suitable for 100 μm pitch.
- Pac Tech foresees 40 μm bumps coming in 1-2 years.

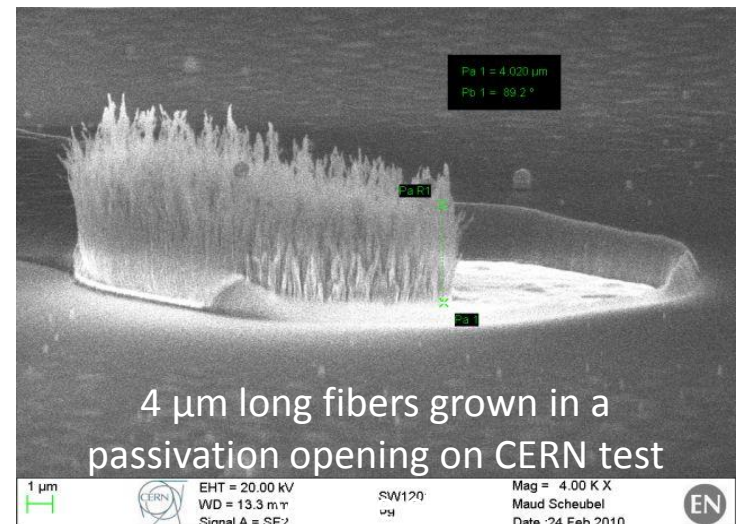
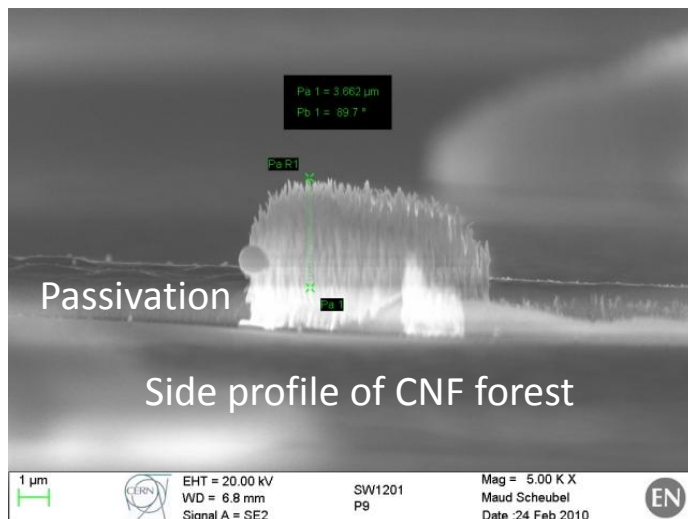


Solder mass transfer is a very efficient process to attach the solder spheres to wafer

CARBON NANO FIBRE (CNF) DEVELOPMENT WORK

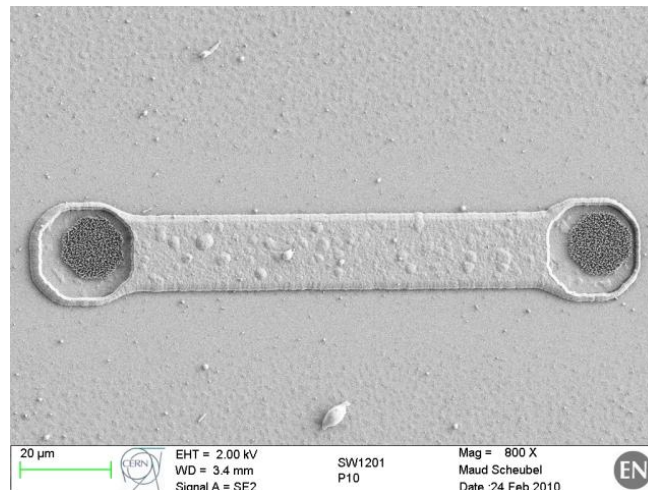
Carbon Nano Fibre (CNF) Interconnections

- CERN has started a small project with Smoltek (Gothenburg, Sweden) to develop fine-pitch CNF interconnection technique for pixel chips.
- Goal is set at growing 5 μm – 10 μm long fibres on chips and joining them together.
 - Electrical contacts will be tested with/without metal contacts.
- CNF's would be ultra-low mass interconnections.
- Technology has prospects to be ultra-fine pitch capable.
- First CNF forests have been deposited on CERN test vehicle chips.
 - Development plan has been made to improve the patterning resolution and to develop suitable flip chip processes.



Carbon Nano Fibre (CNF) Process

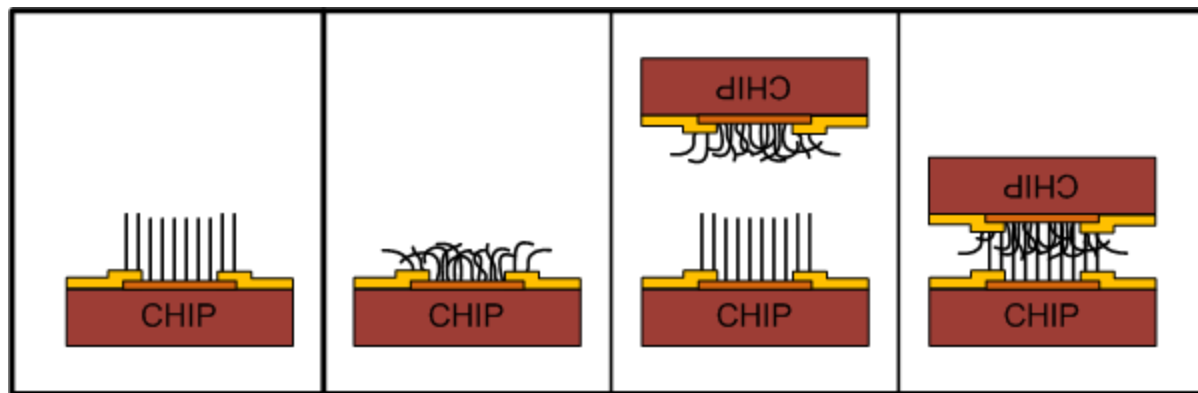
- Solid CNF's can be grown with a special plasma enhanced deposition process.
 - Compared to hollow carbon nanotubes, solid fibres are much easier to grow.
 - Fibres are aligned with electric fields during growth
- In CNF process a catalyst is spread on chips and it is patterned by a standard lithography.
 - Fibers grow on the catalyst
- CNF's will be grown around 400 °C
 - CMOS compatibility
- Fibres are grow in forests of thousands of fibers and the individual fiber diameters vary from tens of nm up to hundreds of μm .
- Test will begin with 10 μm forests (20 μm passivation opening on wafers)



Short fibres grown in the passivation openings of the CERN test wafers.

Flip Chip Using CNF's (1/2)

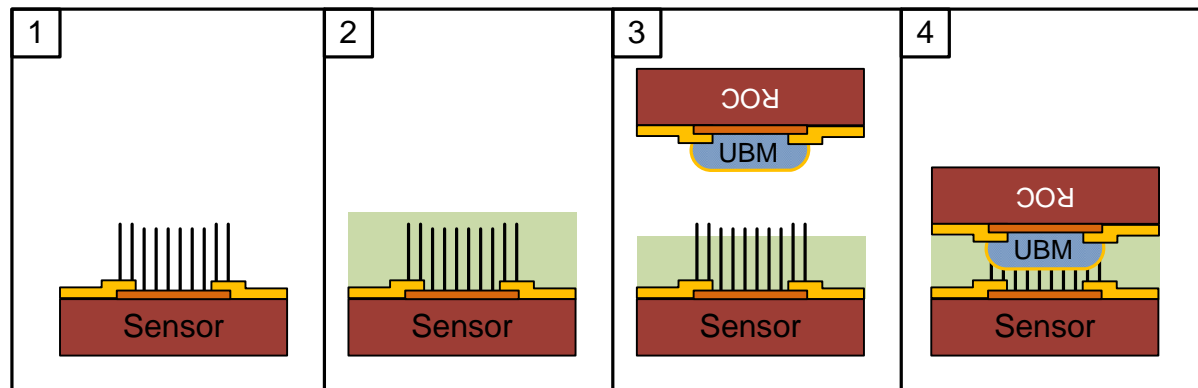
- Two potential flip chip scenarios are foreseen
 1. Joining chips with fibers on both sides (no metal coatings)
 - Bonds are based on weak forces and friction between the forests
- Flip chip process yield will be studied with the help of a test vehicle layout.



Flip chip assembly scenario using CNFs only

Flip Chip Using CNF's (2/2)

- Two potential flip chip scenarios are foreseen
 1. Joining chips with fibers on both sides (no metal coatings)
 - Bonds are based on weak forces and friction between the forests
 2. Spin a polymer coating on chips with CFNs and create an anisotropic adhesive film (ACF)
 - Electroless UBM will be used on one side of the assembled chips to create a vertical interconnection
- Flip chip process yield will be studied with the help of a test vehicle layout



1) Straight CNFs, 2) coating with polymer, 3) Exposing the fiber ends by an etching process, 4) conductive electroless UBM is brought into a contact and melting of the polymer

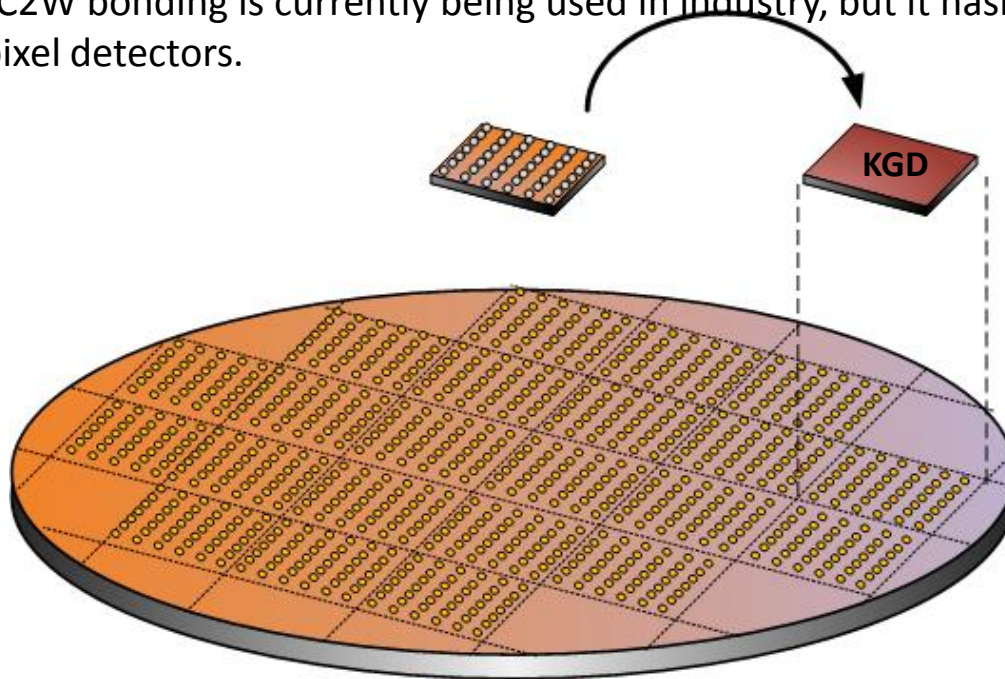
FLIP CHIP ASSEMBLY

Introduction to Flip Chip Bonding

- High-accuracy flip chip bonders are able to perform with $\pm 1.5 \mu\text{m}$ precision.
 - Existed already for more than 10 years and it seems to be sufficient for majority of applications
- Precision of the state-of-the-art flip chip systems is better than $0.5 \mu\text{m}$
- High number of I/O's on large chips require (besides clean environment):
 - High thermocompression force
 - Good placement accuracy
 - Chip to substrate leveling capabilities
 - Good thermal stability
- These requirements cause the rugged nature of the state-of-the-art flip chip equipment and the bonding processes are slow.
 - FC bonders become significantly faster at $10 \mu\text{m}$ placement precision
- Fine pitch flip chip has become interesting for packaging industry
 - Flip chip equipment manufacturers are wrestling with technical issues to increase the throughput without compromising the accuracy.
- The detector assemblies have been done on die level nowadays.
 - Chip-to-Wafer (C2W) is more efficient than die-to-die method
 - C2W assembly technology is the most potential wafer-level technology which could be used for pixel detectors.

Chip-to-Wafer (C2W) Bonding

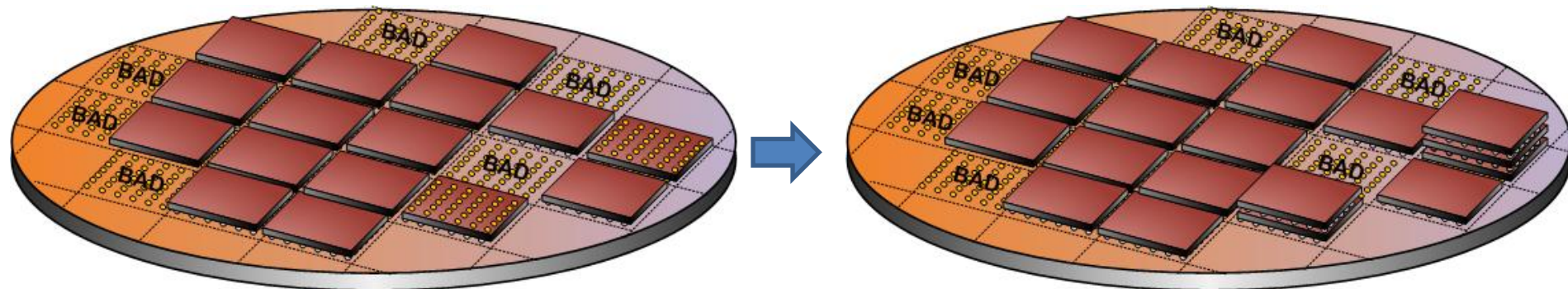
- Advanced flip chip bonding technology.
- C2W bonding is done on a flip chip bonder, which has a large chuck (200 mm).
- C2W bonding is more flexible than Wafer-to-Wafer (W2W) bonding and doesn't suffer from yield issues.
- Technology benefits
 - C2W reduces manual handling of assemblies.
 - Increase in the throughput – the whole wafer has to be assembled at the time.
 - Sensors can be bonded against known good dies (KGD) – economically efficient.
 - Chips with different sizes can be bonded – flexibility!
 - C2W bonding is currently being used in industry, but it hasn't been used much in assembly of pixel detectors.



Edgeless sensor chips or ROC's with TSV's needed - large guard ring structures consume wafer estate.

C2W Bonding (cont'd)

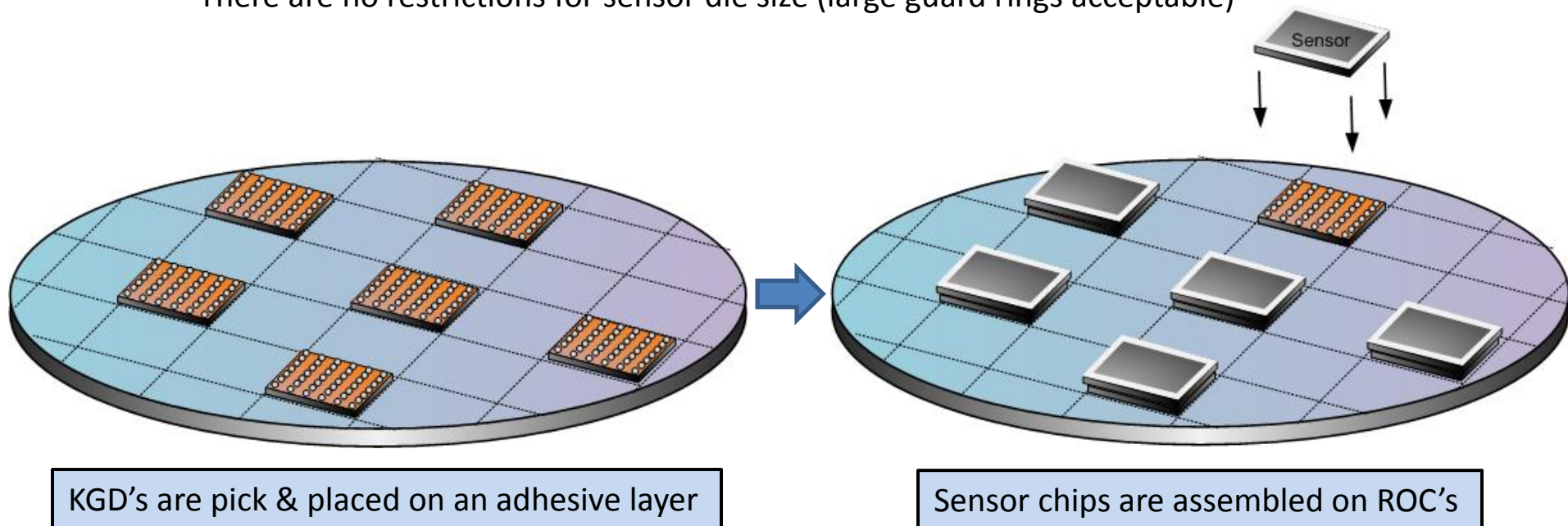
- Similar solder bump structures can be used as in chip-to-chip assembly, except that the wafer-level assembly and interconnections have to withstand larger thermal budget.
- No degradation in soldering properties is tolerated during the long assembly cycle
 - Solid-Liquid-Inter-Diffusion (SLID) soldering preferred – especially in multilayer assemblies!
- Common assembly cycle:
 - a) Tack-bonding (pick & place) of individual chips + mass reflow for the device wafer in reducing ambient.
 - b) Collective bonding can be done in wafer bonder after tack bonding with a cover wafer (slow processes such as hybrid-metal bonding).
- C2W bonding is favored when large and expensive dies are used (such as pixel chips).



If two side processed chips are used, multilayer chip stacking is possible

C2W Bonding Using Build-Up Wafers

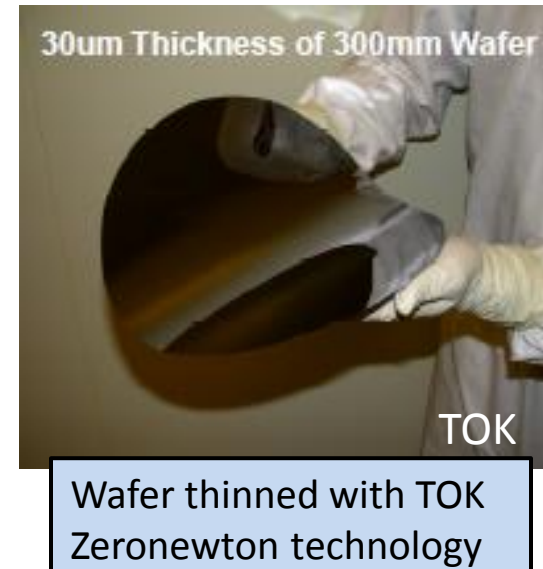
- Readout wafers are diced and the good known dies are picked up and redistributed on a carrier wafer on an adhesive layer.
- Wafer with unique stepping can be made.
- After assembly, the wafer is diced, and the glue will be dissolved
 - Thin assemblies are supported by the carrier chips.
- Technology benefits
 - One can populate wafers with KGD to get fully electrically functioning wafers
 - There are no restrictions for sensor die size (large guard rings acceptable)



WAFER THINNING

Wafer Thinning

- Wafer thinning technology has made a giant leap during 5 last years.
 - Thanks to development of temporary carrier wafers technologies
- Wafers can be basically thinned down to any thickness, but the problems arise when the wafers are handled and moved from process to another.
- Thin wafers break down very easily without a proper carrier wafer technology and wafer breakages become expensive (both for foundry and customer).
- One cannot give a generic figure for wafer thicknesses, because it depends on the wafer manufacturing and thinning technology available.
- Typically wafers are thinned in Through Silicon Via (TSV) processes to 50 μm – 100 μm thicknesses.



Thin Wafer Handling – Temporary Bonding Process

Overall TB/DB Process Flow

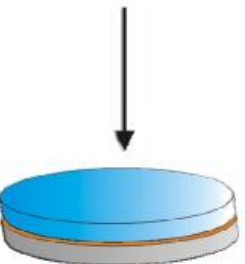
TB : Temporary Bonding



Device Wafer



Release Layer
Carrier Wafer



Temporary Bonding

Device Wafer bonded
on Carrier Wafer



Back Thinning and
further Processing

DB : DeBonding



Device Wafer (thin)
on Carrier Wafer



Debonding



Cleaning



Unloading



**Backside
Processes**



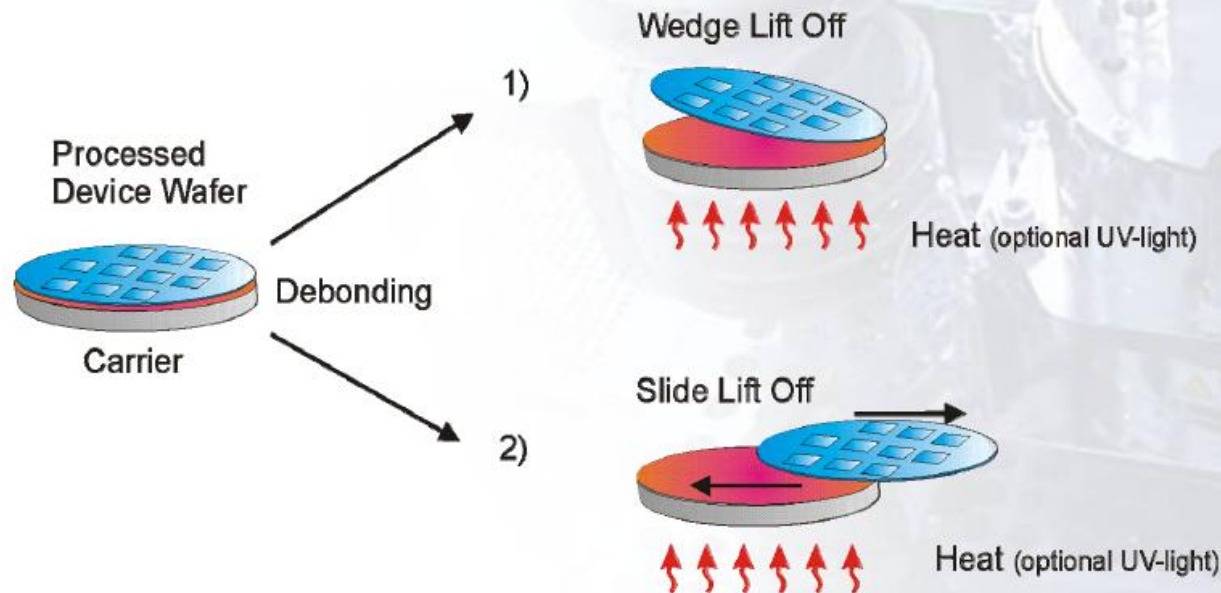
Thin Wafer Handling - Debond

Trends : Adhesive Type

Cont'd

Coating over Lamination

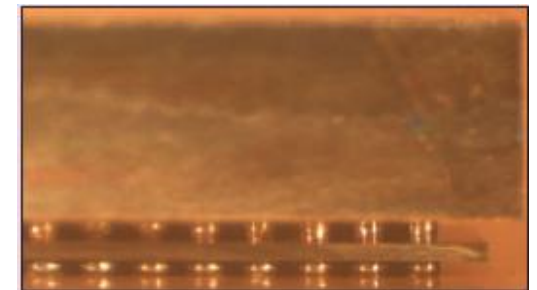
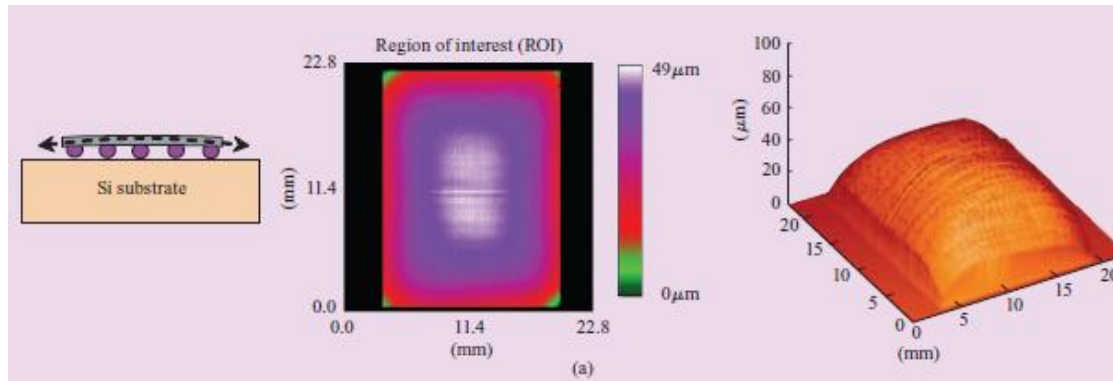
- Better edge protection
- Stable at higher process temperatures
- Compatible with a non-flat surface
- Slide lift-off rather than wedge lift-off



Easier process with less stress to the thin wafer

Wafer Thinning Issues

- Problems arise when the thinned wafer is removed from the carrier.
- Asymmetric stresses will warp the wafers/chips after they are released.
- Unless stresses are balanced the bow on a chip between corners and centre can be significant and cause alignment issues in flip chip bonding
 - Even 50 μm warpage is possible for 50 μm thick chip
- Stresses can be balanced by optimizing film stresses on both sides of the wafer.
- Thin wafers are more difficult to dice than thick ones
 - More chipping on backside.
 - Thin chips are fragile and chipping worsens further the die strength



Chip thickness 75 μm

Summary

- Electroless Ni UBM technology has show its potential for fine pitch structures
 - Combining it with solder mass transfer technologies, bump bonding will become an option for outer silicon trackers.
- Carbon nano fibers will be prototyped for very fine pitch pixel interconnects using solid carbon nano fibers
 - Ultra-low mass solution
 - Project has just begun, first test results available early 2011.
- Flip chip is expensive and it represents about 50 % of the costs of bump bonding.
 - Technology should be taken to wafer-level by using chip-to-wafer bonding technology
 - C2W requires new wafer designs (not necessary with build-up wafer technology)
- Very thin chips ($\leq 100\text{ }\mu\text{m}$) are becoming popular.
 - Carrier wafer technologies to be used in wafer processing or in flip chip bonding.

THANK YOU FOR YOUR ATTENTION!