# IP feedback design status

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***Oxford University***

# Feedback On Nanosecond Timescales

## Beam-based FB R&D for future Linear Colliders

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**Glenn Christian**
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**Javier Resta Lopez**
**Colin Perry**

**Graduate students:**
***Christina Swinson***
**Ben Constance**
**Robert Apsimon**
**Douglas Bett**
**Alexander Gerbershagen**
**Michael Davis**

**Valencia, CERN, DESY, KEK, SLAC**

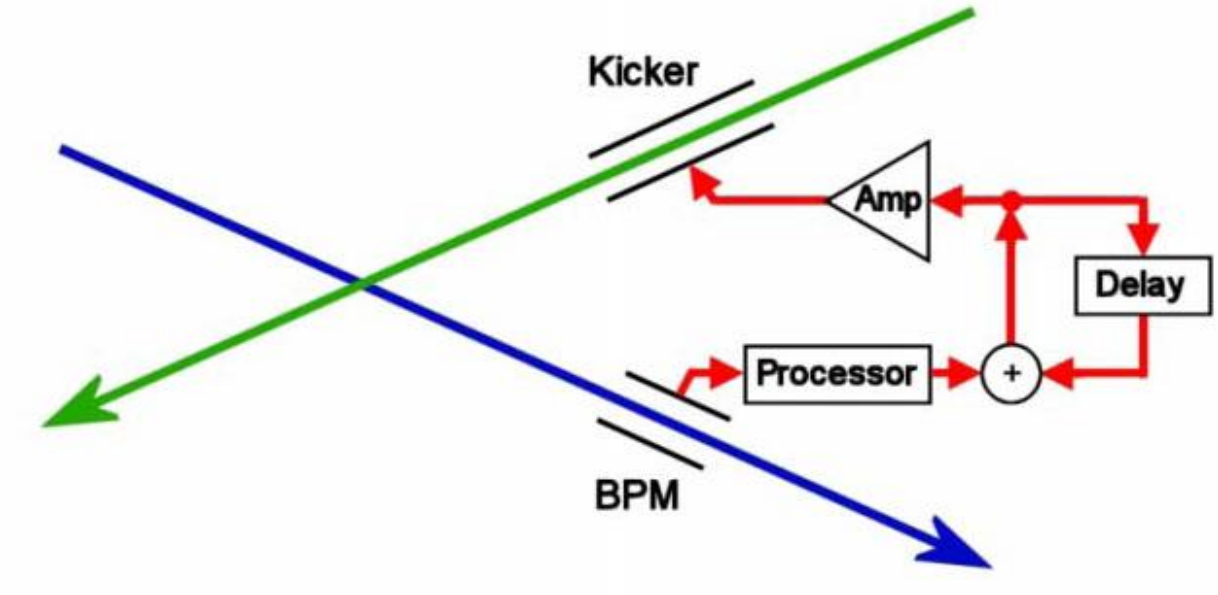
# Outline

- **Brief reminder of intra-train feedback system**
- **Implementation in ILC + CLIC IRs**
- **Prototype hardware development**

  **(FONT systems)**
- **Summary**

# IP intra-train feedback system - concept

- Last line of defence against relative beam misalignment
- Measure vertical position of outgoing beam and hence beam-beam kick angle
- Use fast amplifier and kicker to correct vertical position of beam incoming to IR




**FONT – Feedback On Nanosecond Timescales**

**(Oxford, Valencia, CERN, DESY, KEK, SLAC)**

# General considerations (1)

**1. IP position feedback:**

**hardware located near IP**

**kicker at 90 degrees w.r.t. IP**

**2. IP angle feedback:**

**hardware ideally located near IP**

**kicker in phase w.r.t. IP**

**3. Additional possible inputs:**

**fast luminosity signal (from BEAMCAL)**

**information from alignment systems (eg. QD0 etc.)**

**‘feed-forward’ information from upstream in machine (eg. DR)**

**…**

# General considerations (2)

**Time structure of bunch train:**

**ILC (500 GeV): c. 3000 bunches w. c. 300 ns separation**
**CLIC (3 TeV): c. 300 bunches w. c. 0.5 ns separation**

**Feedback latency:**

**ILC: O(100ns) latency budget allows digital approach**
**CLIC: O(10ns) latency requires analogue approach**

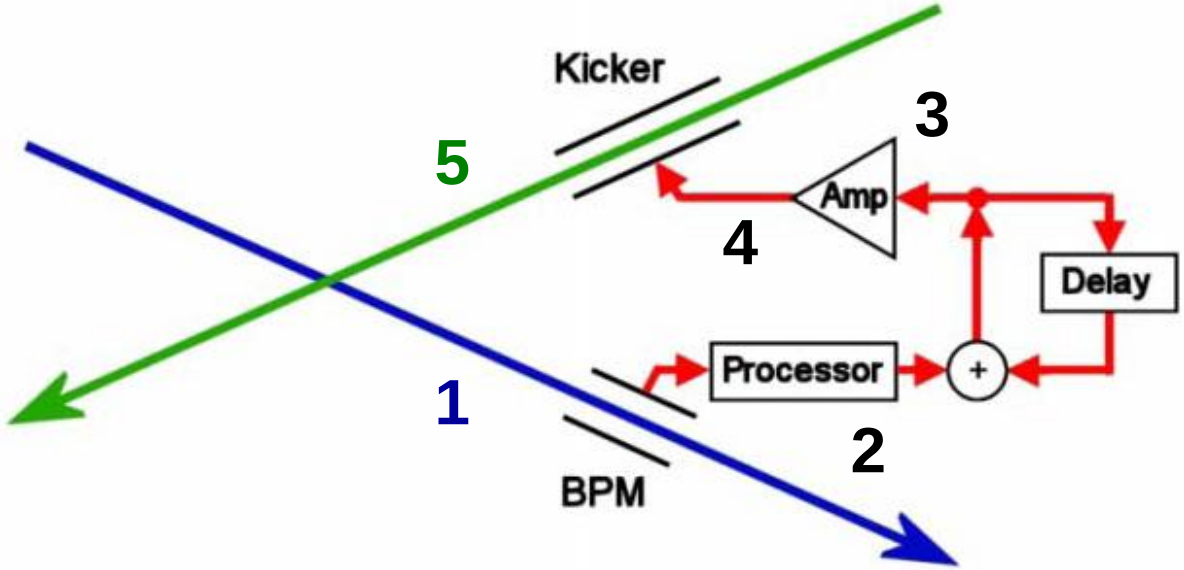
**Recall speed of light: c = 30 cm / ns:**

**FB hardware should be close to IP (especially for CLIC!)**

# IP position feedback latency

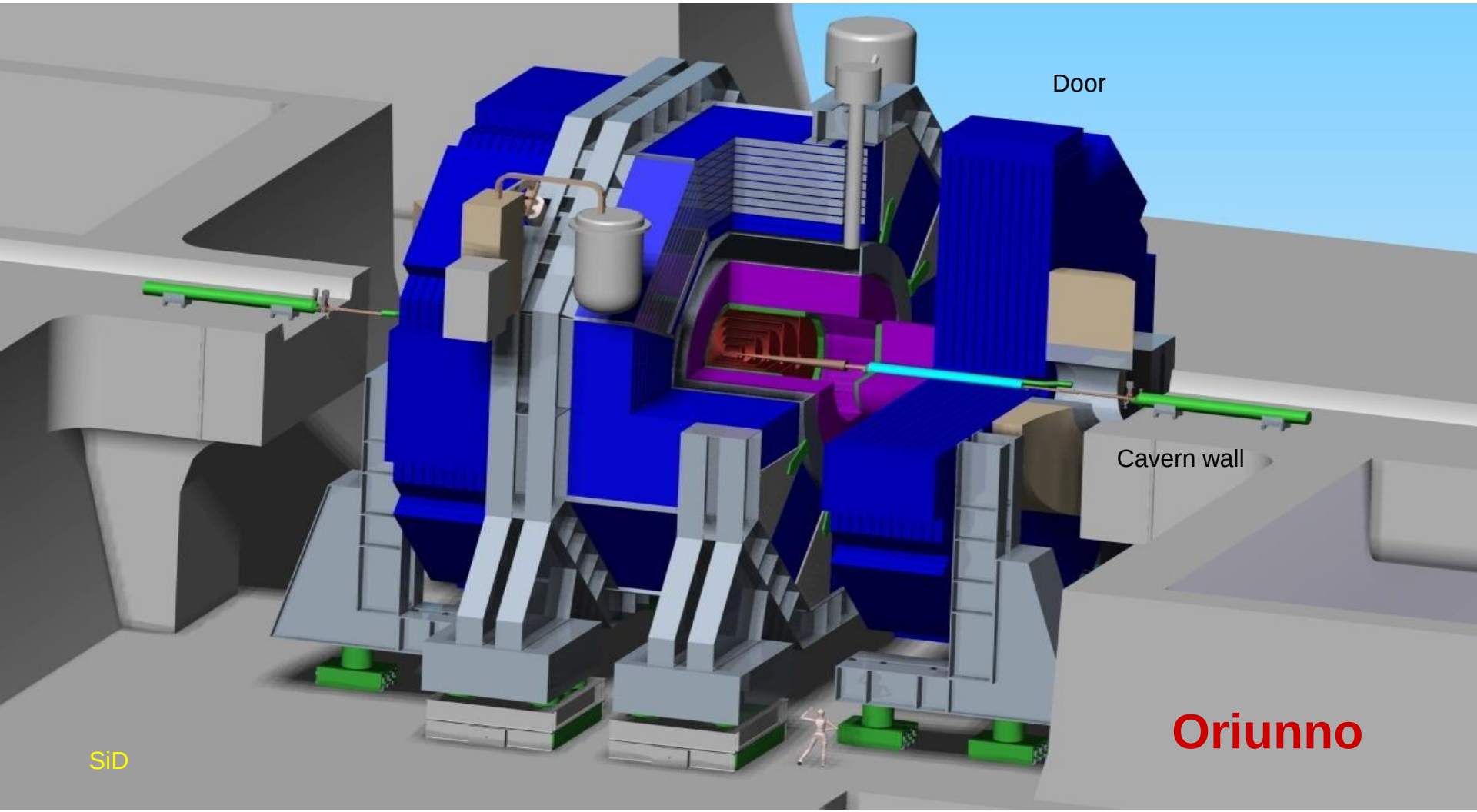
**Latency:**

1. **Beam flight time IP → BPM**
2. **Signal processing, FB calculation**
3. **Amplifier + kicker response time**
4. **Cable delays**
5. **Beam flight time kicker → IP**

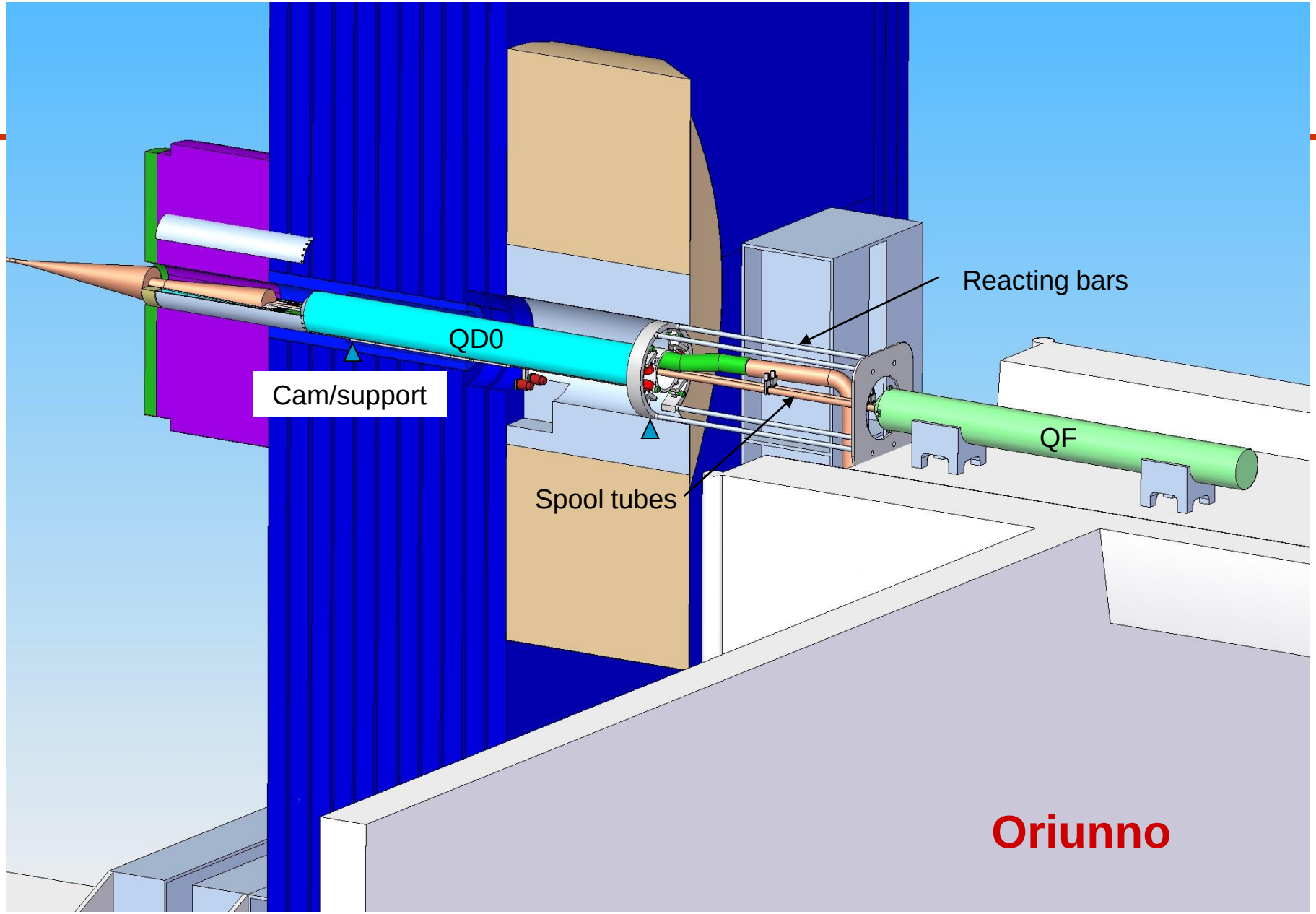



*Philip Burrows*

# ILC IR: SiD for illustration



# Final Doublet Region (SiD for illustration)



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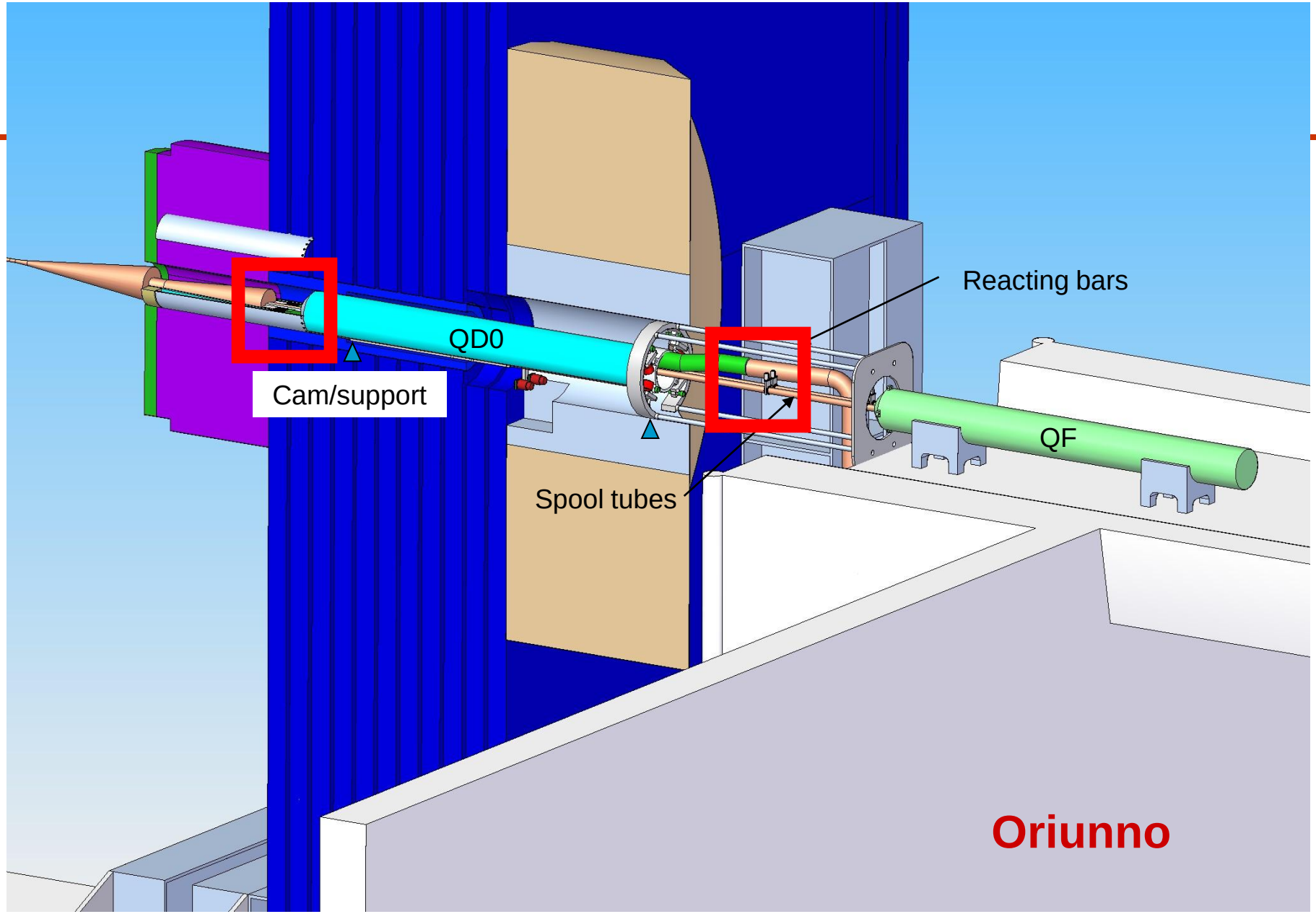
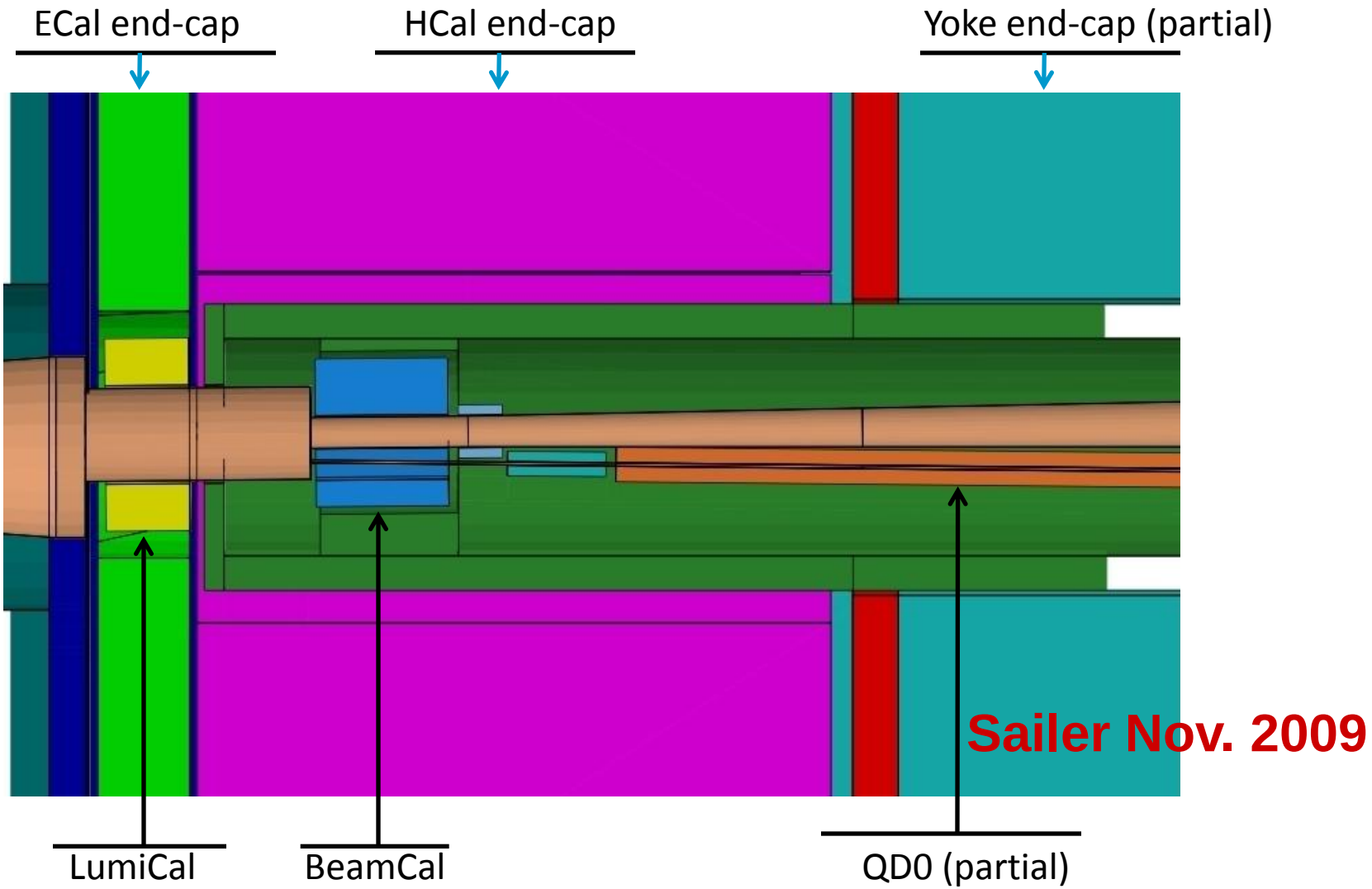
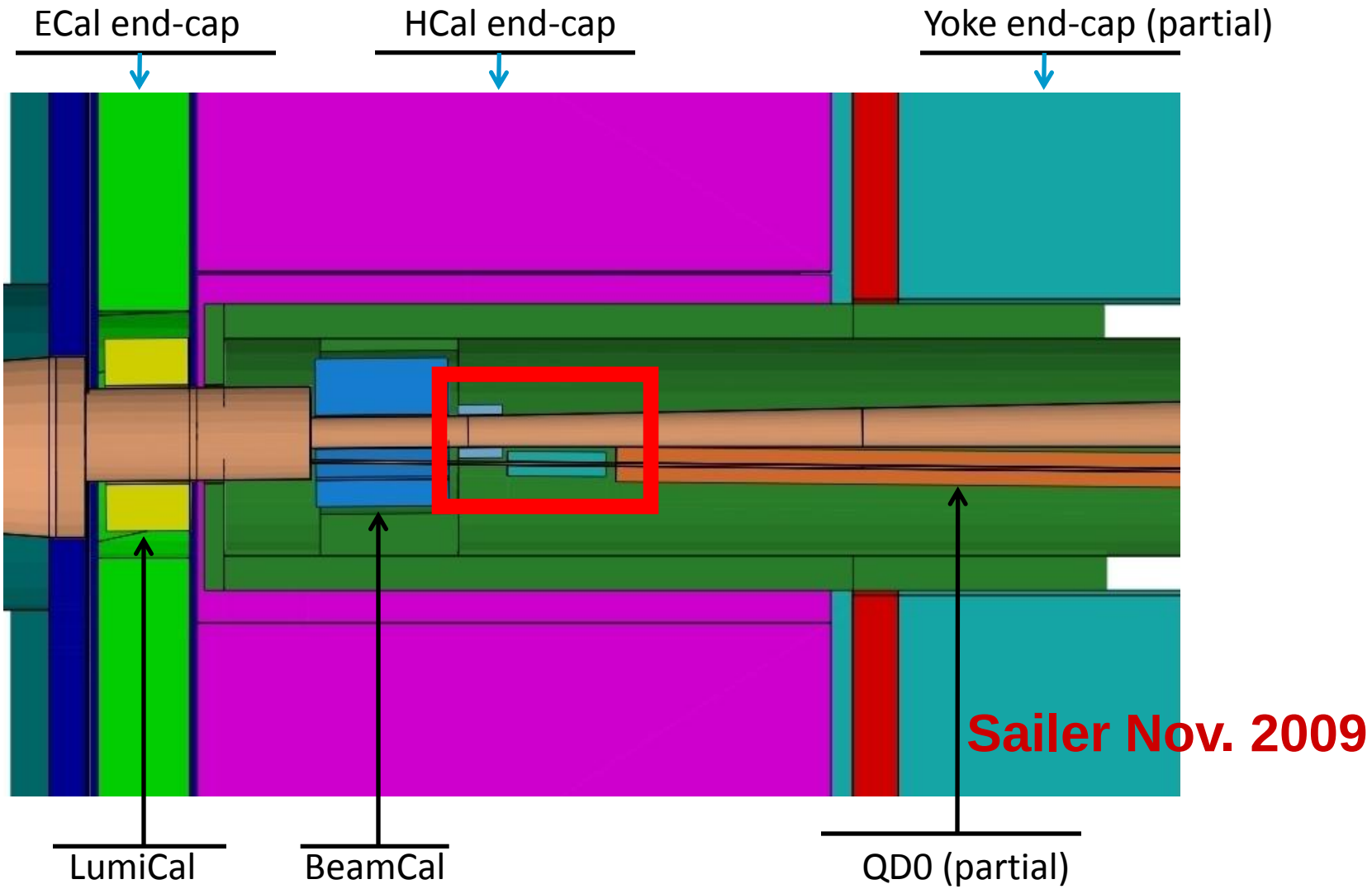


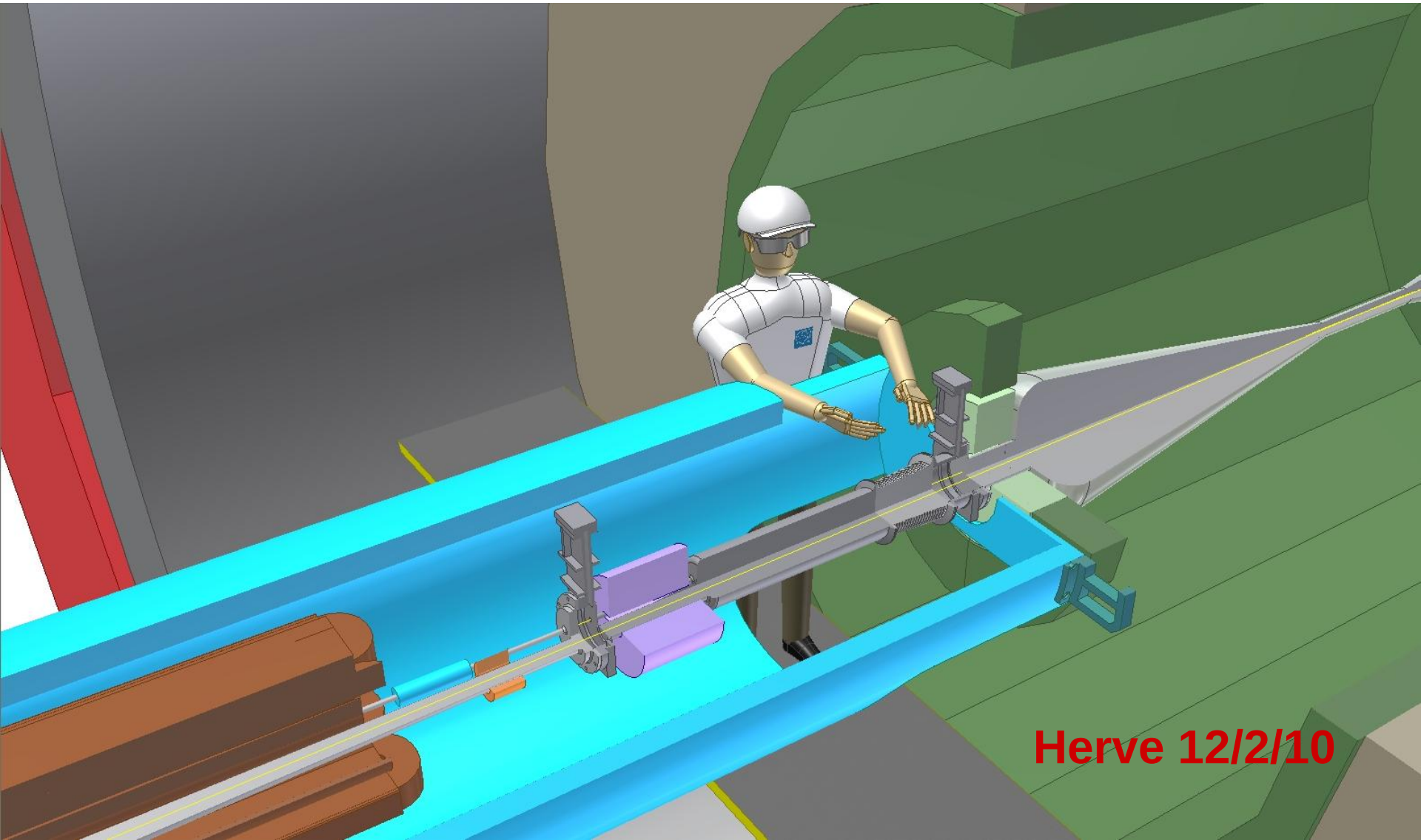
# CLIC: ILD for illustration



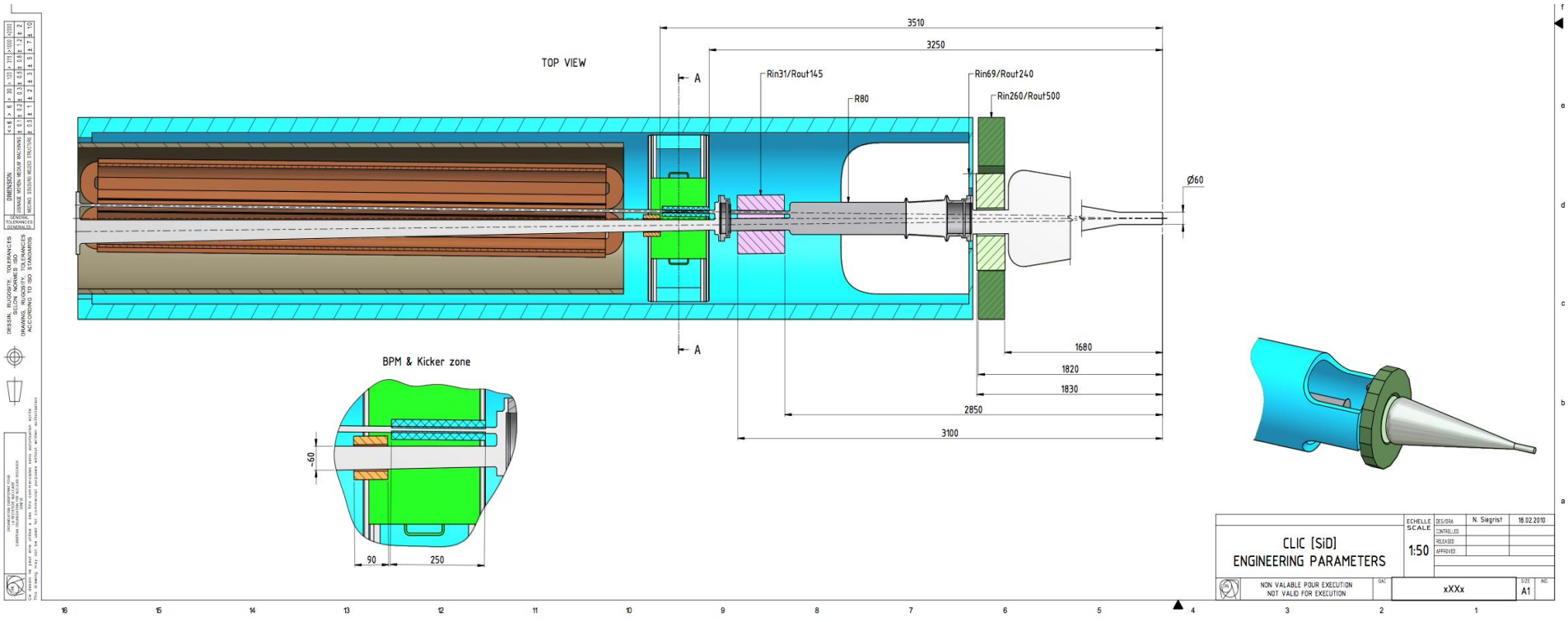
# CLIC: ILD for illustration



# CLIC: zoom-in to QD0

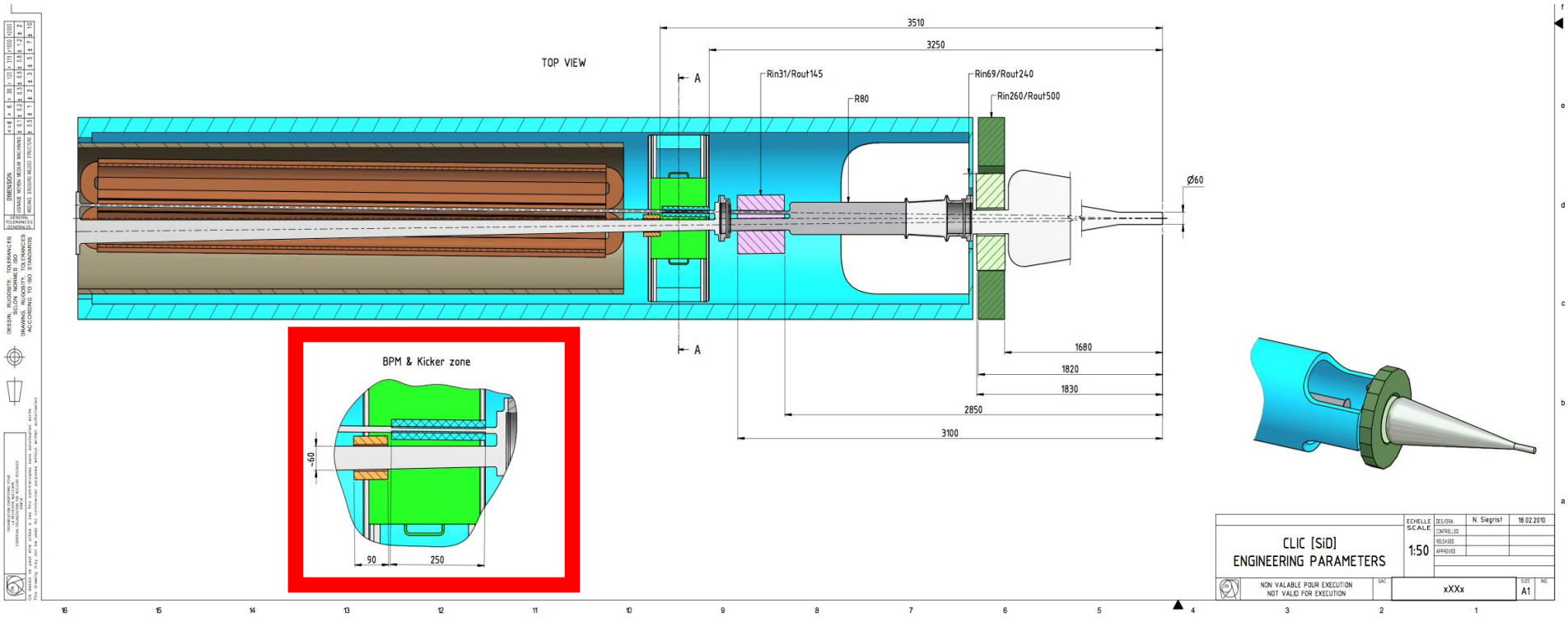


# CLIC: zoom-in to QD0




**Herve 22/2/10**

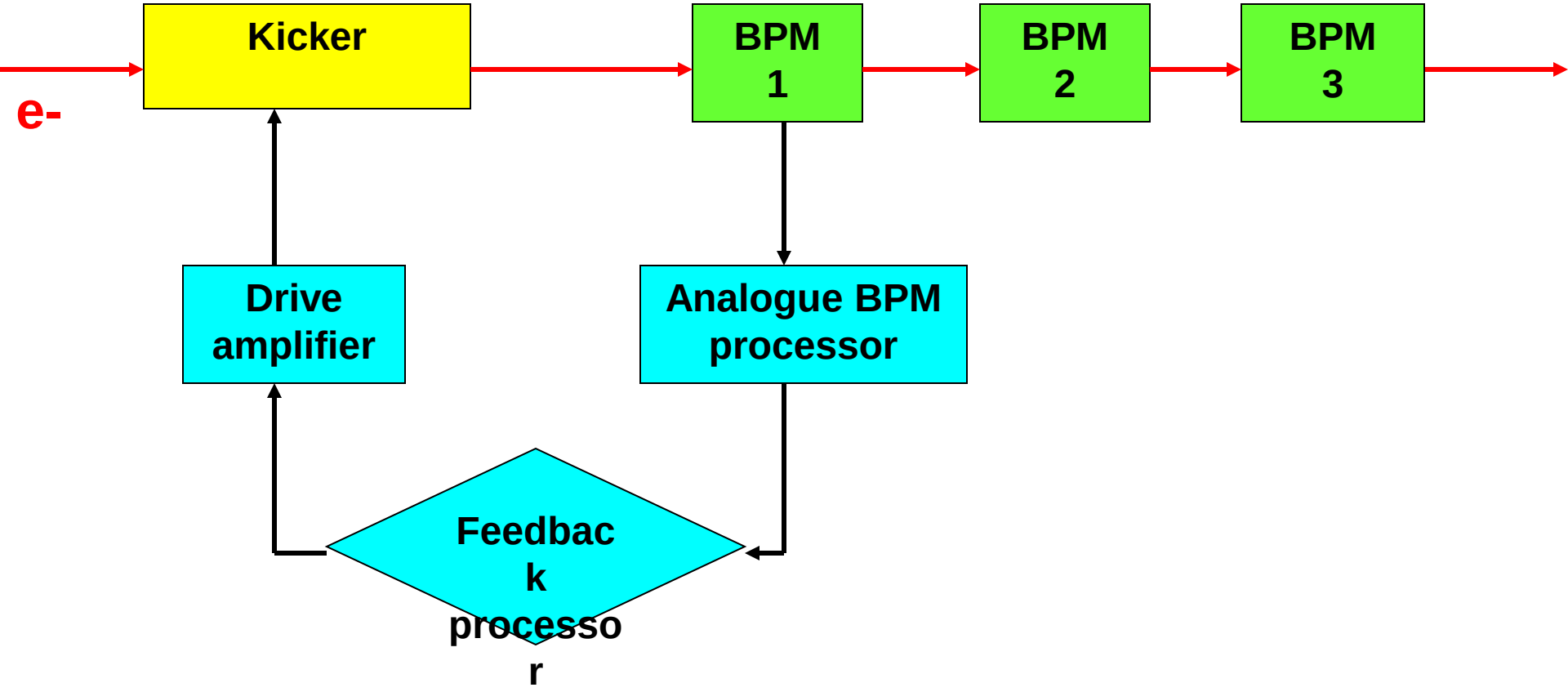
# CLIC: zoom-in to QD0




**Herve 22/2/10**

# Prototyping status

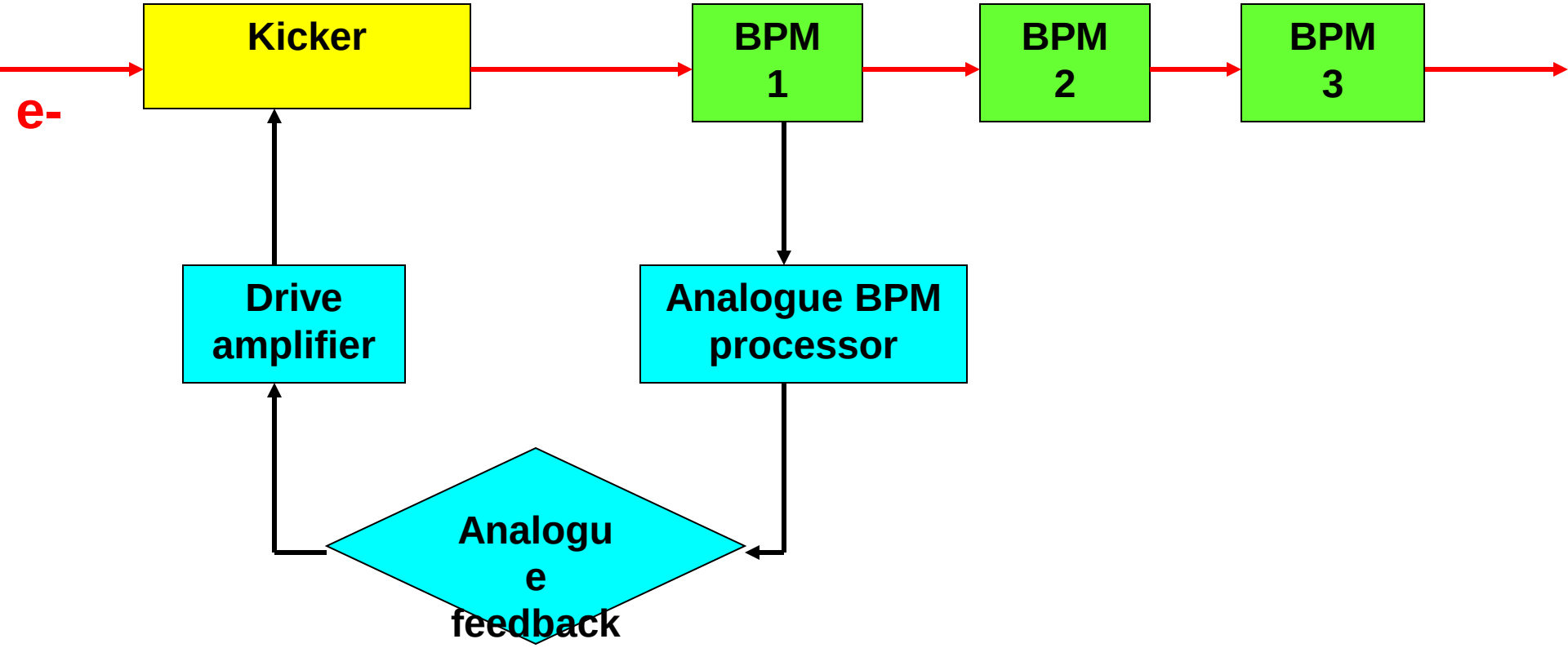
# Generic prototype layout



# Brief prototype history: CLIC

## CLIC-relevant: all-analogue systems

# Generic prototype layout: CLIC



# Brief prototype history: CLIC

## CLIC-relevant: all-analogue systems

- NLCTA (SLAC): 65 MeV beam, 170ns train, 87ps bunch spacing

**FONT1 (2001-2):**

First demonstration of closed-loop FB: latency 67ns

10/1 beam position correction

**FONT2 (2003-4):**

Improved demonstration of FB: latency 54ns

real time charge normalisation with logarithmic amplifiers

beam flattener to straighten train profile

solid-state amplifier

- ATF (KEK): 1.3 GeV beam, 56ns train, 2.8ns bunch spacing

**FONT3 (2004-5):**

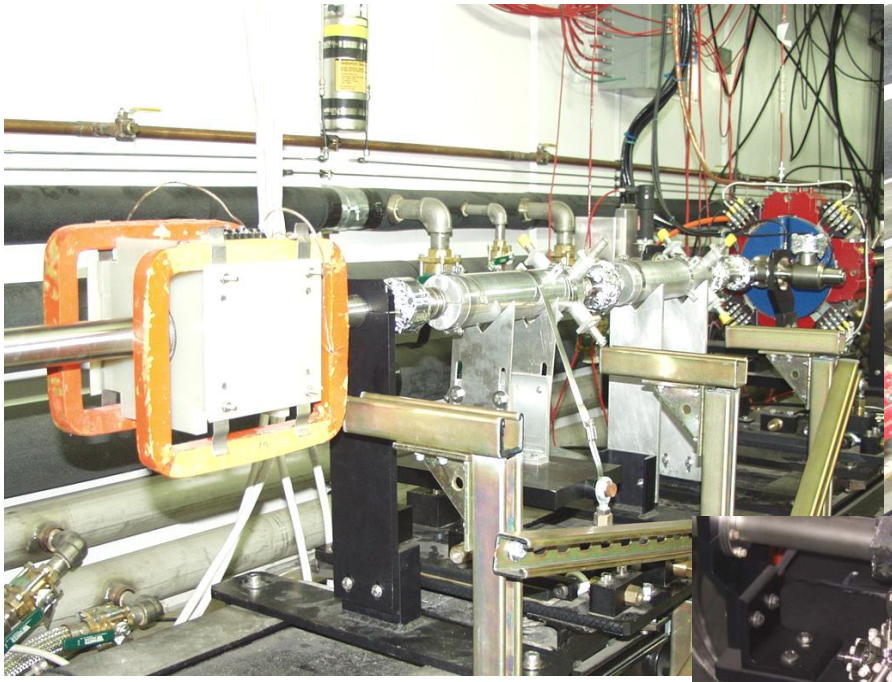
Ultra-fast demonstration of FB: latency 23 ns

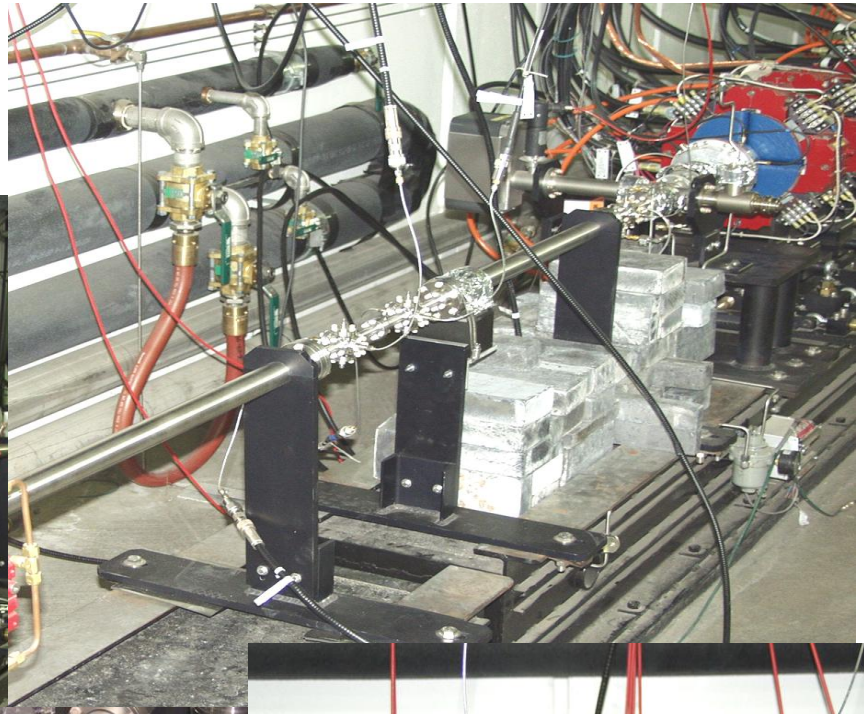
3 stripline BPMs

high-power solid-state amplifier

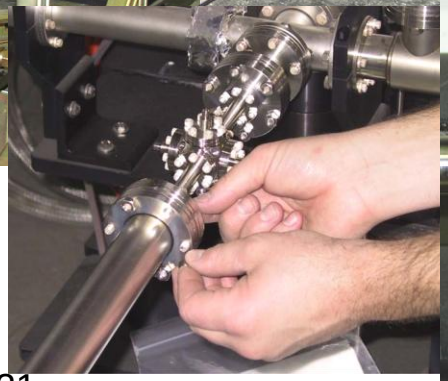
# FONT2 beamline installation at SLAC NLCTA
## (65 MeV 170ns-long train @ 87ns spacing)

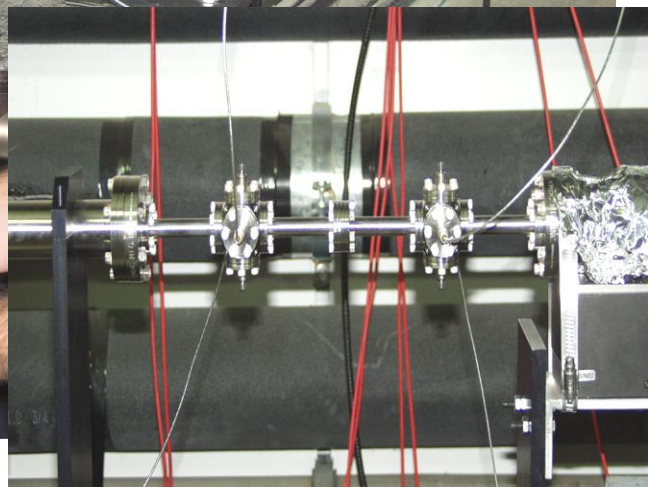
**Dipole and kickers**





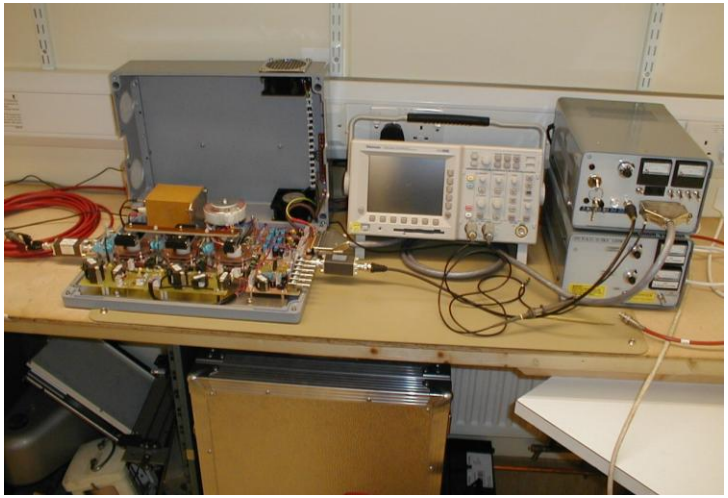
**BPMs**





# FONT: kicker driver amplifiers

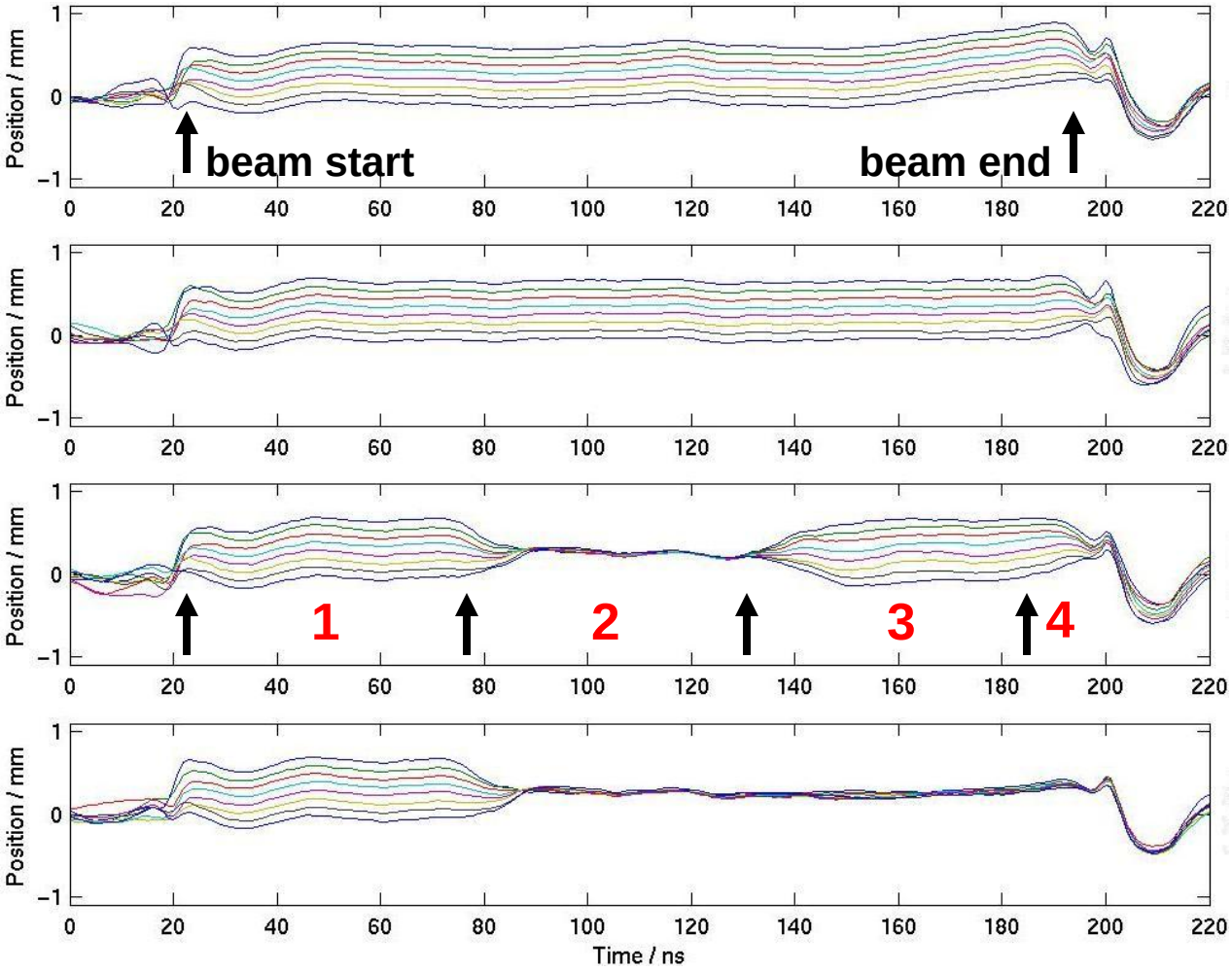
**FONT1 3-stage tube amplifier**



**FONT3 PCB amplifer + FB**

**Same drive power as needed for CLIC**

# FONT2 results




Beam starting positions

Beam flattener on

Feedback on

Delay loop on

# FONT3: latency budget

- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 6ns

  Irreducible latency: 10ns

- BPM processor: 5ns
- Amplifier + FB: 5ns

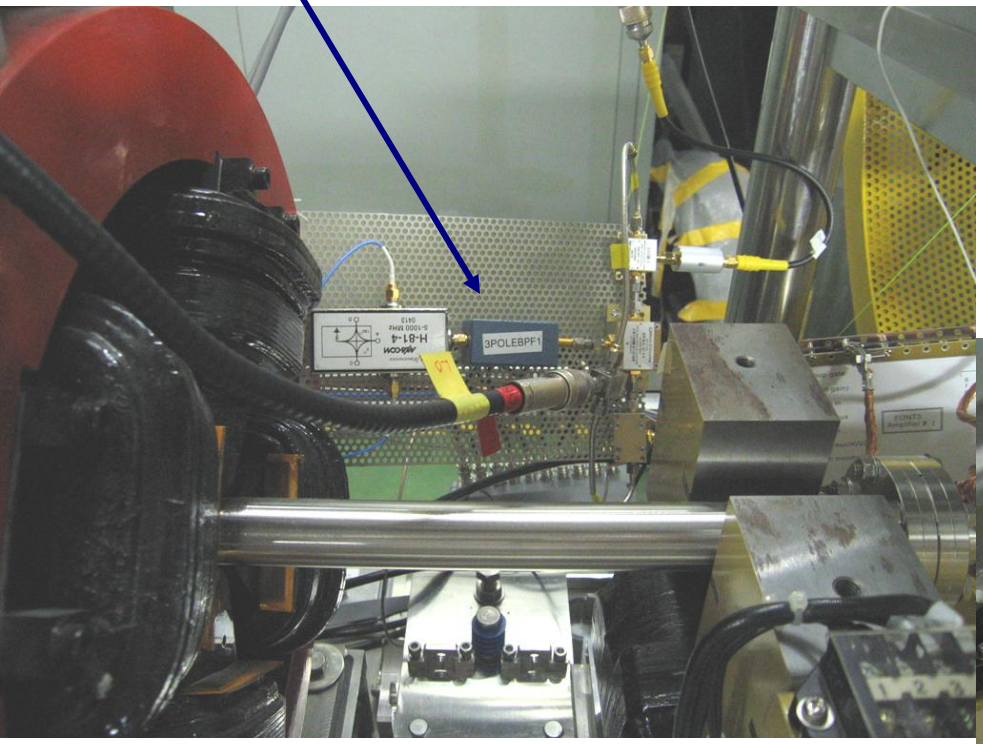
  Electronics latency: 10ns

- Total latency budget: 20ns

Allows 56/20 = 2.8 periods during bunchtrain

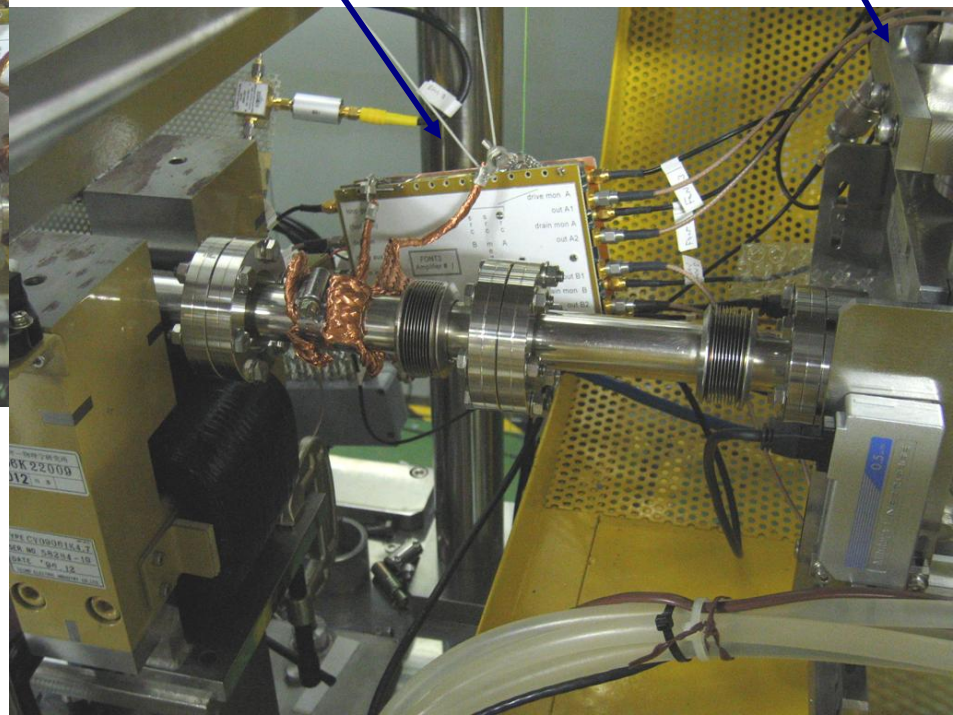
# FONT3: BPM processor + amplifier/feedback installation in ATF beamline

BPM processor board

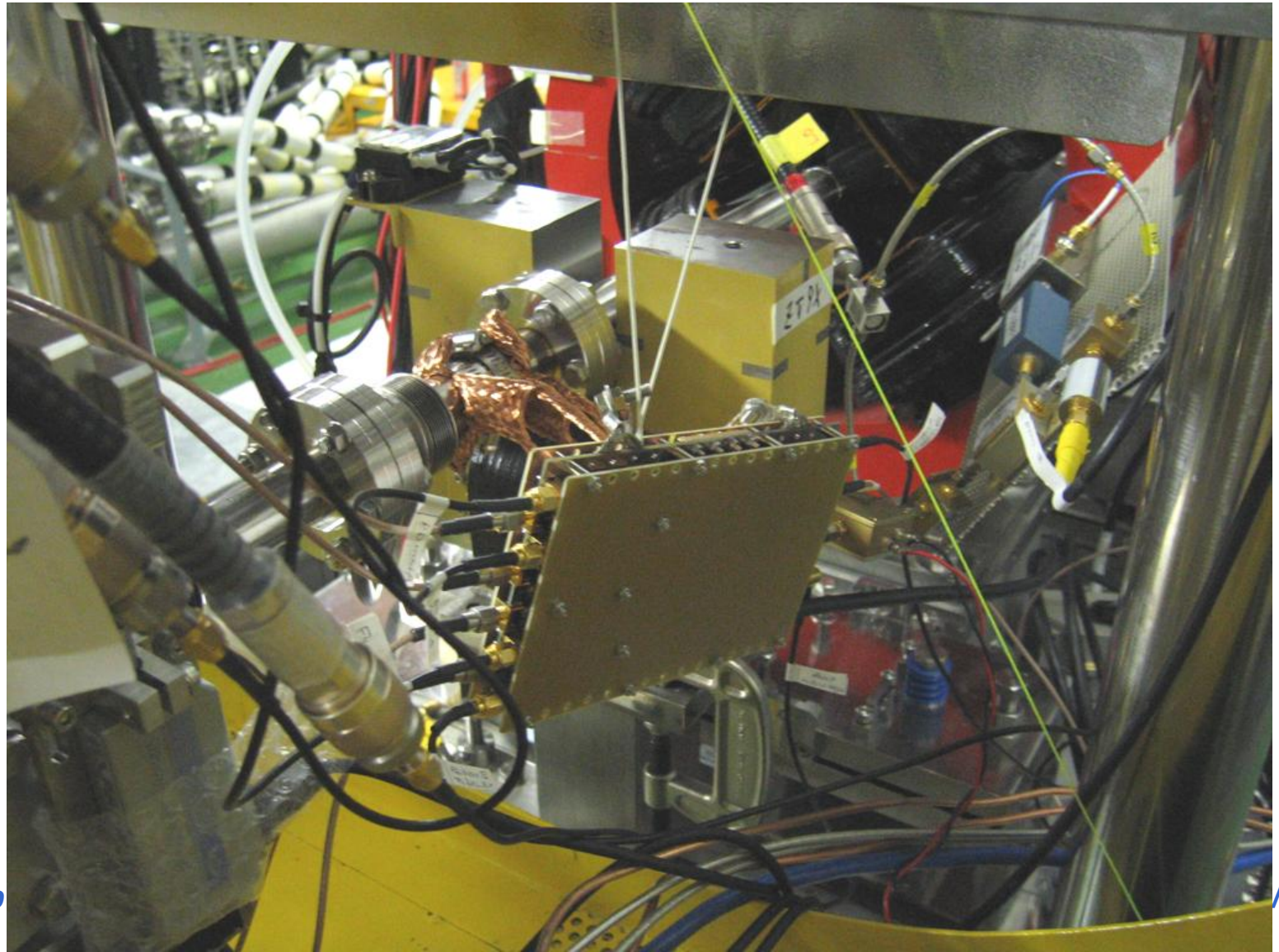



FEATHER kicker

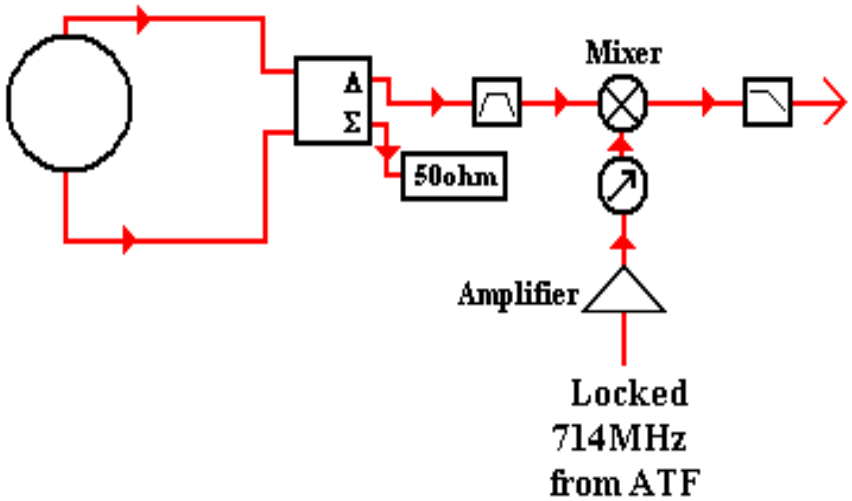
Amplifier/FB board

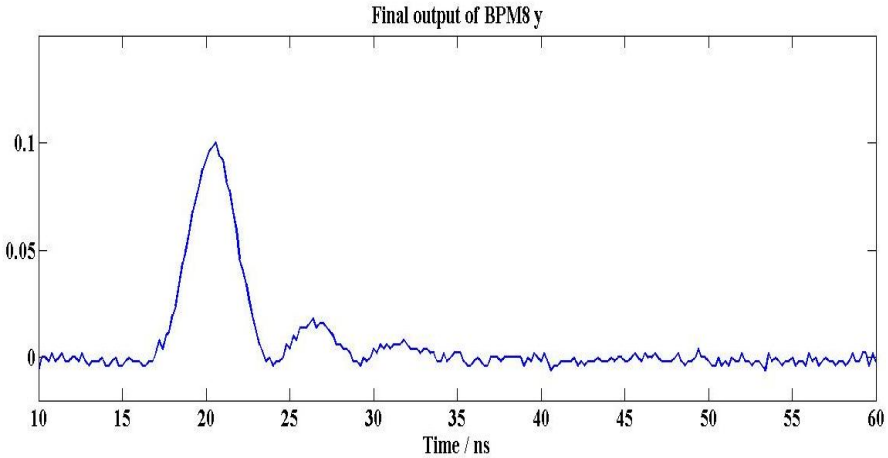


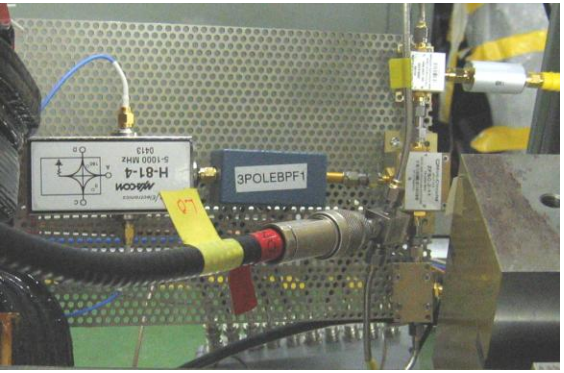
# FONT3: Beamline Installation



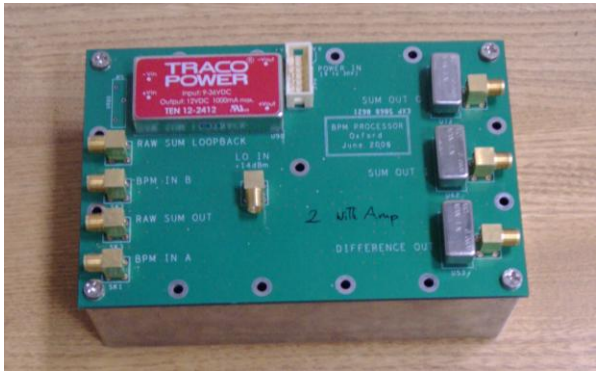
# Fast analogue signal processors



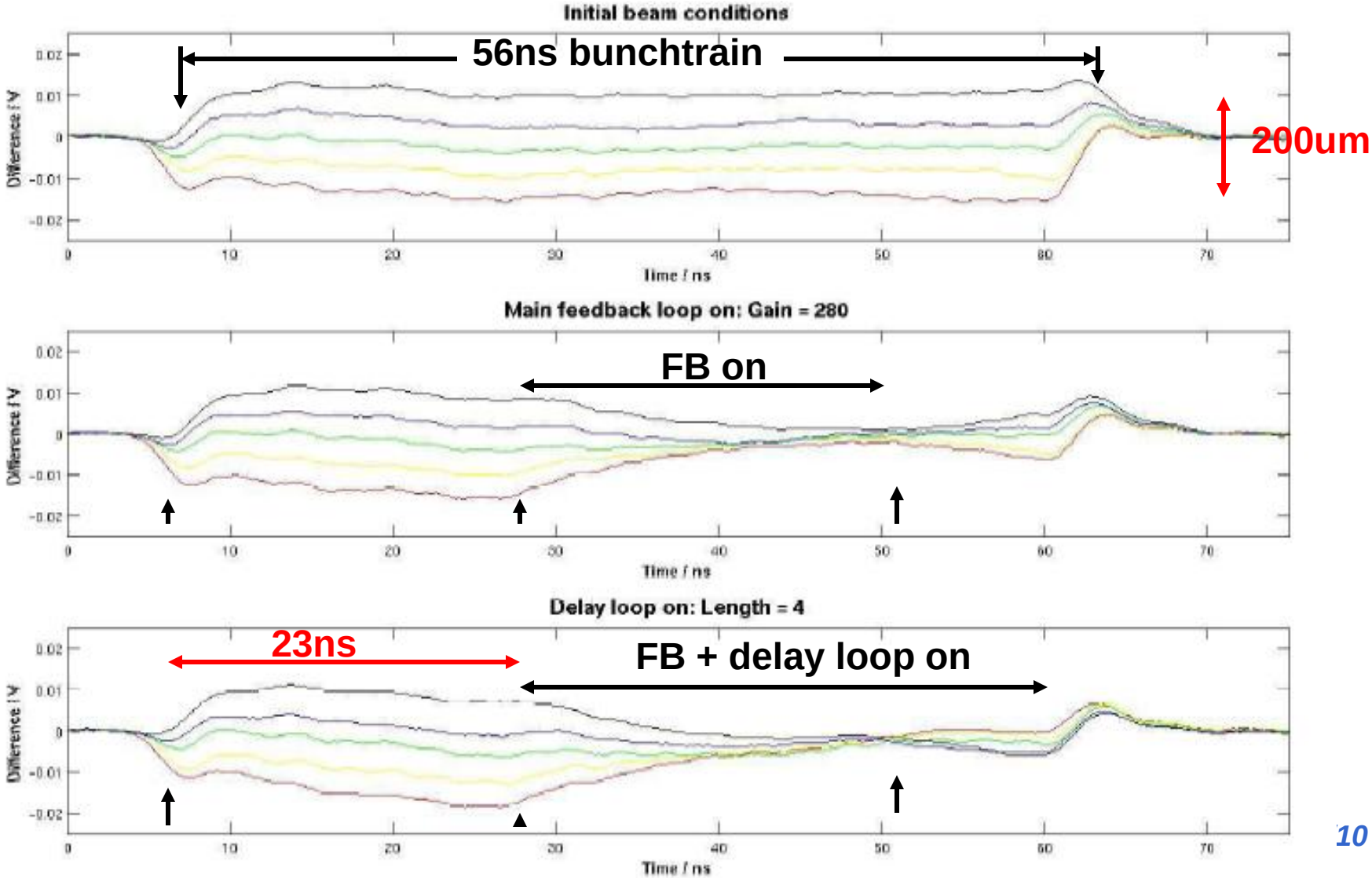

**2005**



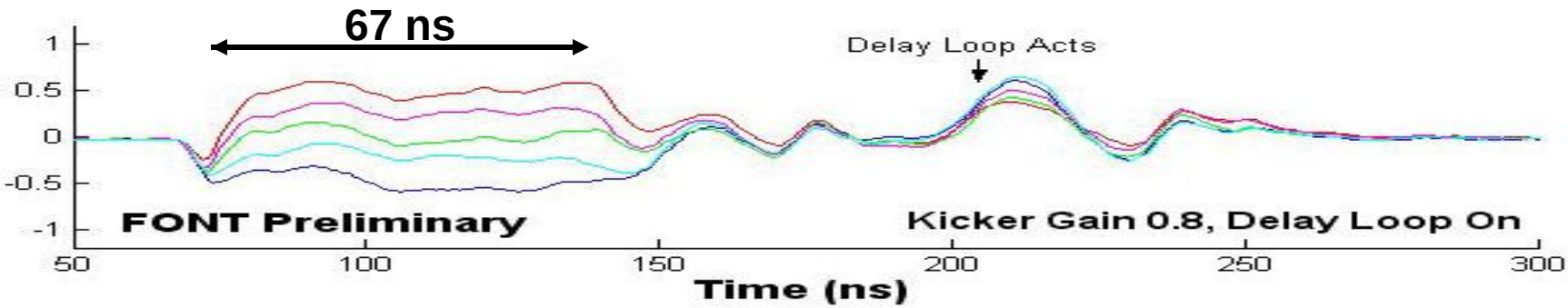

**2006**

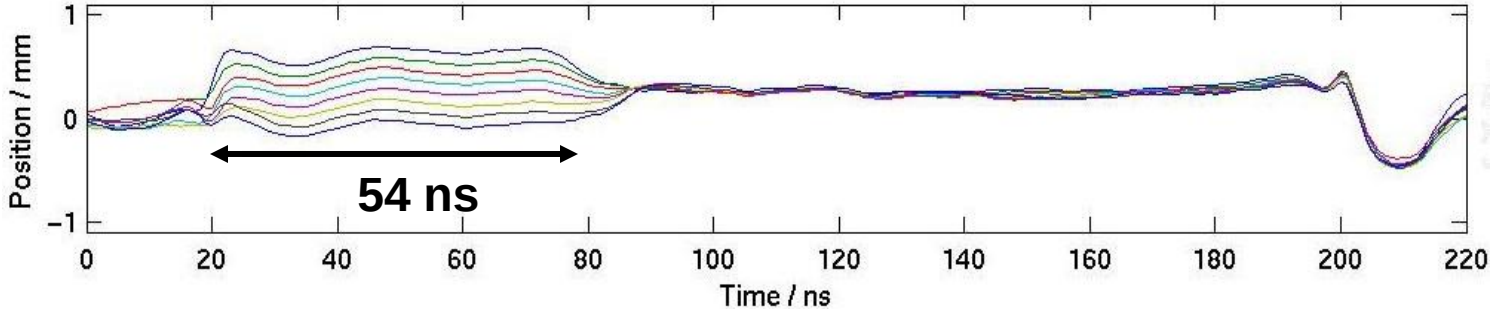

**2007**

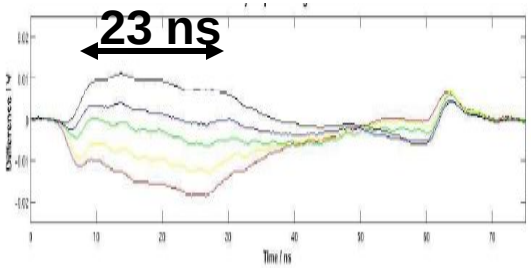
# FONT3: Results (June 3 2005):
## Delay-loop feedback w. latency 23 ns



# CLIC prototype: Summary



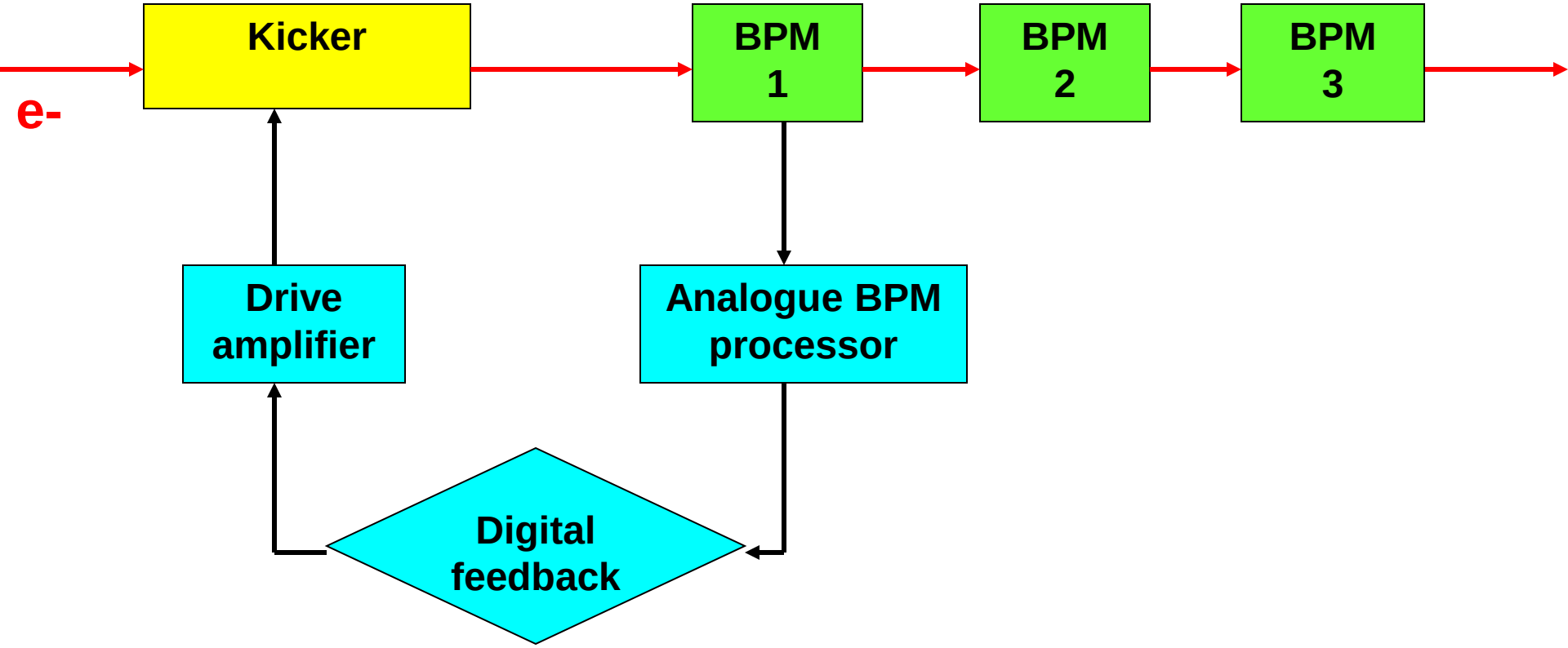




**Basic principle demonstrated.**
**More work needed to optimise**
**Design + system performance.**

# Brief prototype history: ILC

## ILC-relevant: digital feedback processor

# Generic prototype layout: ILC



# Brief prototype history: ILC

## ILC-relevant: digital feedback processor

- ATF (KEK): 1.3 GeV beam, 3-bunch train, bunch spacing c. 150ns

**FONT4 / ATF (2006-9):**

First digital system (Virtex 4): latency 148 ns

high-power solid-state amplifier (pulse length up to 10us)

**FONT5 / ATF2 (2009-10):**

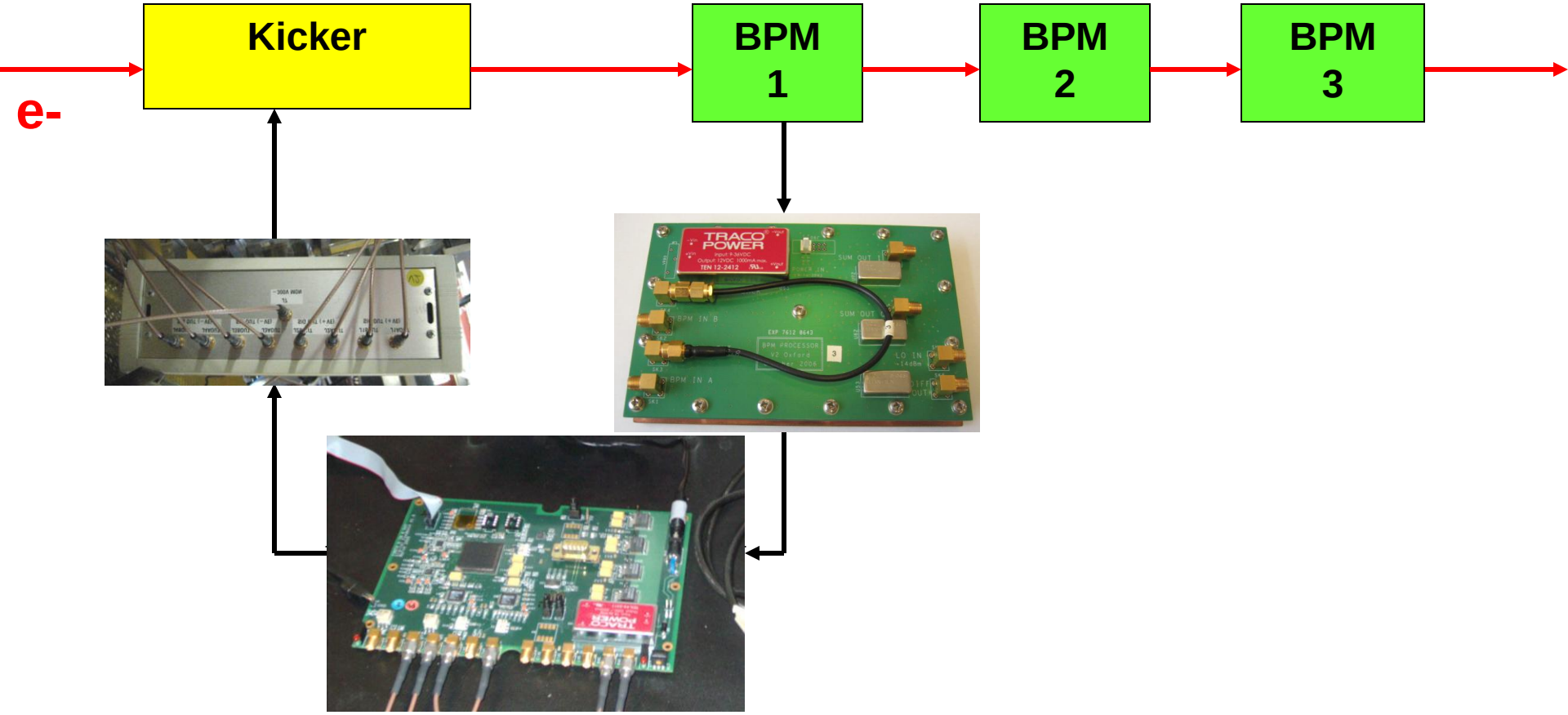
Faster system (Virtex 5): latency 133 ns

coupled-loop system

correction of y and y'

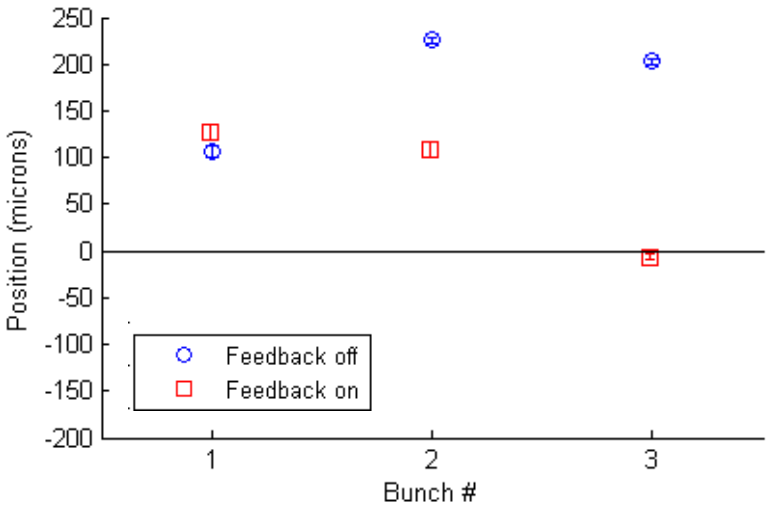
3 BPMs and 2 kickers

# FONT4 ILC prototype at KEK/ATF



# FONT4 results

- **FONT4 basic operation demonstrated in 2008 running:**



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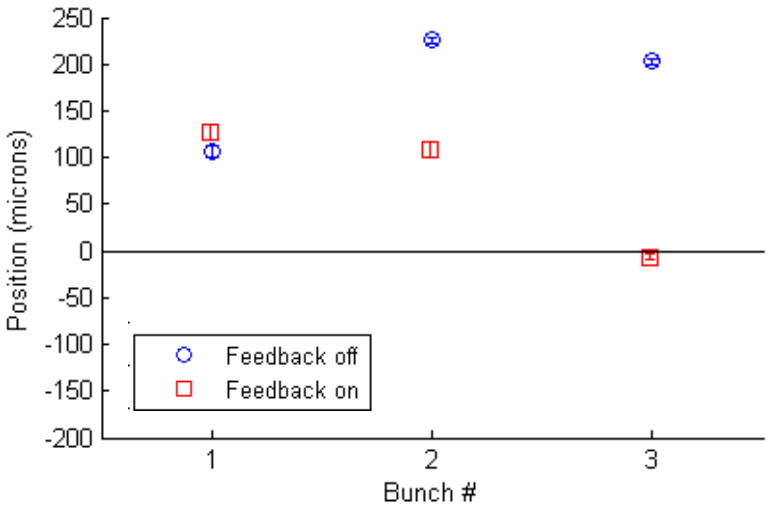


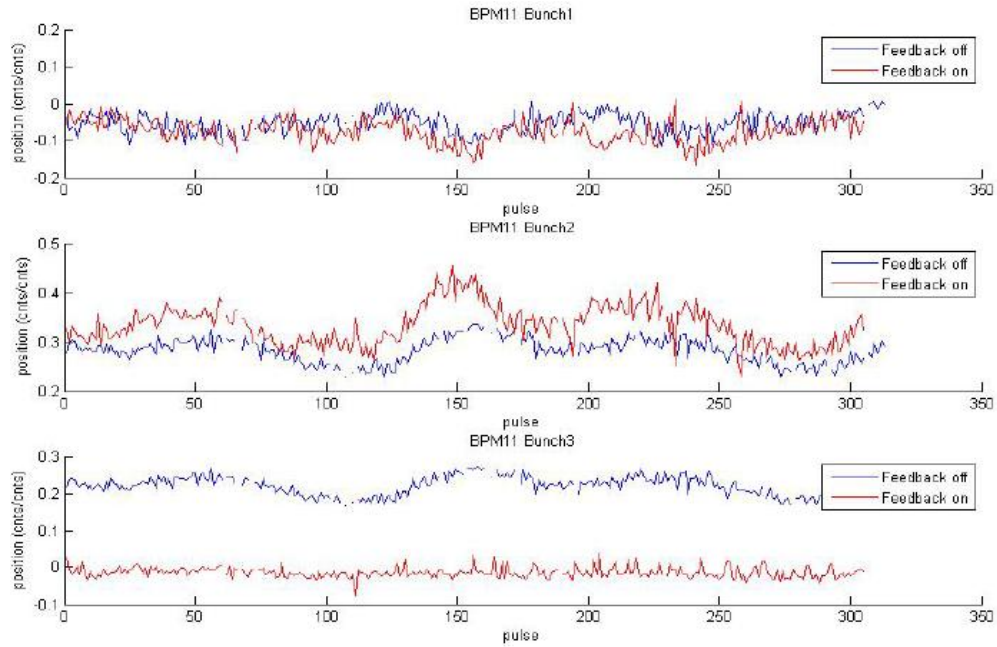

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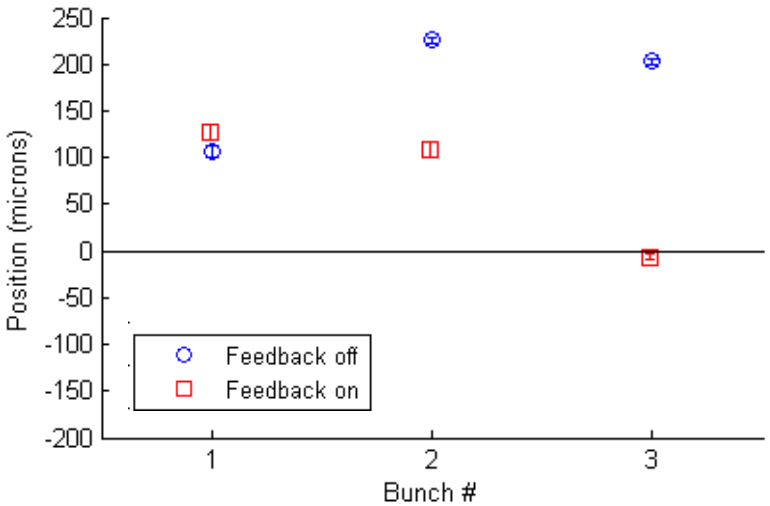
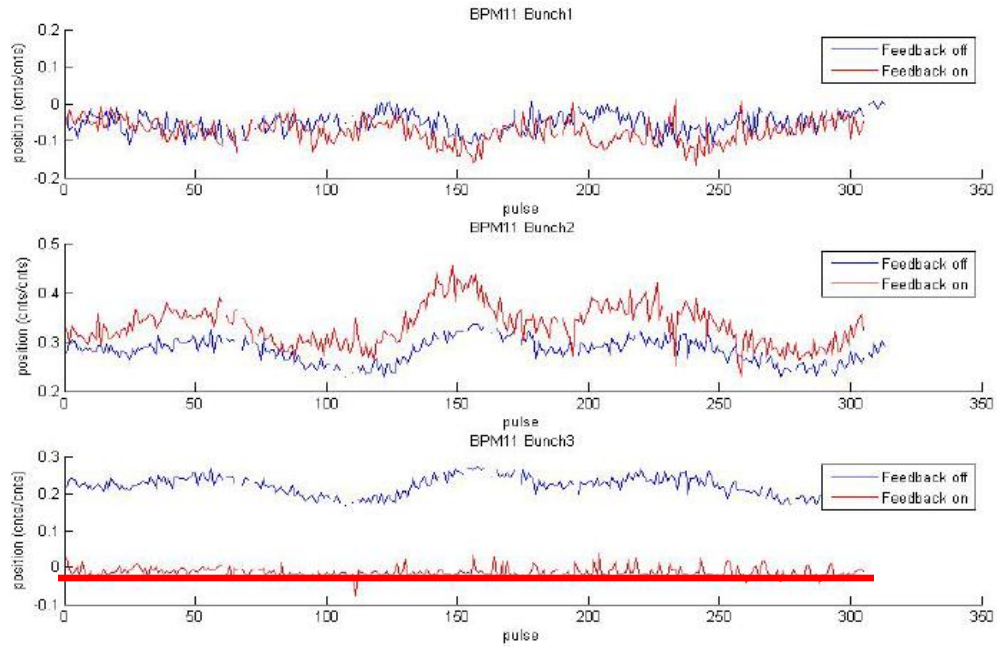
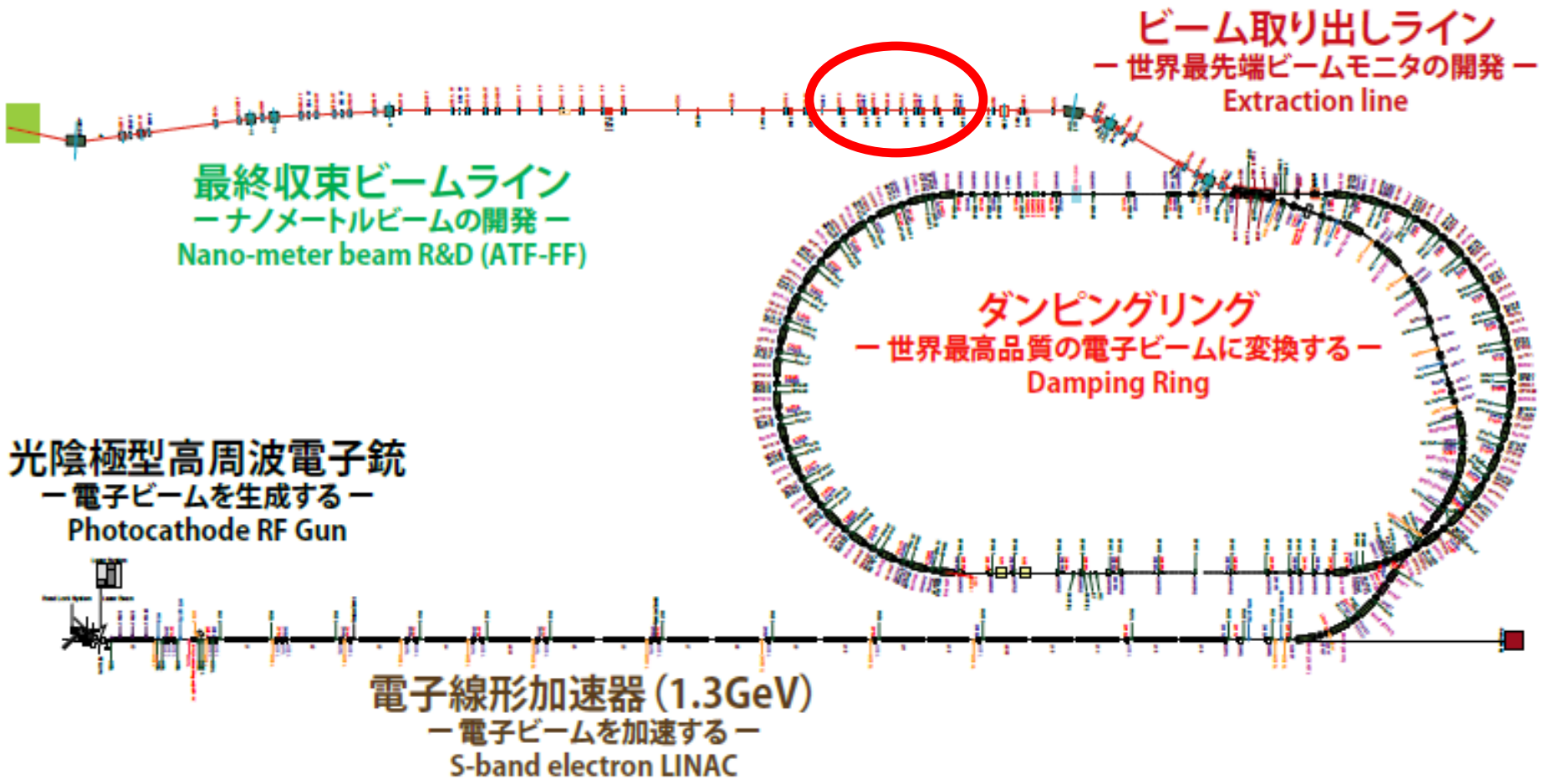


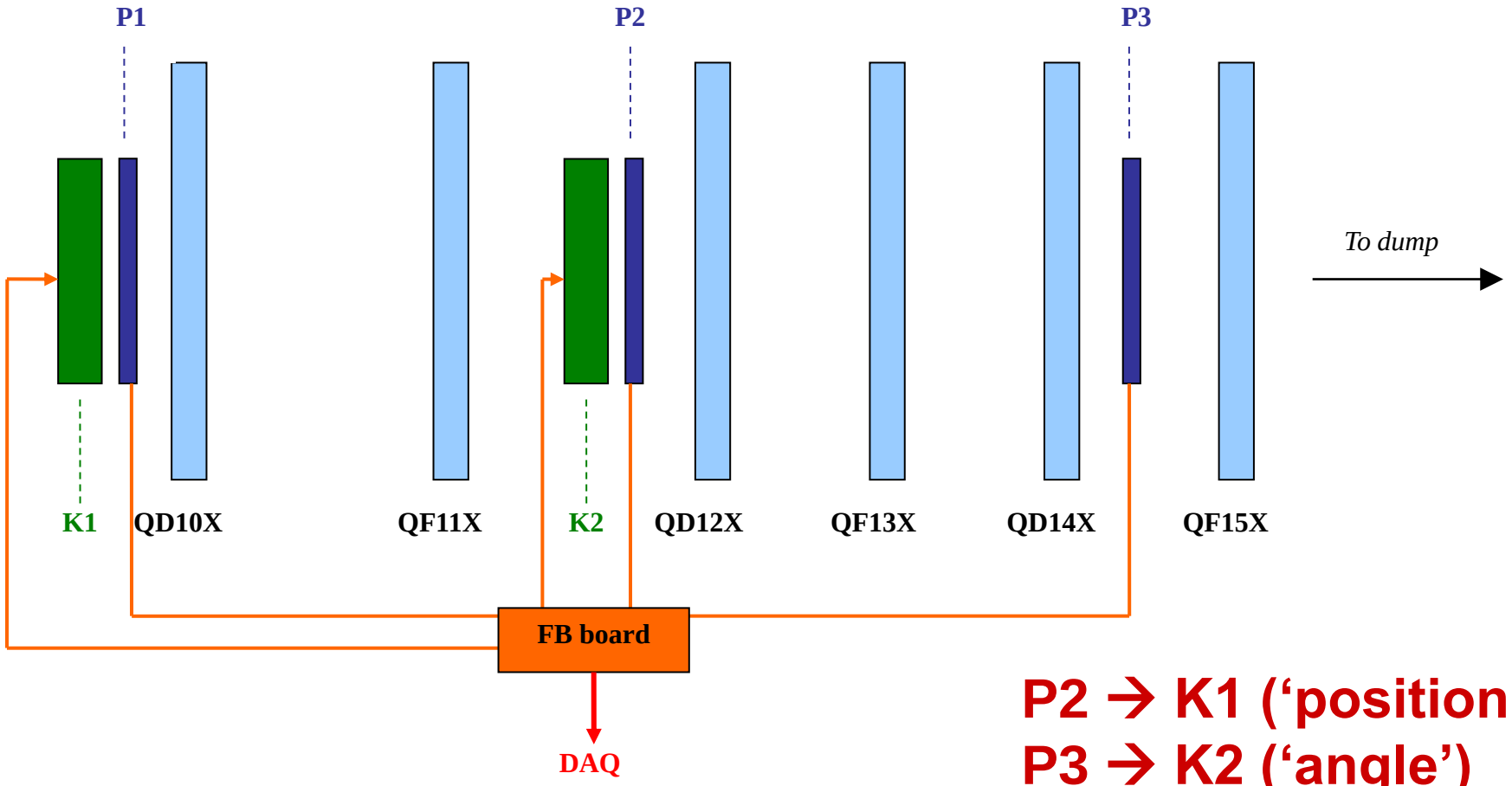




**beam feedback along single axis (y) with few micron resolution**

# FONT5 location

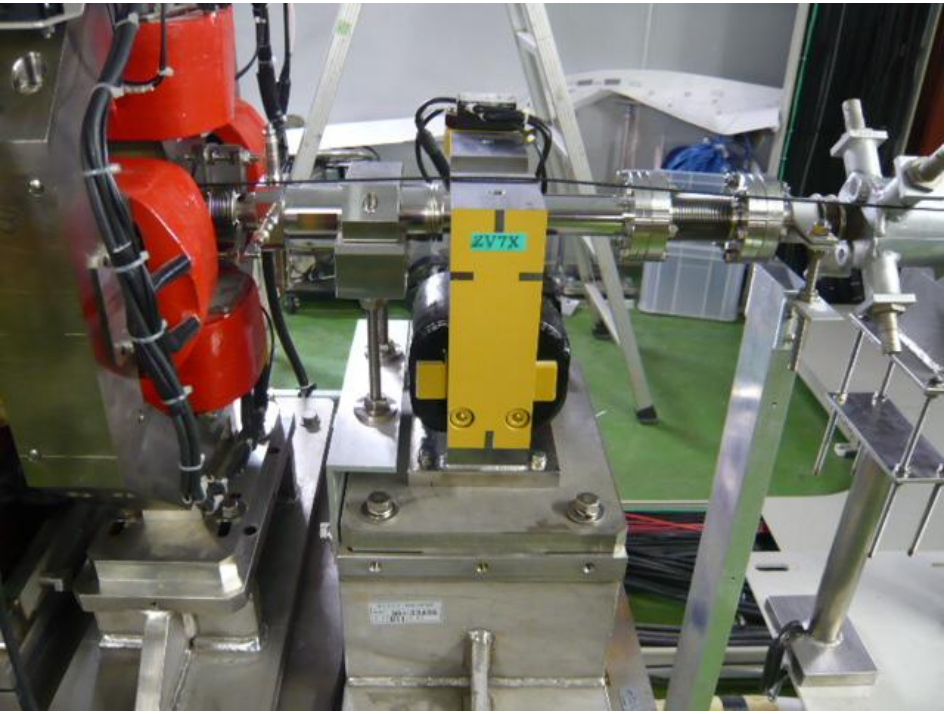


# Flexible operation mode

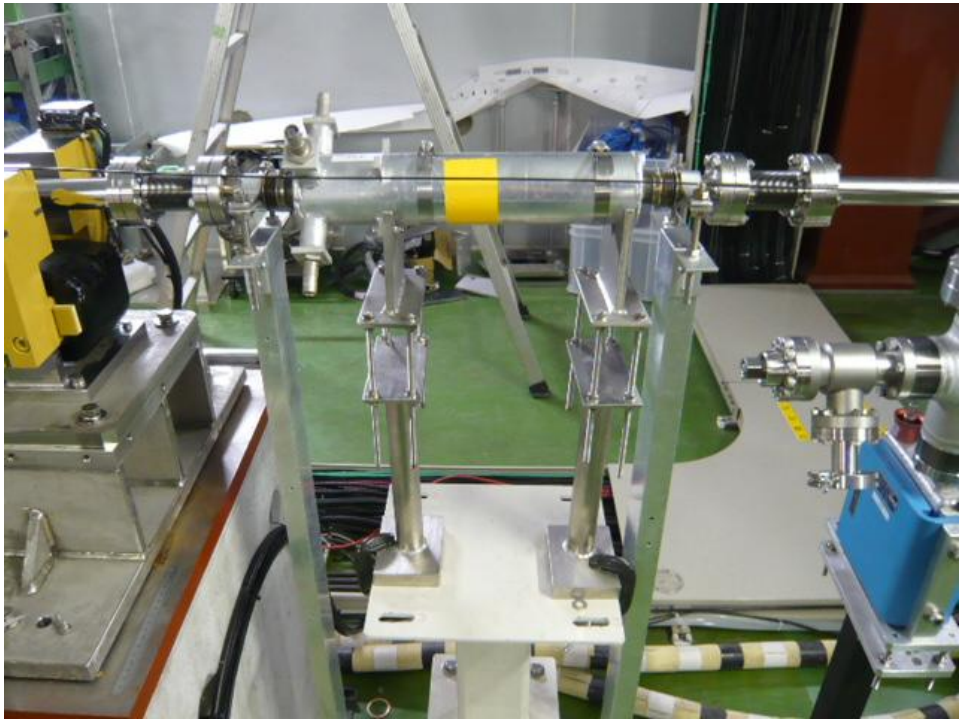



**P2 → K1 ('position')**
**P3 → K2 ('angle')**
**P3 → K1**

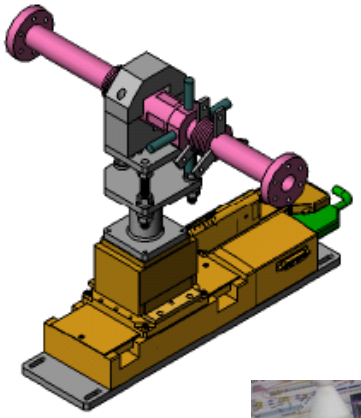
# FONT5 hardware

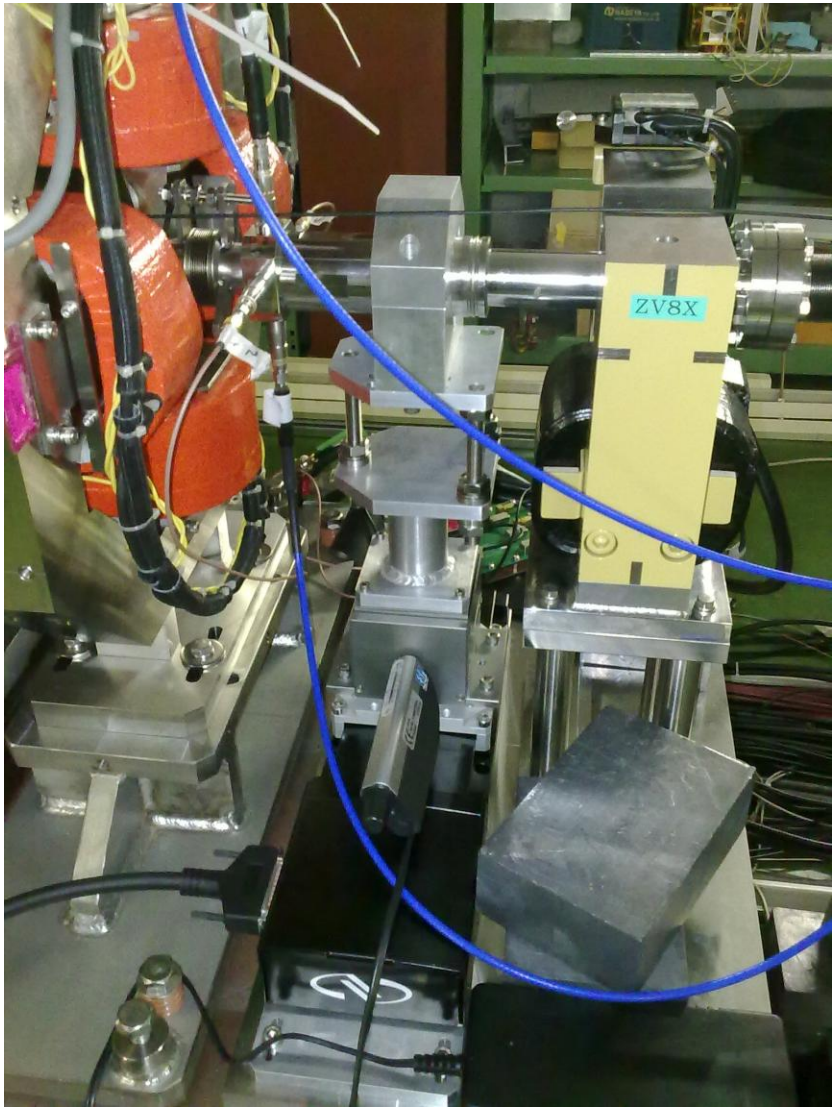



**3 new BPMs and 2 new kickers installed in new ATF2 extraction line February 2009**

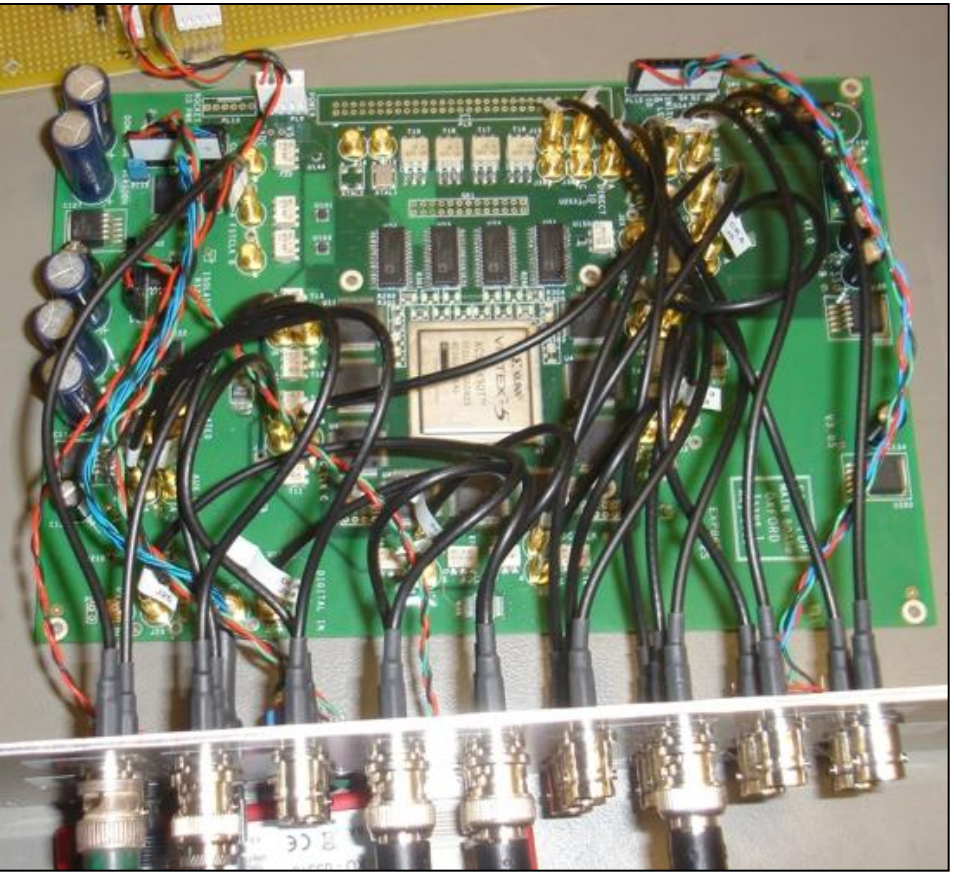


# Valencia FONT BPM movers





# New FONT5 digital FB board



**Xilinx Virtex5 FPGA**

**9 ADC input channels (TI ADS5474)**

**4 DAC output channels (AD9744)**

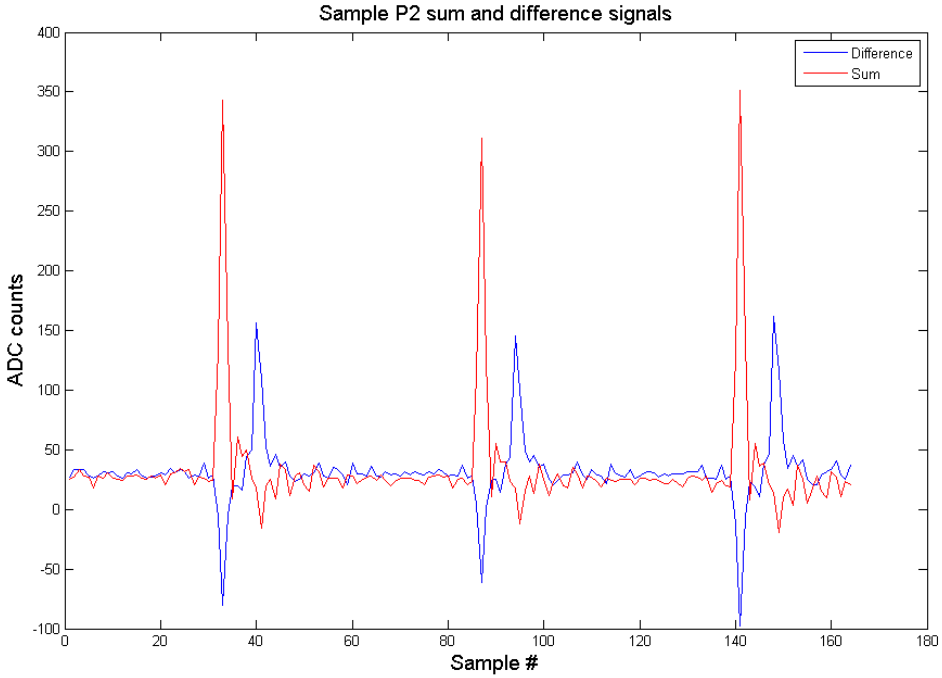
**Clocked at 357 MHz phase-locked to beam**

**4x faster than FONT4**

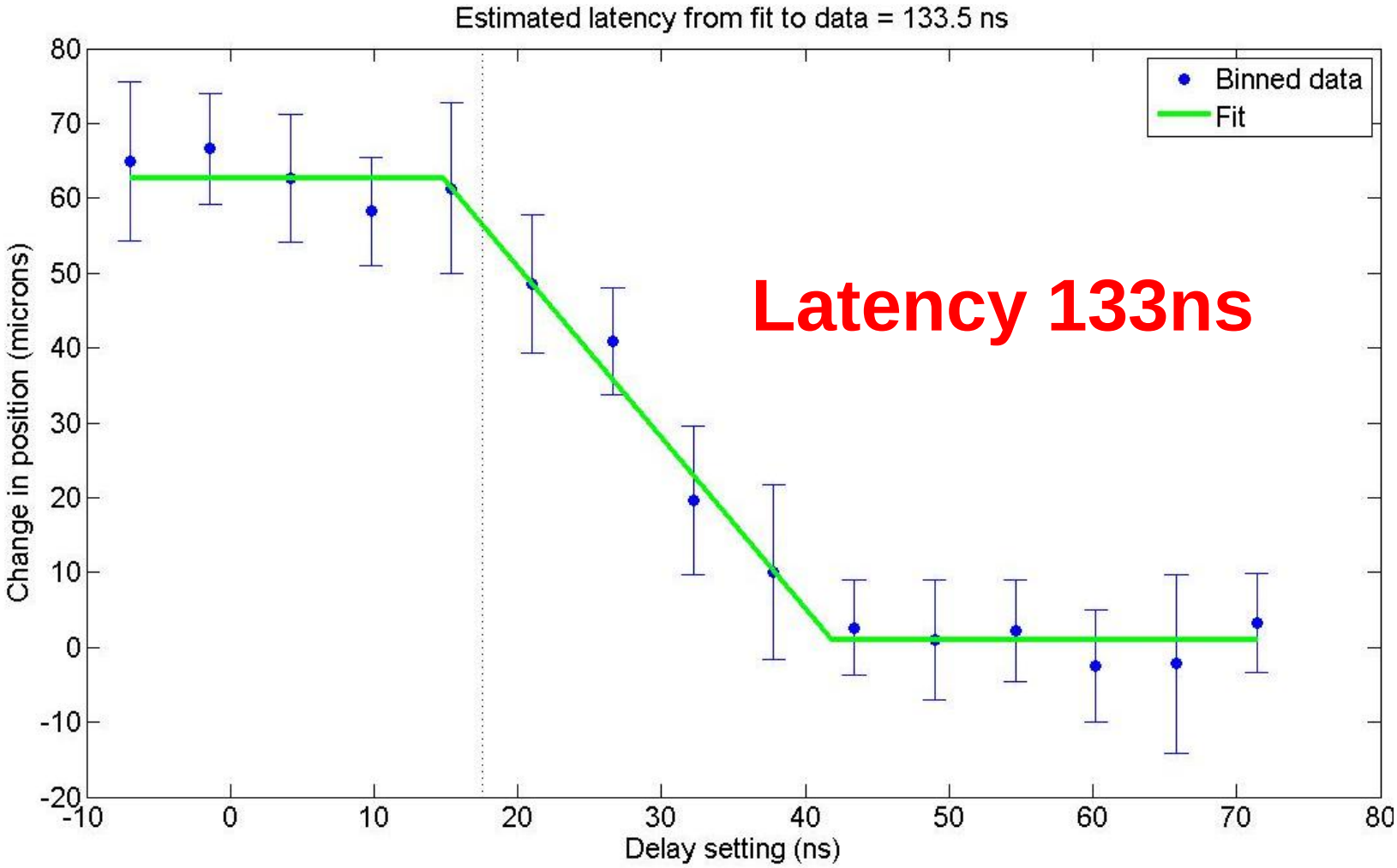
# FONT5 DAQ

**One damping ring cycle (463ns) data returned each pulse:**

- **RS232 over ethernet**
- **All BPM sum (charge) and difference signals**
- **Absolute sample time adjustable in 70ps taps: accurate peak sampling**
- **Ratio of difference to sum peaks gives y-position**
- **Pedestal subtraction w. on-board trim DACs (no latency gain)**



# FONT5 latency: P2 → K1 loop
## (February 2010)



# Latency estimate

- Time of flight kicker – BPM: 12ns
- Signal return time BPM – kicker: 32ns

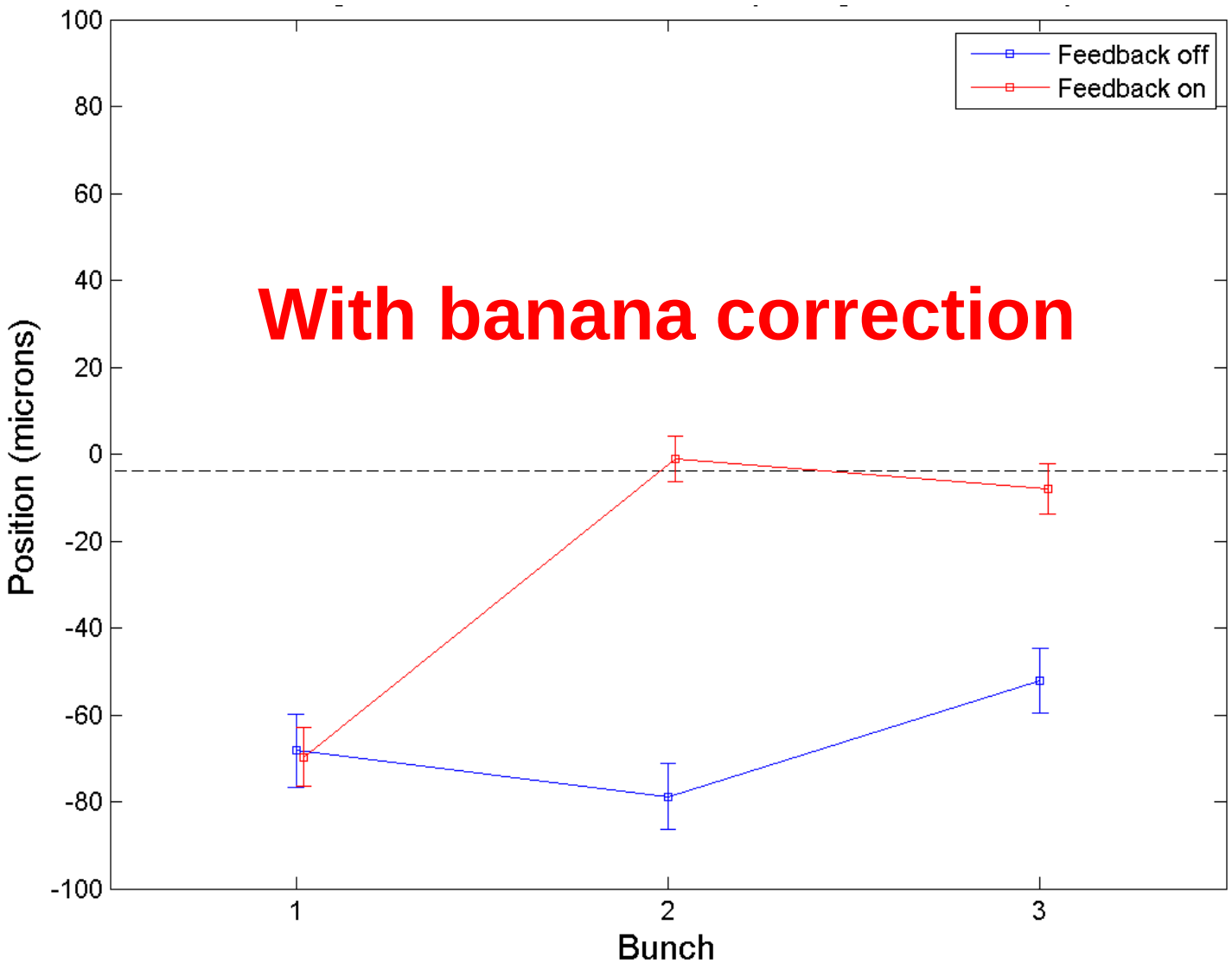
  Irreducible latency: 44ns

- BPM processor: 10ns
- ADC/DAC (4.5 357 MHz cycles) 14ns
- Signal processing (8 357 MHz cycles) 22ns
- FPGA i/o 3ns
- Amplifier 35ns
- Kicker fill time 3ns

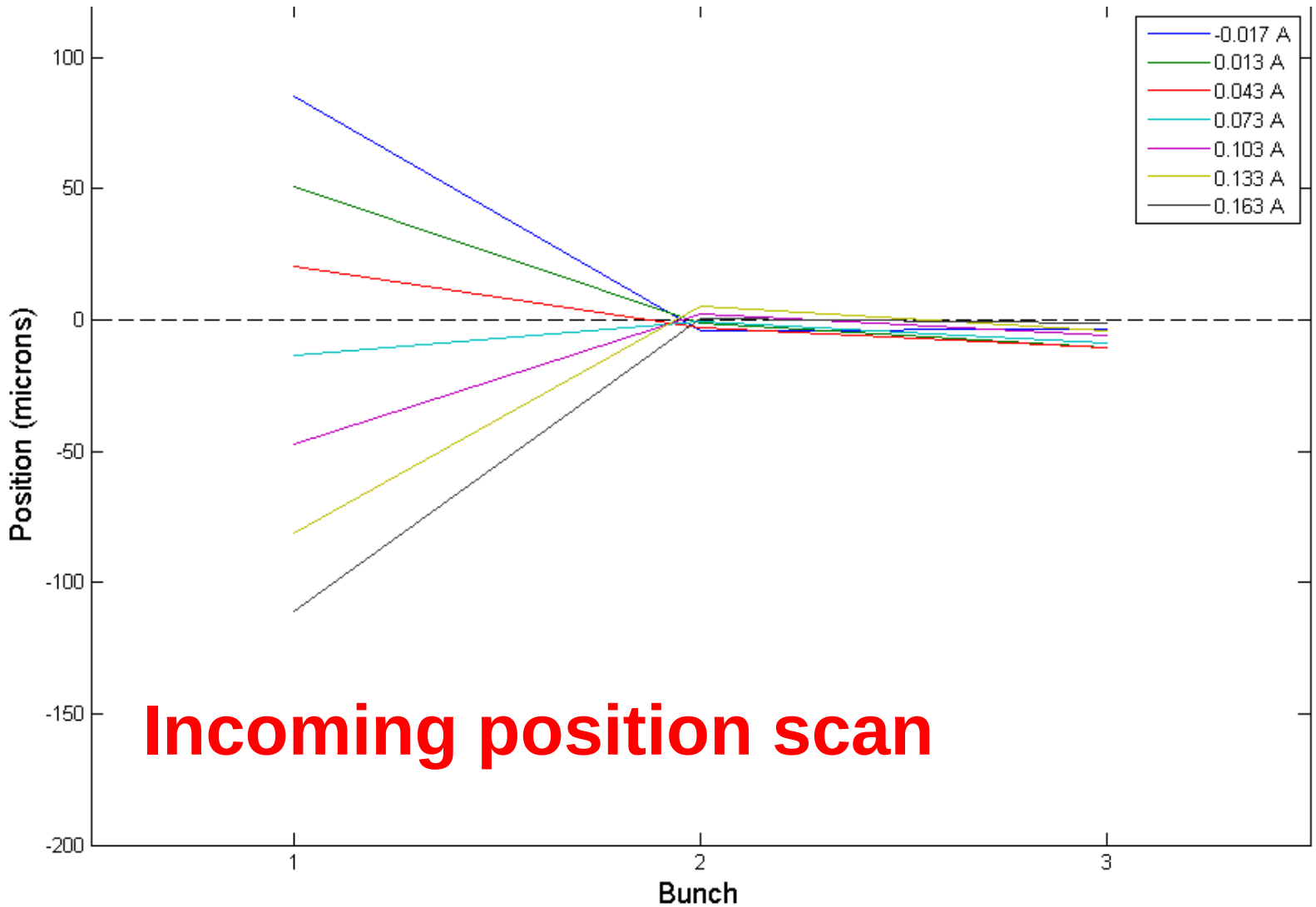
  Electronics latency: 87ns

- Total latency budget: 131ns

# P2 → K1 loop performance
## (February 2010)

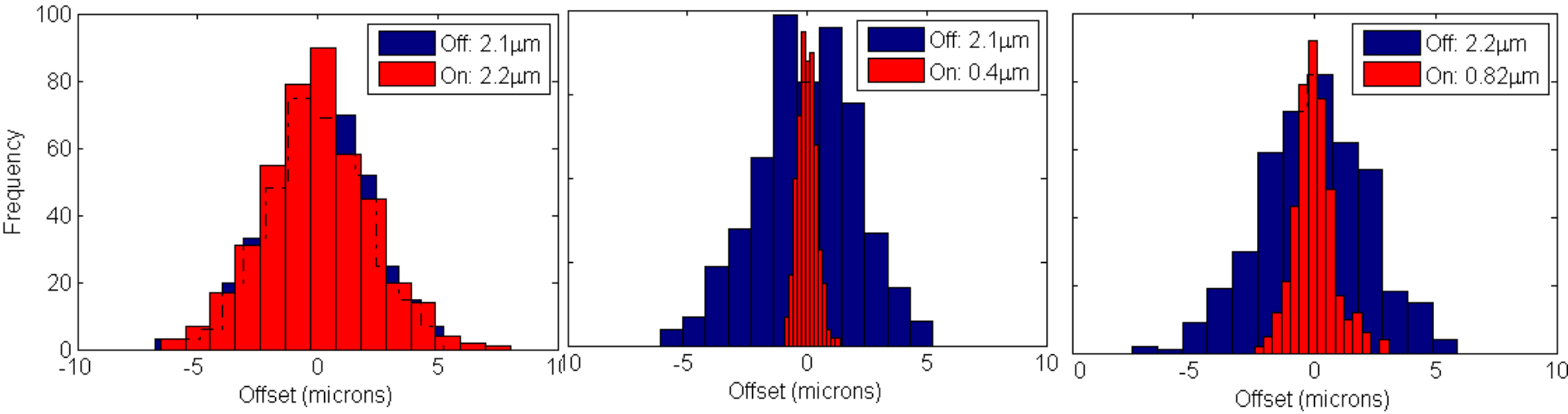


# P2 → K1 loop performance
## (February 2010)



# P2 → K1 loop jitter reduction
## (April 2010)

**Bunch 1** **Bunch 2** **Bunch 3**

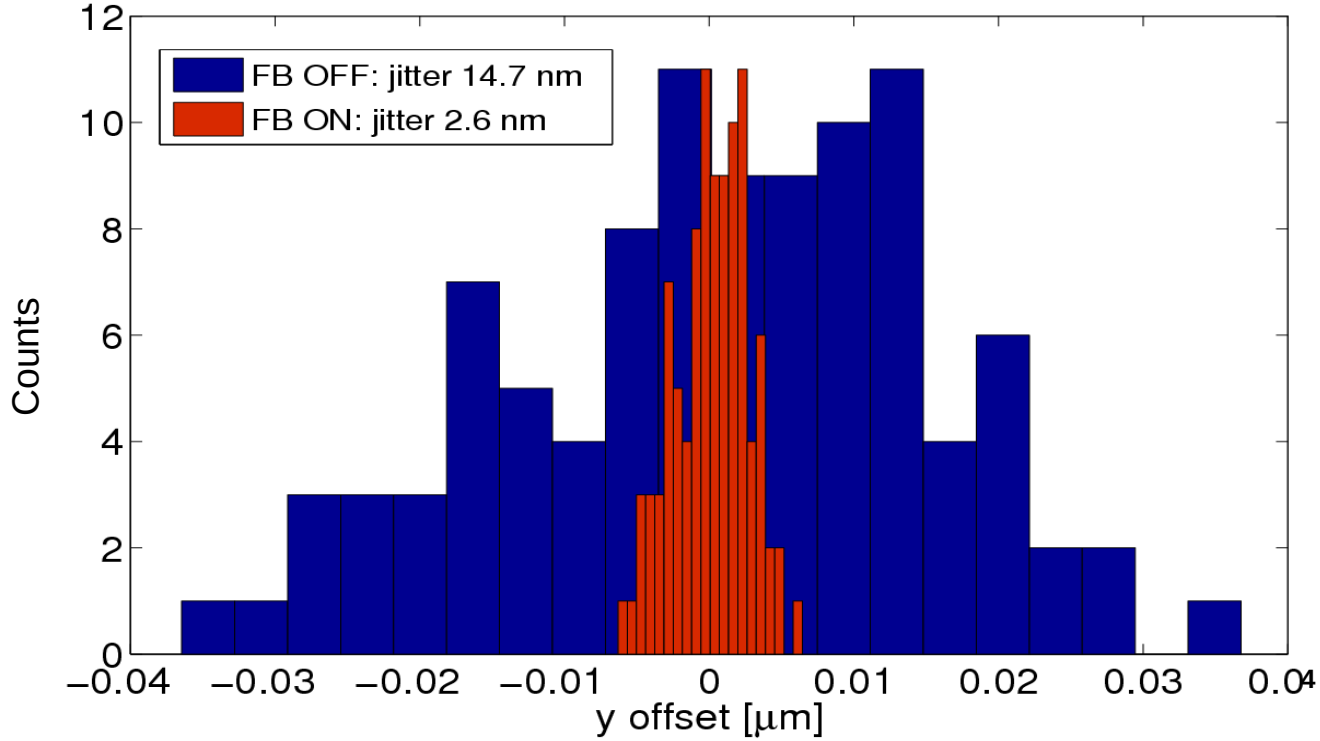



**2.1 um → 0.4 um → 0.8 um**

**Factor of 5 jitter reduction**

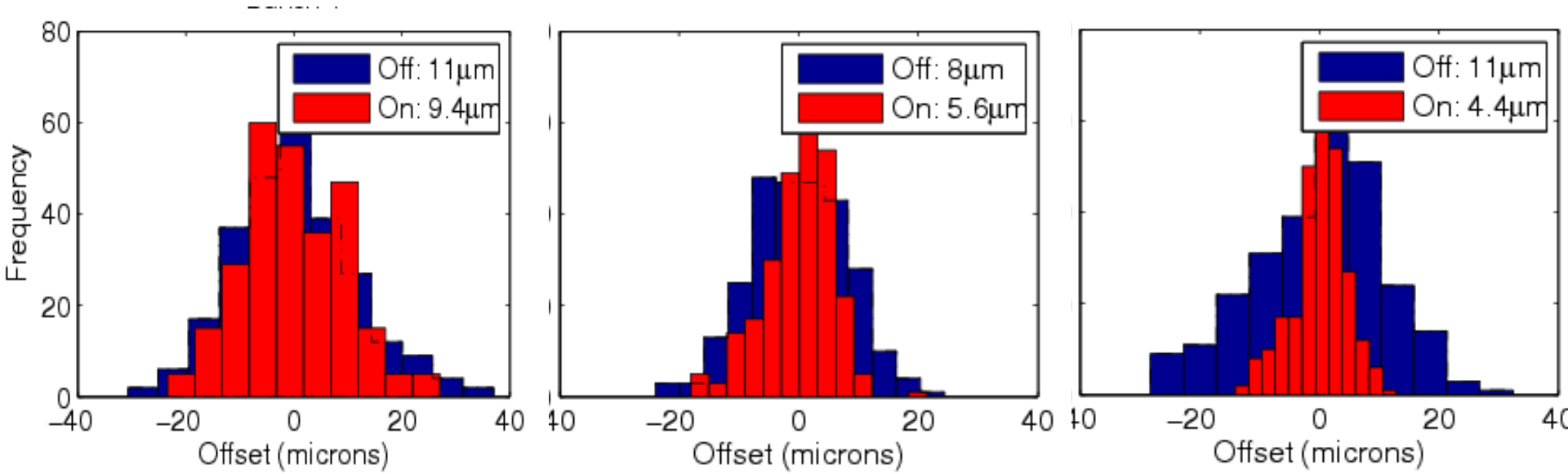
# Jitter comparison at ATF2 IP

**Assuming perfect lattice, no further imperfections (!)**



# Coupled loop jitter reduction
## (May 2010)

**Bunch 1** **Bunch 2** **Bunch 3**




**9.4 um → 5.6 um → 4.4 um**

# Summary

- **IP feedback concept well advanced**
- **Conceptually-engineered designs for ILC + CLIC**
- **All-analogue prototypes (CLIC) developed and tested at NLCTA + ATF:**

  **→ electronics latency c. 13ns**
- **Digital prototypes developed and tested at ATF + ATF2:**

  **→ electronics latency c. 90ns**
- **To do: real engineering + component optimisation**

  **radiation hardness, EM interference …**