AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Progress in development of LumiCal readout electronics and first testbeam results of a prototype detector sector

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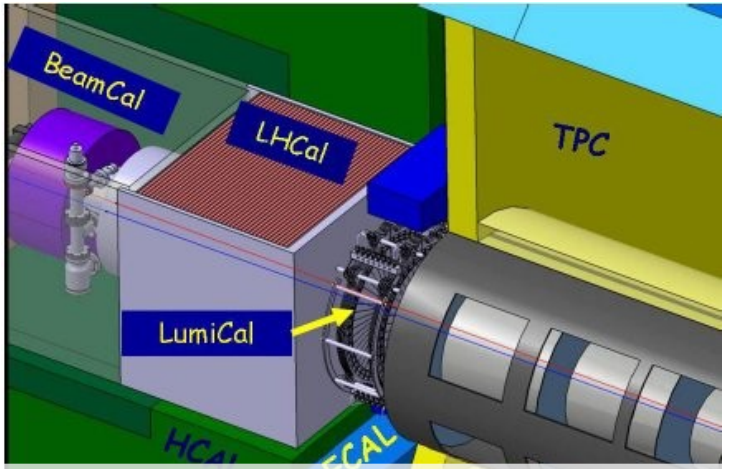
International Workshop on Linear Colliders 2010 (ECFA-CLIC-ILC Joint Meeting)
CERN and CICG (International Conference Centre Geneva, Switzerland)

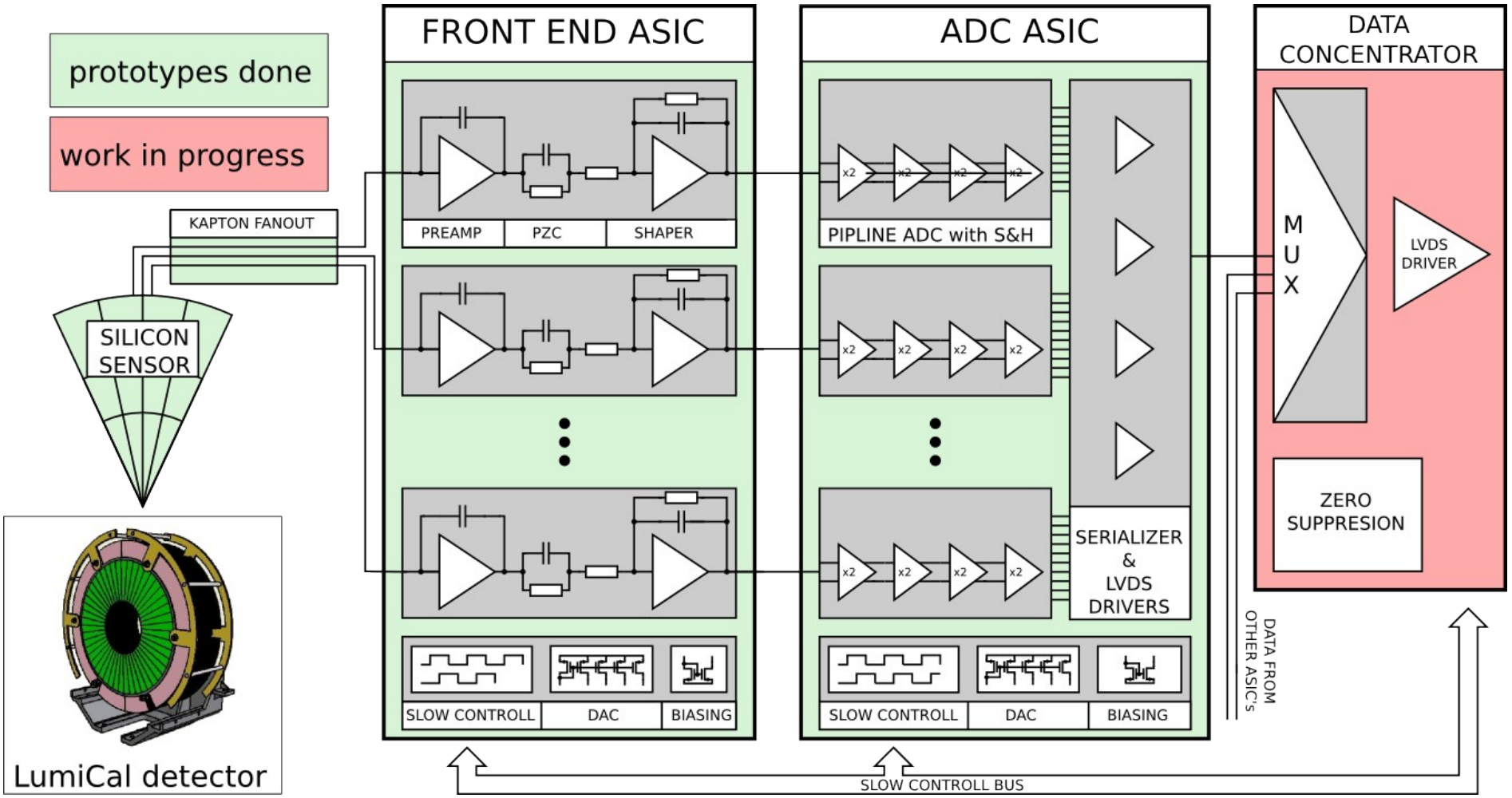
Agenda

- LumiCal readout architecture
- Readout ASICs development within EUDET
- First LumiCal Testbeam
- Multichannel ADC System on Chip development
- Summary and future plans

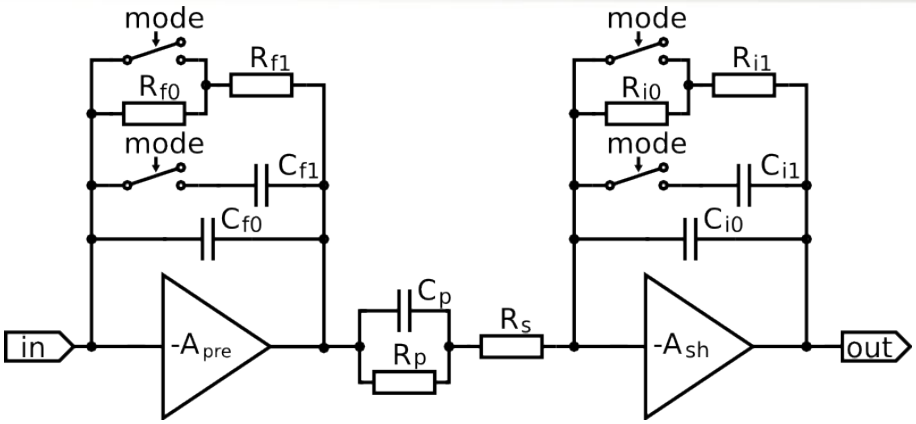


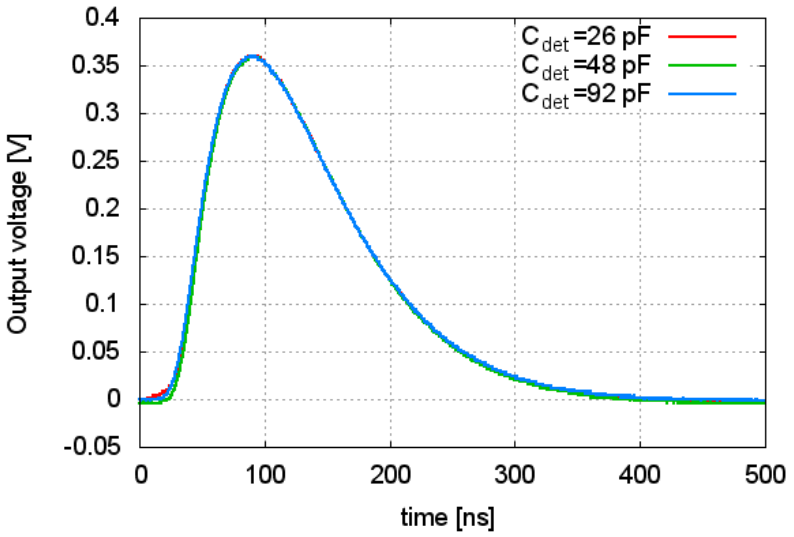
ILD @ ILC
Very Forward Instrumentation

LumiCal readout architecture



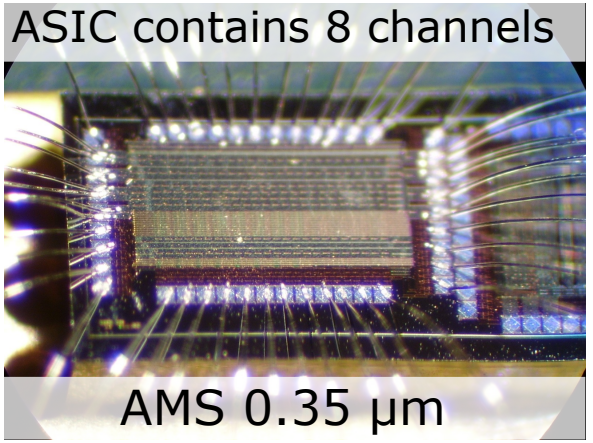
Front-end Electronics





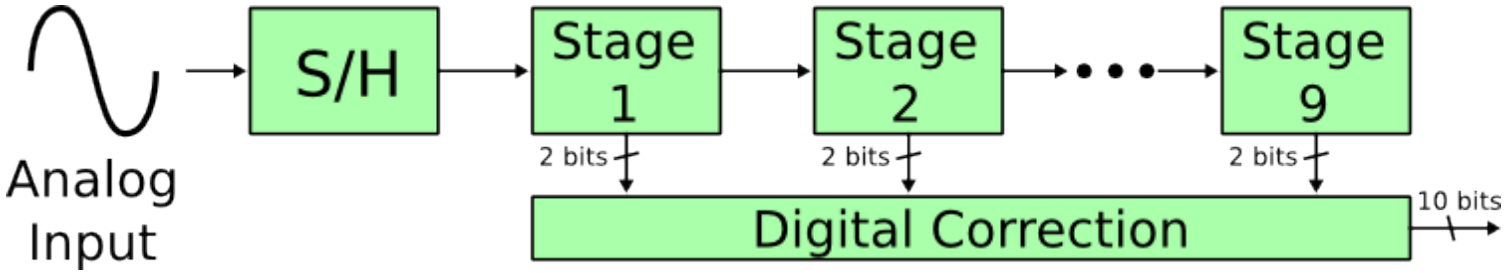
- Cdet ≈ 0 ÷ 100pF
- 1st order shaper (Tpeak ≈ 60 ns)
- variable gain:
  - calibration mode - MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC

- prototypes fabricated and tested → **fully functional**
  - power consumption 8.9 mW/channel
  - event rate up to 3 MHz
  - Crosstalk < 1%



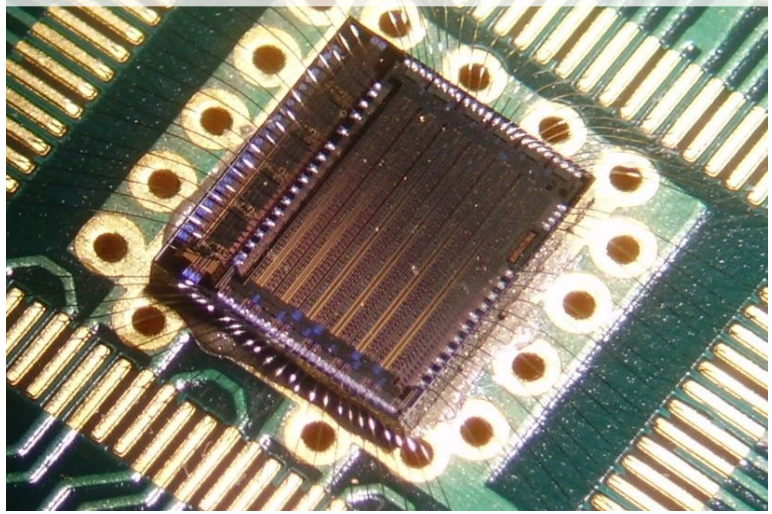
See more : M. Idzik, Sz. Kulis, D. Przyborowski "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174

10-bit pipeline ADC



- 1st prototype
  - 8 pipeline fully differential stages
- 2nd prototype of complete ADC
  - 9 stages + S/H
  - digital correction
  - clock and power switching
  - external reference voltages

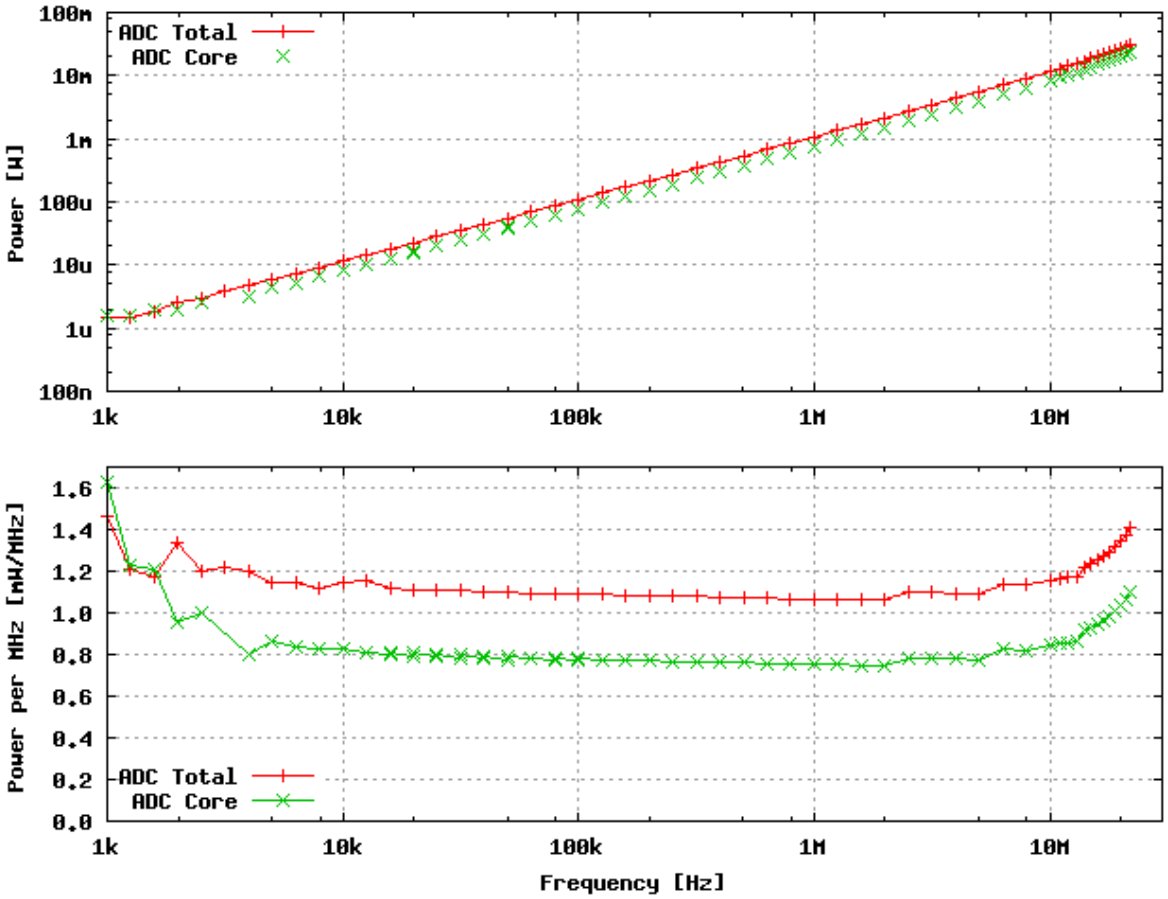
ADC ASIC 2nd prototype



Both prototypes fully functional

See more: M Idzik, K Swientek, Sz. Kulis "Development of pipeline ADC for the Luminosity Detector at ILC" JINST 5 P04006 2010

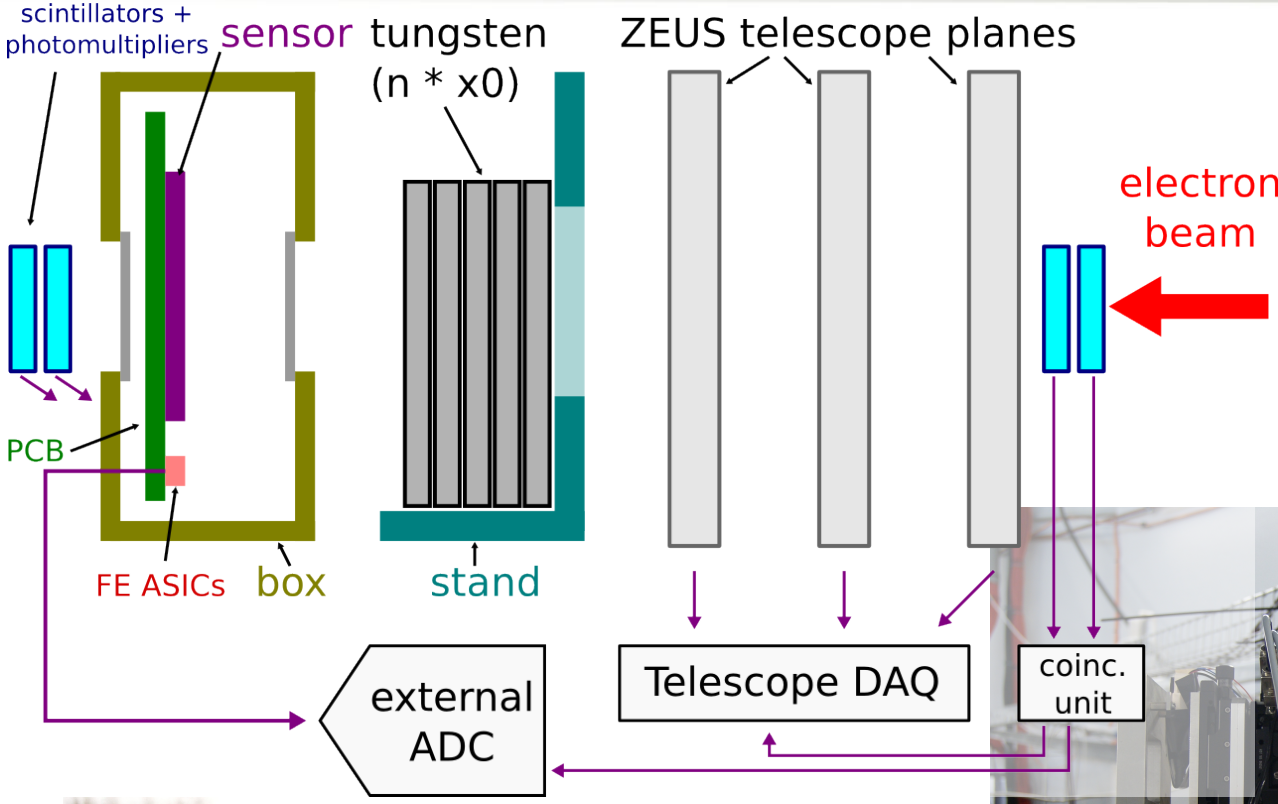
10-bit pipeline ADC | 2nd prototype performance and power scaling



Total power includes also input/output buffers

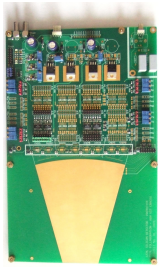
- Typical parameters:
  - INL < 1LSB , DNL < 0.5LSB
  - SINAD = 57.7 dB
  - ENOB = 9.3
- power consumption scales linearly in wide frequency range (4 orders of magnitude !)
  - 0.8 mW/MHz @ 3.0 V (plot)
  - 0.6 mW/MHz @ 2.6 V
  - Useful also for slow control applications (voltage/ temperature monitoring)
- Power on/off switching implemented and verified (~10 clocks needed to restart correct conversion)

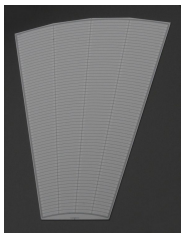
First Testbeam | Experimental setup

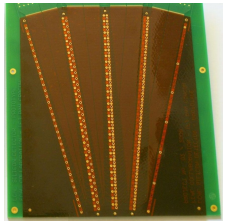


Setup contains:

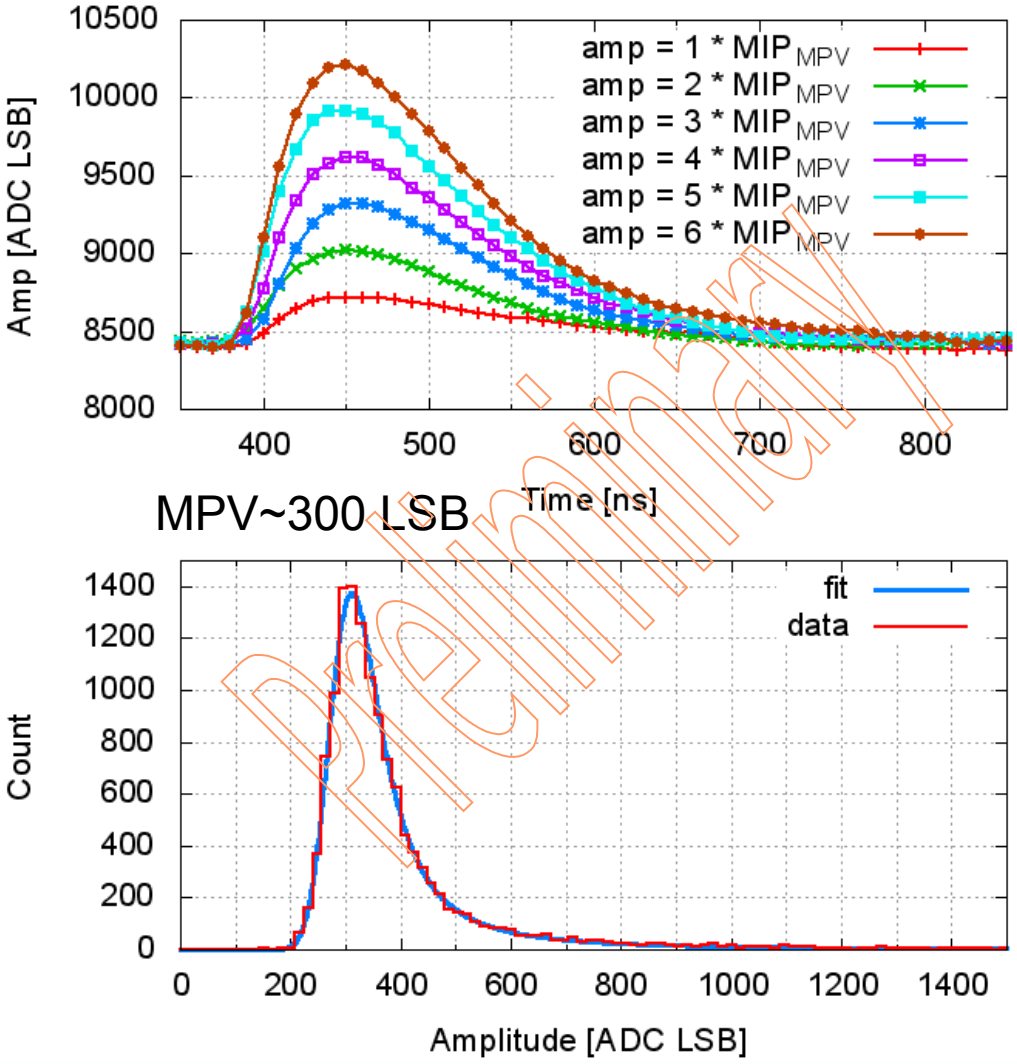
- Sensor+fanout
- Front-end ASICs
- ADC - CAEN v1724
- ZEUS Telescope
- X-Y table





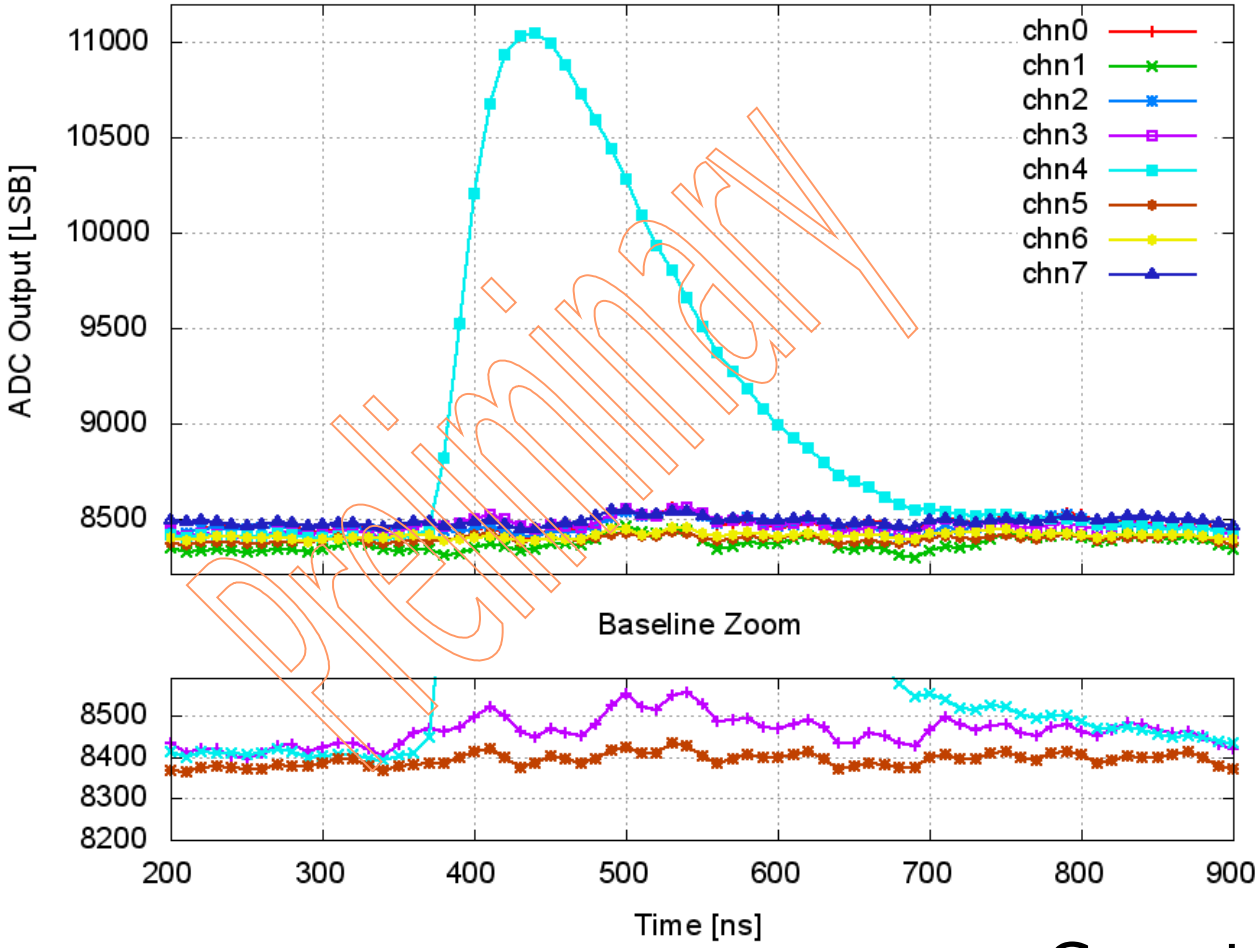


First Testbeam
Front-end pulses & energy spectrum



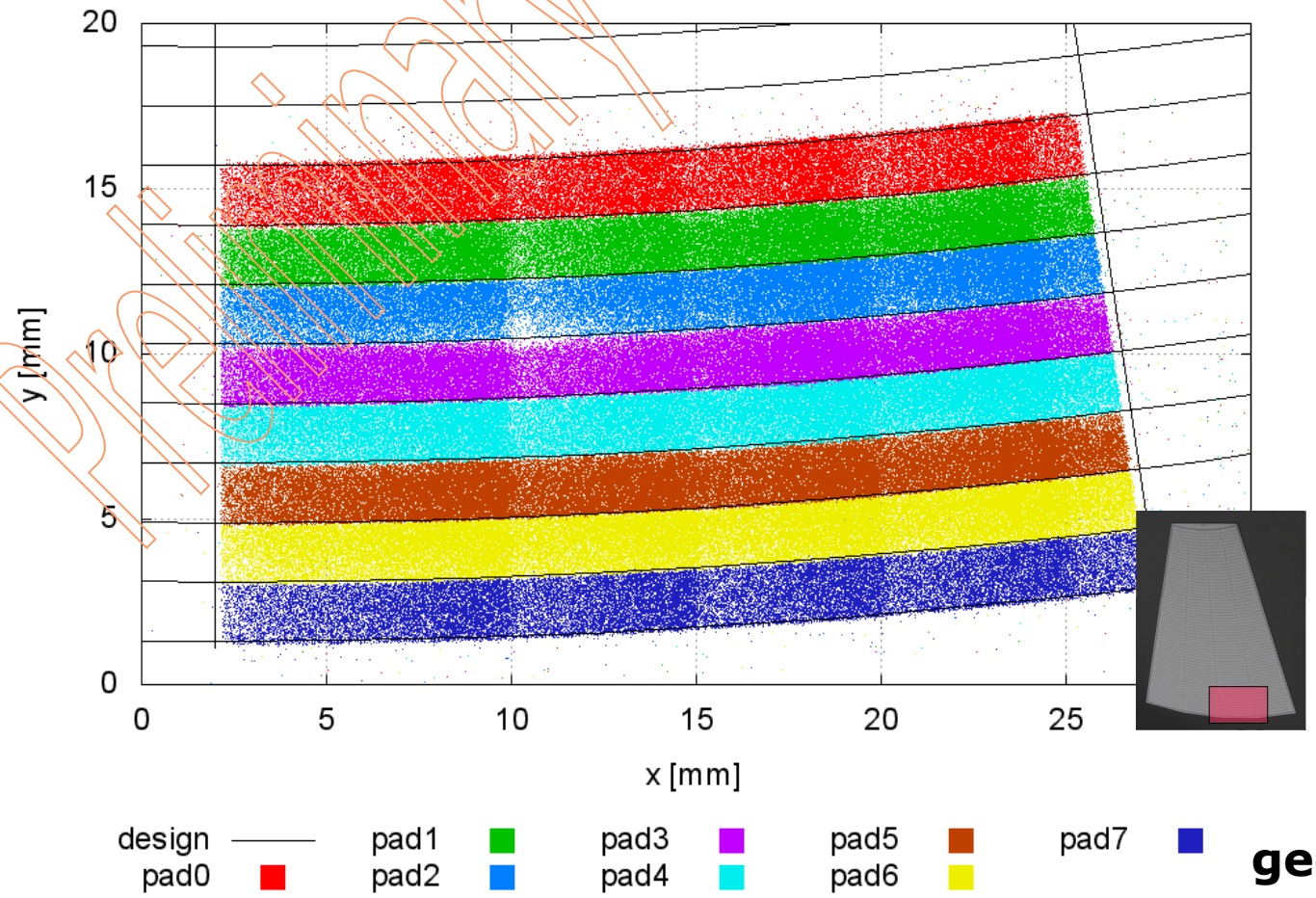
- Time response for electrons with different energies (top)
  - Shape doesn't depend on amplitude
- Energy spectrum for 4.5 GeV electrons
  - Fits very well to Landau distribution
  - SNR ~ 19
    (for largest sensor capacitance)

First Testbeam | Crosstalk



Crosstalk < 1%

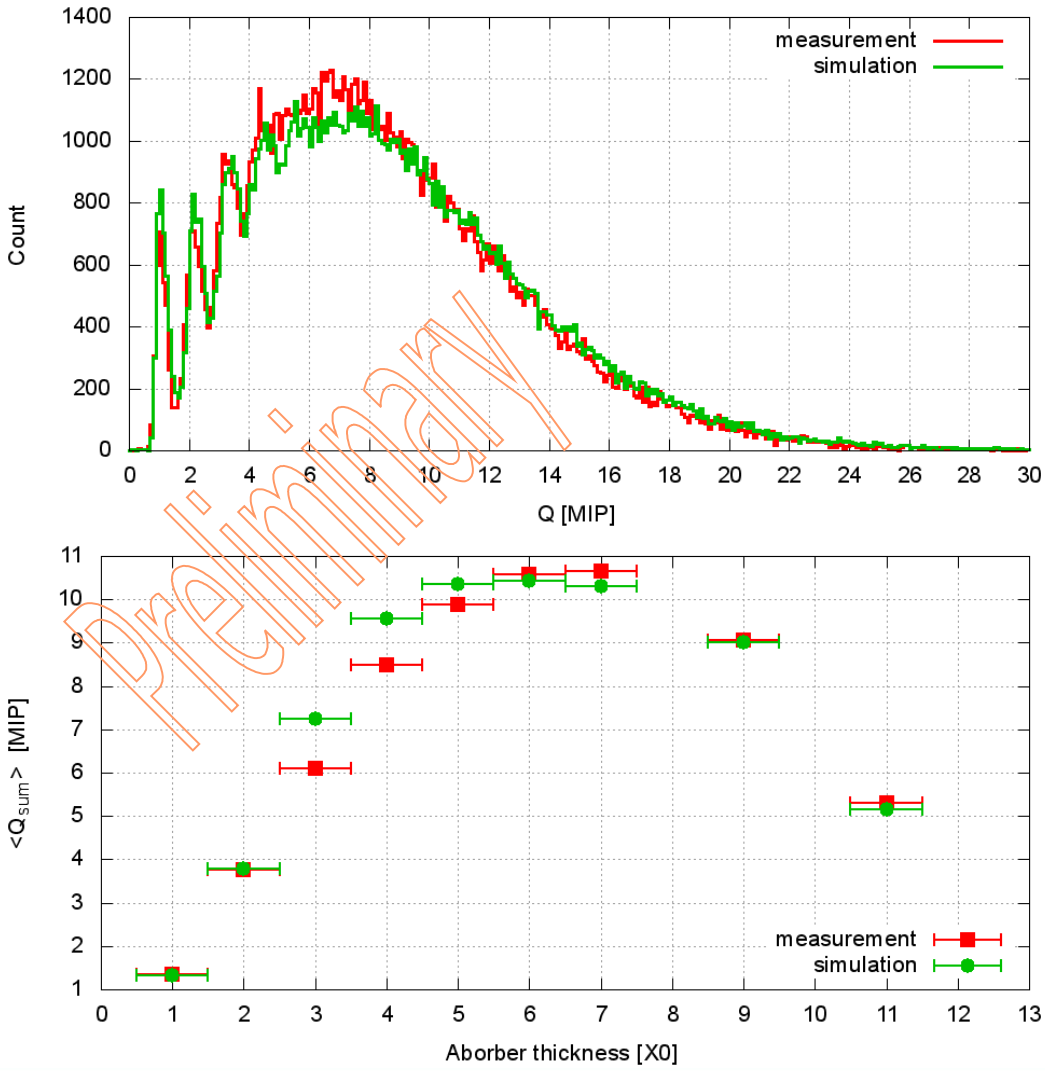
First Testbeam
Position reconstruction



- Combined events from LumiCal sensor and Zeus telescope
- Each dot – single event
- 2 million events

LumiCal sensor geometrical structure is reflected on reconstructed tracks

First Testbeam
Shower development



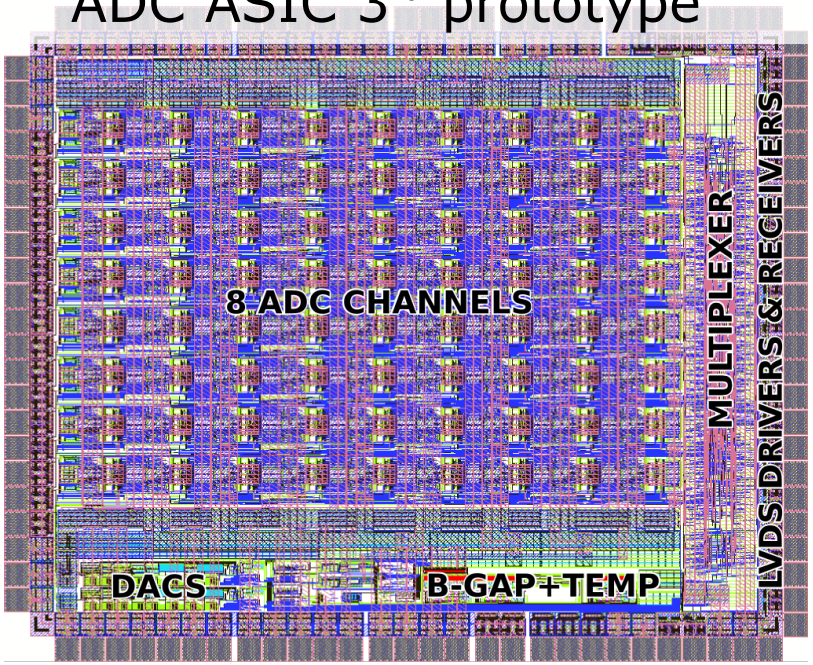
- Histogram of charge deposited in instrumented area for 2 x0 absorber thickness (top)
- Average charge deposited in instrumented area as a function of tungsten thickness (bottom)

Good agreement between measurements and MC simulations

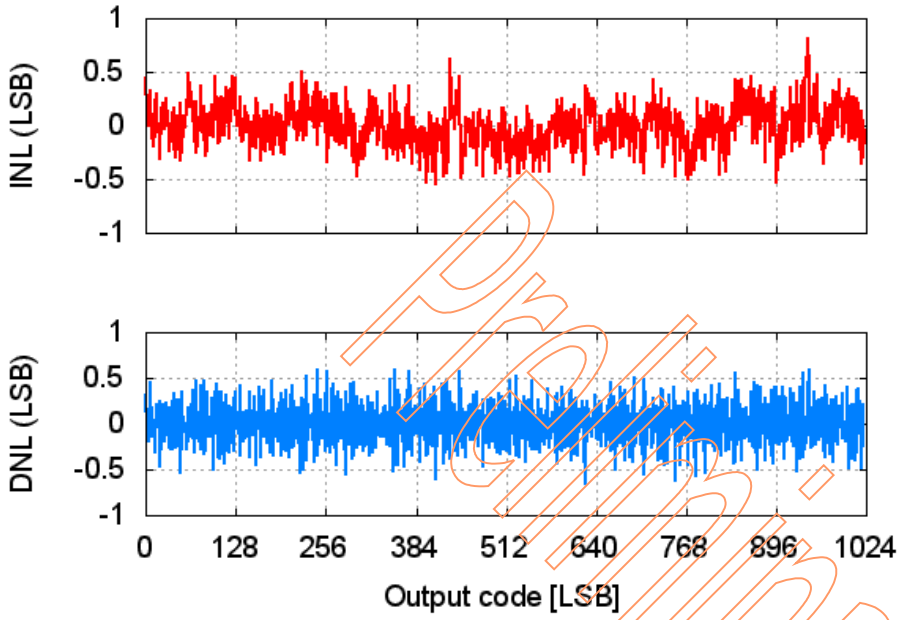
Multichannel ADC SoC | 3rd prototype

- 8 channels of pipeline ADC
- Digital multiplexer/serializer:
  - Serial mode (ILC baseline): one data link per all channels (max f_{smp} ~ 4 MSps)
  - Parallel mode: one data link per channel (max f_{smp} ~ 30MSps)
  - Test mode (single channel readout)
- High speed LVDS drivers (~1GHz)
- Low power DAC control references
- Precise BandGap reference source
- Temperature sensor

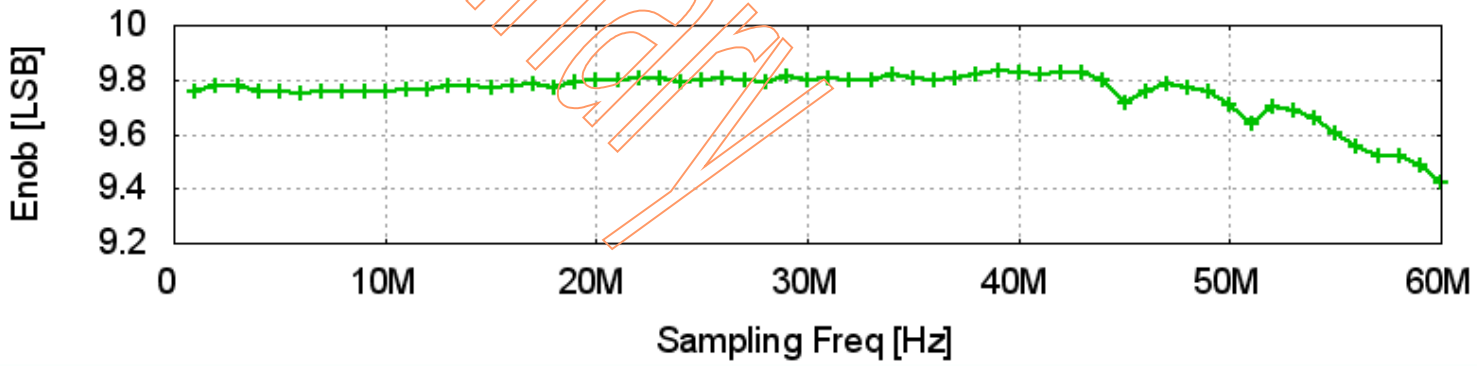
ADC ASIC 3rd prototype



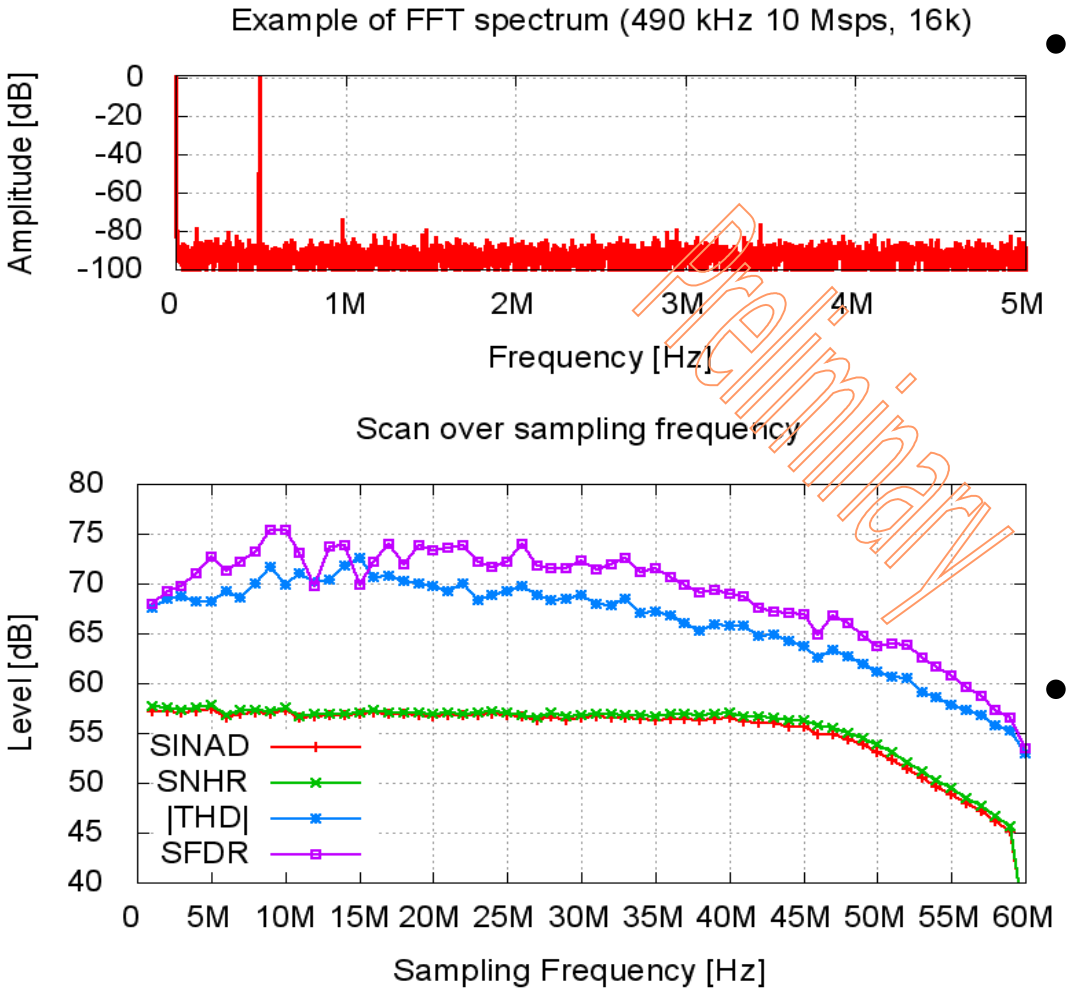
Multichannel ADC SoC | 3rd prototype static measurements



- Typical static measurement (left)
  - f_{smp} 50Msps
  - ENOB ~ 9.7
  - INL < 0.8 LSB
  - DNL < 0.6 LSB
- ENOB as a function of frequency (bottom)
  - Work up to ~ 50 Mhz

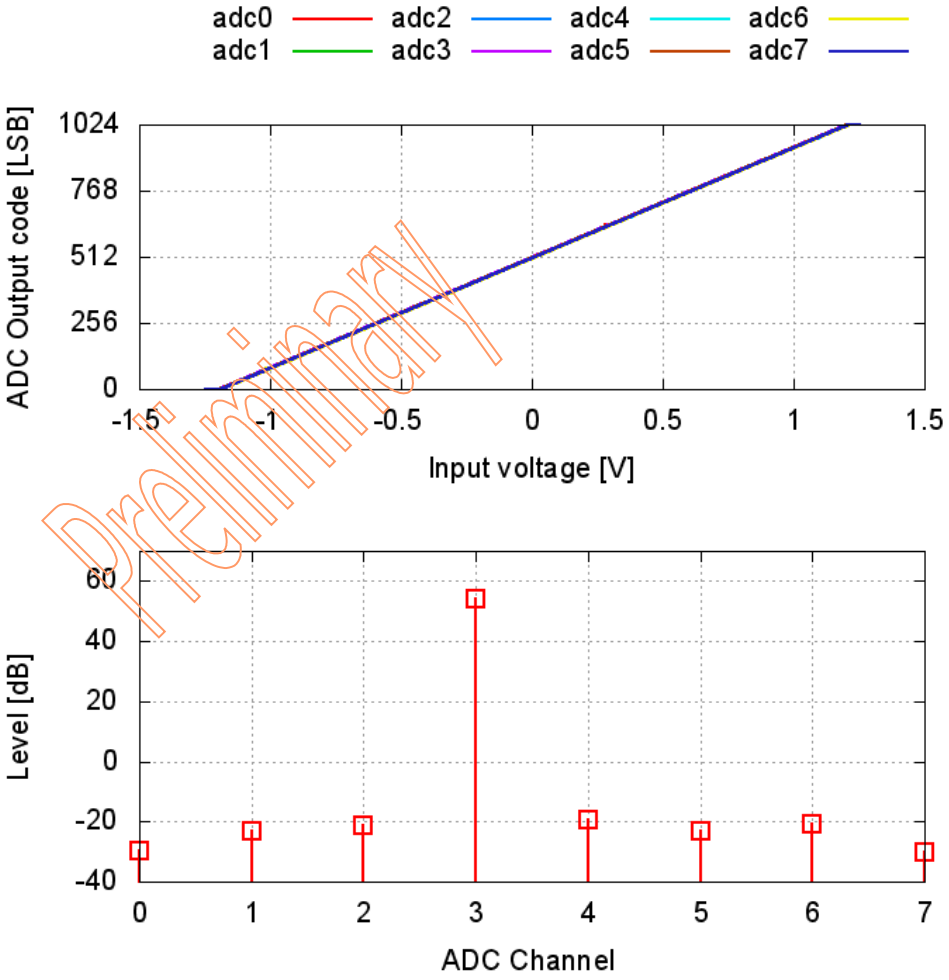


Multichannel ADC SoC | 3rd prototype dynamic measurements



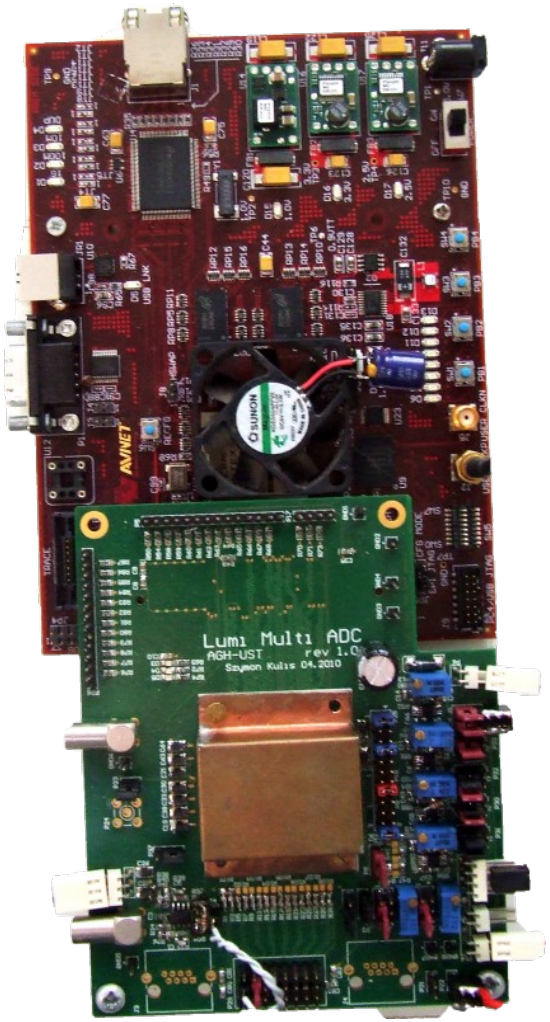
- Typical dynamic (FFT based) measurement (top)
  - Fsmp 10 Msps
  - Finput ~500 kHz
  - SINAD 58.0 dB
  - THD -70.0 dB
  - SNHR 58.2 dB
  - SFDR 74.1 dB
- Dynamic parameters as a function of frequency (bottom)
  - Work up to ~ 50 Mhz

Multichannel ADC SoC | 3rd prototype multichannel characteristics



- Transfer function measurement (top)
  - Gain spread <0.1%
  - Offset spread ~ 1%
- Crosstalk measurement (bottom)
  - Full scale sinus applied on channel 3
  - Channels separation > 75dB (no crosstalk)

FPGA based DAQ for multichannel ADC SoC



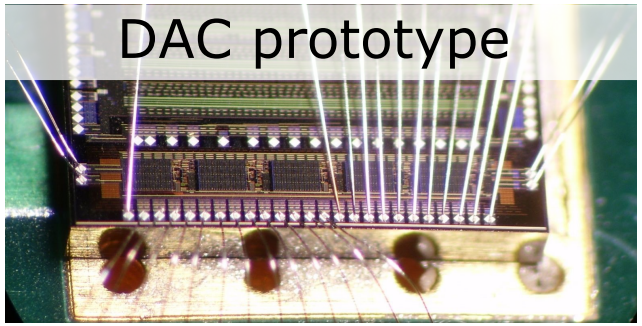
- ADC readout DAQ utilizes:
  - Xilinx Virtex5FXT FPGA with embeded PowerPC 440
  - 64MB DDR2 SDRAM
  - GigaBit Ethernet
  - XilKernel & lwIP based software
- Capturing data from ADC up to 400 MHz in LVDS standard

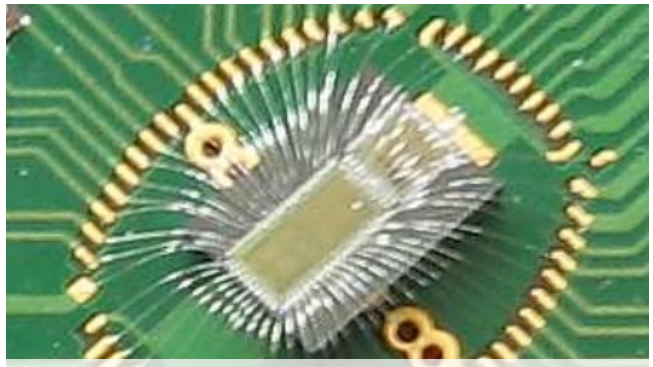
Present **FPGA based DAQ** is a first step for **data concentrator**

Readout system peripherals

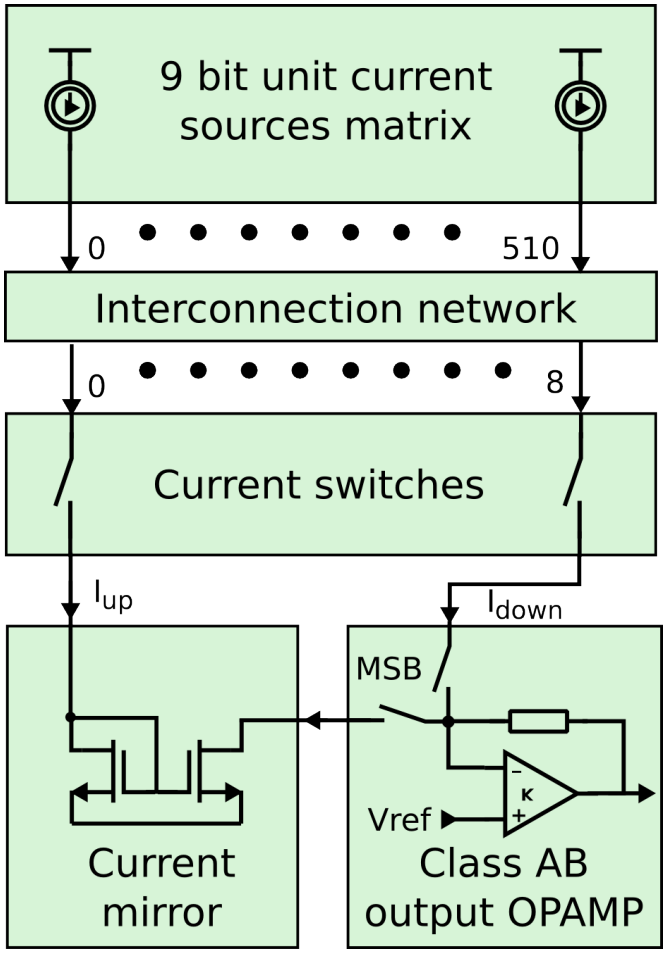
- bandgap based precise reference voltage source
  Vout =1.214 V +/- 1mV
- bandgap based temperature sensor
  ~ 5mV / deg
- fast LVDS driver and receiver
  (~ 1 Gb/s)
- low power small area voltage and current DACs
- first prototype of 1 GHz PLL based wire transceiver

All prototypes manufactured in AMS 0.35 technology and fully functional

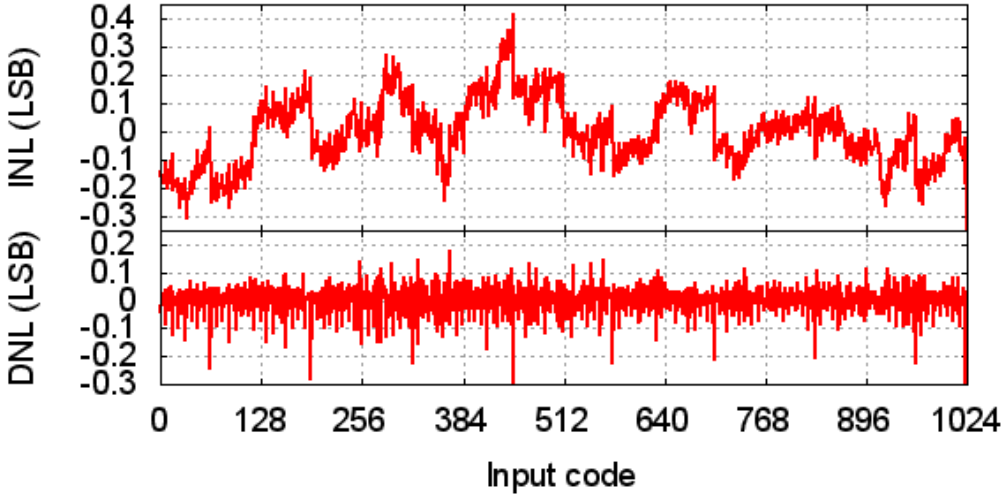

DAC prototype


Prototype of wire transceiver

Readout system peripherals
10-bit low power high swing DAC



- 10th bit achieved by current reversing
- nonlinearities DNL & INL < 0.42 LSB
- ENOB ~ 9.8
- settling time 0.5 – 2 μs
- Low power consumption < 0.6 mW
- Small area ~ 0.22 mm^2

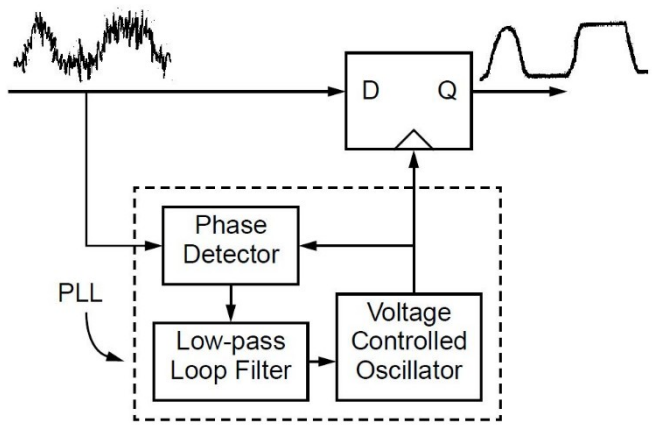


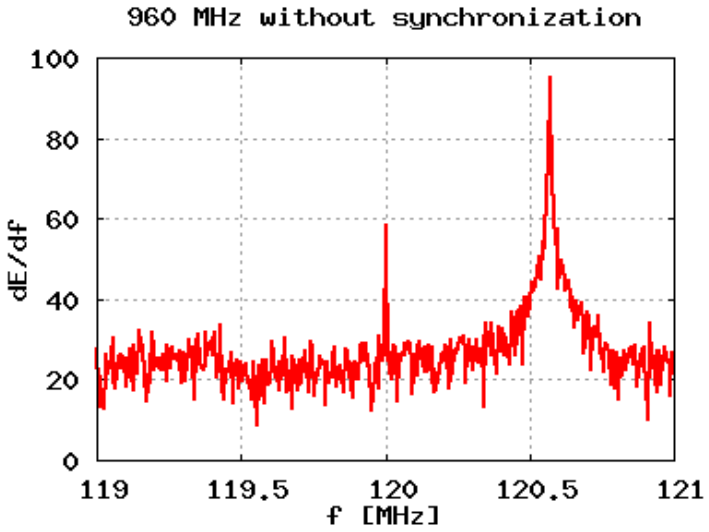
See more: D. Przyborowski, M. Idzik "A 10-bit Low-Power Small-Area High-Swing CMOS DAC" IEEE Transactions on Nuclear Science, Vol. 57, No 1, pp 292-299

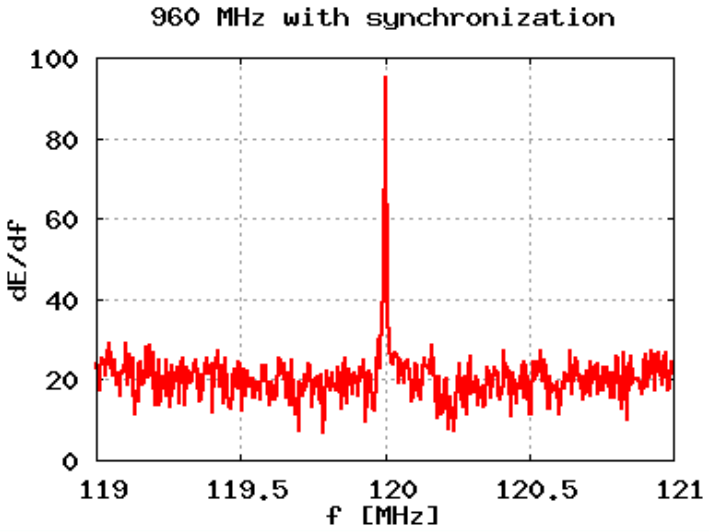
Readout system peripherals
1 GHz PLL based wire transceiver

First prototype of serial transceiver (PLL based), using Clock & Data Recovery

- both transmitter (with 8 bit serializer) and receiver (with 8 bit deserializer) fully functional
- wide frequency range 120MHz - 1GHz





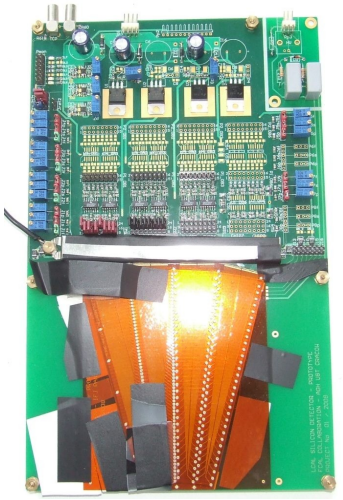


VCO frequency spectrum in CDR circuit divided by 8

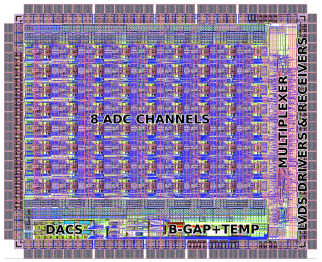
(960 MHz mode)

Summary & future plans

- Two readout ASICs: front-end and ADC designed and fabricated within EUDET 6FP. Prototypes fully functional and ready for system integration
- Functionality of the chain: front-end + fanout + sensors, positively verified on test beam
- Prototype of Multichannel ADC System on Chip (containing: multiplexer, DACs, LVDS, bandgap reference, temperature sensor) fully functional and under tests, development will be continued within AIDA 7FP
- Prototype of PLL based fast (~1GHz) serial transceiver functional, work in progress...



Short term plans (~6months) for the next test-beam: Integration of multichannel front-end with multichannel ADC SoC and applying power pulsing



Longer term plans (few years, AIDA 7FP): move some readout blocks to smaller size technology (promising candidate IBM 0.13 μm), works already started...