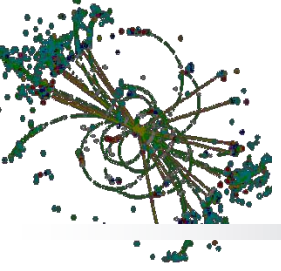


Status of the Chronopixel Project

N. B. Sinev
University of Oregon, Eugene

*In collaboration with J.E.Brau, D.M.Strom (University of Oregon,
Eugene, OR), C.Baltay, H.Neal, D.Rabinovitz (Yale University,
New Haven, CT)*

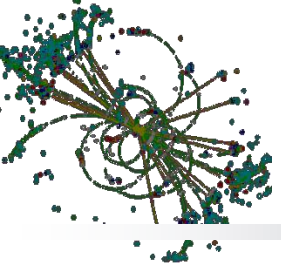
EE work is contracted to Sarnoff Corporation



Outline of the talk



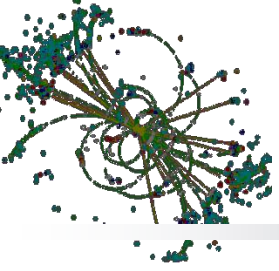
- **Just reminder: what is chronopixel?**
- **Project timeline**
- **Prototype 1 design and problems**
- **What is new in prototype 2**
- **Simulations of expected performance.**
- **Results of the second prototype tests.**
- **Conclusions and plans**



What is chronopixel?



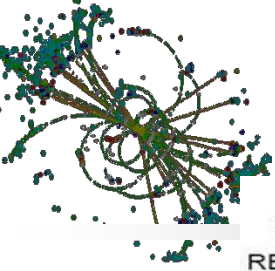
- **Need for pixel detector with good time resolution:**
 - ↪ **Background hits density in ILC environment is of the order of 0.03 hits/mm² per bunch.**
 - ↪ **Bunch train at ILC, which lasts only 1 ns, has about 3000 bunches ⇒ 100 hits/mm² – too high for comfortable track reconstruction.**
 - ↪ **So we need to slice this array of hits into at least 100 time slices, and reconstruct tracks from hits belonging to the same slice. To do this, we need to know time of each hit with at least 10 μs accuracy.**
- **CCDs, often used as pixel detectors, by the nature of their readout, are very slow. Row by row readout takes tens if not hundreds of ms to read image. So we would integrate the entire bunch train in one readout frame.**
- **There is a number of pixel sensor R&D addressing this problem – CPCCD, different types of monolithic designs (readout electronics on the same chip as sensor), 3D technology. Neither of them (except, may be 3D) allows assigning time stamp to each hit.**
- **Chronopixel project was conceived to provide such ability.**
- **Chronopixel is a monolithic CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.**



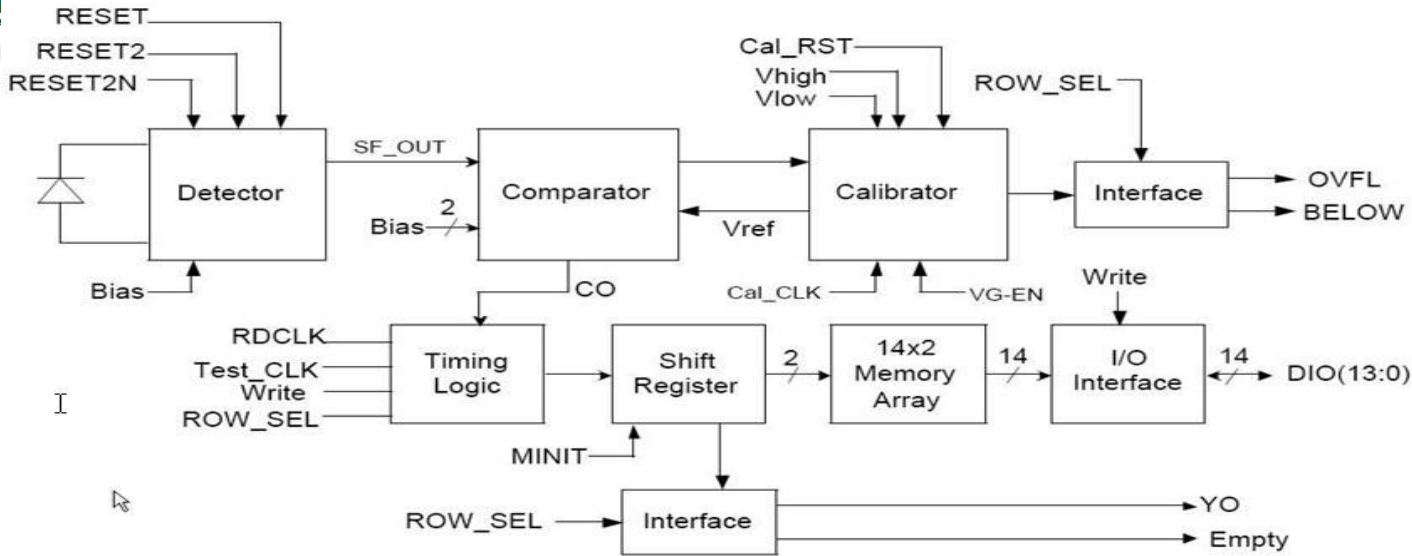
Timeline



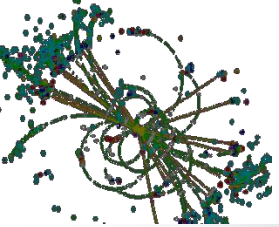
- **2004 – talks with Sarnoff Corporation started.**
 - ↻ Oregon University, Yale University and Sarnoff Corporation **collaboration formed.**
- **January, 2007**
 - ↻ Completed design – Chronopixel
 - ❖ **2 buffers, with calibration**
- **May 2008**
 - ↻ **Fabricated 80 5x5 mm** chips, containing 80x80 **50 μm** Chronopixels array (+ 2 single pixels) each
 - ↻ **TSMC 0.18 μm** ⇒ **~50 μm** pixel
 - ❖ Epi-layer only 7 μm
 - ❖ Low resistivity (~10 ohm*cm) silicon
- **October 2008**
 - ↻ Design of **test boards** started at SLAC
- **August 2009**
 - ↻ **Debugging and calibration** of test boards
- **September 2009**
 - ↻ Chronopixel chip **tests started**
- **March 2010**
 - ↻ **Tests completed**, report written
- **May 2010**
 - ↻ Second prototype **design started**
- **September 2010**
 - ↻ **contract** with Sarnoff for developing of second prototype **signed.**
- **October 2010**
 - ↻ Sarnoff works **stalled**
- **September 2011**
 - ↻ Sarnoff **resumed** work.
- **February 2012**
 - ↻ **Submitted** to MOSIS for production at **TSMC.**
 - ↻ **Modification** of the **test stand** started as all signal specifications were defined.
- **June 6, 2012**
 - ↻ **11 packaged chips** delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
 - ↻ Tests at SLAC started



First prototype design



- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with **Sarnoff** company.
- When **signal** generated by particle crossing sensitive layer **exceeds threshold**, snapshot of the **time stamp**, provided by 14 bits bus is **recorded** into pixel memory, and **memory pointer is advanced**.
- If **another particle** hits the same pixel during the same bunch train, **second memory cell** is used for this event time stamp.
- During readout, which happens between bunch trains, **pixels which do not** have any time stamp **records**, generate **EMPTY** signal, which **advances IO-MUX** circuit to next pixel without wasting any time. This **speeds up readout** by factor of about **100**.
- **Comparator offsets** of individual pixels are determined in the **calibration cycle**, stored in digital form, and reference voltage, which sets the comparator threshold, is shifted to **adjust thresholds** in all pixels to the **same signal level**.
- To achieve required noise level (about **25 e r.m.s.**) **special reset** circuit (**soft reset** with feedback) was developed by **Sarnoff designers**. They claim it reduces reset noise by **factor of 2**.



Sensor design

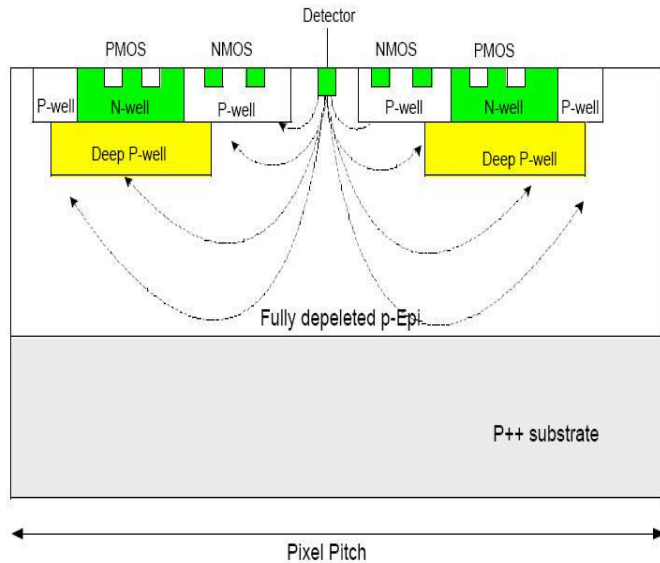


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

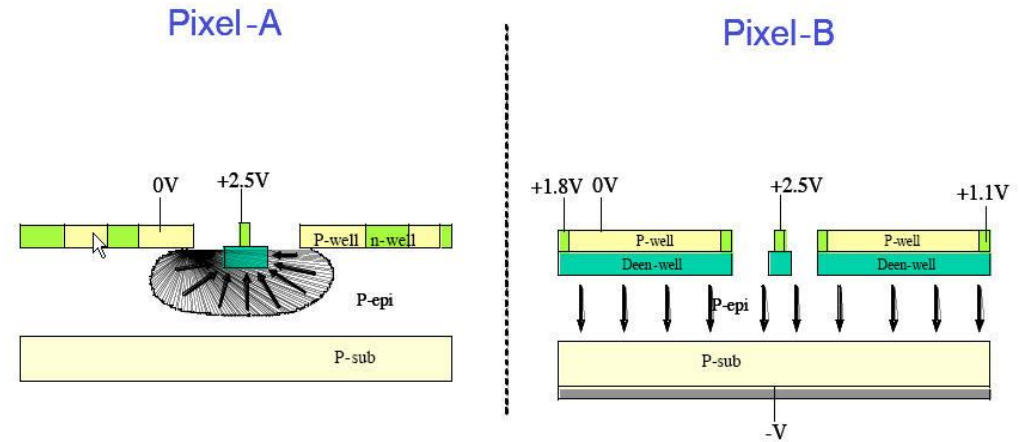
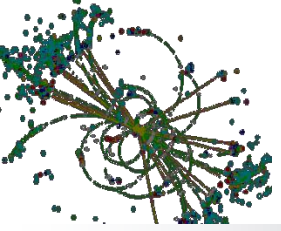


Figure 6.3 Comparison of the vertical cross section views of two pixels

Ultimate design, as was envisioned Two sensor options in the fabricated chips

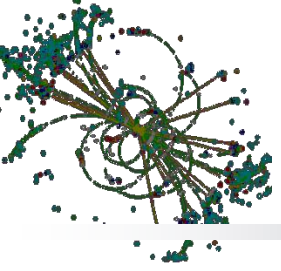
- TSMC process **does not** allow for creation of **deep P-wells**. Moreover, the test chronopixel devices were **fabricated** using **low resistivity** ($\sim 10 \text{ ohm} \cdot \text{cm}$) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs **deep n-well**, **encapsulating** all **p-wells** in the NMOS gates. This allow **application of negative** (up to **-10 V**) bias on **substrate**.



Conclusions from prototype 1 tests



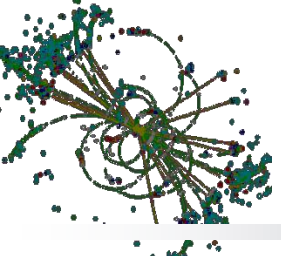
- Tests of the first chronopixel prototypes are now completed.
- Tests show that general **concept is working**.
- **Mistake was made in the power distribution** net on the chip, which led to only **small portion of it is operational**.
- Calibration circuit **works as expected in test pixels**, but for unknown reason **does not work in pixels array**.
- Noise figure with “soft reset” is within specifications ($0.86 \text{ mV}/35.7 \mu\text{V}/e = 24 \text{ e}$, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is **2.7 times larger** required (250 e). Reduction of sensor capacitance (increasing sensitivity) may help in bringing it within specs.
- Sensors leakage currents ($1.8 \cdot 10^{-8} \text{ A}/\text{cm}^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz .
- No problems with **pulsing analog power**.



Prototype 2 features



- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge collection without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.
- **New** comparator offset compensation (“**calibration**”) scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.
- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.
- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25 μ x 25 μ**
- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.



Prototype 2 design

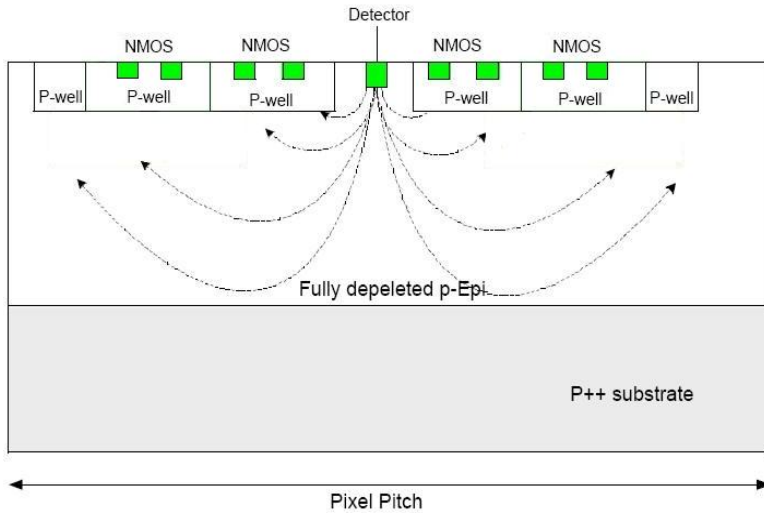
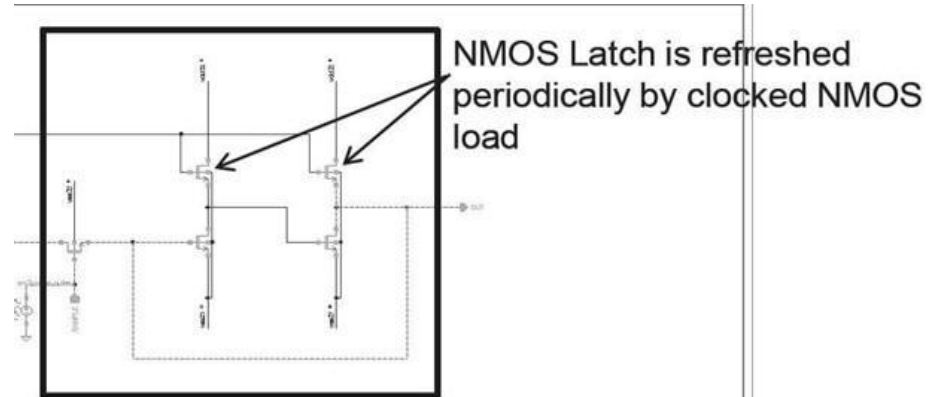
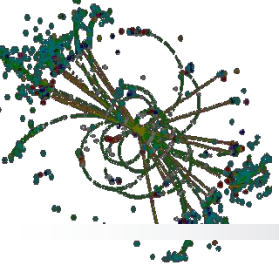


Figure 11.1 Proposed pixel architecture

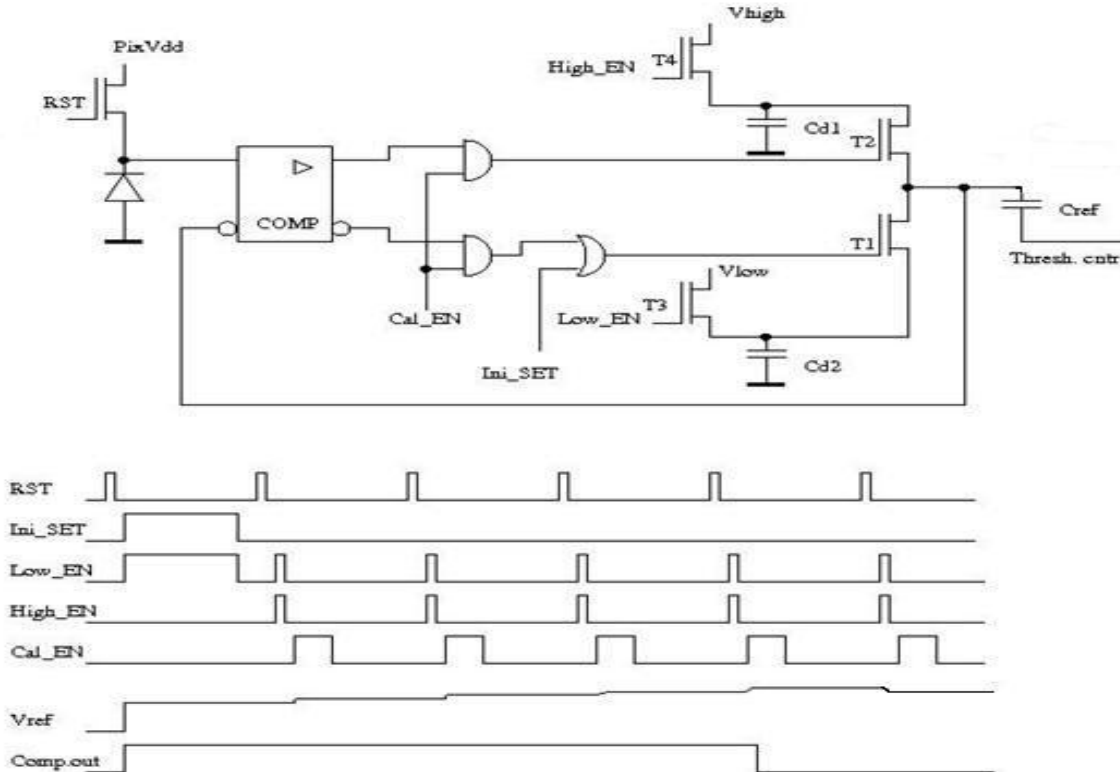


Clocked Dynamic NMOS Latch is a very efficient memory element. NMOS inverters and NOR gates can also be clocked to save on static power consumption.

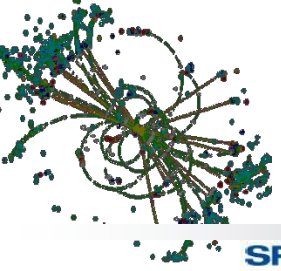
Proposed dynamic latch (**memory cell**) has technical **problem** in achieving very **low power** consumption. The problem is in the fact, that **NMOS loads can't** have very **low current** in conducting state – lower practical **limit is 3-5 μ A**. This necessitate in the use of **very short pulses** for refreshing to **keep power within** specified limit. However, we have **suggested solution** to this problem, which allows to **reduce average current** to required value **without need for short pulses**.



Prototype 2 design - continue



- Next idea was to **replace calibration circuit from digital** where offset is kept as a state of **calibration register** with **analog circuit** in which offset is kept as a **voltage on a capacitor**. This **eliminates the problem of the limited by number of bits in calibration register range** of offsets circuit is **able to compensate**. Sarnoff engineer farther simplified this schematics by eliminating part of circuit connected to inverting output of comparator.

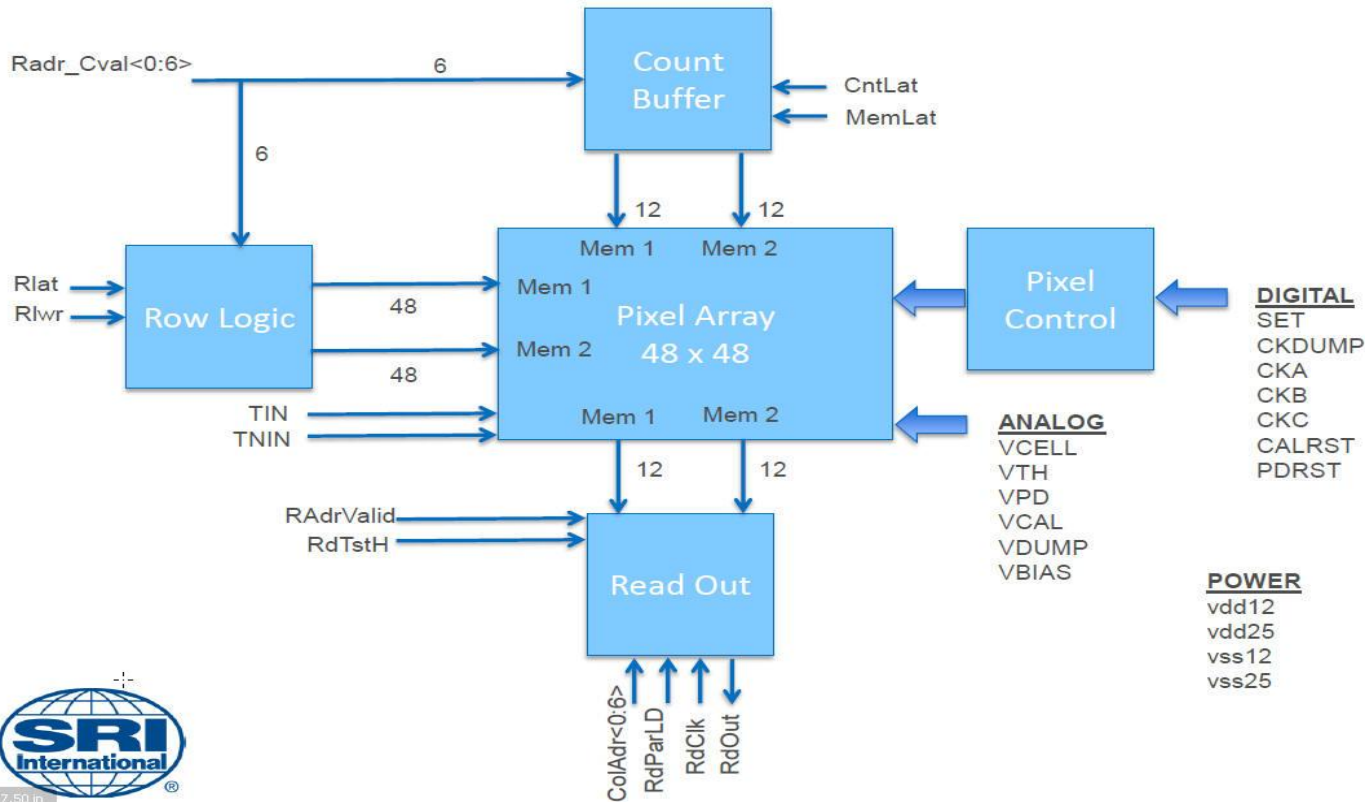


Prototype 2 chip

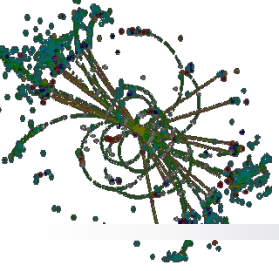


SRI International
SARNOFF

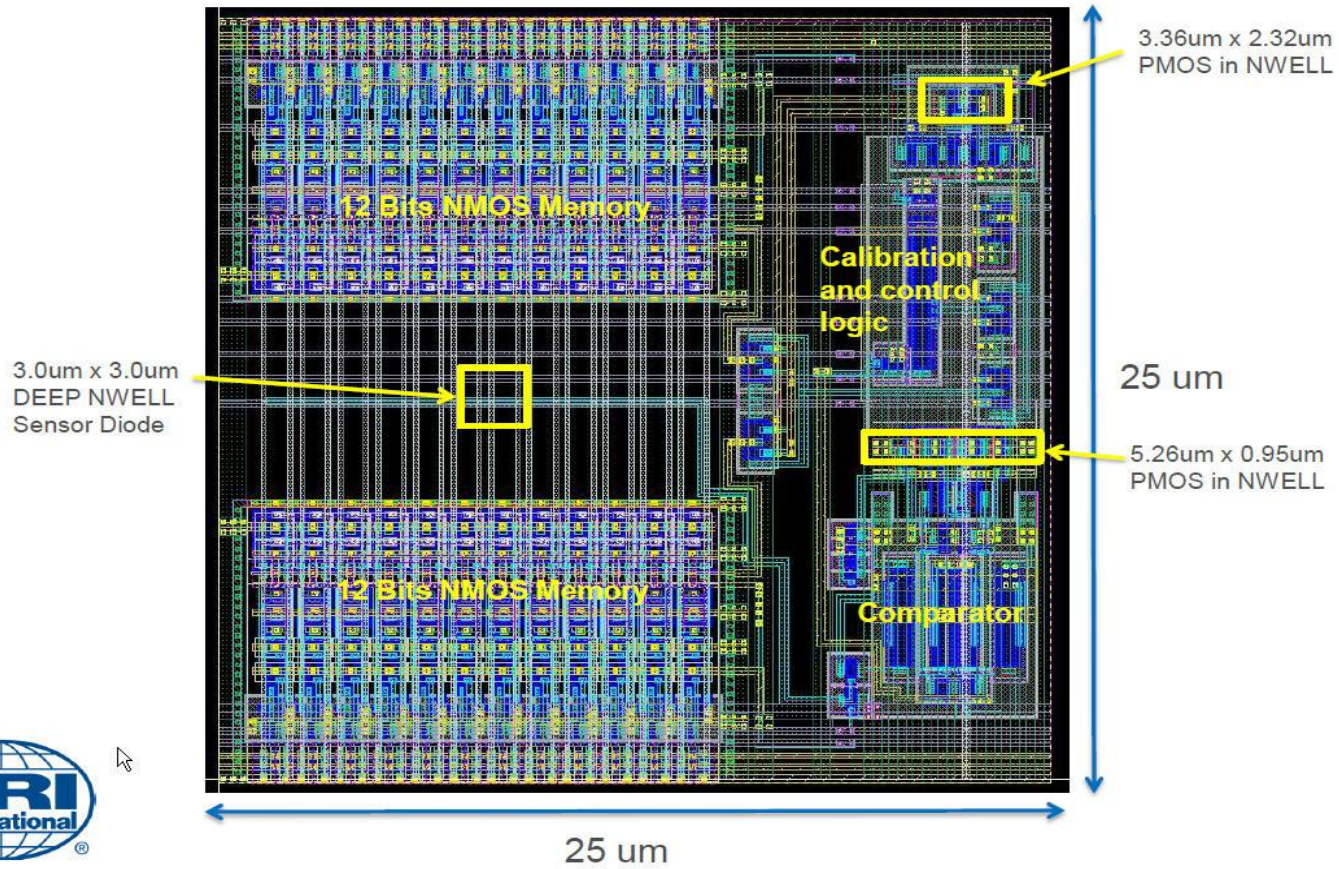
Chronopixel 2 Block Diagram Detail



One of the **technical problems** was in the **size of the chip** – to make production **cheaper** we agreed to limit chip size to **1.2x1.2 mm²** . This limits the **number of pads** on the chip to not more than **40**. And that leads to the need of **multiplexing some signals** – for example, **12 bit** time stamp is provided via **6 bit** `Radr_Cval` bus with most significant bits on the high phase of `CntLat` signal and least significant – on low, with **de-multiplexing** in Count Buffer.

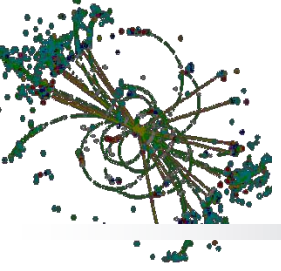


Prototype 2 pixel layout

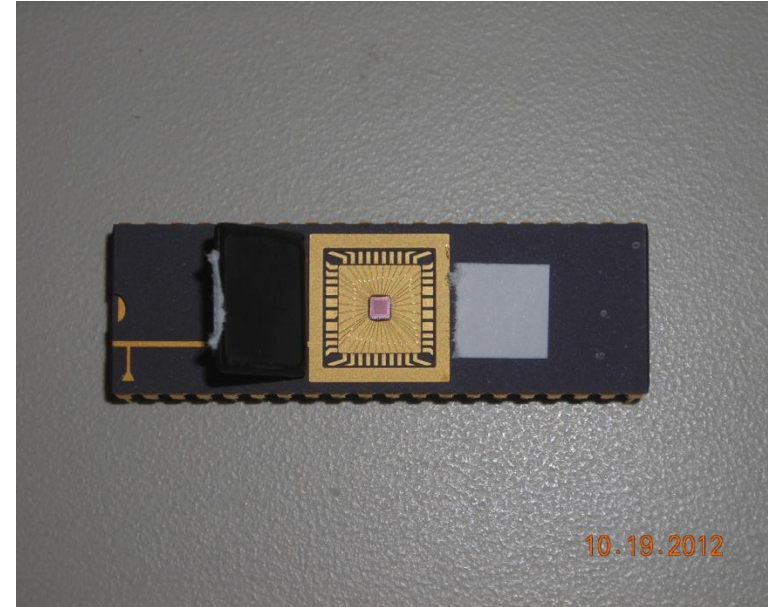
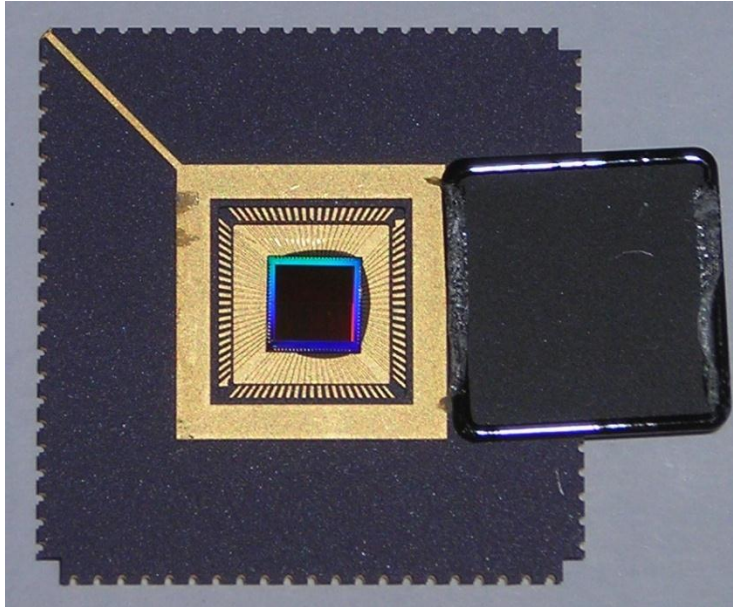


12

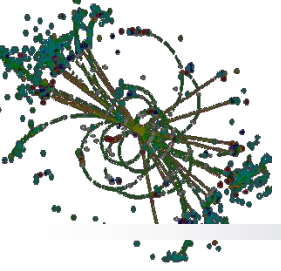
All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to $4 \times 5.5 \mu^2$.



Prototypes 1 and 2



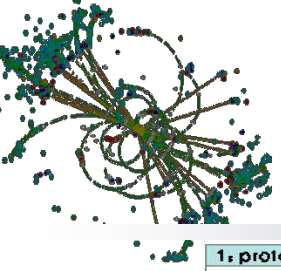
- **Because of much smaller chip size for prototype 2, there is not enough room on chip periphery to make 84 pads, as it was in prototype 1. So, 40 pads and 40 pins package were used.**



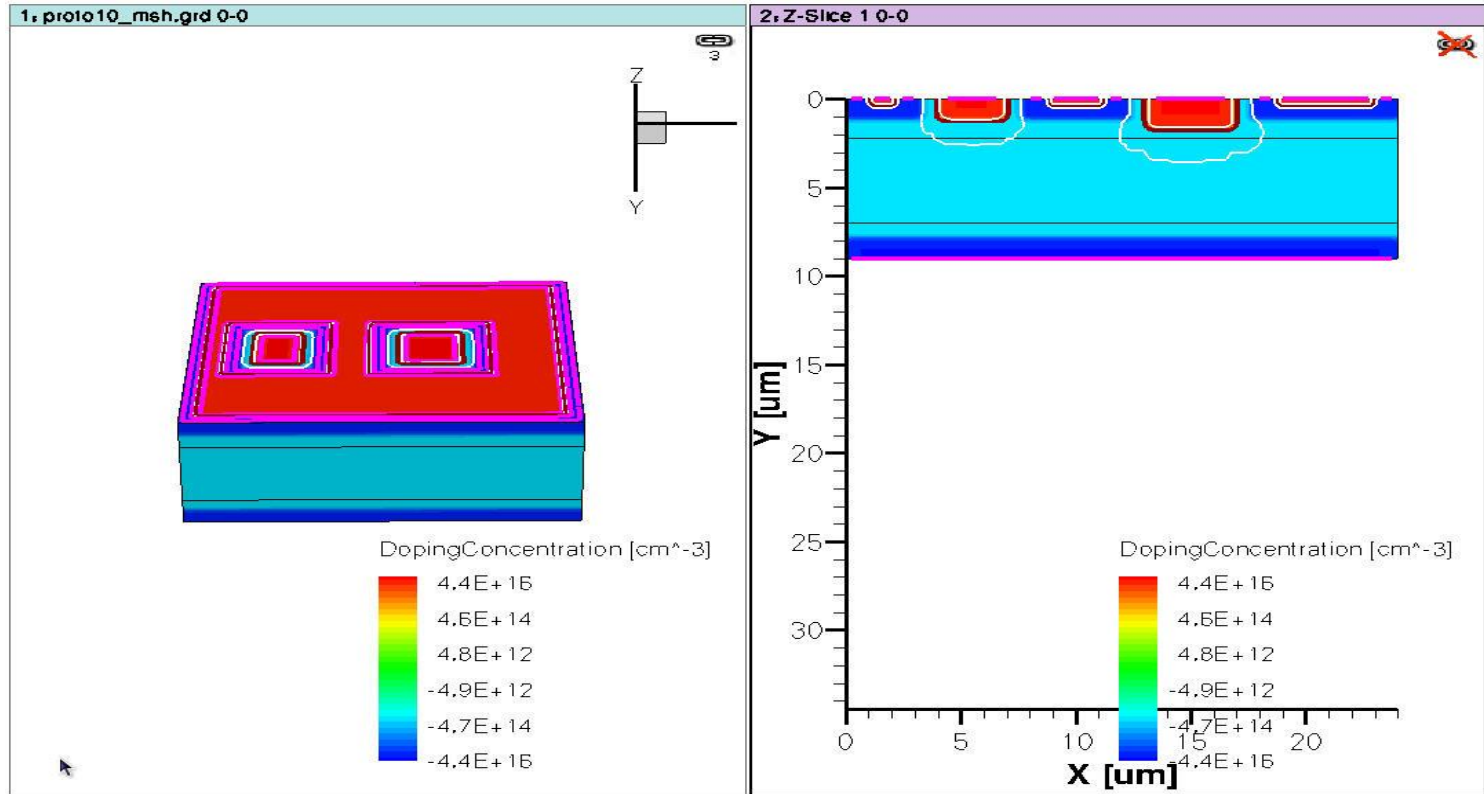
Price for allowing PMOS in pixels



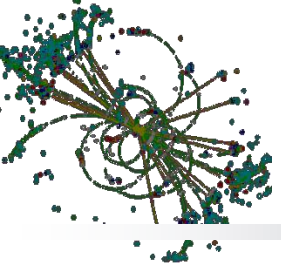
- Because of **shorter** channels and **lower voltage** in **90 nm** technology, it is very **difficult** to build comparator with **large gain** and **low power** consumption, using **only** NMOS transistors.
- So, we decided to **allow** use of **PMOS** transistors inside pixels, but **minimize** their use only to **comparators**.
- It will **reduce** charge collection efficiency to $S_{se} / (S_{pm} + S_{se})$, where S_{se} is **sensor electrode area** and S_{pm} is the **area of all PMOS** transistors in the pixel. We hoped to have the S_{pm} to be around $1\mu^2$. However in the final Sarnoff design this area appeared to be close to $12\mu^2$. To reduce noise we want to **reduce** S_{se} from about $100\mu^2$ as it was in the first prototype to something like $25\mu^2$.
- From this, we can expect our **charge collection** efficiency be only about **67.5%**.
- However, we need to **add width** of depleted layer to electrode areas. It **will reduce** area ratio and **reduce** charge collection efficiency. But taking into account **larger depth** of the signal charge collection electrode will **increase** efficiency.
- Next slides show **simulation** of prototype 2 performance



Prototype 2 simulations



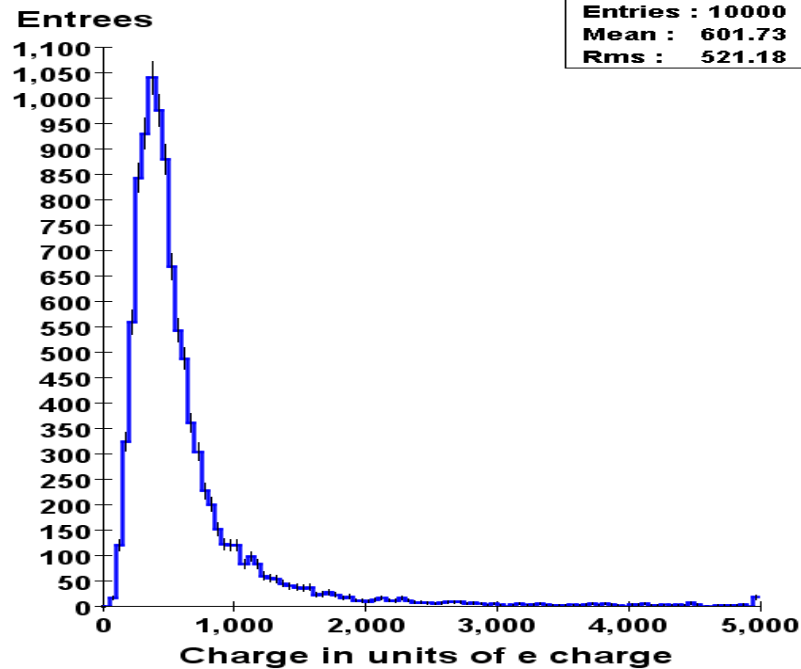
Here you can see **simplified** pixel model I used to **simulate** charge collection. Large red squire in the center – **signal collecting** electrode, smaller red squire at the left – **area taken by pmos** transistors, the rest of the red on left picture shows n-wells of electronics , which are sitting on the **top of p++** doped areas (NMOS transistors). White line outlines depleted region.



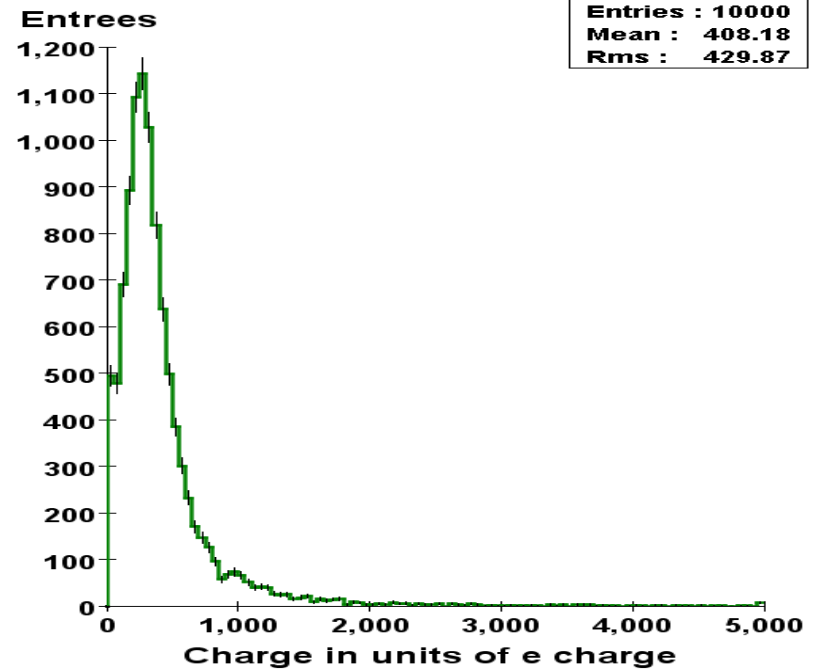
Prototype 2 simulations



Charge generated by track

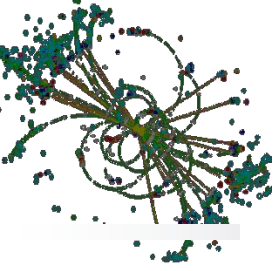


Collected charge



Here are **results** of charge collection **simulation**.

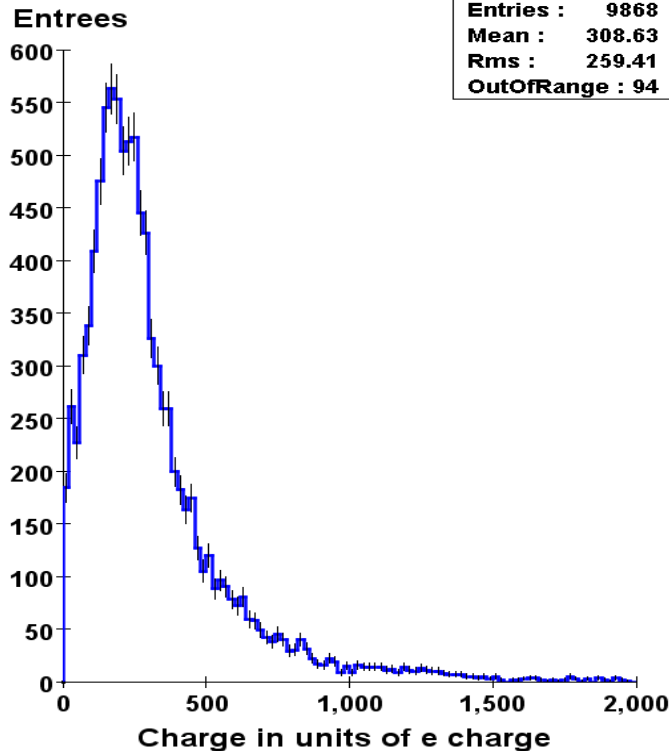
On the left is the distribution of number of electron-hole pairs, **generated by track** in the sensor (generated charge). On the left - amount of **collected** by all nearby pixels charge. From the numbers charge collection efficiency is **67.8 %**



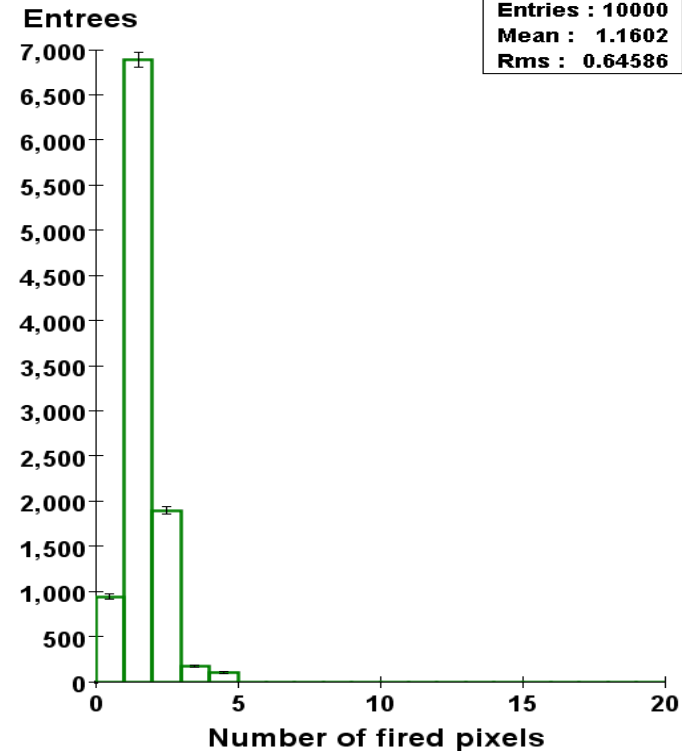
Prototype 2 simulations



Charge collected by central pixel

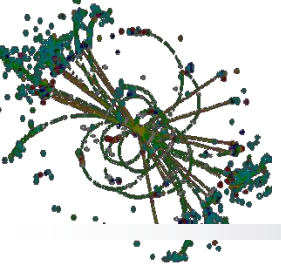


Number of pixels above threshold



Here are results of hit **registration efficiency** simulation.

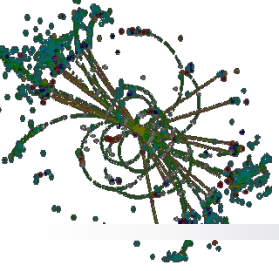
On the left is the distribution of **amount** of charge, collected in the **central pixel** in cluster. On the right - number of **fired pixels** when track passes the sensor with pixel **threshold 75 e**, which is **5 sigma** of noise if its level is **15 e**. Number of events with **0 fired pixels** is about **9%**, so hit registration efficiency is **91%**.



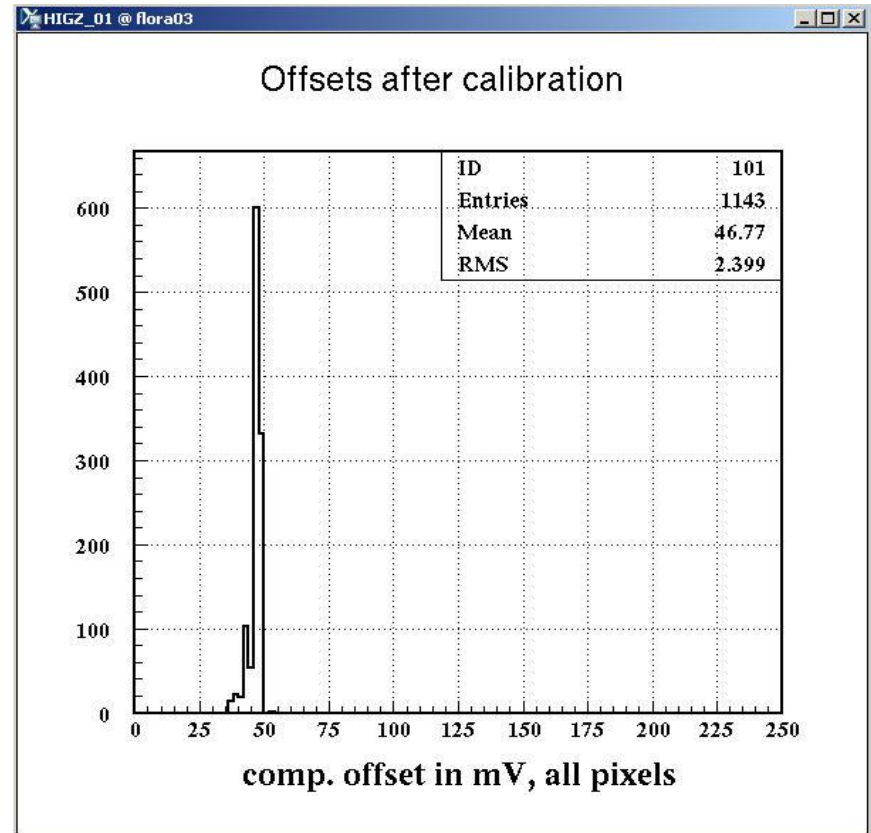
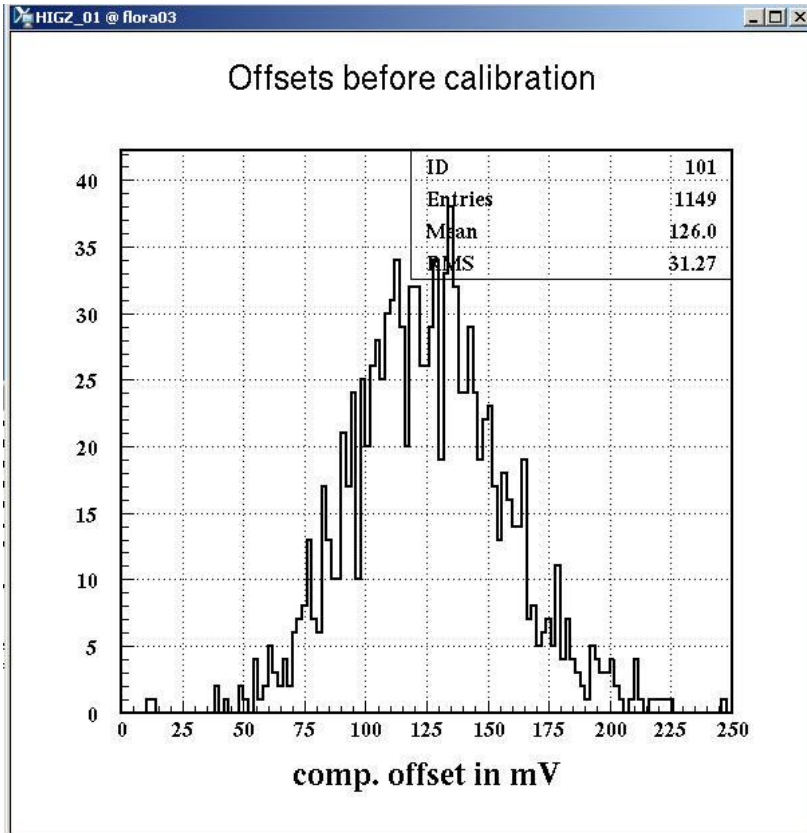
Pixel variations



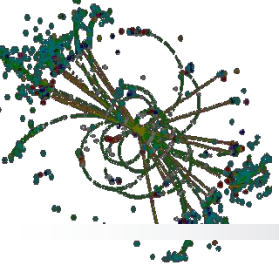
- As soon as Sarnoff design manager gave me **final schematics**, I started **SPICE** simulation of its performance to **double check** their simulations. Suggested by them comparator design **did not pass** my check – it appeared **very sensitive** to the **rise time** of the latch signal. So I insisted that they **use old** (prototype 1) **comparator**, which **did not** have such a problem. But they also **wanted** to **test** their **new** design as they believed that with **additional** latch signal **shaping** it should work and it have **better switching** characteristics. So, we agreed to have **half** of the pixels have their **new** design.
- They wanted to have **charge collection** electrode only **3x3 μ^2** to have **low noise** level. However, with **12 μ^2** of PMOS transistors in the pixel would lead to charge collection efficiency **less than 50%**. From my calculations of noise and charge collection efficiency the **optimal** (providing **maximum signal/noise** ratio) charge collection electrode should have about **22 μ^2** area. So, we decided to have half of the pixels with **9 μ^2** charge collection electrode area (to check how much it helps with noise reduction), and half – with **22 μ^2** .
- That leads to **4 different variants** of the pixel, which will be implemented in **each chip**.



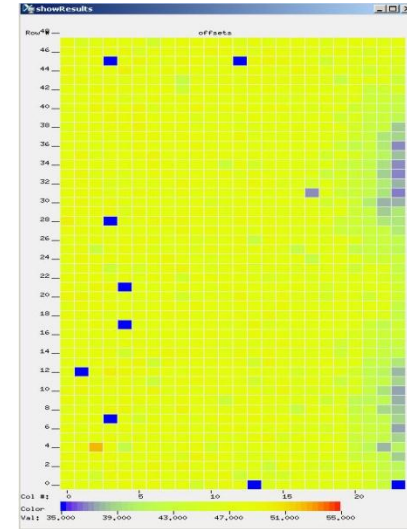
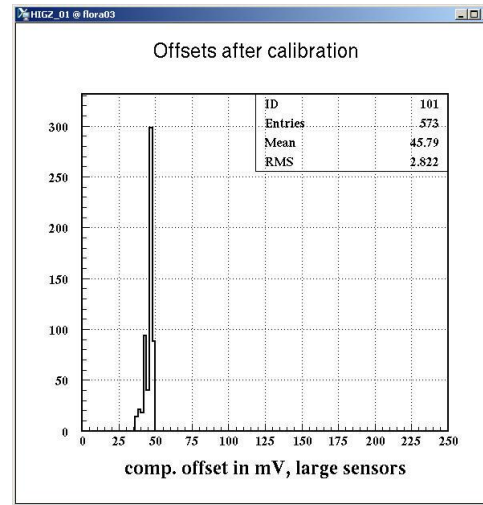
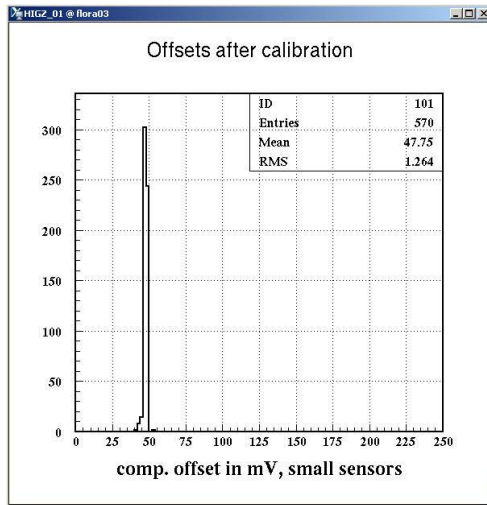
Test results - calibration



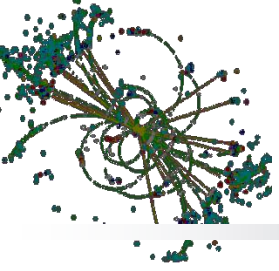
Before calibration voltage on the calibration capacitors were set to value that all comparators are in fired state at 0 threshold. During calibration this voltage changes to the point when comparators flip to non-fired state. To measure offsets I have used 50 mV pulse to get S-curves – probability of comparator be fired as function of threshold.



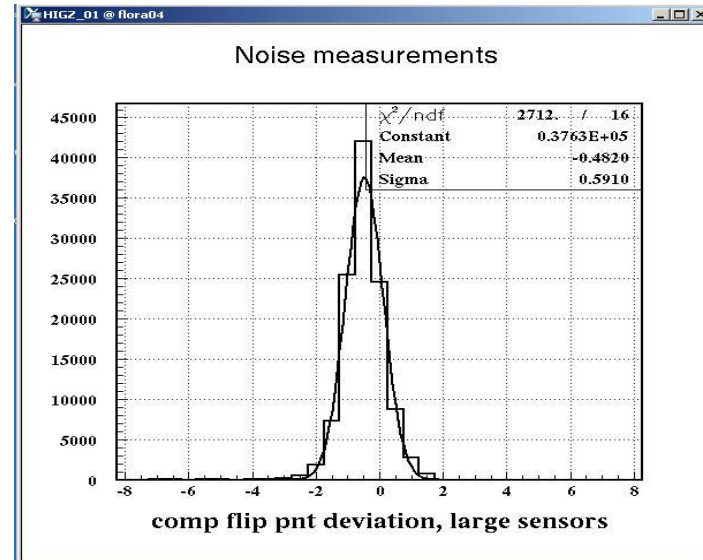
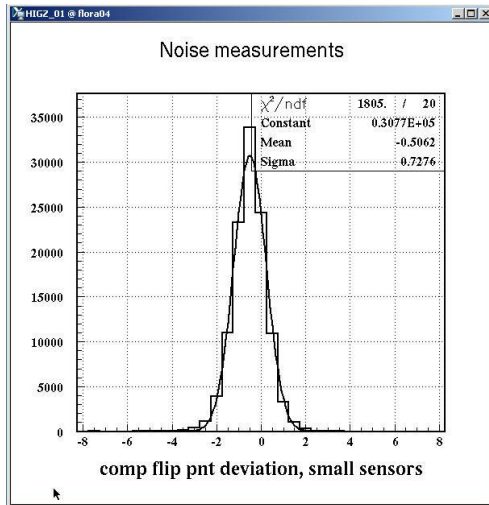
Test results - calibration



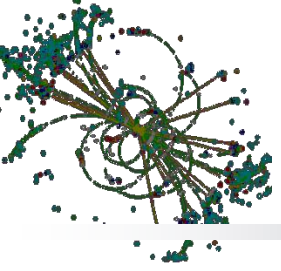
- **Why calibration did not make offsets distribution like δ -function? On the left plot we see this distribution for pixels in the left part of the chip (look at map at right). They have small sensor diodes, but what matters here is that they are far from chip periphery, where all drivers are sitting. This distribution is close to what we expect. Distribution on the plot in the middle is for 12 columns at the edge of the chip (large sensor diodes). And anomalous offsets, seen on the pixels map in bluish colors are in the pixels, close to clock drivers. So, there are some cross-talks from drivers. (9 completely blue pixels on this map – just “bad pixels”, having memory problems, we don’t care about them for now.)**



Test results - noise



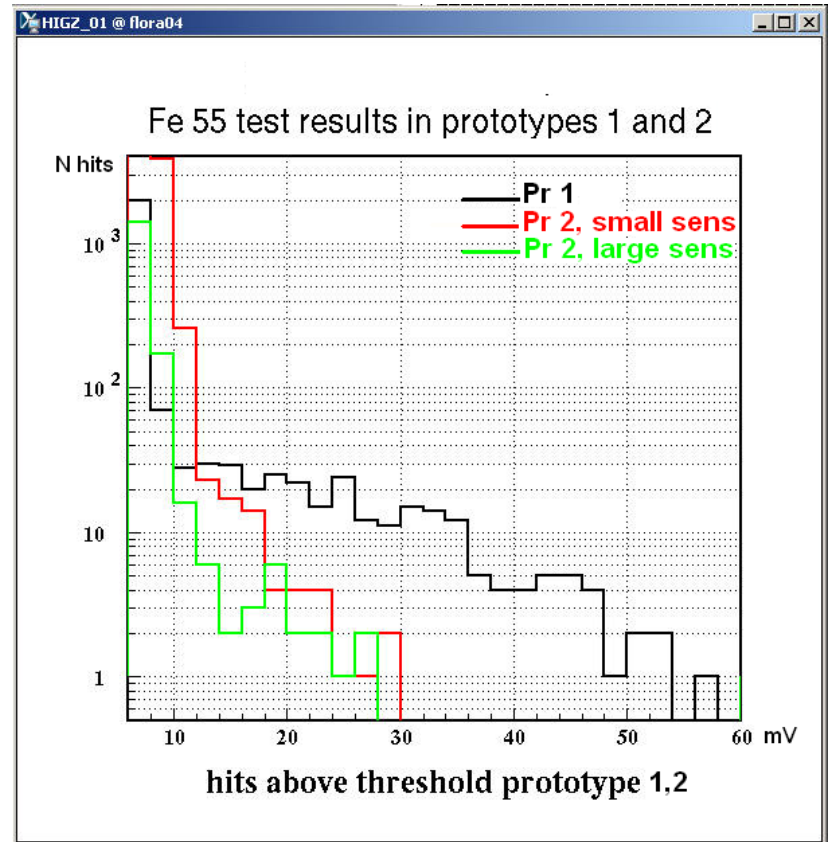
- Noise distributions for pixels **with smaller** (on the left) **and larger** (right) sensor diode area. If we assume, that reset (KTC) noise is dominant, we can calculate the value of sensor capacitance is **7.6 fF** and **11.5 fF**. It is about 2 times larger than in prototype 1 (about 5 fF), and almost 10 times larger than we expected from sensor area. The reason for that appeared to be in **90 nm technology** – design rules **prohibiting blocking p++ implant**. That means that diodes are sitting in very low resistivity layer, not in 10 ohm*cm epi layer, as was in prototype 1. We don't know yet if this design rule is specific for TSMC process and if there are foundries allowing bypassing it. In principle we don't see fundamental reasons for this rule, as the sensor area does not contain parts requiring 90 nm feature size.

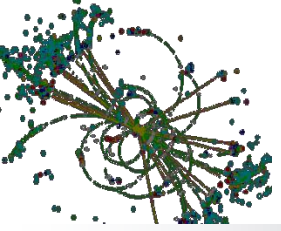


Test results – Fe55 signal



- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – $9 \mu^2$ and $22 \mu^2$ (“small” and “large” on the plot) . The maximum signal value is **roughly in agreement with capacitance estimation from noise distributions**, though we would expect larger difference in maximum signal values here. **But statistics is very small here to do precise measurements.**





Conclusions and plans



- From both, first and second prototype tests we have learned:
 - ↵ 1. We **can** build pixels which can record **time stamps with 300 ns** period (1 BC interval) - prototype 1
 - ↵ 2. We **can** build readout system, allowing **to read all hit pixels** during interval between bunch trains (by implementing **sparse readout**) - prototype 1
 - ↵ 3. We **can** implement **pulsed power** with 2 ms ON and 200 ms OFF, and this **will not ruin** comparator performance - both prototype 1 and 2
 - ↵ 4. We **can** implement **all NMOS** electronics **without** unacceptable **power consumption** - prototype 2. We **don't know yet** if **all NMOS** electronics is **a good alternative solution** to deep P-well option.
 - ↵ 5. We **can** achieve comparators **offset calibration** with virtually **any required precision** using **analog calibration** circuit.
 - ↵ 6. Going down to **smaller feature size is not as strait forward** process as we thought.
- As for the **plans**: we need more **close cooperation** with foundries to understand the way to move forward. For the next prototype we may find the way to **bypass design rules** or we may return to larger feature size (180 nm, or may be 130nm?). This way we will be able to understand if all NMOS design really provide high charge collection efficiency. In any case, **we plan to start** next prototype design **by the end of this year** .