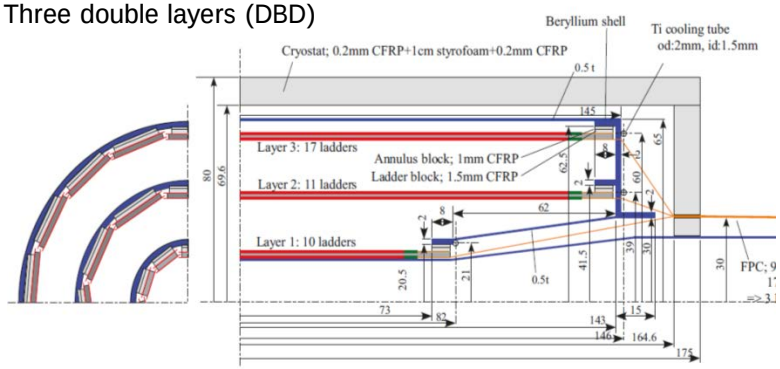
# DEPFET APS for future collider applications

## - Status and prospects of the DEPFET project –

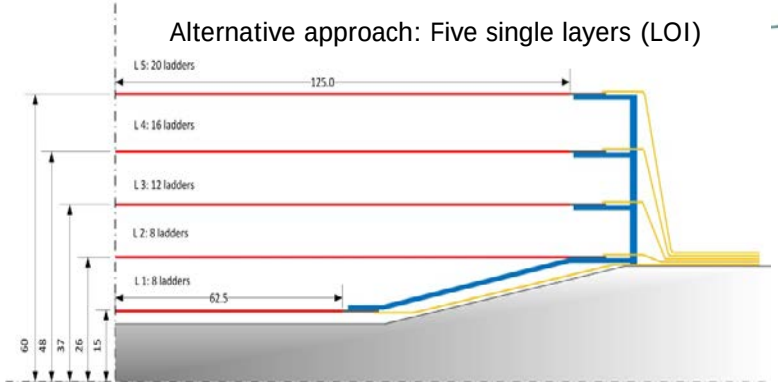
*Laci Andricek for the DEPFET Collaboration*
*www.depfet.org*

# Introduction – The ILD VXD

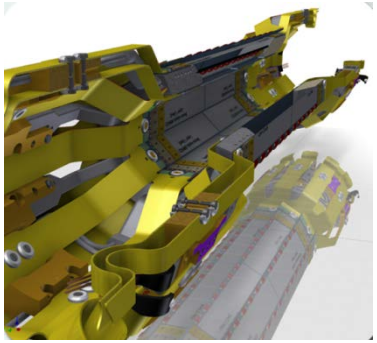
Three double layers (DBD)

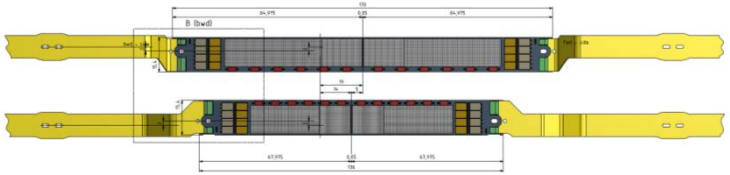



Alternative approach: Five single layers (LOI)




| | ILD LOI 5-layer layout | Belle II | |
|---|---|---|---|
| Radii | 15, 26, 38, 49, 60 | 14, 22 | mm |
| Sensitive length | 123 (L1), 250 (L2-L5) | 90 (L1), 122 (L2) | mm |
| Sensitive width | 13 (L1), 22 (L2-L5) | 12.5 (L1-L2) | mm |
| Number of ladders | 8, 8, 12, 16, 20 | 8, 12 | |
| Pixel size | 25x25 (L1-L5) | 55x50 & 60X50 (L1), 70x50 & 85x50 (L2) | $\mu m^2$ |
| frame rate | 20 (L1), 4 (L2-L5) | 50 | kHz |
| Number of pixels | 800 | 8 | Mpix |





Belle II PXD ladder:
(almost) prototypes for L1 and L2 of ILD LOI layout!!

# The most challenging requirements

:- small pixels (~20µm) for excellent single point resolution (~3µm)

:- minimal material

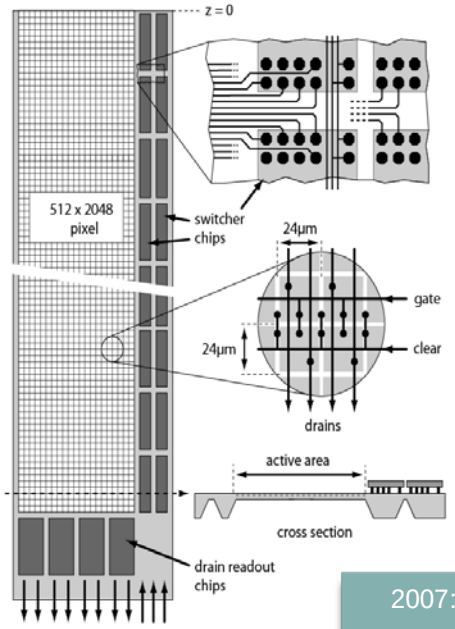
→ thin sensors with large S/N; minimize support, services, and cooling material

:- like the CPS option, the DEPFET runs in a rolling shutter mode (read-out during the bunch train)

→ due to background, take as many frames as possible to minimize occupancy!

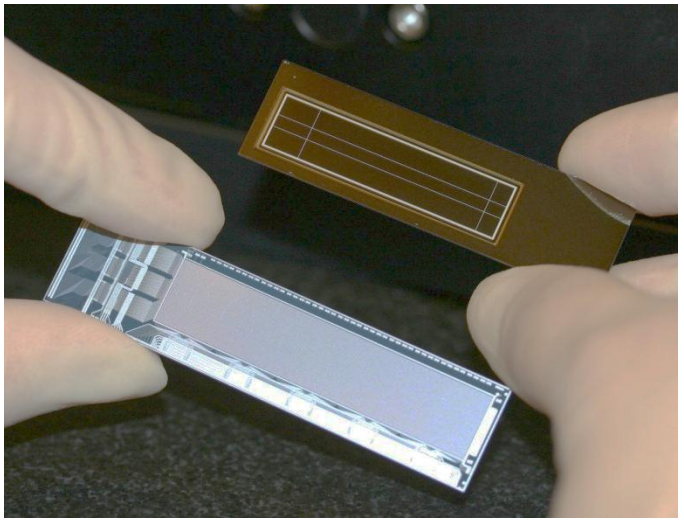
→ our goal is (as written in the LOI) ~1/50µs frame rate (innermost layer)

:- radiation tolerant up to ~1Mrad and ~$10^{12}$ $n_{eq}/cm^2$ for 10 years operation ($e^-$ in the MeV range)




2007: ILC Module concept

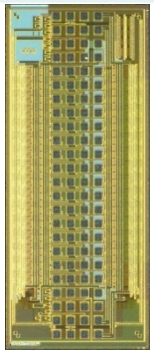
2011: DEPFET prototype Modules for Belle II

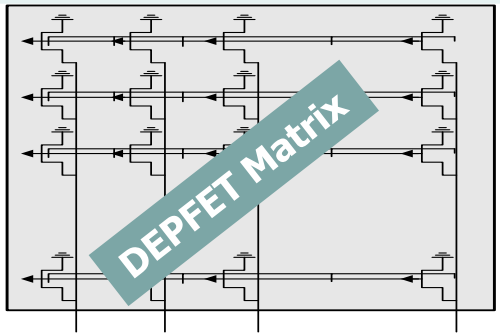


# Auxiliary ASICs - status as of today

## Switcher

- » 3.6 × 1.5 mm²
- » Gate and Clear signal
- » Fast HV ramp for Clear





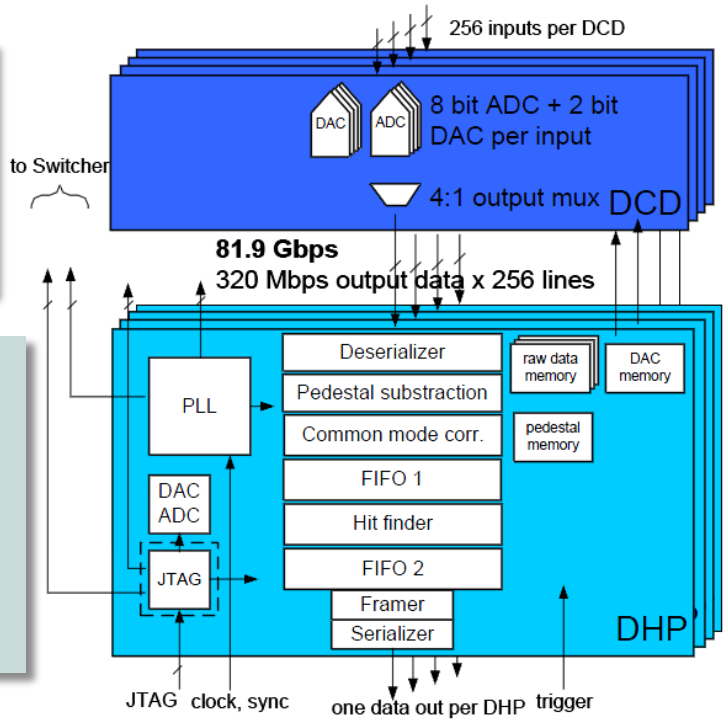

**10 MHz** row frequency
100 ns ADC conversion time

## Switcher

- » 350nm, HVCMOS AMS
- » and 180nm, HVCMOS AMS/IBM
- » available since 9/2011

## DCD

- » 5 × 3.2 mm²
- » "Drain Current Digitizer"
- » UMC 180nm
- » transimp. amp. and ADC




**5 Gbps** (1.25 Gbps link per DHP)

## DCDBv2

- » available since 9/2011
- » 256 channels, 512 ADC
- » 35nA noise @ 100 ns/row
- » optional analogue CM Correction

## DHP

- » 4 × 3.2 mm²
- » "Data Handling Processor"
- » IBM 90nm → TSMC 65nm
- » Digital control chip
- » first data compression

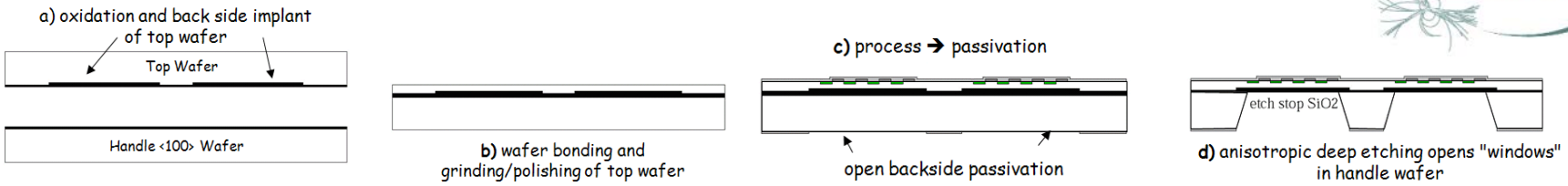
## DHP 0.2, 90nm IBM

- » full size chip, 64 channels
- » received Dec. 2011, runs with DCD

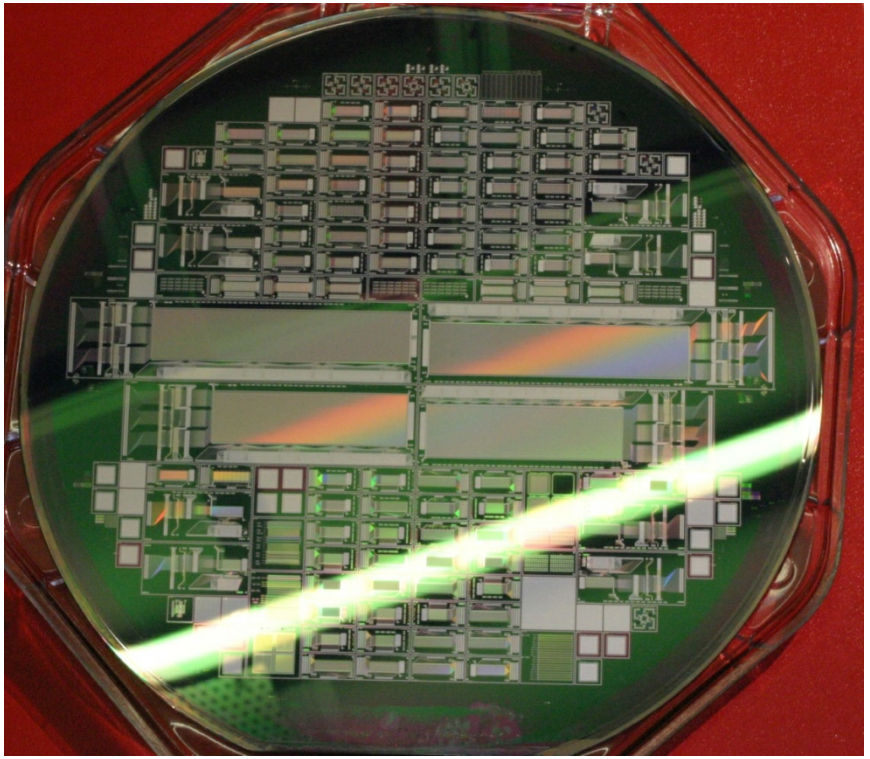
## Future plans (for ILD ...)

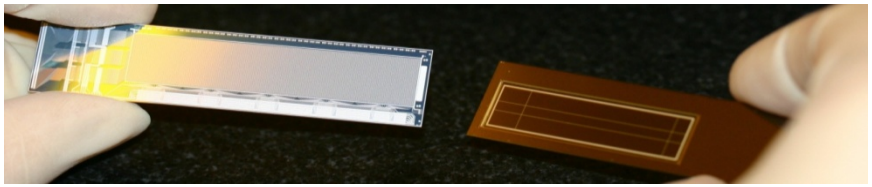
- » combine DCD and DHP in one chip

# PXD6: first thin DEPFETs on SOI



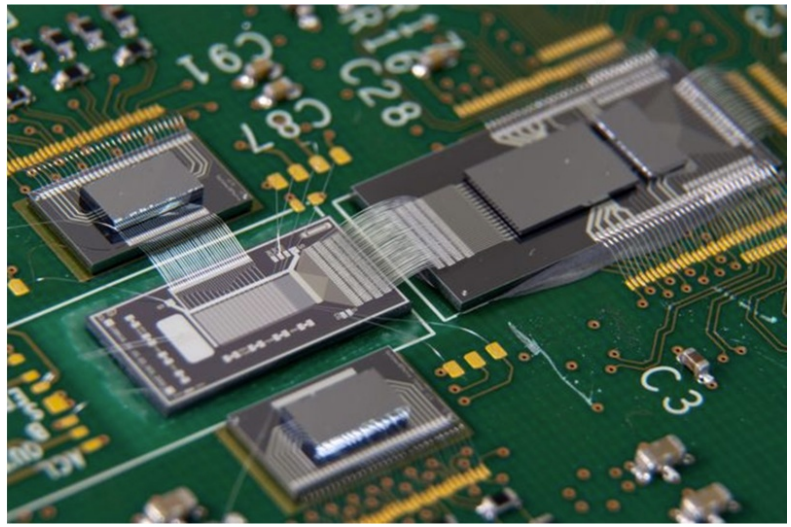

- 8 SOI wafers (50 µm top layer, 400 µm handle)
  + 2 reference wafers on std.
- Technology variations on the wafer and wafer-to-wafer (new dry etch techniques, oxide thickness.. )
- 9 impl., 19 litho., 2 poly Si, 2 Al (.... & 3rd metal Cu later)
  - ↳ 3m (SOI) + 16m (main process incl. thinning)
- About 100 test matrices in different variations
  - ↳ pixel sizes from 20 µm to 200 µm
  - ↳ shorter gate length, improved clear structures ...
  - ↳ various drift region and pixel designs ...
- 4 large half-ladders with the most promising options
- purpose of this production run:
  - ↳ practice full process sequence (incl. thinning)
  - ↳ build sensors for system tests
  - ↳ test design variations and verify simulations
  - ↳ gain yield experience

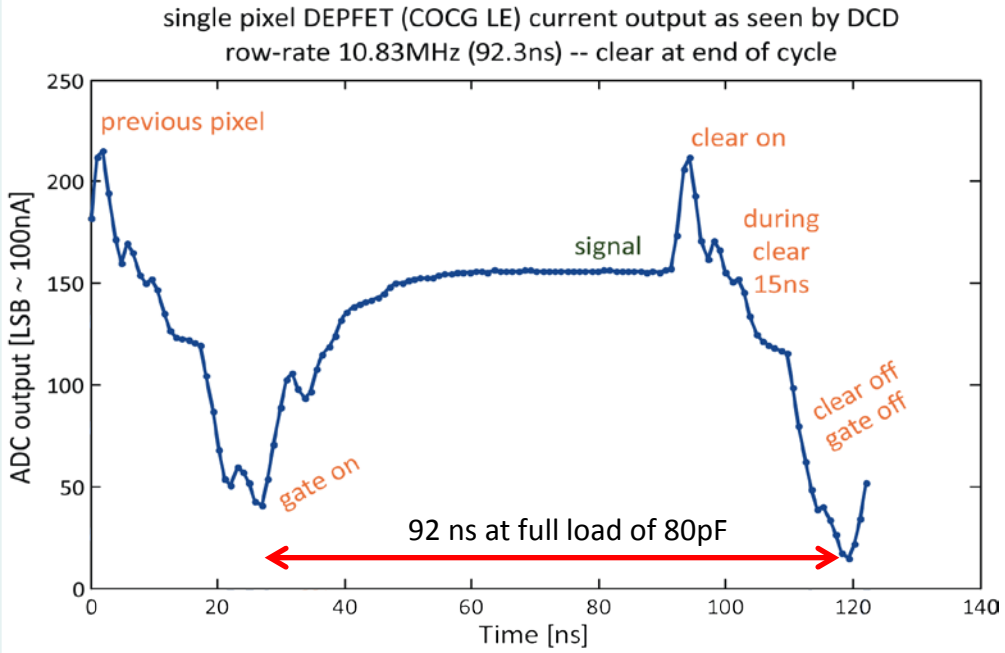


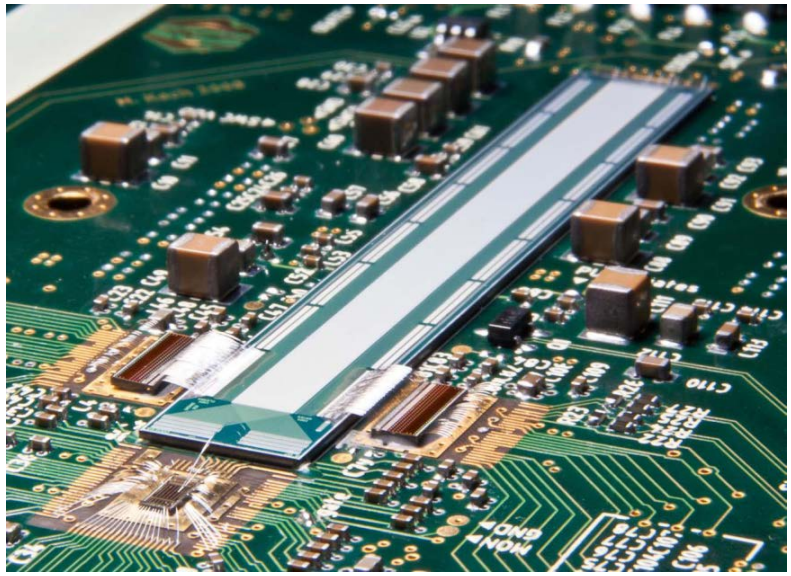


# PXD6 testing in the lab

- bench tests in the lab
  - ↳ determine best operating point (Clear, ClearGate, Drift..)
  - ↳ in-pixel studies with laser
  - ↳ radioactive source tests
  - ↳ **read-out speed...**
- goal @Belle II
  - 320 MHz system clock
  - 50 kHz frame rate (20µs r/o time per frame)
  - 768 rows, 4-fold r/o → **~100 ns per row**





# r/o speed with ILC-type sensor: status and prospects

» 100ns per r/o → 2048 rows per half-ladder, 2-fold r/o → **~1/100µs frame rate state of the art**

» possible improvements (with current f/e electronics and ADC)

↳ **Sensor technology**: a third metal layer in the sensitive area is within reach (Cu, see later)

→ 4-fold read-out with small pixels → **1/50µs frame rate**

↳ **optimization** of cluster size for shallow(er) tracks

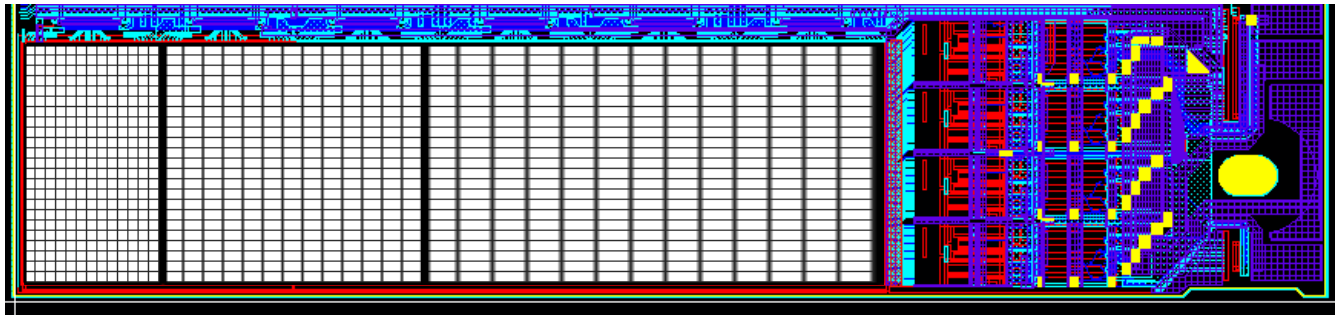
→ Introduce three regions in z with ~25µm/50µm/100µm pixel pitch in z (similar to Belle II)

→ #rows reduced by factor ~2 → **1/25 µs frame rate possible**

» **R&D status and plans:**

↳ **3rd metal layer well advanced, used already at ladder periphery for Belle II PXD**

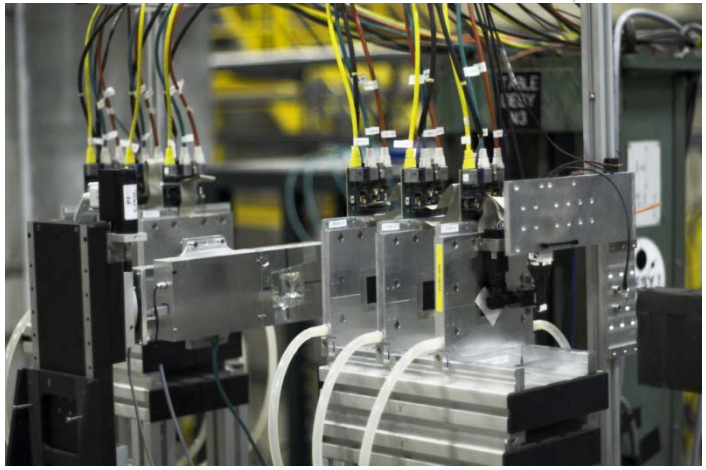
↳ **simulation work planned: variable pixel sizes in z and impact on physics**

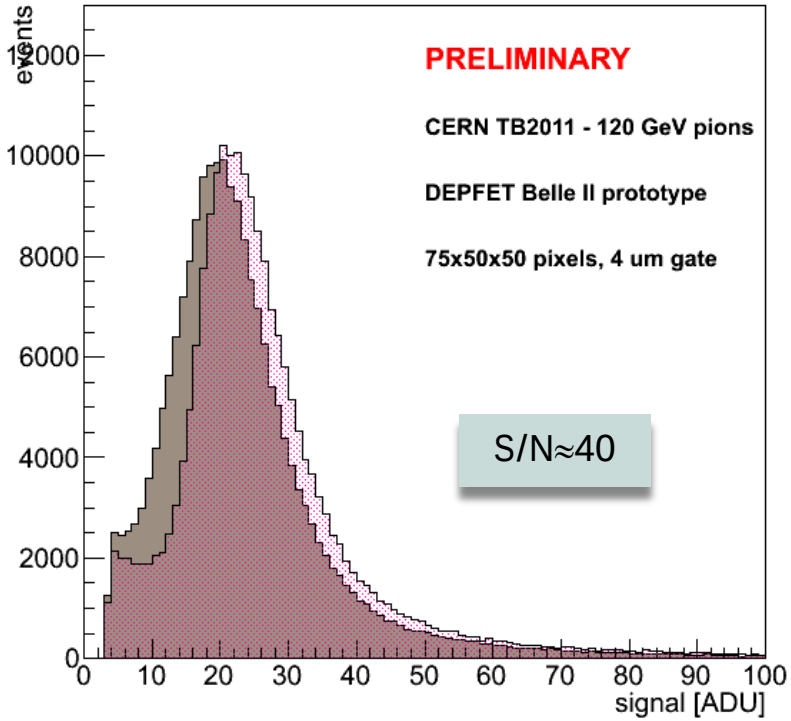


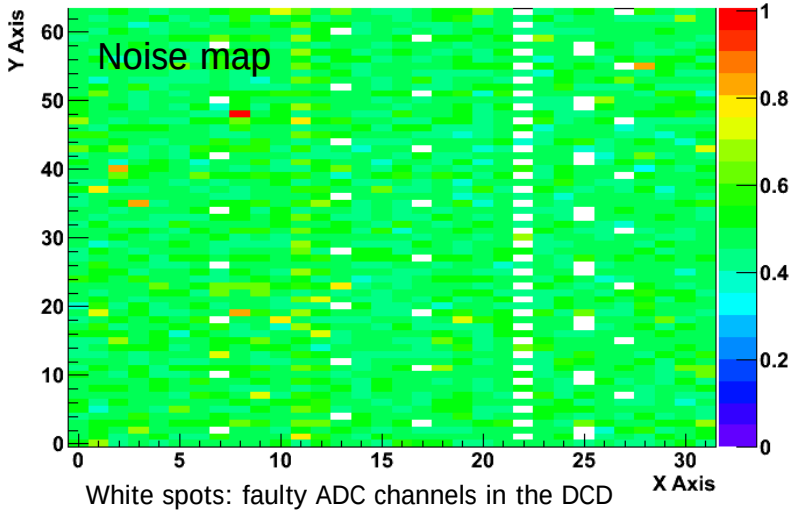
# 120 GeV pions beam test results

» latest beam test Oct. 2011, CERN SPS, 120GeV pions
  ↳ PXD6 matrices, thickness 50µm
  ↳ L=4µm, 75x50µm$^2$ pixel

» very homogeneous noise and hit maps, few ADC channels bad



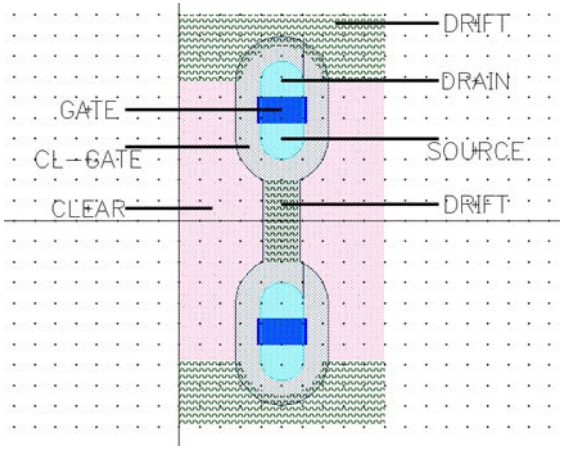


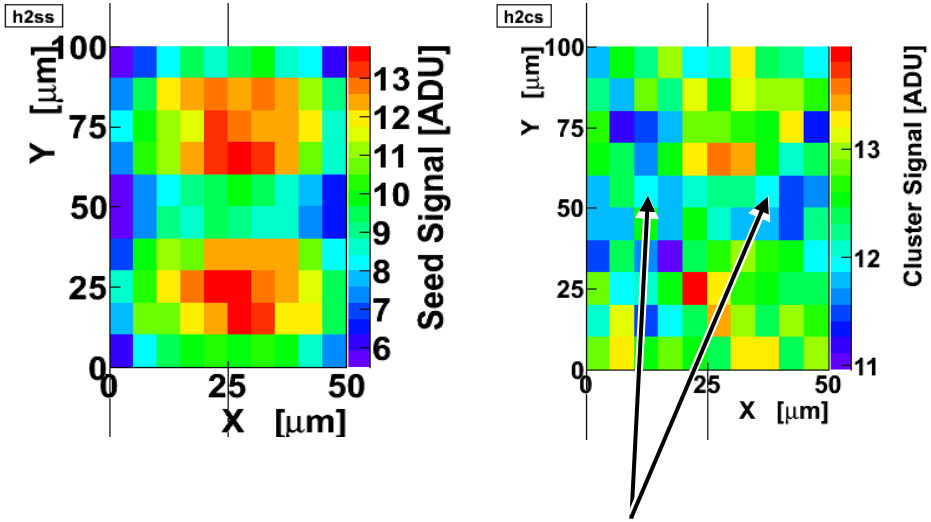



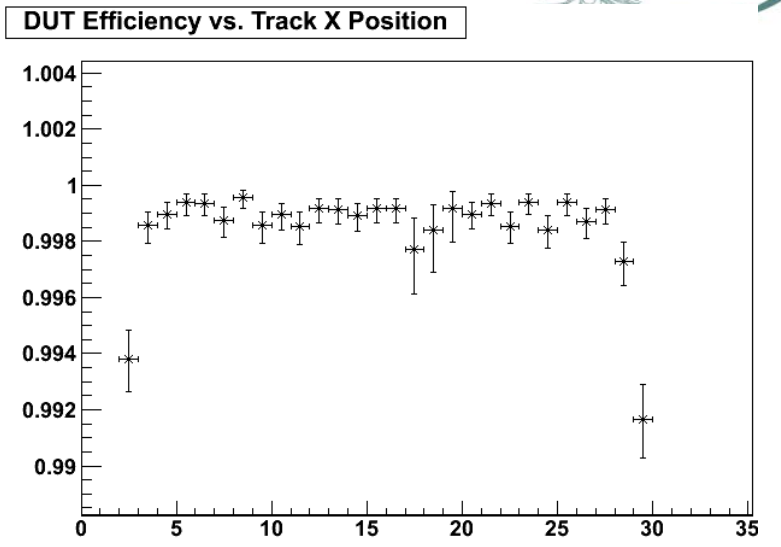

White spots: faulty ADC channels in the DCD

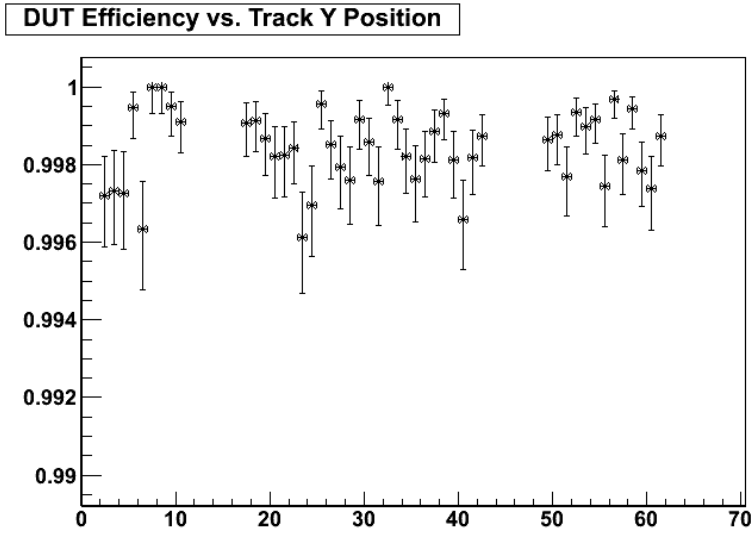
# Beam test – efficiency, charge collection

- small charger losses <10% in clear region
- efficiency >99.5%, both in X and y



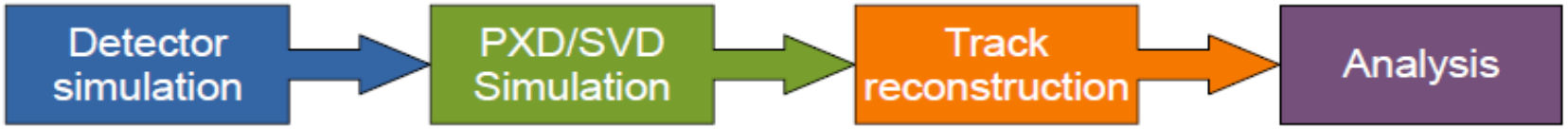




Small charge losses in “clear” regions

# Beam test – expected resolution at ILC




Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

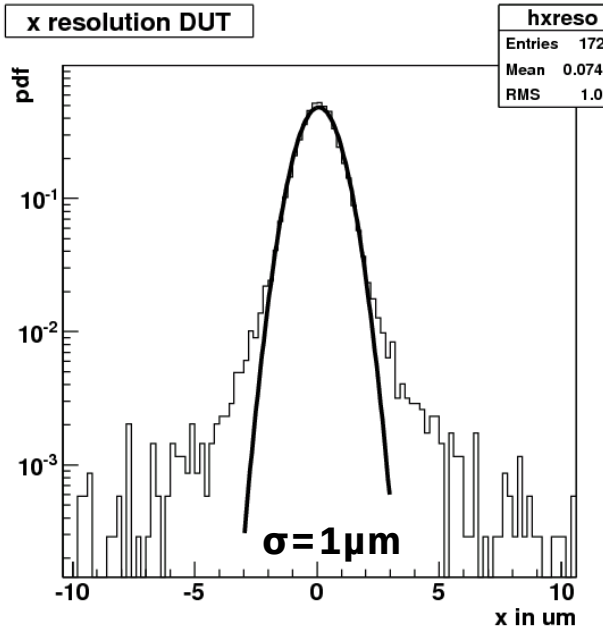
Marlin tracking
PXD+SVD+CDC

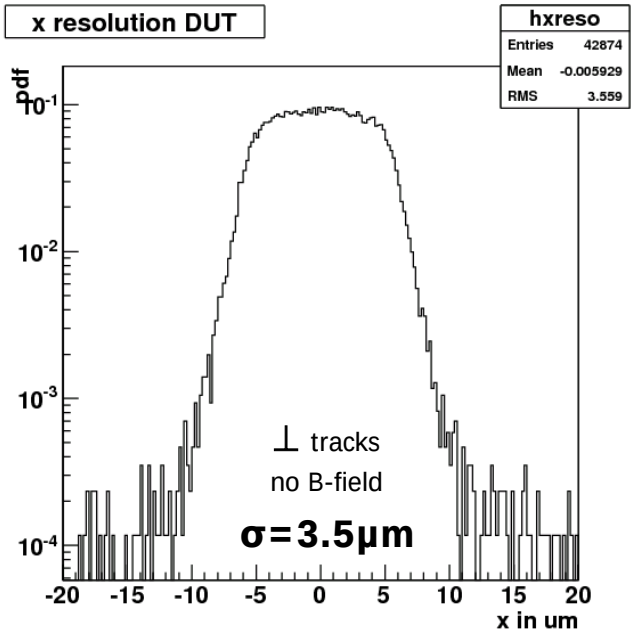
Physics channels

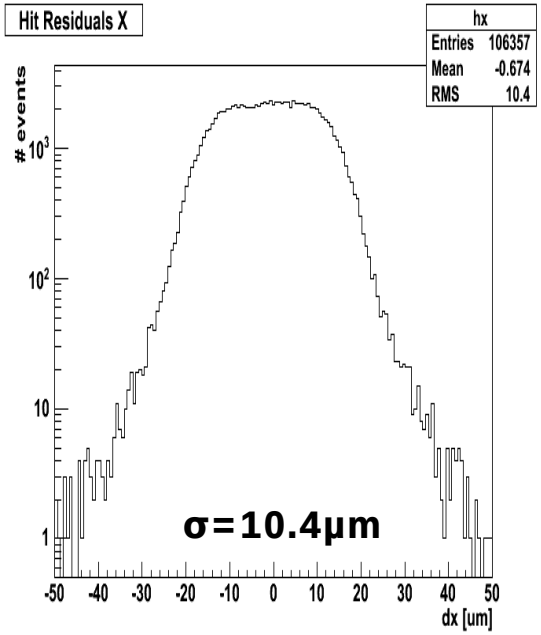
**Test Beam Data**
20x20x450 µm³
Single point resolution: 1 µm

**ILC (Simulation)**
20x20x50 µm³
Single point resolution: 3.5 µm

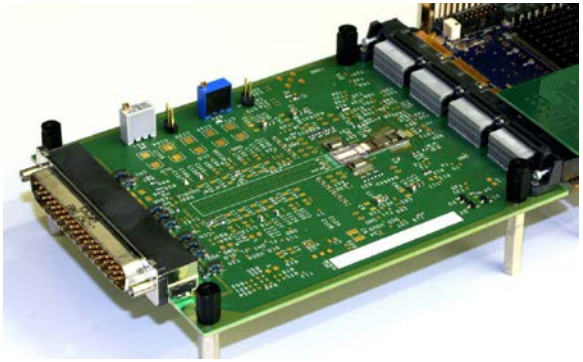
**Test Beam Data**
50x50x50 µm³
Single point resolution: 10.4 µm

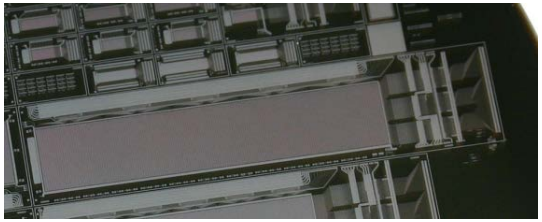


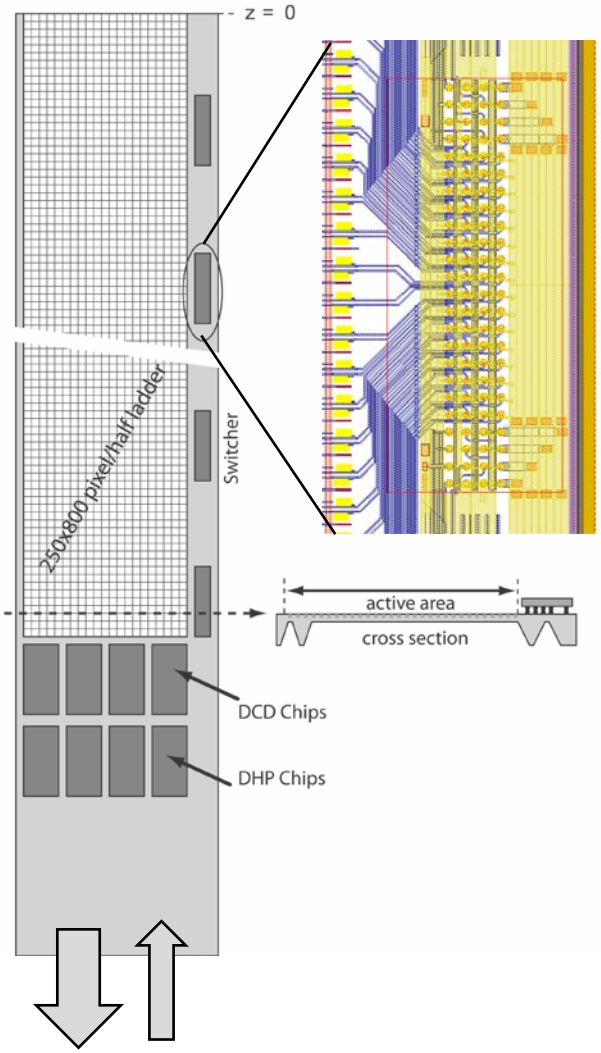



# Towards a real ladder







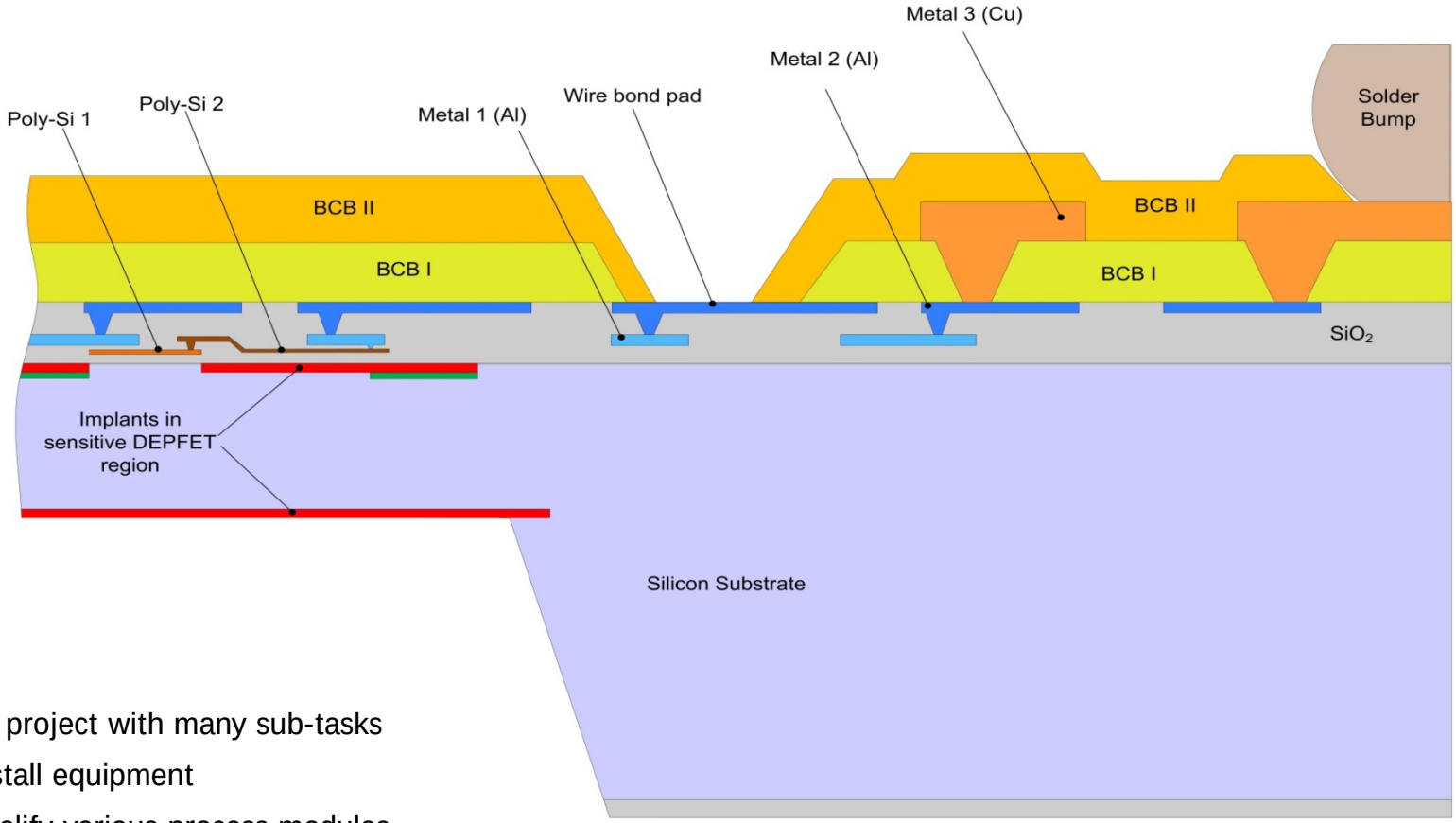

**Transition from test systems to integrated modules**

» PCB for the various matrices ….. “hybrids”

» first bump bonded chip on PXD6 matrices
- ↳ 2 metal layers, not the final geometry, simple 3rd metal later
- ↳ need still support PCB for I/O
- ↳ not perforated balcony, Au studs as UBM

» Belle-II PXD Module (two modules form a ladder)
- ↳ **three metal layers, Cu as LM only on periphery**
- ↳ 4 DCD, 4 DHP, 6 Switchers → ~3000 bonds/module
- ↳ **Cu as UBM, bumps partly on thinned perforated frame**
- ↳ passive components soldered to substrate
- ↳ I/O and power over Kapton cable

# Introducing a Cu layer on the DEPFET module




- complex project with many sub-tasks
  - ↳ install equipment
  - ↳ qualify various process modules
  - ↳ many(!!) test runs
    - ↳ dummies and test diodes

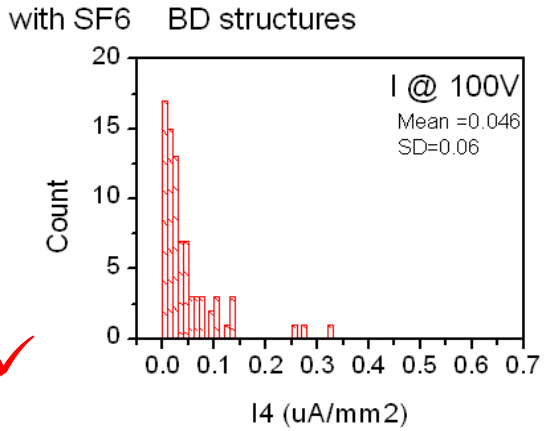
# Cu Layer – Status in Summary

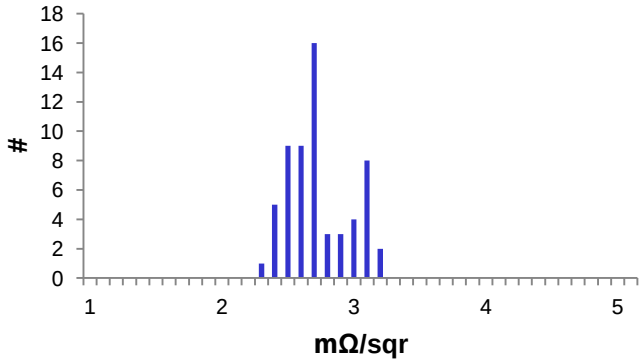
:- BCB isolation layer to last Al: **stands 100 V with negligible current** ✓

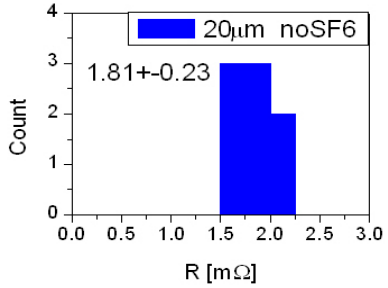
:- 6µm Cu layer: **sheet resistance ~3 mΩ/sq.** ✓

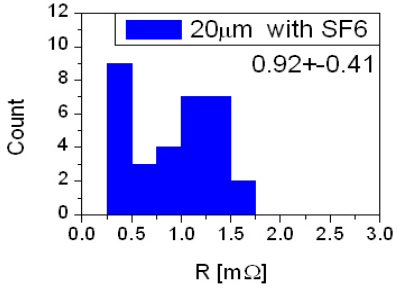
:- contacts to Al through BCB isolation: **diameter 20 µm → 1 .. 2 mΩ/contact** ✓

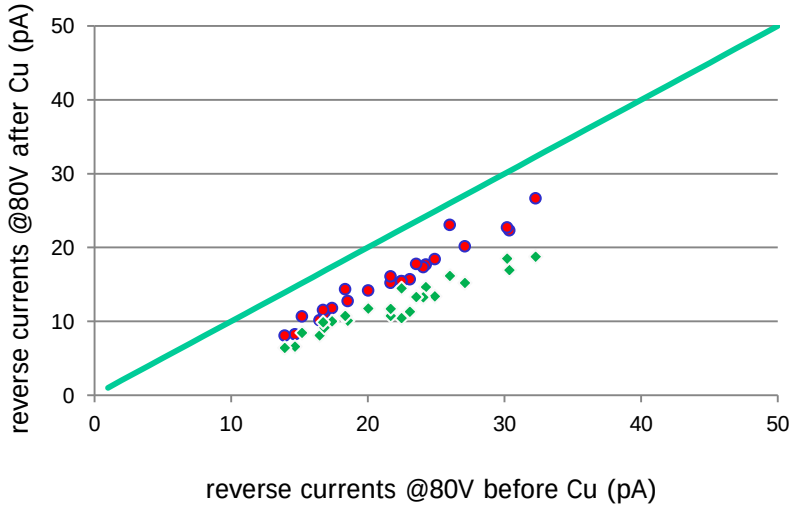
:- basic properties of **test diodes and MOS caps not affected** by copper process ✓



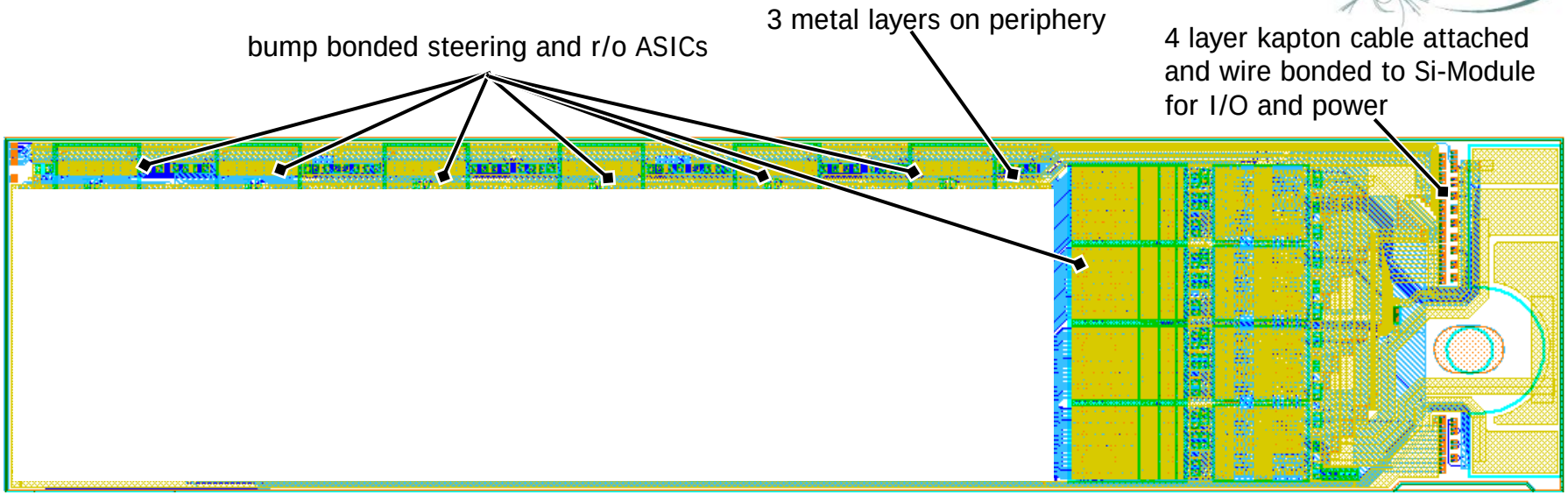



# E-MCM – everything but the DEPFET

Electronic Multi-Chip Module



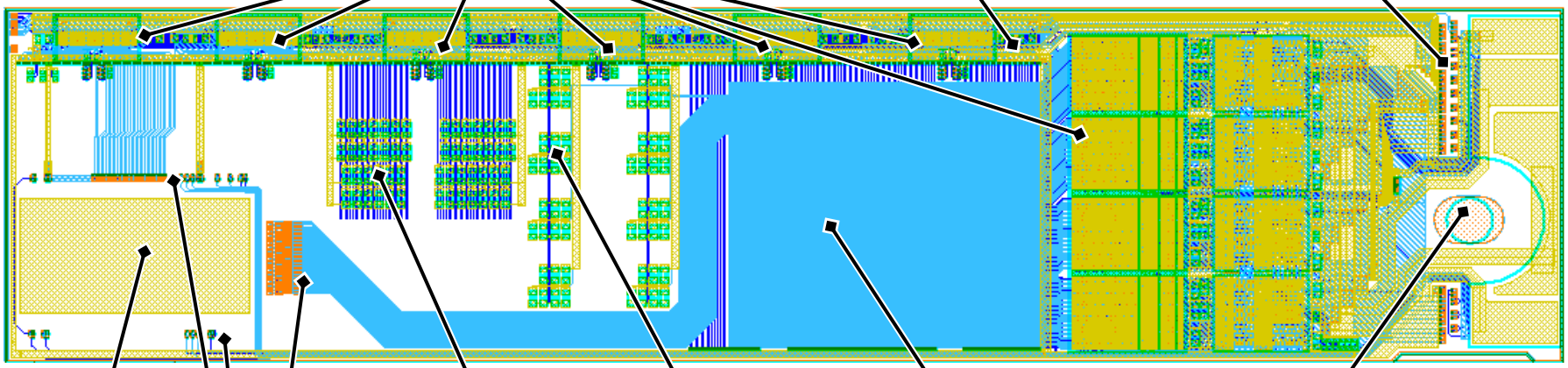

» metal system as close as possible to final, best guess for the layout → same as for final production

↳ full schematic at the periphery for 6 Switcher, 4 DCD, 4 DHP
↳ landing pads for solder bumps on ASICs
↳ space for passives (caps and termination resistors)

↳ I/O and power over 4-layer kapton cable at EOS

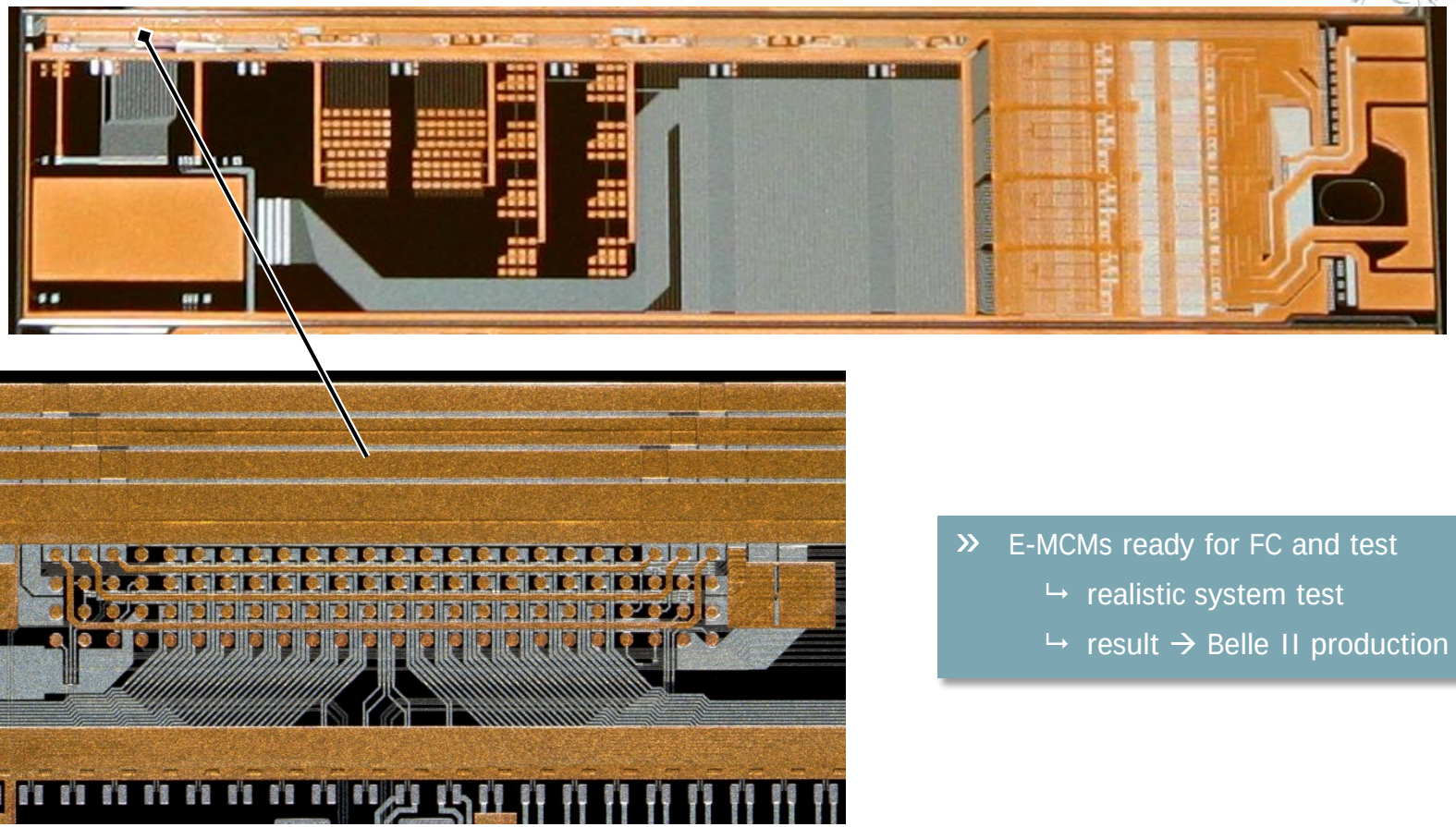
↳ mechanically attached to cooling end-flange

# E-MCM in the “sensitive area”




- basically an electrically active prototype of half-ladder
- even beam tests are possible with small piggy-back matrix
- thinned “sensitive” area planned in second iteration

# Status of the E-MCM



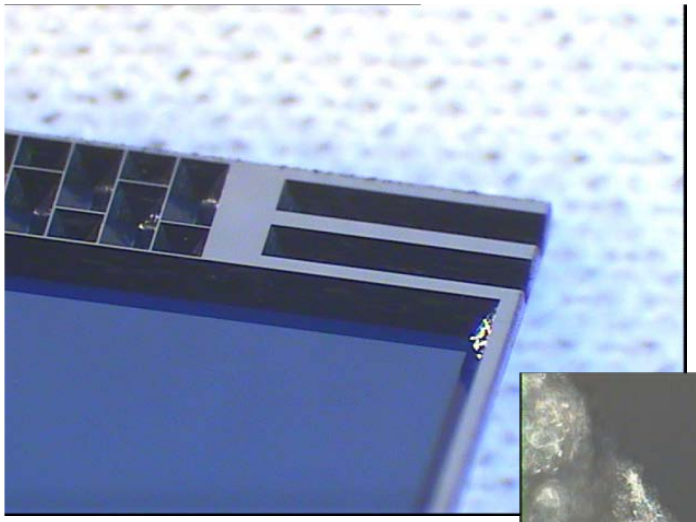
- E-MCMs ready for FC and test
  - realistic system test
  - result → Belle II production

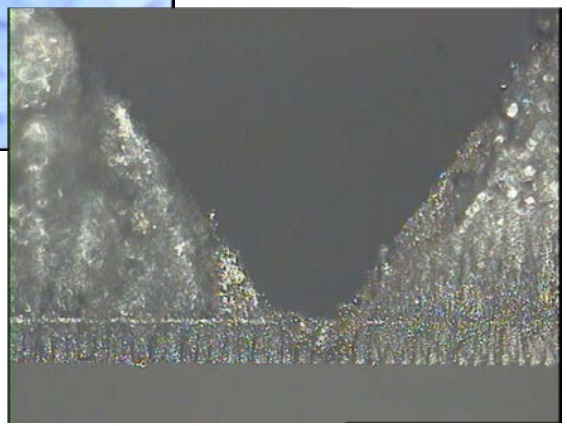
DEPFET technology with 3rd low impedance metal layer!!

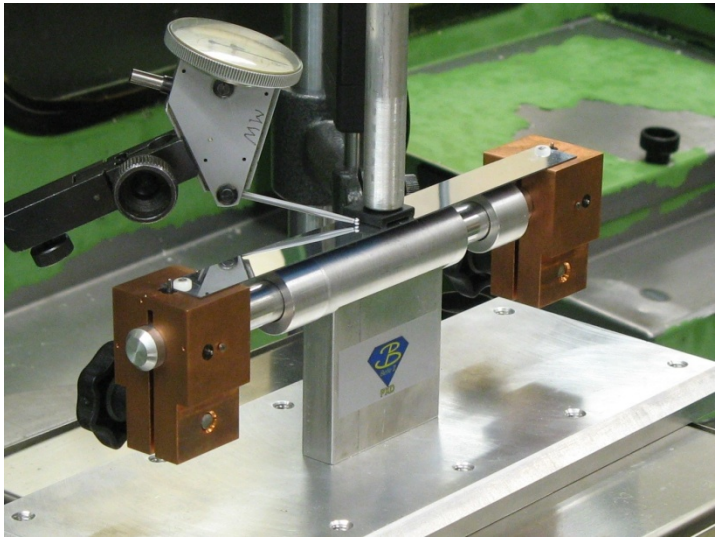
Also for ~20µm pixels: 2-fold read-out → 4-fold → 2x higher frame rate at same row rate

# Thinning step → µ-joint between half-ladders

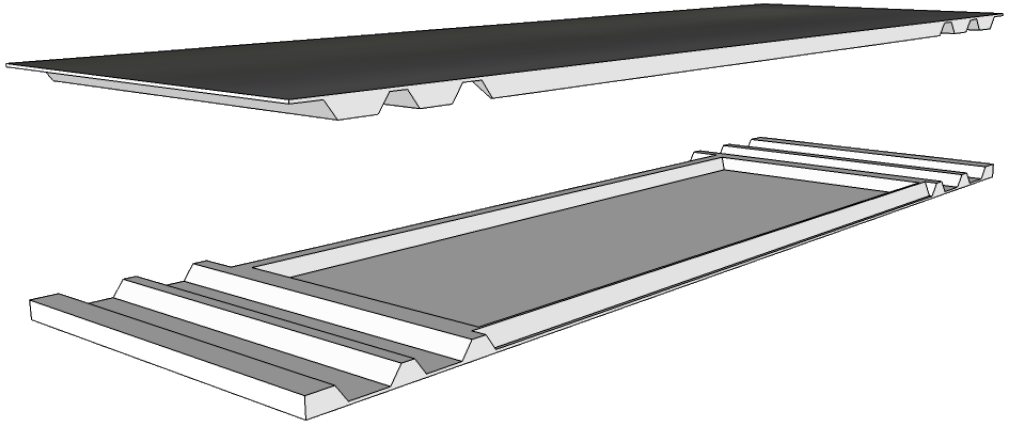
- v-grooves in support silicon
- butt-joint between two half-ladders
- reinforced with 3 ceramic inserts
- 2x300µm dead area per ladder
- mechanical tests → remarkably robust!!
- bowing: up to 1 mm sag (over 10 cm)
- tension: 40 to 60 N, then the Si broke







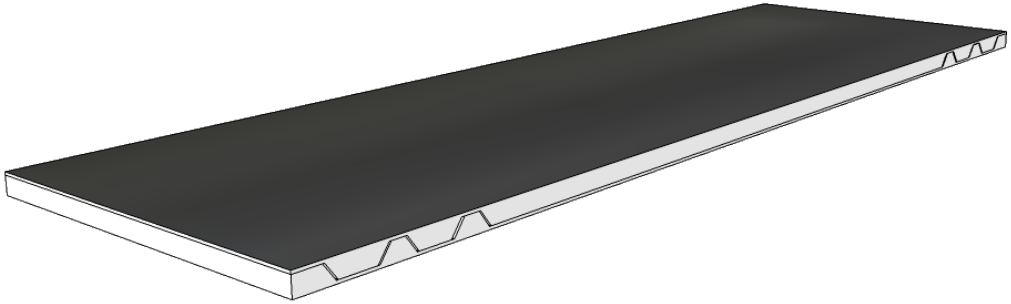
# Thinning step → all-silicon double layers



» Complementary etch grooves in support frames

» same process step as thinning and µ-joint

» Adhesive joint between layers

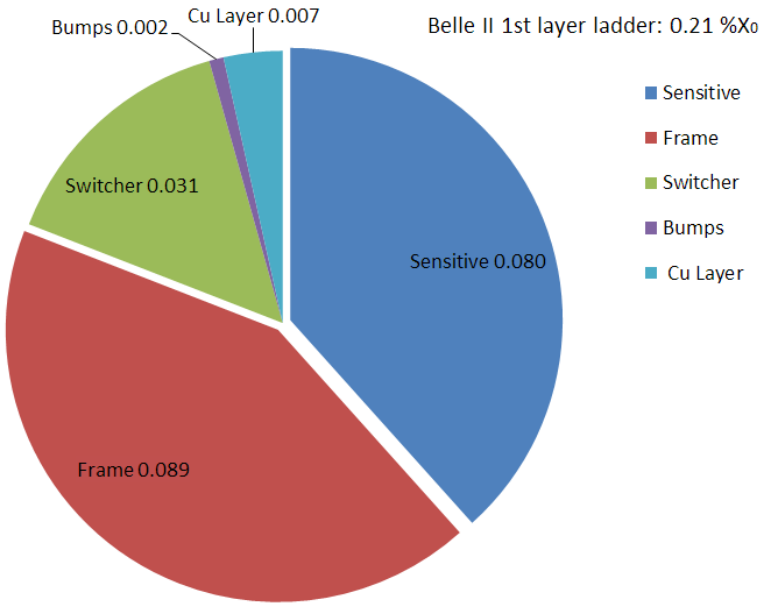


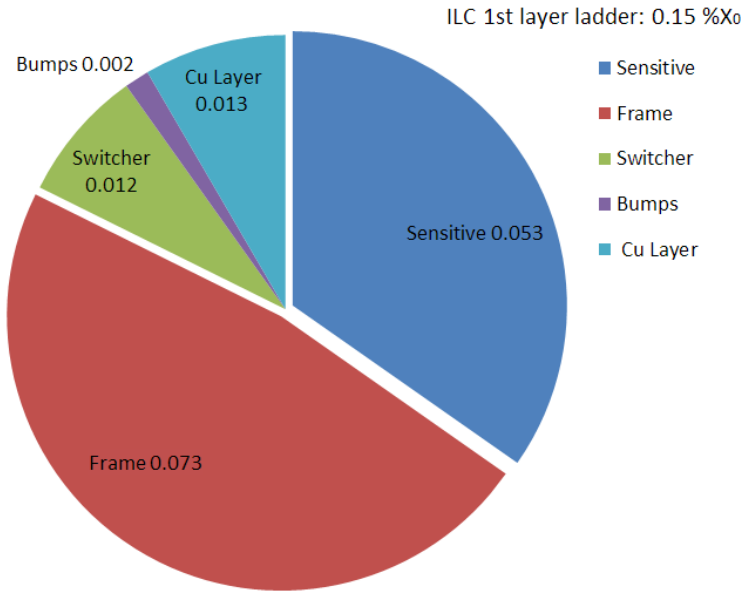
» DEPFET option **not** linked to 5-layer VXD!

» **R&D needed for this**

» single layer ladder engineered to a large extent

# All-silicon module – material budget (single layer)



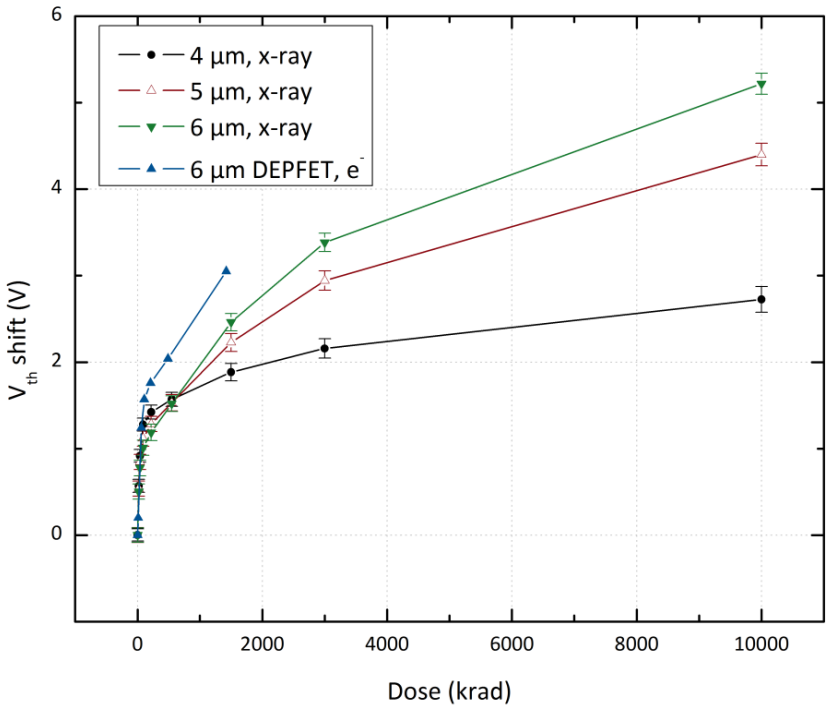

| | Belle II | ILC |
|---|---|---|
| Frame thickness | 525 µm | 450µm |
| Sensitive layer | 75 µm | 50µm |
| Switcher thickness | 500µm | 100µm |
| Cu layer | only on periphery | 50% cover over all |
| Total | 0.21 %X0 | 0.15 %X0 |

# In Summary

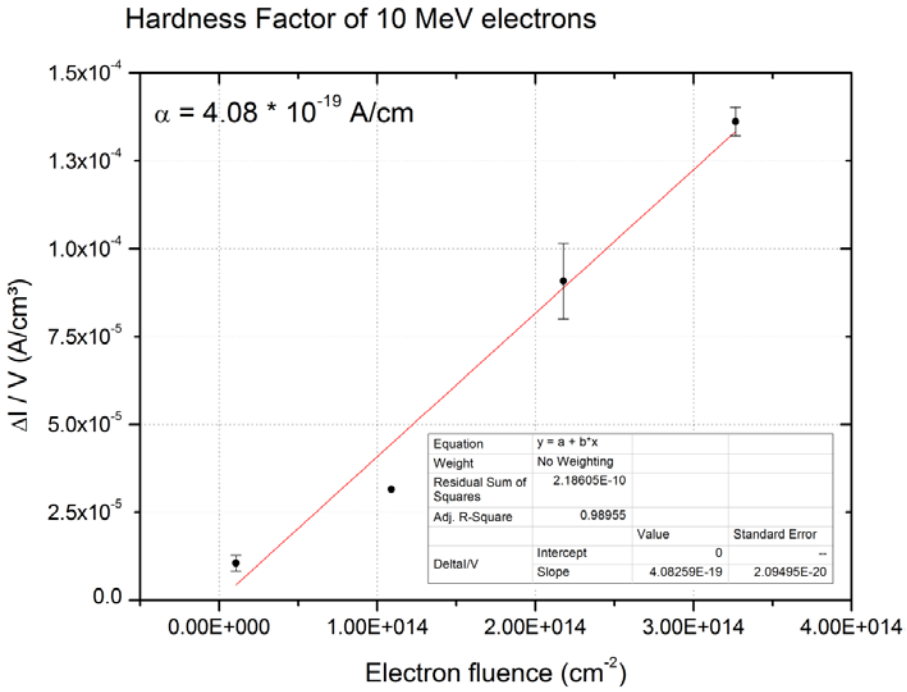
- Test of first thin DEPFETs (PXD6) well advanced
  - beam tests show the expected resolution and S/N at full-speed readout
- First batch of Belle II production of 75µm thin DEPFETs launched
- Full set of auxiliary ASCIs available and tested at full speed (320 MHz, 10MHz row rate)
- test of on- and off-ladder interconnect with dedicated test devices
  - "E-MCM": Third metal layer, flip-chip, kapton attachment... → full system test!
- prospects for the DEPFET at ILC:
  - gain of 2x-4x in speed with optimized pixel layout and 3rd metal layer (→ 1/25µs frame rate)
  - ladder concept for the ILD 5-layer layout can be used as engineered
    - with little R&D material budget down to 0.15 %X0 possible
  - concept for all-silicon double layers shown, DEPFET is not linked with the 5-layer ILD layout!!
- I had to skip:
  - mechanical/thermal measurements on thin ladders ... (gas cooling, vibrations of thin sensors..)
  - radiation tolerance of DEPFETs: irradiation results with 10 MeV electrons (→ backup slides)
  - and many other (important technical!!!) details → ~300 pages Belle II PXD "White Book"
- Paper to be published in IEEE TNS: "DEPFET active pixel detectors for a future linear e+e- collider"

# Electron irradiations

» Compare 10 MeV electrons and x-ray irradiation
» e- irradiation in commercial irradiation facility in Dresden



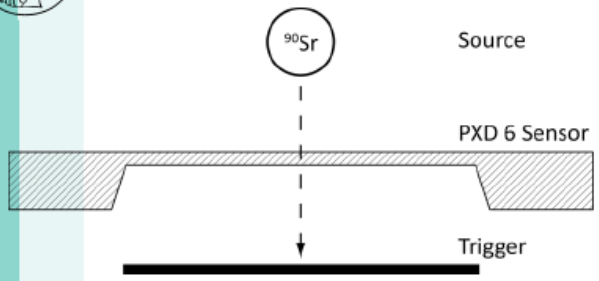

DEPFET $V_{th}$ shift after e- and x-ray irradiation




NIEL damage measured on pin-diodes
α(10 MeV n)=4e-17 (A/cm) (RD50)
α(10 MeV e-)=4e-19 (A/cm) (this work)

„hardeness factor“ e-: 0.01 (0.04 expected)

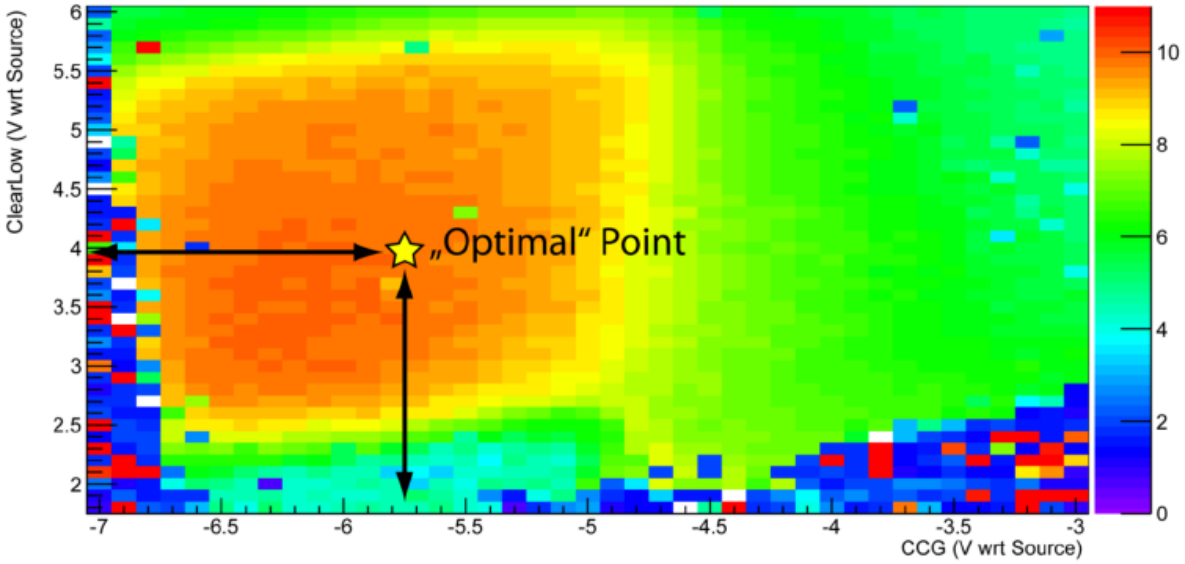
# Electron irradiation of DEPFET matrix




Matrix irradiated with 10 MeV electrons in increasing dose steps.

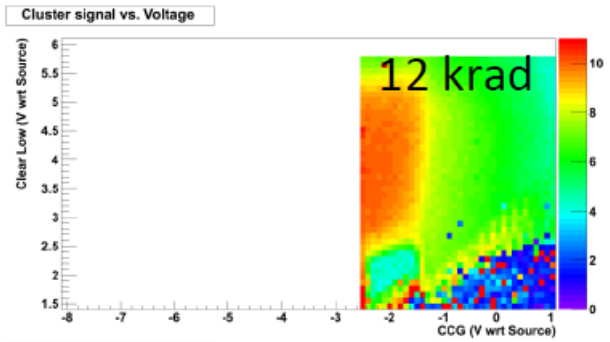
Shift in $V_{th}$ of Clear Gate via a $^{90}$Sr and fitting a Landau to the MPV. Then choose optimal operation point.

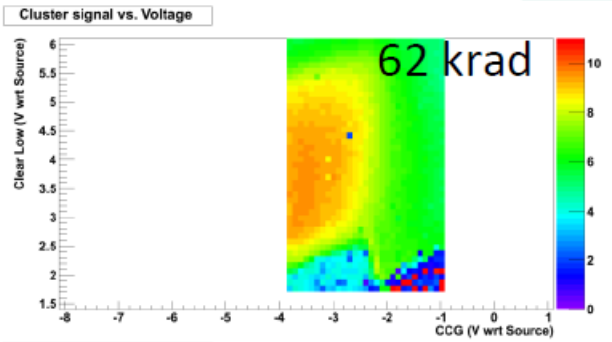
Cluster charge collection in the ClearLow-ClearGate parameter space

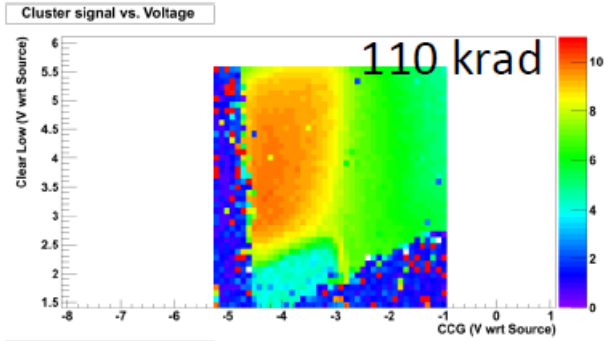


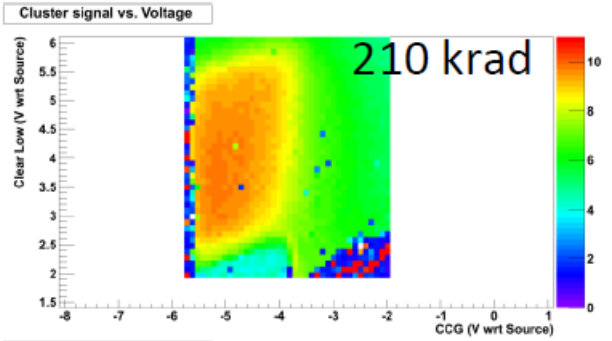

| Dose steps | |
|---|---|
| 0 | krad |
| 12 | krad |
| 62 | krad |
| 110 | krad |
| 210 | krad |
| 490 | krad |
| 1420 | krad |

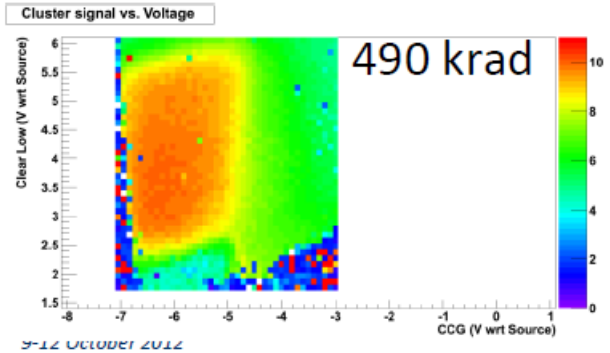
# Evolution of optimal operation point with dose

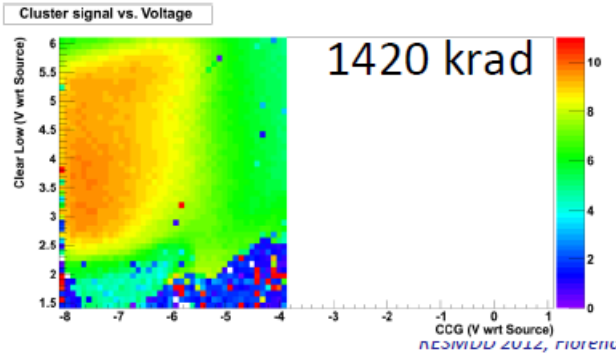


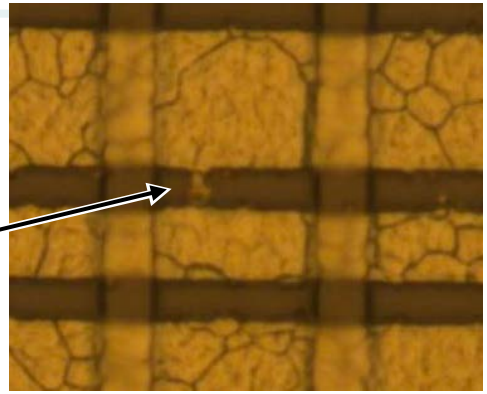



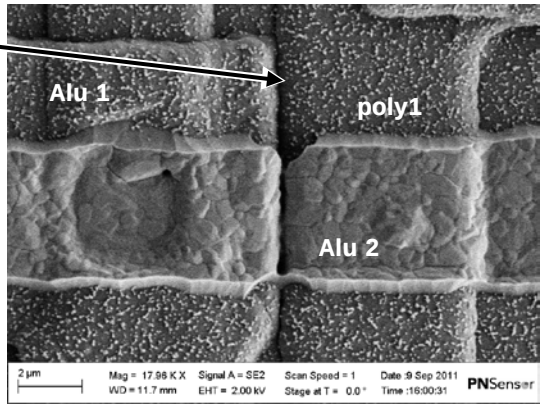



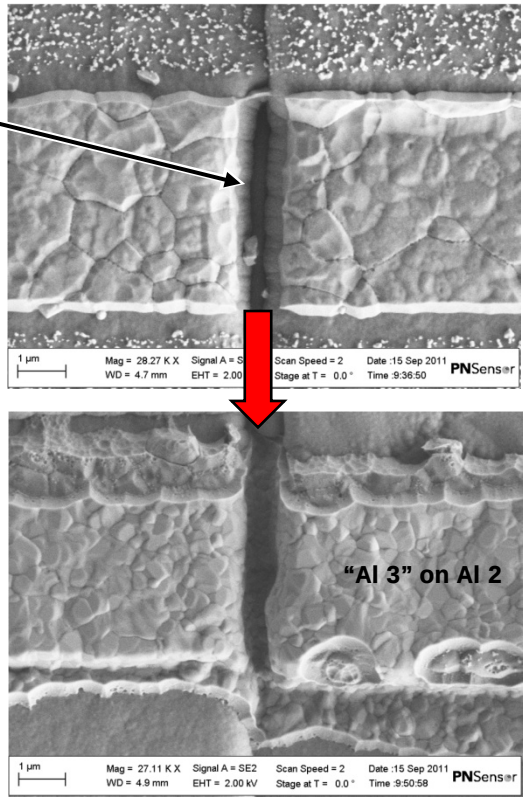



# PXD6 production batches – the yield issue



- PXD6 was split into three batches before 1st metal
  - batch 1: 3 SOI + 1 std.
  - batch 2: 3 SOI + 1 std.
  - batch 3: 2 SOI (modified Al 2 layout for DHP 0.2 and Cu pads)
- lessons learned:
  - batch 1 had shorts in Alu 1 layer
    - ✓ Litho improved in batch 2 and 3
  - batch 1 and 2 had problems with Al 2 during thinning procedure
    - ✓ repair was possible and successful
    - ✓ modify process in batch 3
  - all batches: distance poly1-Al1 to narrow
    - ✓ will be fixed in next production
- 3rd metal in Cu on batch 3 still to be done
- **yield improved drastically during PXD6 processing**
- **main concern remains to be double Alu system!**




| Yield | Batch 1 | Batch 2 (after repair) | Batch 3 |
|---|---|---|---|
| Small matrices | ~30% | >99% | >98% |
| Half ladders | ~6% (1/16) | 25% (4/16) | 50% (4/8) |

(good pixel)

(metal shorts opens)