INSTITUTO TECNOLÓGICO DE ARAGÓN

Base line design for the ILC-FTD sub-detector power distribution system

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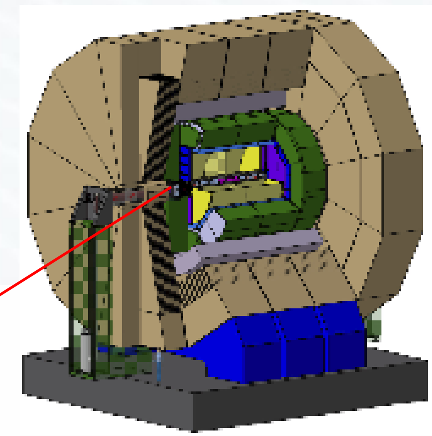
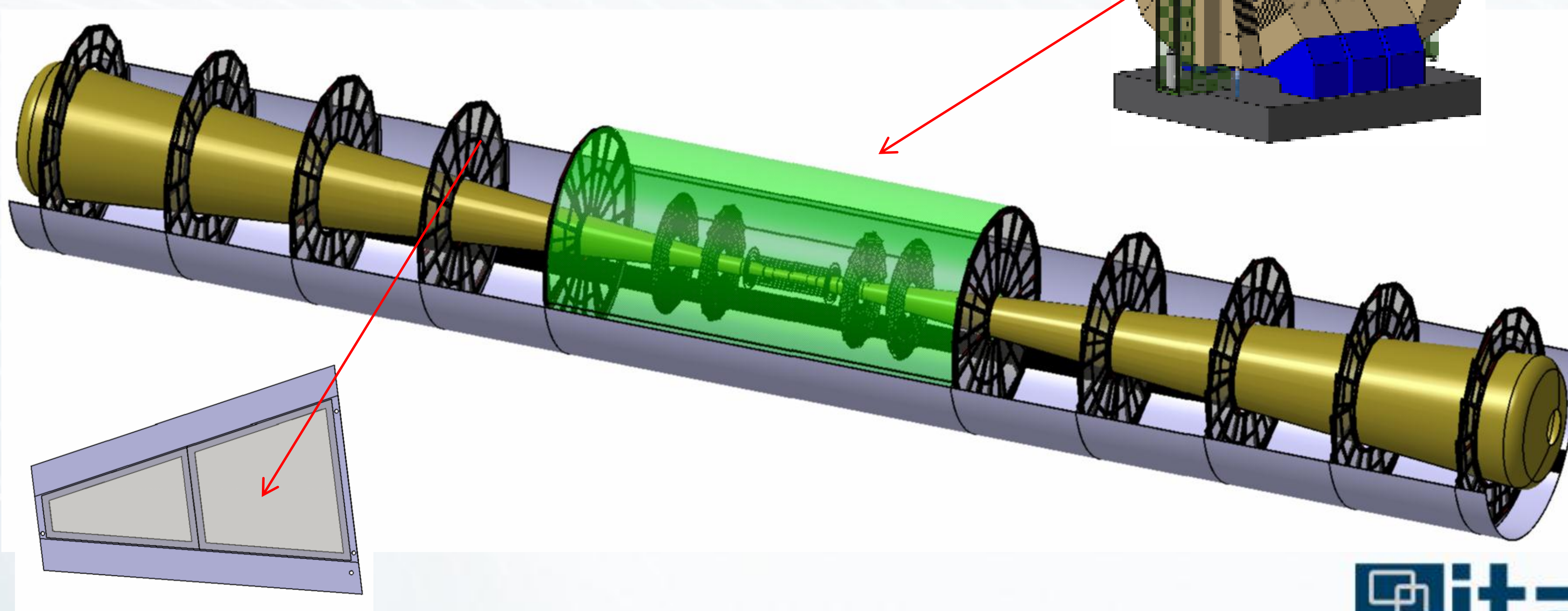
OUTLINE

- 1. Introduction
- 2. Power requirements
- 3. Powering schemes
  - DC-DC converters based power distribution
  - Super-capacitors based power distribution.
- 4.Conclusions

1. Introduction

- The mstrip-FTD system is a silicon strip tracker located in the innermost part of the tracker region of the ILD.
- It consists of 10 disks.
  - Each disk has 16 petals





2. Power requirements

- The ILC accelerator has a duty cycle of 0.5%
  - 1 ms bunch train every 200ms

- If the power demanded by the FEE is synchronized to the bunch train, it helps to save energy
- Several conservative considerations have been assumed in the power distribution operation:
  - A conservative duty cycle operation.
    - 1 ms power up / down
    - 3 ms operation state to stabilize power and operate.
  - During the standby estate .
    - Power decreases to 20%.
  - FTD power consumption based on CMS Tracker upgrade FEE designs.

2. Power requirements

- **CMS Tracker upgrade FEE power consumption:**

Mark Raymon´s calculation for CBC and GBT

  - CBC chip:
    - 128ch – I1.25V – 30mA / I2.5V – 20mA
  - Optical link
    - 1 GBT – Max number of channels: 20480
    - 100% ocupp. – I1.25 – 1000 mA / I2.5V – 280mA (2 W)
- **Estimated power values for FTD FEE:**
  - FTD chip :
    - 256 ch. – I1.5V – 60mA / I2.5V – 40mA (≈ 740 μW/ch)
  - Optical link
    - Max number of channels: 20480
    - 1Channel – I1.5 – 5.13 μA / I2.5V – 14.4μA
  - Power – stand-by status (20 % of max power)

2. Power requirements

- Current consumption of Strip - FTD

	MIDDLE PITCH									
FTD	FTD3		FTD4		FTD5		FTD6		FTD7	
	INN	OUT	INN	OUT	INN	OUT	INN	OUT	INN	OUT
Nº Readout channel	33920	61504	41600	64224	45472	65504	51232	67424	63424	
Chips per petal (256 ch)	24		26		28		29		16	
Optical links per petal	1/2		1/2		1/2		1/2		1/2	
I1.5 (A) per Petal	1.75 / 0.35		1.9 / 0.38		2.05 / 0.41		2.12 / 0.42		1.16 / 0.23	
I2.5 (A) per Petal	1.05 / 0.21		1.13 / 0.23		1.22 / 0.24		1.27 / 0.25		0.7 / 0.14	
I per petal	2.79 / 0.56		3.03 / 0.61		3.26 / 0.65		3.39 / 0.68		1.86 / 0.37	
I per disk	44.6 / 8.9		48.5 / 9.71		52.08 / 10.42		54.19 /10 .84		29.76 /5.95	
TOTAL Mstrip- FTD Current (both sides)			458 A / 91.6 A							

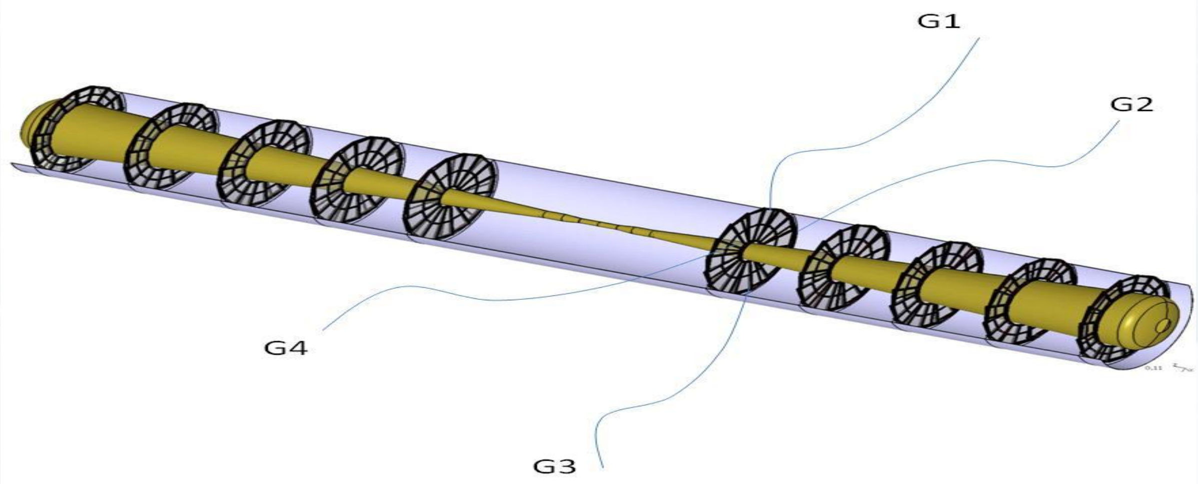
(active / stand-by currents)

3. Powering schemes

- The total Strip-FTD current demanded is:
  - Bunch crossing state 458 A
  - Stand-by state 91.6A
- Several important issues have to be considered during the design of the power system:
  - **Transient phenomena**
  - **EMI phenomena**
  - **Power dissipation effects**
- All these phenomena have an impact on the design of the power supply distribution system
  - Topology
  - Cooling
  - Material budget

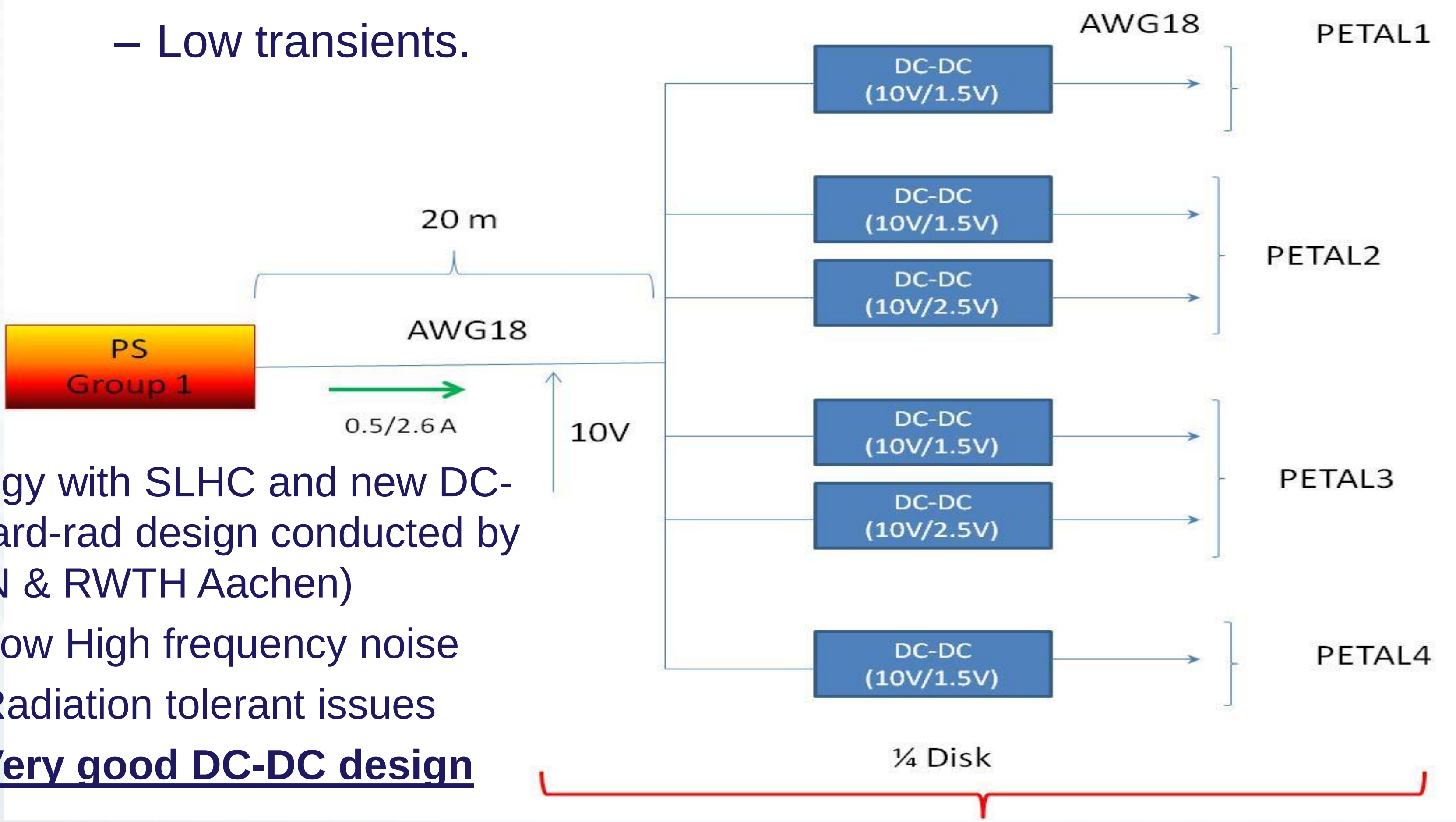
3. Powering schemes

- There are several topologies that may be used for FTD.
  - DC-DC-based power distribution
  - Super-capacitor based power distribution
- Each of them has advantages and disadvantages
  - Both systems are under study.
    - Real measurements
    - Simulations (MATLAB & Cadence tools)
- It has been considered a granularity based on ¼ per disk.



3.1 Powering schemes: DC-DC-based Power System

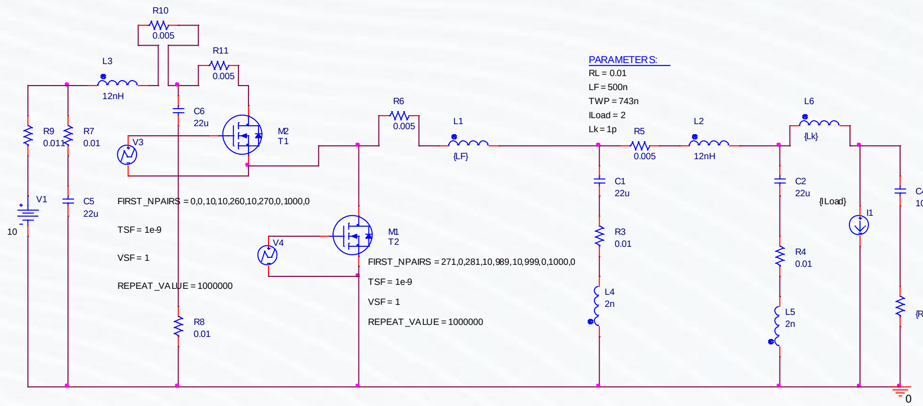
- It is based on the installation of DC-DC converter at FTD level.
  - It absorb transients related to power pulsing system.
    - Low currents before DC-DC due to converter ratio.
      - Low transients.

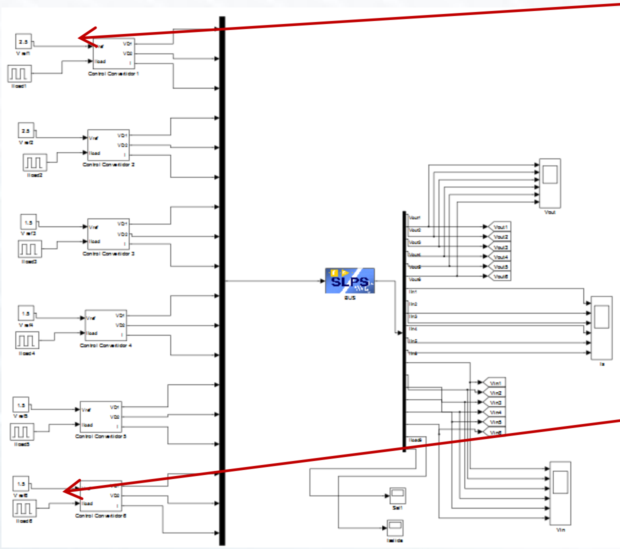


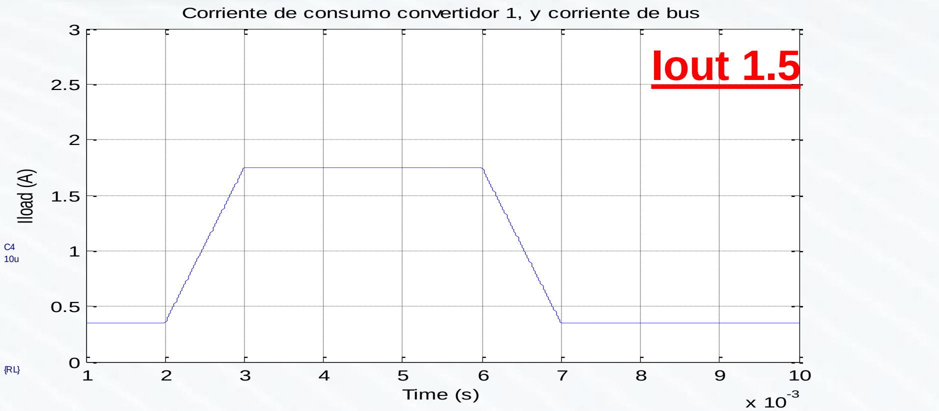
- Synergy with SLHC and new DC-DC hard-rad design conducted by CERN & RWTH Aachen)
  - ➢ Low High frequency noise
  - ➢ Radiation tolerant issues
  - ➢ **Very good DC-DC design**

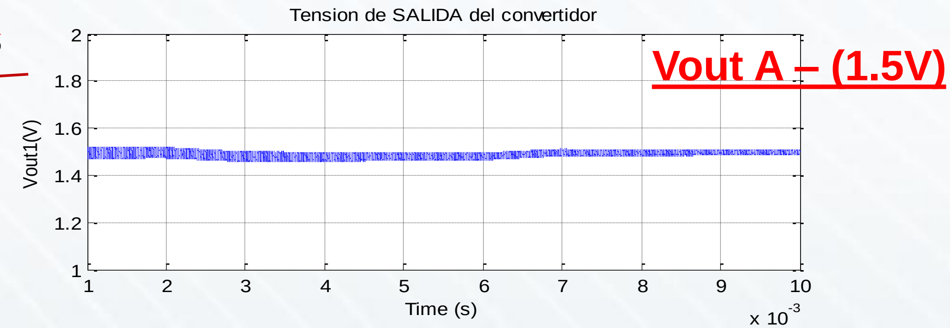
3.1 Powering schemes: DC-DC-based Power System

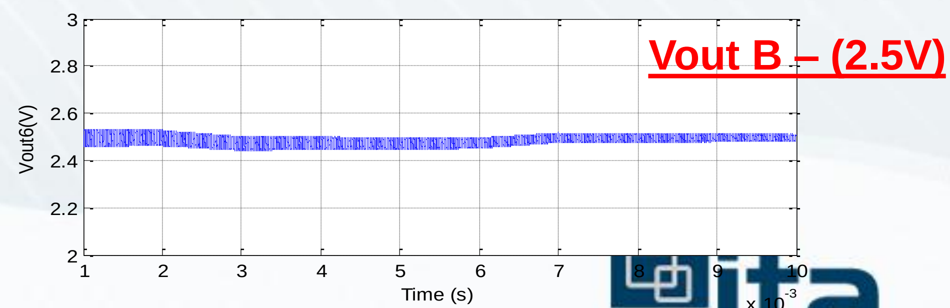
- A Matlab – Pspice model has been prepared to study the power distribution











2.1 Powering schemes: DC-DC-based Power System

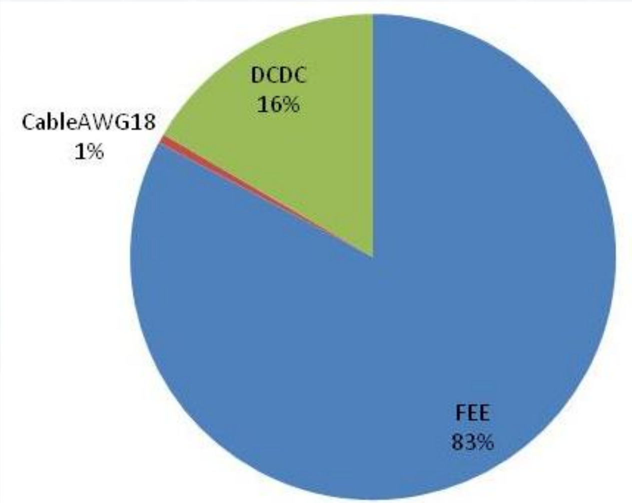
- Example (1/4 disk) : Power values per **group FTD 6+:**
  - FTD level – 4 petals:
    - 6 DC-DC converters
      - 4 DC-DC (10V - 1.5V) – 2.1A / 0.4A
      - 2 DC- DC (10V - 2.5V) –2.5A / 0.5A
    - Short cabling – Low current (low transients) – AWG18
  - Outside FTD (1cable per ¼ disk)
    - Max out current per DC-DC less than 3 A (2.5A /0.5A)
      - Transients attenuated by the DC-DC
    - Primary power unit
      - Imax=3 A / V= 12V – Power required > 36 W
  - **TOTAL INSTALED POWER REQUIRED FOR FTD**
    - 1.4kW
- A similar number of HV cable will be considered to keep the same granularity
  - 1 HV cable and HV power unit per ¼ disk
  - It will drive a few mA

2.1 Powering schemes: DC-DC-based Power System

- Power dissipation per ILC cycle (W): ***DC-DC converter efficiency : 80%**

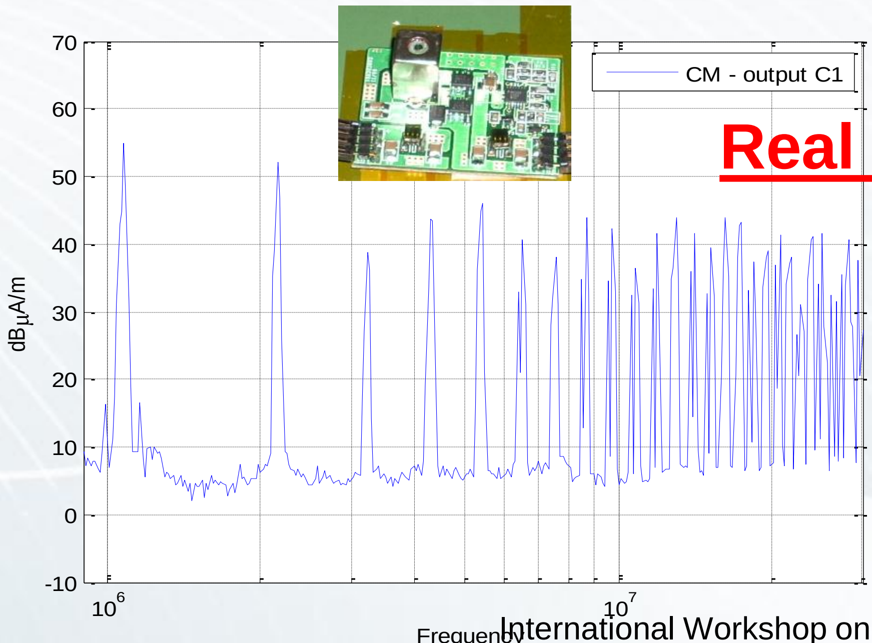
Group	FTD 3+	FTD4+	FTD5+	FTD6+	FTD7+
FEE	4.6	5	5.4	5.6	3
CABLE	0.02	0.033	0.039	0.041	0.012
DCDC*	0.92	1	1.07	1.11	0.61
TOTAL (1/4)	5.55	6.04	6.48	6.74	3.69
TOTAL DISK	22	24.1	26	27	14.7
External cable (20m)	0.23	0.27	0.31	0.34	0.1

	POWER (W)
HALF SIDE	114 W
TOTAL FTD	228 W

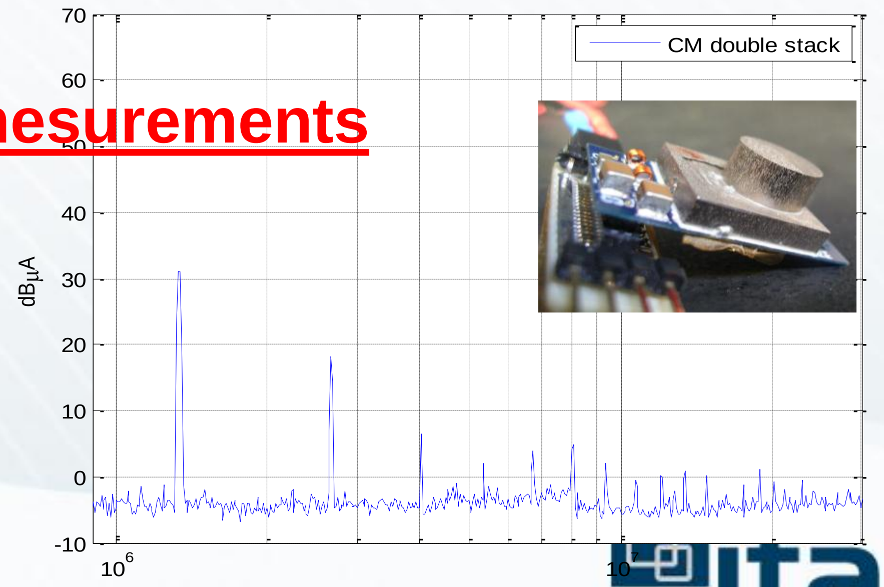


3.1 Powering schemes: DC-DC-based Power System

- Important topics associated with DC-DC converters
  - Material
    - Shielding – Main inductor.
  - Dynamic
    - Dynamic behavior: Negative impedance & Transients
  - EMI phenomena (Noise)
    - Conducted & Radiated



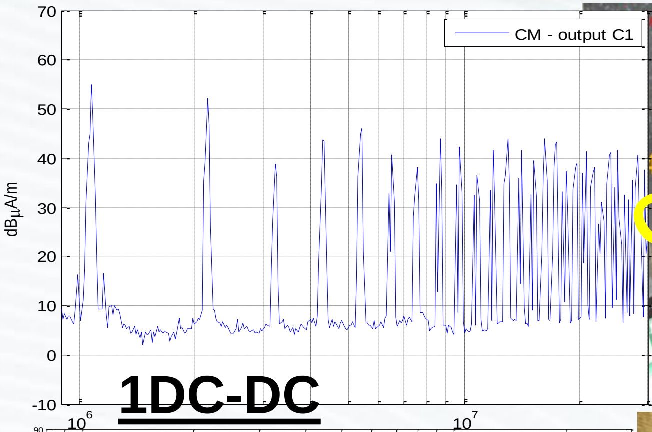
Real mesurements

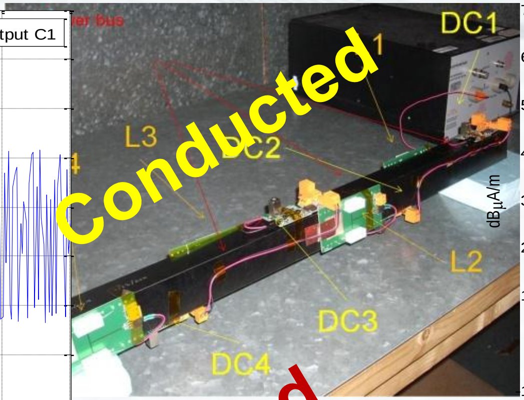


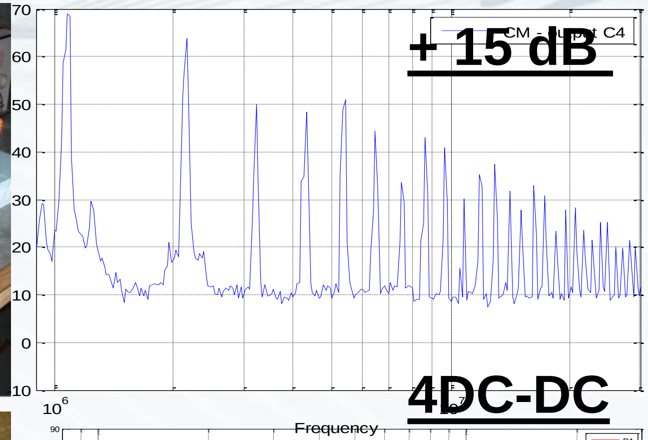
3.1 Powering schemes: DC-DC-based Power System

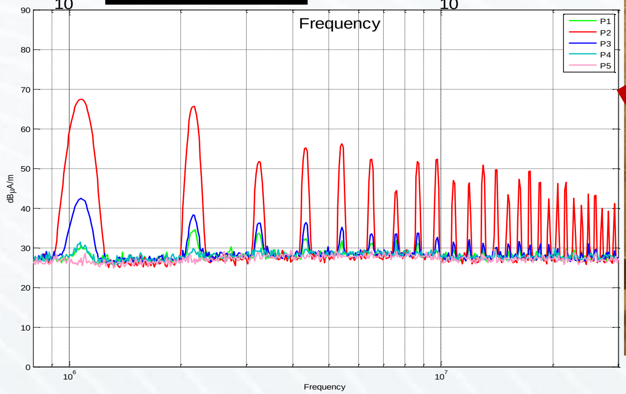
- Increasing the number of units - Increase noise locally

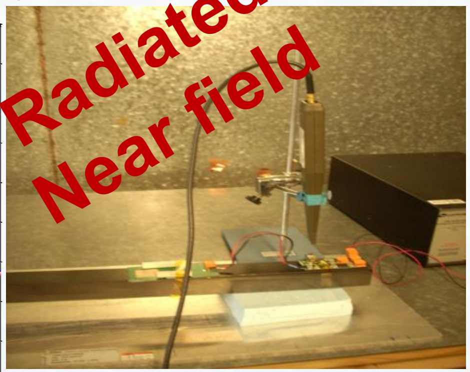
(Real mesurements (SLHC)

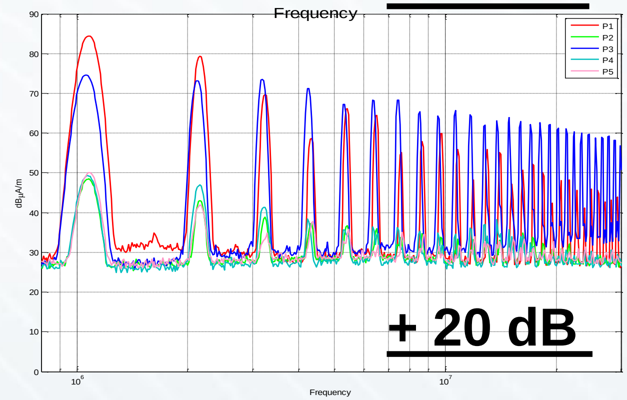




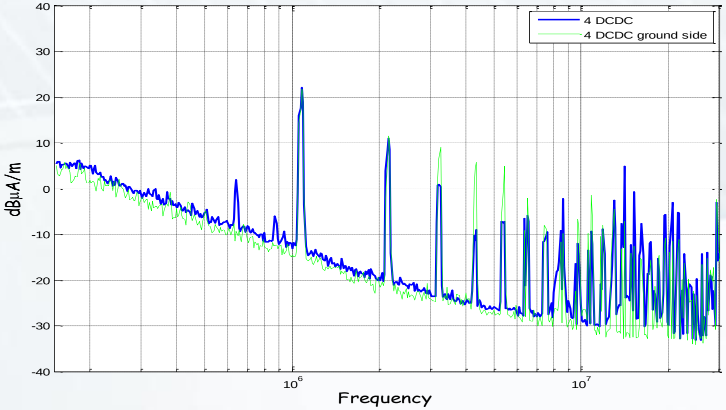






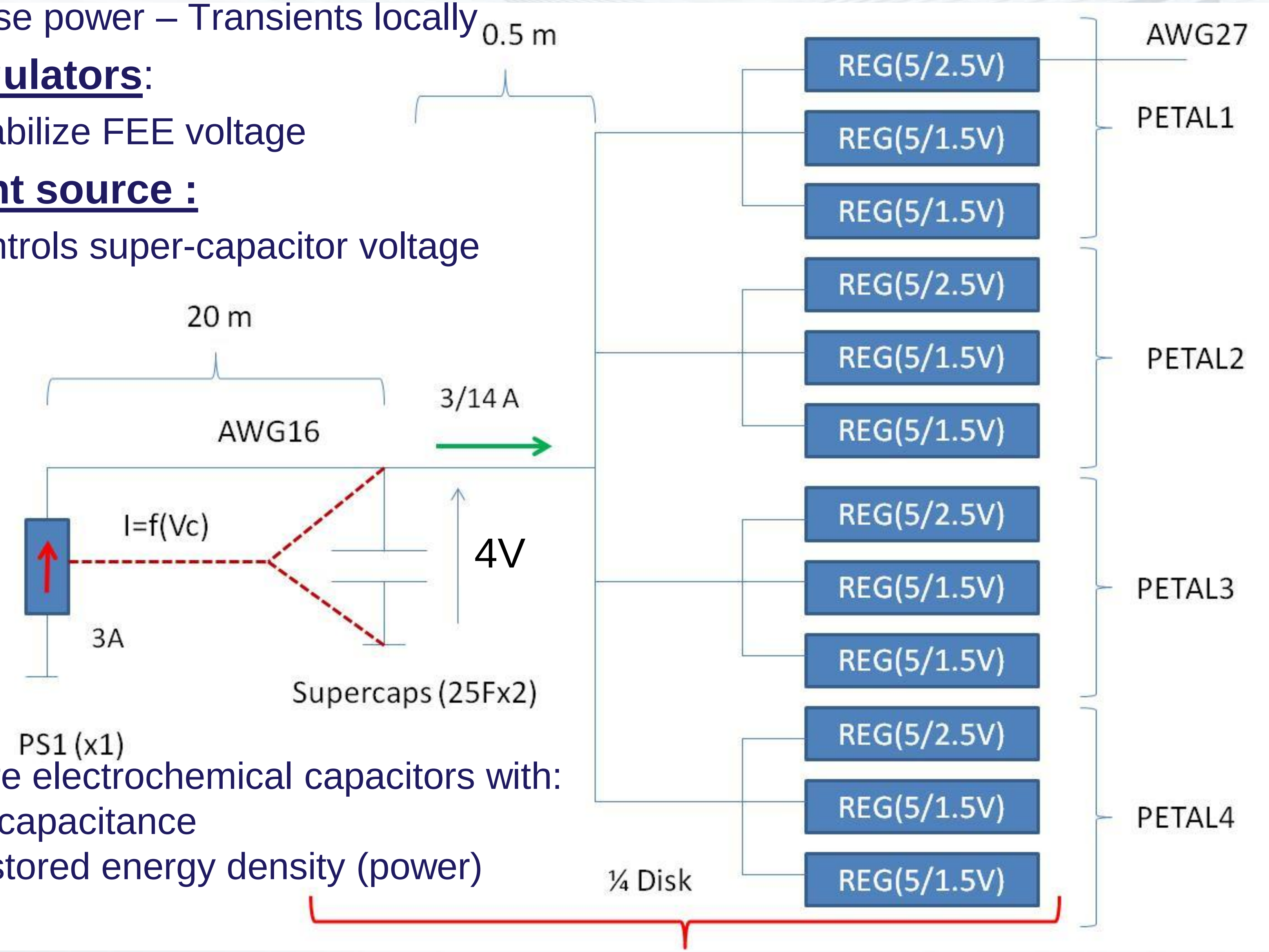


Radiated
Far field
No change



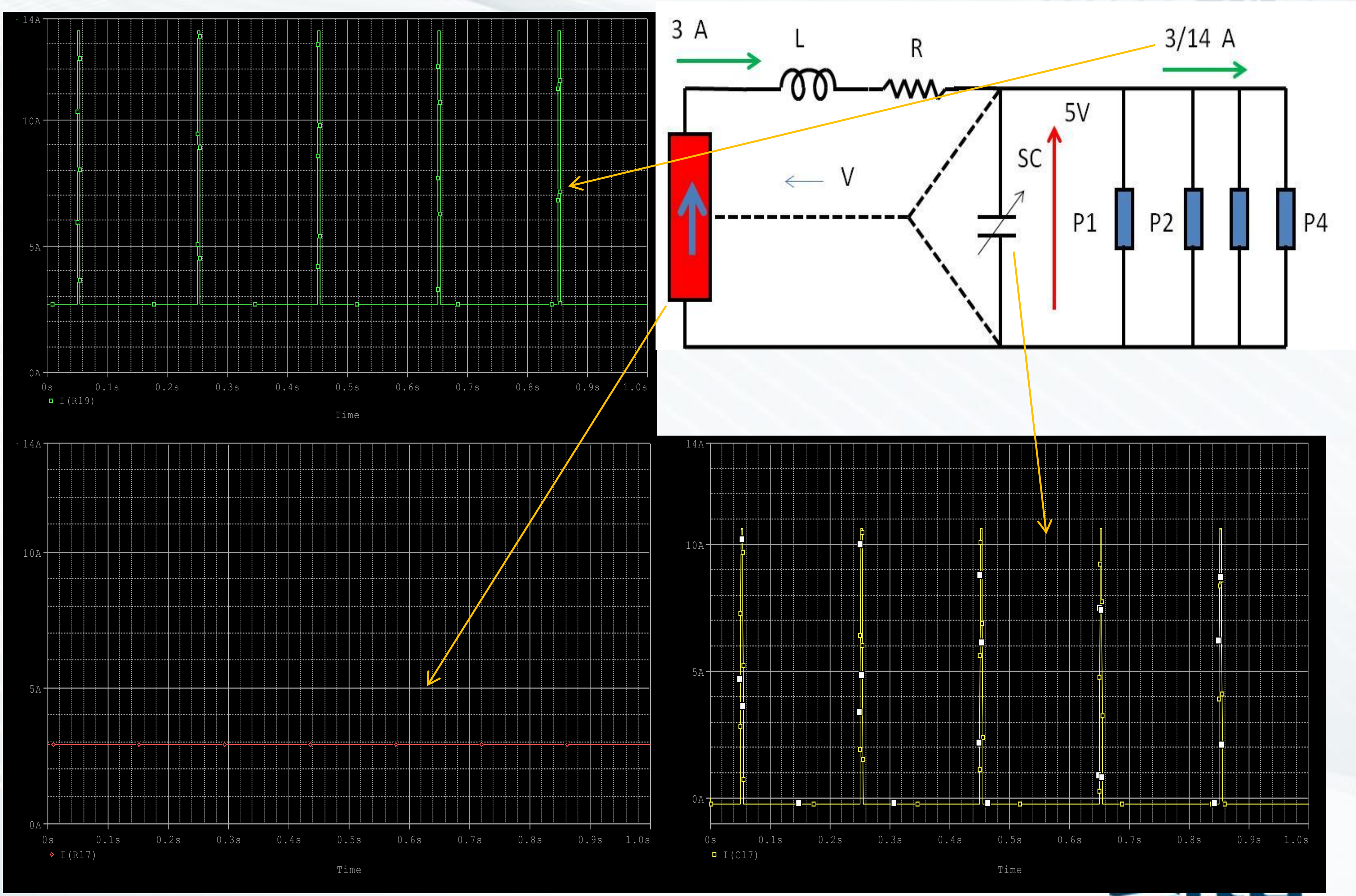
3.2 Powering schemes: Supercapacitor based PS

- **Supercapacitors:**
  - Pulse power – Transients locally
- **LV regulators**:
  - Stabilize FEE voltage
- **Current source :**
  - Controls super-capacitor voltage



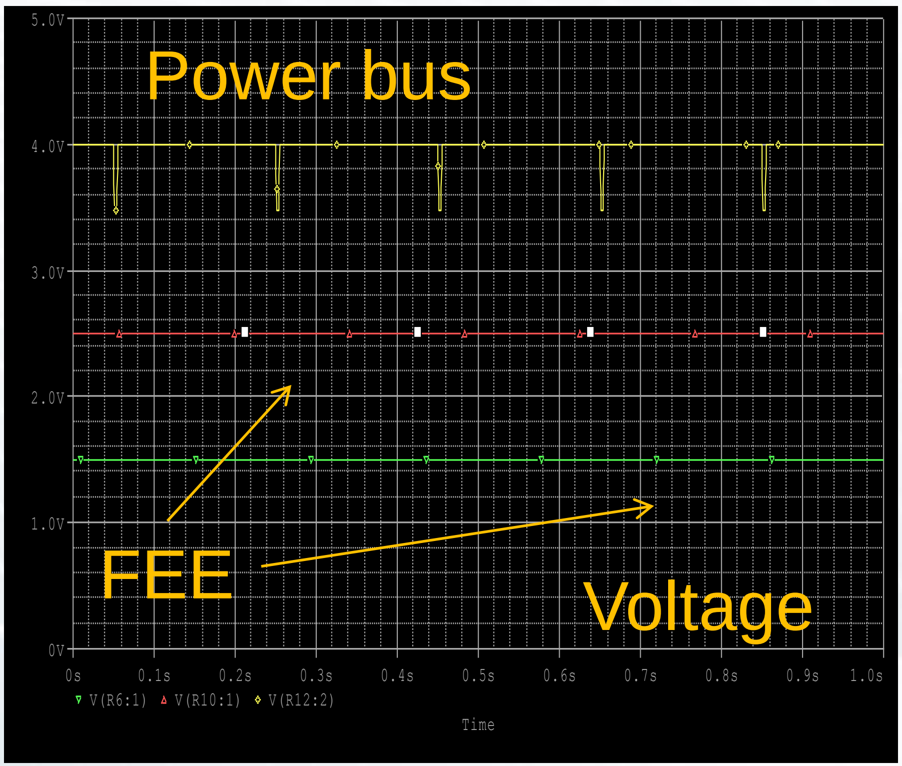
- The SC are electrochemical capacitors with:
  - high capacitance
  - high stored energy density (power)

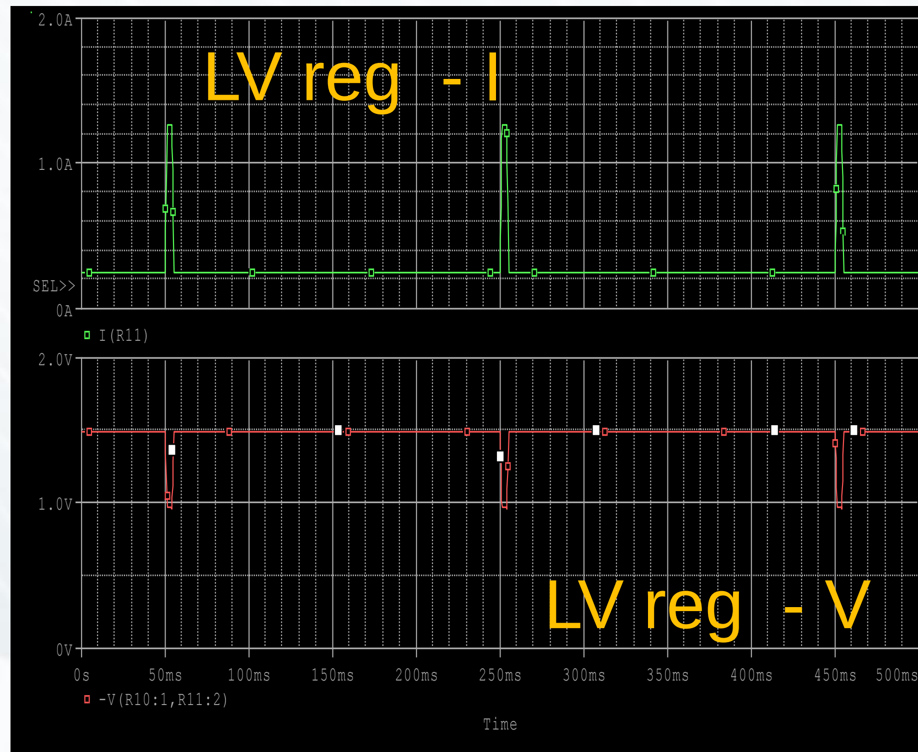
3.2 Powering schemes: Supercapacitor based PS



3.2 Powering schemes: Supercapacitor based PS

- Each pulse generates a voltage dip
  - It is mainly influenced by the ESR of the super-capacitors
    - Line impedance, too.
- Transient can be easily absorbed by the LV regulator
  - It should be a RAD tolerant component
- The voltage dips helps to decrease the power dissipated by LV reg.





3.2 Powering schemes: Supercapacitor based PS

- The high capacitance has two advantages:
  - It will protects the system in case mains failure – Similar to UPS
    - It helps shutdown the system in a controlled way.
  - The dynamic response of primary power unit may be very slow
    - Remote regulation of the supercap voltage will be easy

- The duration of the shut-down capability will depend on :
  - Capacitance
  - Voltage

International Workshop on Future Linear Colliders (LCWS12)
University of Texas, October 2012

3.2 Powering schemes: Supercapacitor based PS

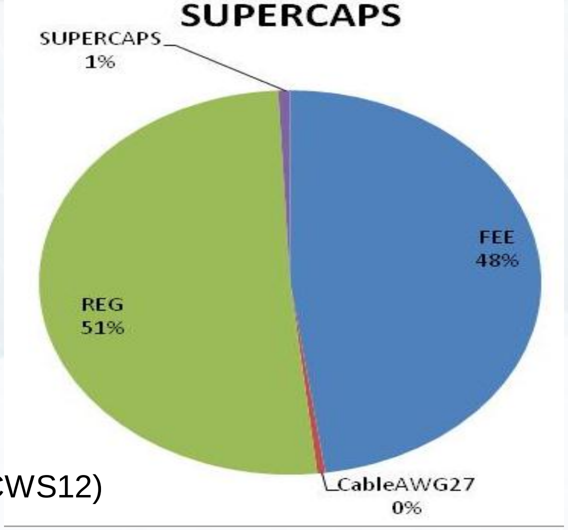
- Power values per ¼ disk (power group 6)
  - Routing Inside each petal
    - 3 Regulators
      - 2 REG (4V -1.5V) / 1. A Pk – 0.21A
      - 1 REG (4V- 2.5V) / 1.2 A Pk – 0.25A
    - Short cabling – Less than 0.2 meter (low voltage drop)
  - Per Group- ¼ disk
    - 2 Super-capacitors per (1/4 disk) – C=25 F / V=4 V / Imax=11 A /Imin≈0
    - 1 Cable per disk
    - Max out current per cable around 2/3 A (defined by FEE stand-by)
  - Primary power unit
    - I max = 3 A / V ≈ 4V – Power = 12W
  - **Total installed power required for FTD**
    - Power – 480 W
- A similar number of HV cable will be considered to keep the same granularity
  - 1 HV cable and HV power unit per ¼ disk

3.2 Powering schemes: Supercapacitor based PS

- Power dissipated per ILC cycle (W):

Group	FTD 3+	FTD4+	FTD5+	FTD6+	FTD7+
FEE	4.6	5	5.4	5.6	3
CABLE AWG 27	0.04	0.04	0.05	0.06	0.02
LV REG	4.9	5.41	5.74	5.96	3.24
SUPERCAPS	0.06	0.072	0.083	0.089	0.027
TOTAL (1/4)	9.63	10.6	11.3	11.7	6.4
TOTAL DISK	38.5	42.1	45	46.5	25.5
External cable (20m) – AWG 16	2.92	3.515	4	4.4	1.26

	POWER (W)
HALF SIDE	197 W
TOTAL FTD	**395 W**

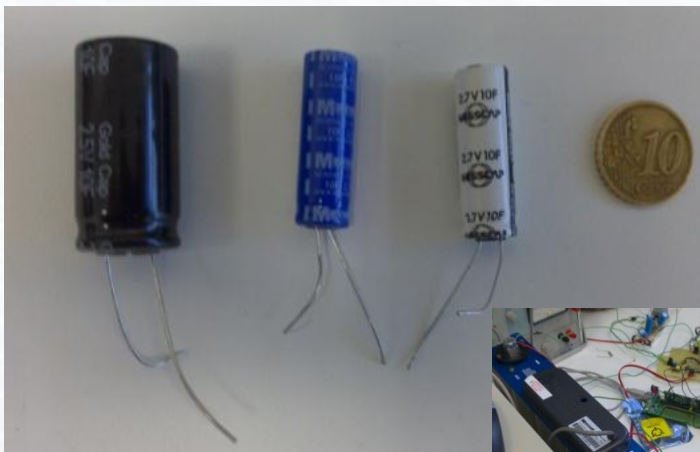


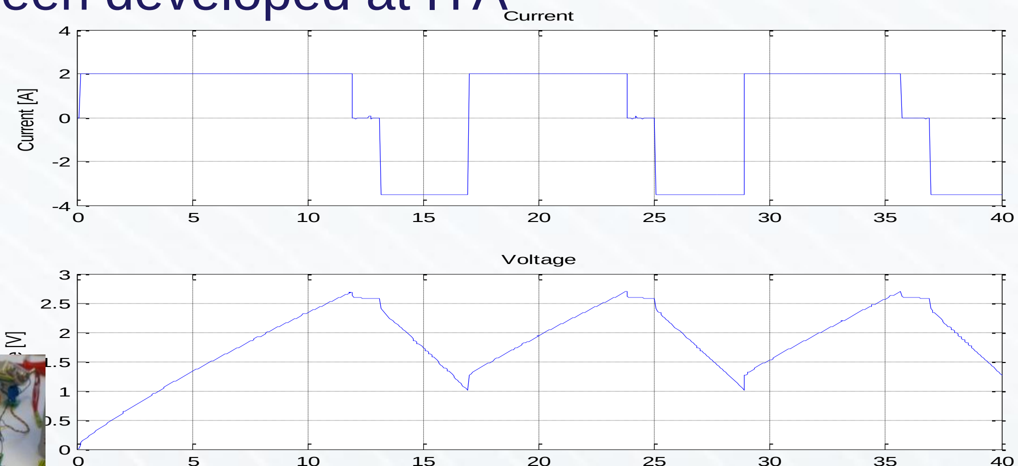
3.2 Powering schemes: Supercapacitor based PS

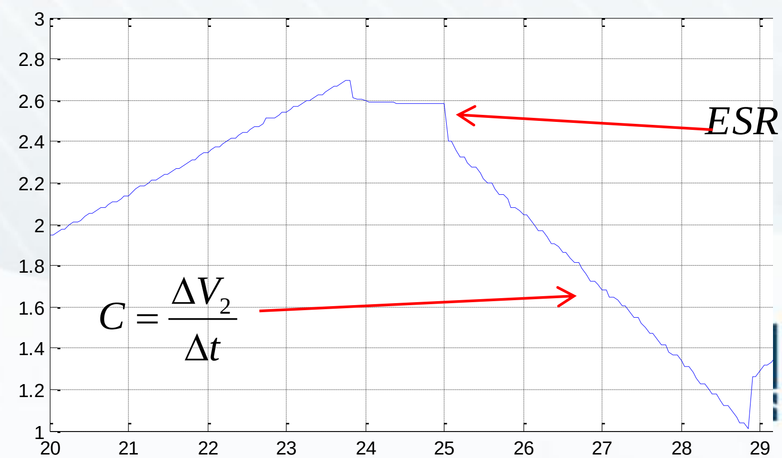
- The most important element is the super-capacitors.
  - It is new for HEP but not for industrial applications
- There are two elements that has to be analyzed in detail for HEP applications
  - Radiation issues
  - Cycling issues.
- Radiation issues
  - Type of radiation: Gammas & electrons
  - Total dose : Around 2 MRAd.
- Cycling issues (Reliability).
  - Super-capacitor should be able to operate more that 10 million of cycle per year (DC-DC too)
- A detailed test plan is on going to study both effects

3.2 Powering schemes: Supercapacitor based PS

- Super-caps degradation is characterized by two effects
  - ESR degradation
  - Capacitive degradation
- This parameters will be characterized via constant current test
  - A power converter has been developed at ITA







$$ESR = \frac{\Delta V_1}{I}$$

$$C = \frac{\Delta V_2}{\Delta t}$$

	ESR	C
Nesscap	0.033	9.7
Maxwell	0.058	10.4
Pannasonic	0.037	15.5

(Real mesurements)

4. Conclusions

- A general overview of the two power supply distribution system for FTD has been presented
  - Each of them has some advantages and disadvantages

	DC-DC	Super-caps
Power dissipation	228 W	395 W
EMI phenomena	Yes	No*
RAD tolerant	Yes	?
Material budget	(240 DC-DC) ?	(80 SC) ?
Reliability	?	?
Power pulse applications	Not frequent	Yes
Installed power	1.4 kW	0.48 kW
Primary PS	≈ 36 W	≈ 15 W
Mains protection (UPS effect)	No	Yes

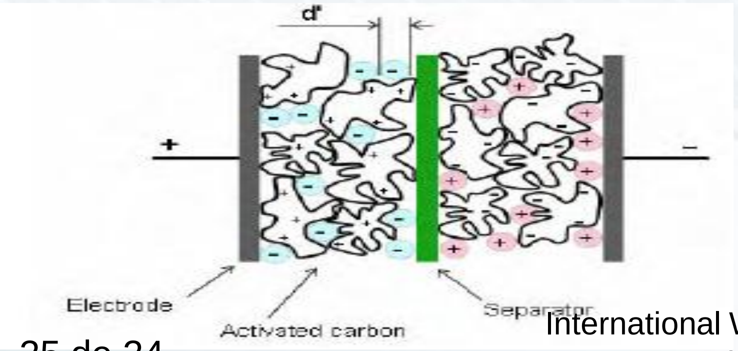
4. Conclusions

- Future plans
  - Super-capacitor option :
    - Radiation effects on super-capacitor : Test campaign
    - Reliability issues : Power cycling effects
    - Material budget
  - DC-DC option:
    - It is plan to follow the development of DC-DC converters RAD and magnetic field tolerant.
      - SLHC project – CERN & RWTH Aachen
    - Simulation model improvement - Transients
    - Power cycling effects
    - Material budget
- These topologies may be extended to any other sub-systems

BACKUP SLIDES

3.2 Powering schemes: Supercapacitor based PS

- It is based on the installation of super-capacitor at FTD level
  - It will keep the transients – high currents locally
- The super-capacitors are electrochemical capacitors with high capacitance and high stored energy density (power)
  - Double layer capacitor (DLC) is the most common one
    - ALU (anode)- active carbon -SEP- active carbon - ALU(catode)



- Low nominal voltage - (2.7V max),
- No memory effect & High efficiency
- State of charge depends on voltage and capacity. C = f(V)
- It may stand millions of cycles
- Temperature operation:
  - Between –35 ºC y 65 ºC