Universitat de Barcelona

Design of a FE ASIC in TSMC-65nm for Si tracking at the ILC

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International Workshop on Future Linear Colliders 2012

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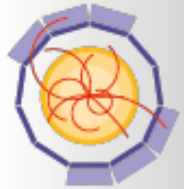


AIDA

Advanced European Infrastructures for Detectors at Accelerators

Co-funded by the European Commission within FP7 Capacities, GA 262025

Started Feb'11, 4 years

80 institutes and laboratories from 23 European countries

26 million Euro (8 million Euros from the EU)

Coordinated by CERN

Spainsh participation: CSIC (IFIC, IFCA, CNM), CIEMAT, IFAE, USC, UB

AIDA

Advanced European Infrastructures for Detectors at Accelerators

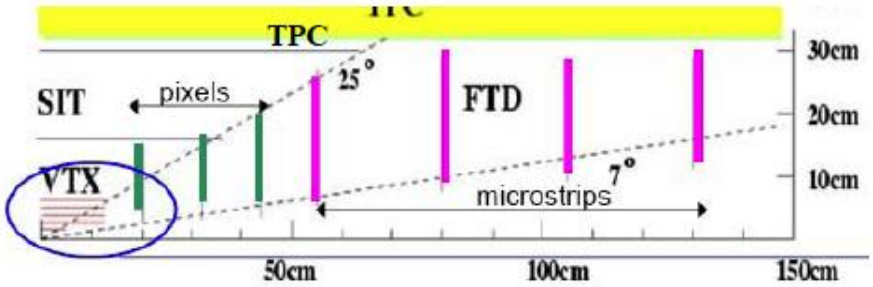
Co-funded by the European Commission within FP7 Capacities, GA 262025

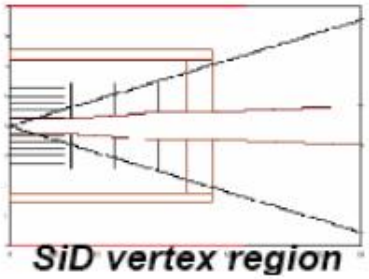
WP9.4 Silicon Tracking

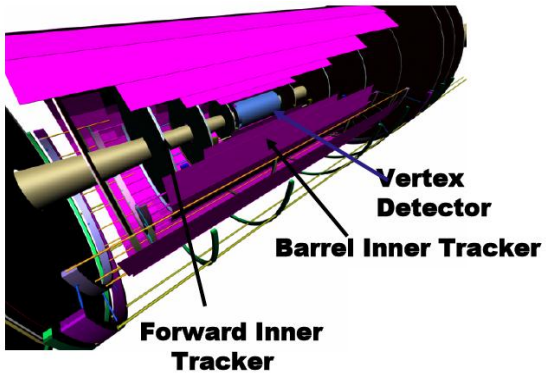
Coordinated by Thomas Bergauer (HEPHY)

Goal is the creation of a multi-layer micro-strip detector coverage for the calorimeter infrastructure (Task 9.5) to provide a precise entry point of charged particle

- The calorimeter infrastructure of task 9.5 will be preceded by several layers of Silicon micro-strip detectors to provide a precise entry point over a large area.
- Finely segmented and thin Silicon micro-strip detectors will be designed and procured by the participating institutes.
- Baseline design system with readout with APV25. New readout chip designed by UB targetted for longer shaping time.







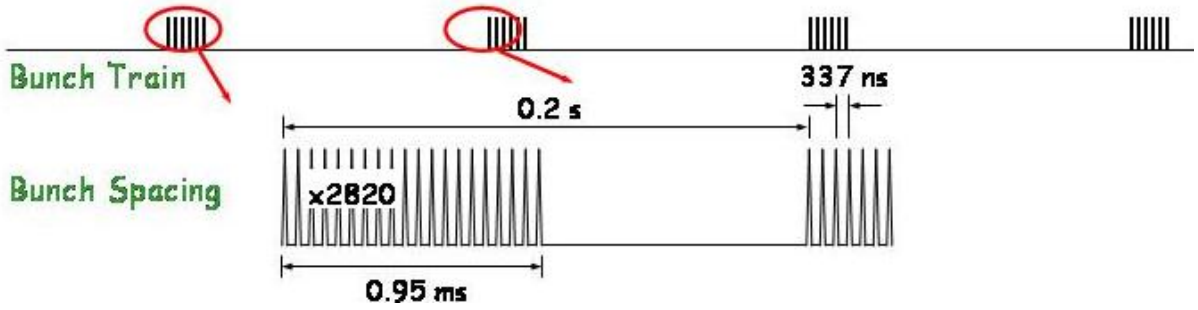
The Si tracking system:

a few 100m^2, a few 10^6 strips

Events tagged every bunch (300ns) during the overall train (1 ms)

Data taking/pre-processing ~ 200 ms

Occupancy: < a few %



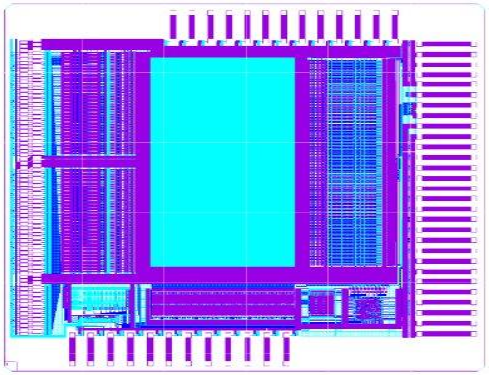
SiIC Silicon µstrip Sensor Baseline

– a few 10^6 Silicon strips 10-60 cm long
– p-on-n sensors: n-bulk material, p+ implants for strips
– high resistivity (5-10 kOhm cm)
– Readout strip pitch of 50µm (intermediate strips in between - 25µm pitch)
– Thickness around 100-300µm, mostly limited by readout chip capabilities (S/N ratio)
– Low current: <1nA per strip
– Baseline for inner layers:6” inch, Double sided, AC coupled
– Baseline for outer layers:8” (12”?) inch, Single sided, Preferably DC coupled

SiLC Sensors from HPK

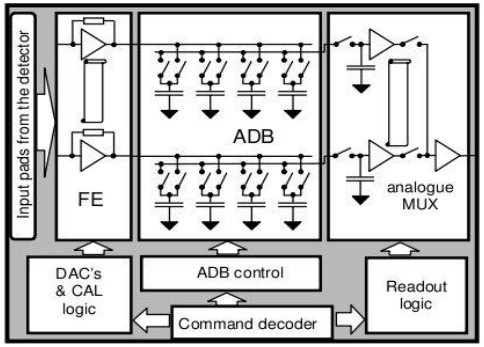
Similar HEP detectors

APV25, CMS, 0.25µm, 128 channels, Slow frontend, deconvolution mode:



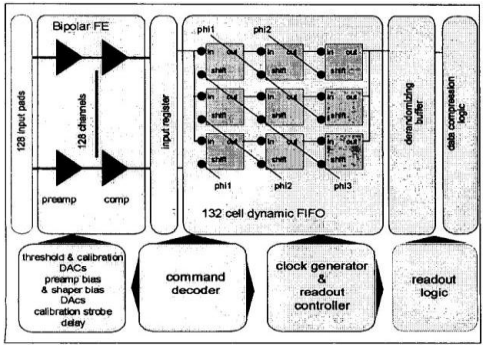
L.L.Jones et al., “The APV25 Deep Submicron Readout Chip for CMS Detectors”

SCTA128, general purpose, DMILL process, 128 channels , fast bipolar front-end



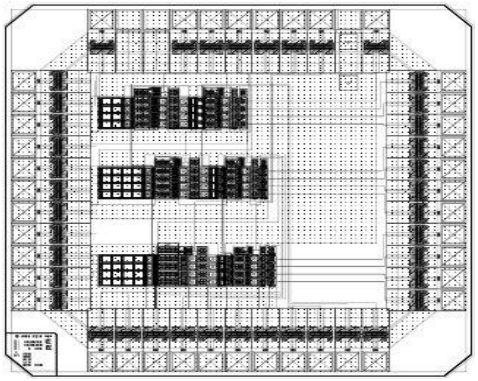
J. Kaplon et al., “Analogue Read-Out Chip for Si Strip Detector Modules for LHC Experiments”

ABCD, ATLAS, DMILL process, 128 Channels, fast bipolar front-end

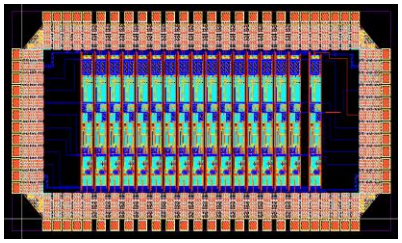


W. Dabrowski et al. "Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS semiconductor tracker,”.

Beetle, LHCb, 0.25µm, 128 channels, Fast front-end, derandomizing buffer



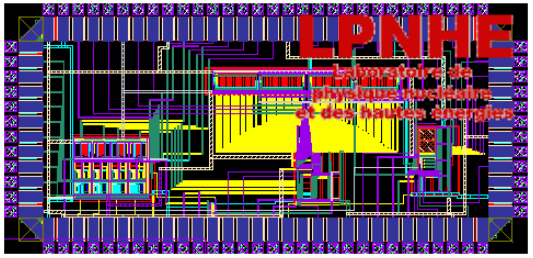
Niels van Bakel et al. “Design of a Readout Chip for LHCb”



180nm @ 3 µs : 360 + 10.5 e-/pF

Process migration

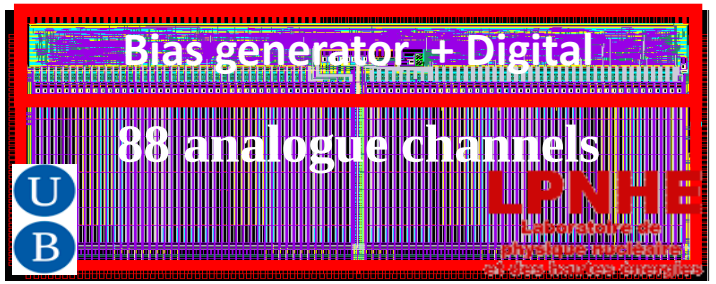
SiTR



130nm @ 2 µs : 625 + 9e-/pF

x 88 channels
+
slow control

SiTR-88



Front-end electronics main features:

– 30mV/MIPS

– Shaping time (from 0.5 to 2 µs)

– sparsifier

– 8 x 8 analog sampler

– 12-b ADC

SiTR- J.F. Genat et al., A 130 nm CMOS digitizer prototype chip for silicon strips detectors readout, IEEE Nuclear Science Symposium Conference Record, N29-6, November 2007, pp.1861–1864.

SiTR-88- Pham. T. H., et. Al., "A 130 nm CMOS mixed mode front end readout chip for silicon strip tracking at the future linear collider", (2010) *Nuclear Instruments and Methods in Physics Research, Section A*, 623 (1) , pp. 498-500.

SiLC timeline

FPA2008-04122-E

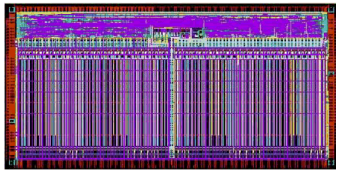
FPA2008-05979-C04-02

FPA2010-21549-C04-01 **AIDA**

2007 | 2008 | 2009 | 2010 | 2011

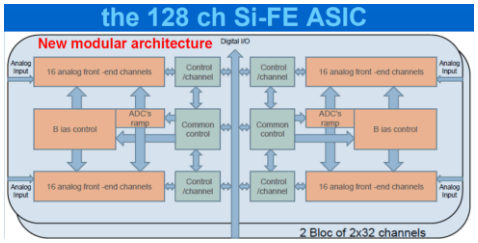
LNPHE/IN2P3-CNRS
Start of collaboration with IN2P3
Design of the digital part

SiTR-88-130UMC



(1st mixed signal chip)

Definition of new architecture



Complete new design (responsability of UB)

Andreu Montiel (AIDA), Dr. Oscar Alonso (FPA2010), Dr. Raimon Casanova (post-doc UB), Dr. Angel Diéguez (UB professor)

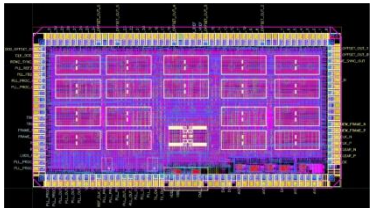
DEPFET collaboration timeline for Belle II

FPA2008-05979-C04-02

FPA2010-21549-C04-01

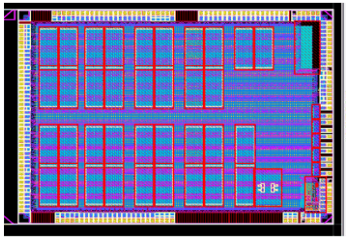
2009 | 2010 | 2011 | 2012

DHPv1



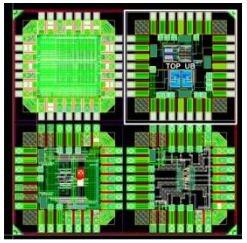
Slow control JTAG (digital)
Analog blocks for configuration and basic blocks (bandgap, DAC, ADC, amplifier)

DHPv2



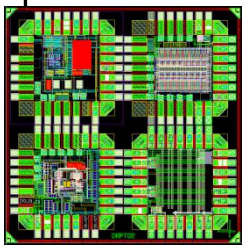
T sensor included,
IBM 90nm
LAST RUN!!!

DHPTv1



TSMC 65
T indep current source
current steering DAC-8b

DHPTv2

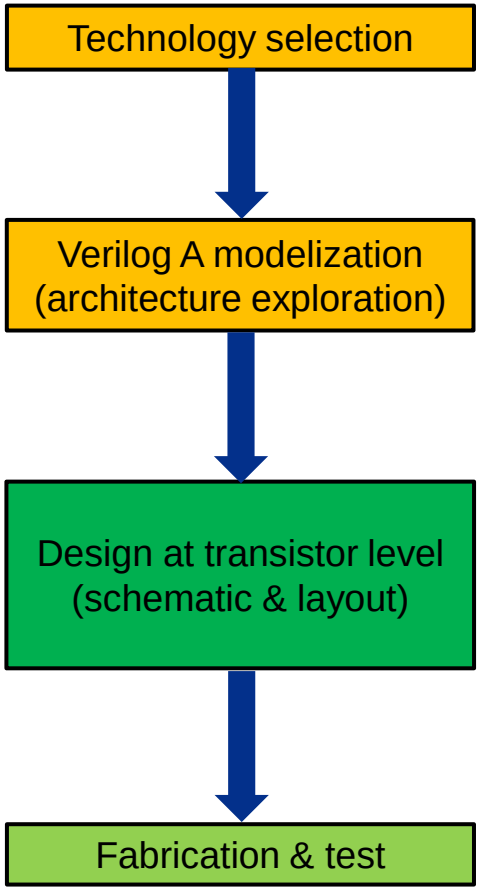


TSMC 65
T sensor

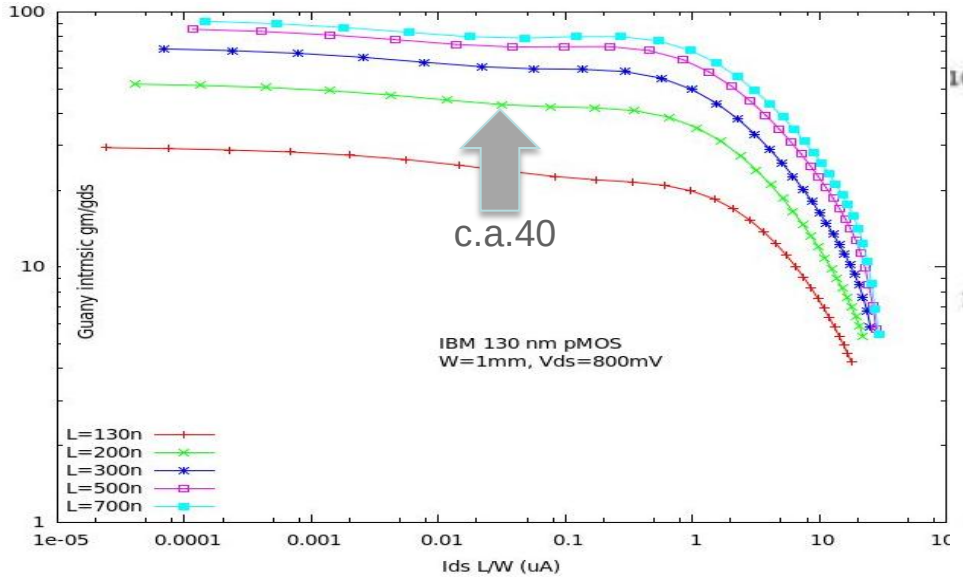
Dr. Oscar Alonso (FPA2010), Dr. Raimon Casanova (post-doc UB),Dr. Angel Diéguez (UB professor)

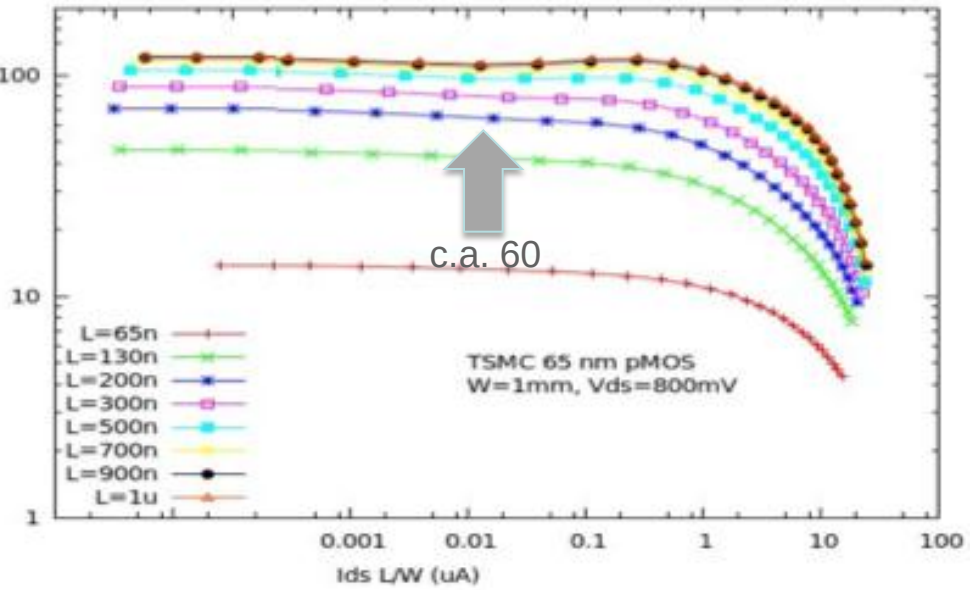
- **Front-end electronics main features:**
  - S/N = 25000 e-/1000e-~ 25
  - Low noise preamplifiers, preamplifier+shaper
  - Linearity 1%, calibration on-chip, DR 100MIPs
  - Coarse sampling @ 150-300ns for BCO tagging.
  - Shaping time (from 0.5 to 3 μs, depending the strip length)
  - Analog sampling, Analog pipelines
  - Trigger decision, digitalization, sparsification
  - Low power:
    - lossless compression
    - Dynamic power management
    - DSM process
  - 256 channels (+pitch adapter)
  - Fault tolerant

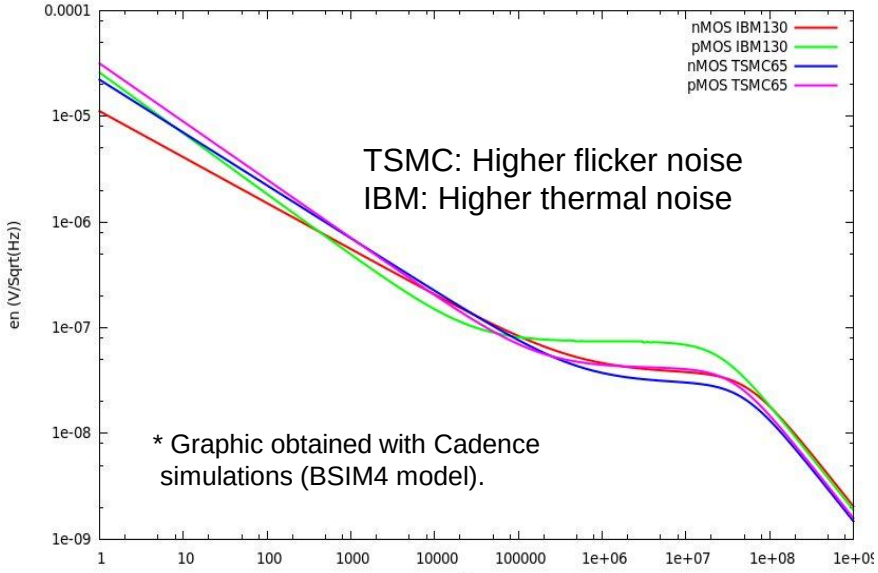
Channel design, status



Technology analysis: Intrinsic gain





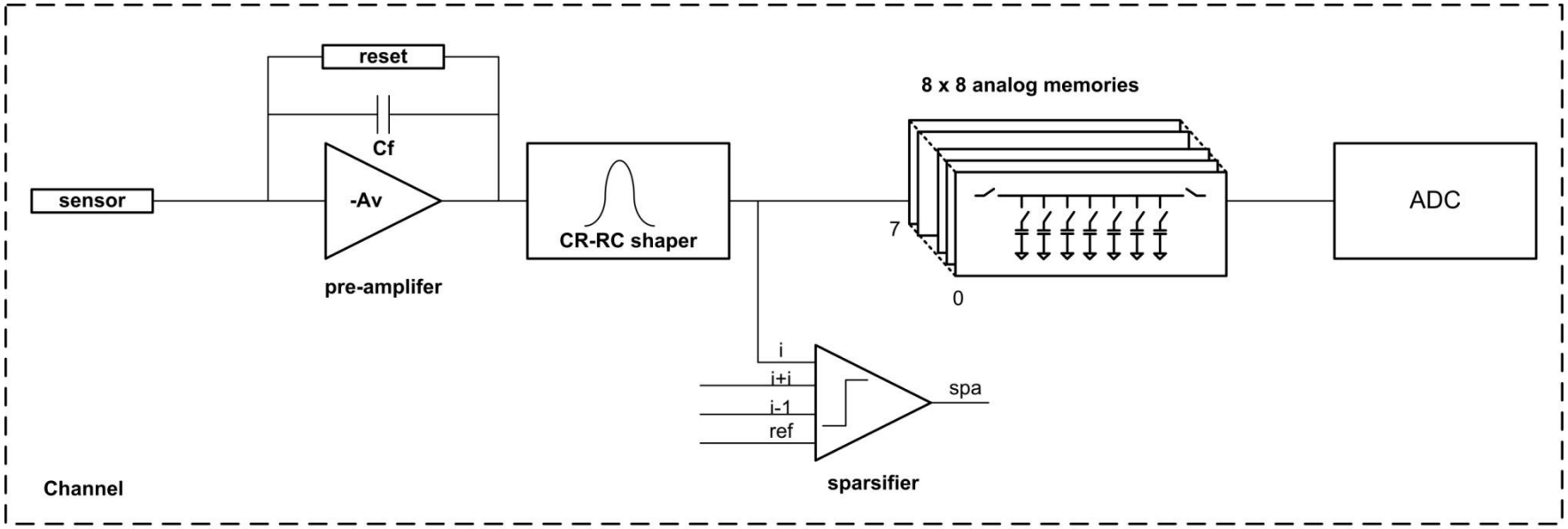


- **Motivation for 65nm CMOS technology**
  - Benefits
    - Higher intrinsic gain, similar noise compared with 130nm
    - Higher density (digital part), faster (fast shaping in CLIC)
    - Low power
    - Enhanced radiation hardness (t_{ox})
    - Extensive existing standard cells libraries
    - A. Marchioro (CERN) is evaluating 65nm CMOS providers (UMC, ST, TSMC, IBM)
    - CERN will provide a design-kit + rad-hard libraries + MPW to the community
    - 65nm TSMC is used in the DHP chip for Belle II (sharing IP, experience)
  - Drawbacks
    - Cost (TSMC through Europractice MPW):

      -130nm: 2.3kEuros/mm^2

      - 65nm: 5kEuros/mm^2 (100 chips!)

Verilog-A model: Overall architecture



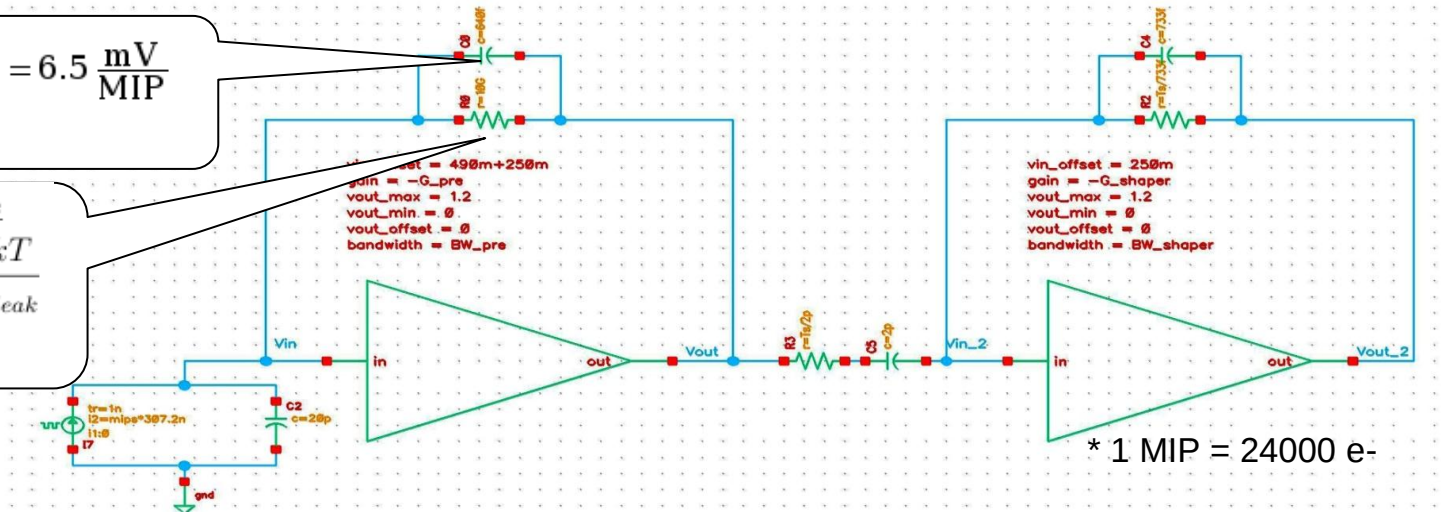
Bias generators
(bandgap, cuurent reference, DAC)

Slow control
(pipeline, time stamp, event stamp, calibration, ADC conversion, I/O interface)

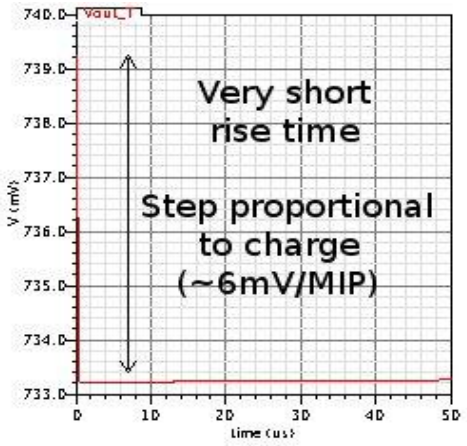
Verilog-A model: Preamplifier + Shaper

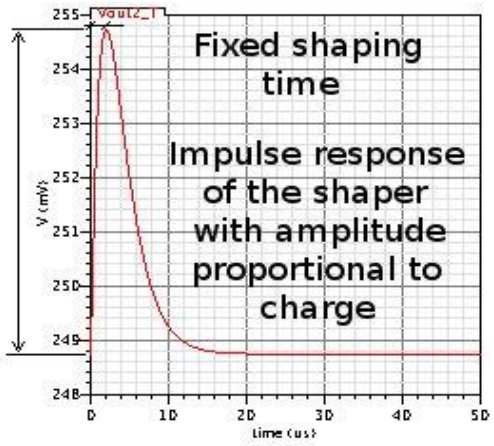
$$G = \frac{1}{Cf} = 6.5\ \frac{mV}{MIP}$$

$$R > \frac{\frac{noise}{2kT}}{eI_{leak}}$$



* 1 MIP = 24000 e-

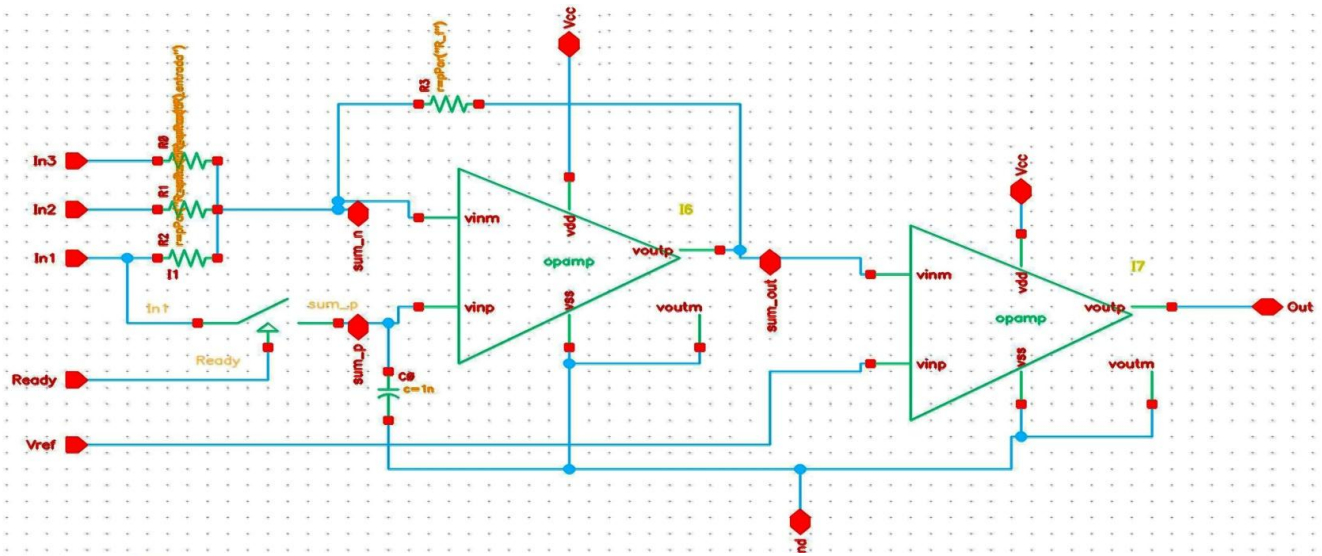


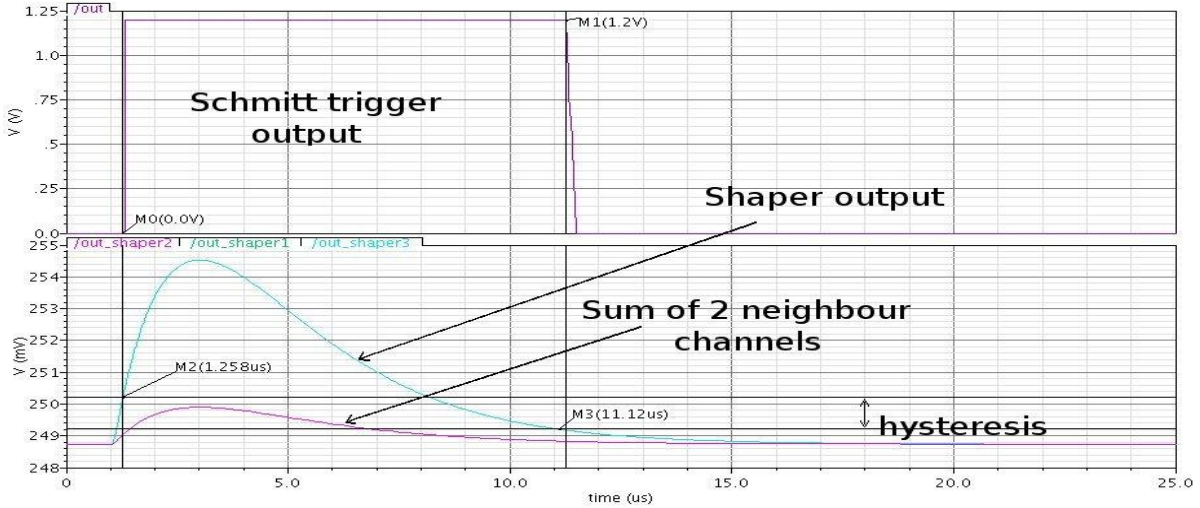


This functional model allows to check correct functionality from specs of pre-amplifier and shaper without need of transistor level design.

Circuit	Av(dB)	f_{-3dB}(kHz)
Pre-amplifier	> 60dB	100
Shaper	> 60 dB	700

Verilog-A model: Sparsifier + Comparator





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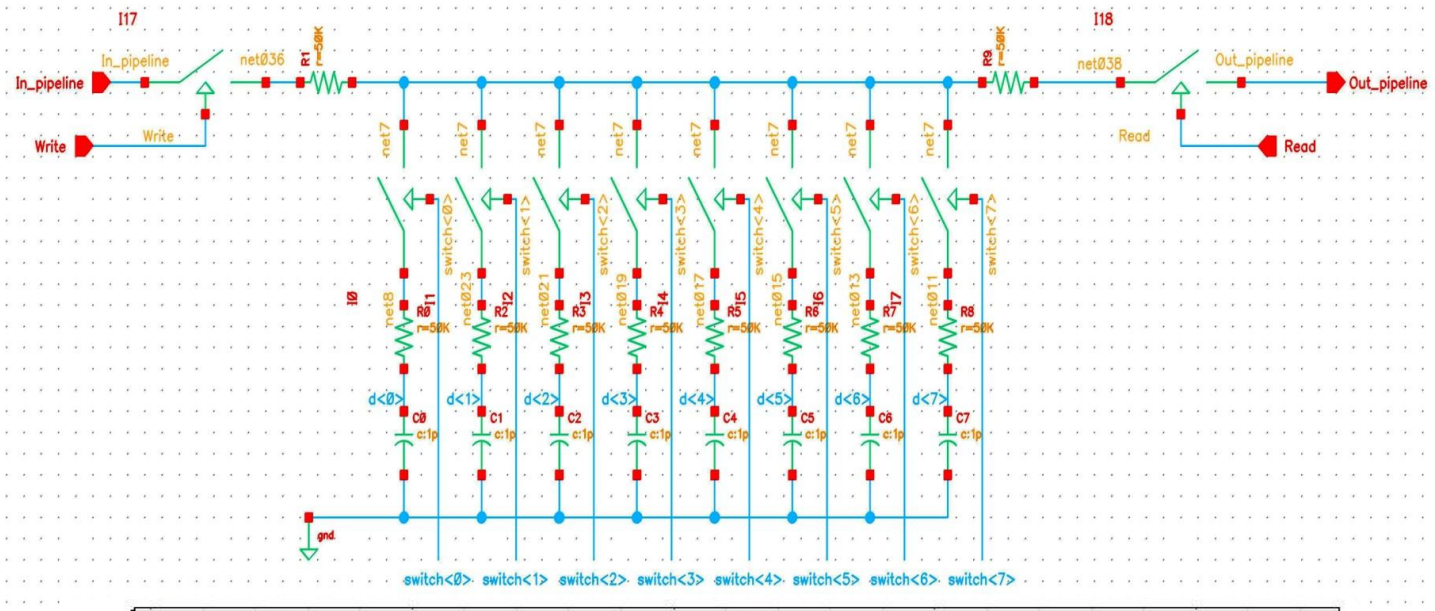
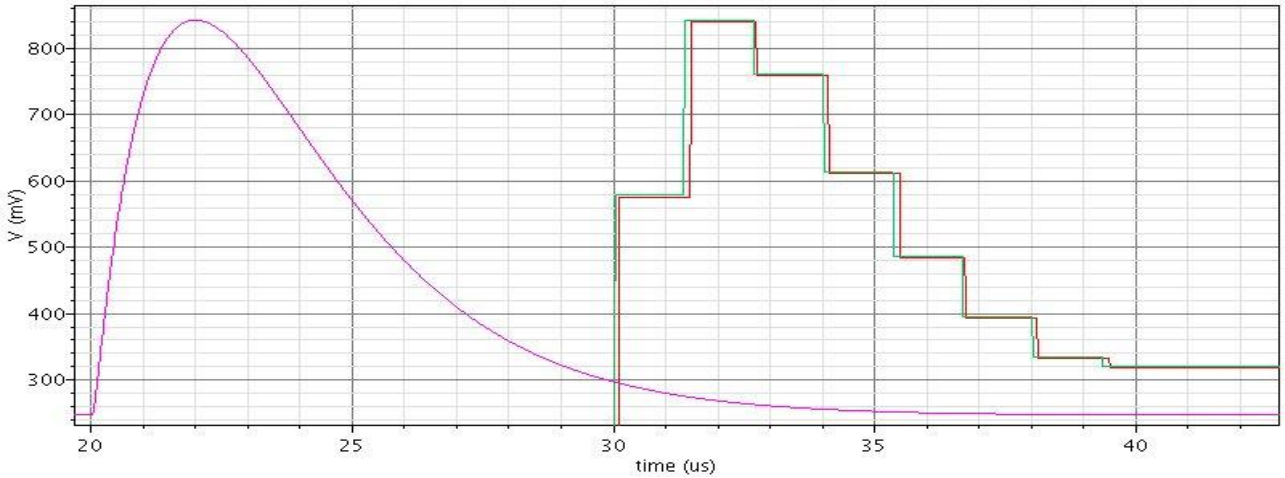
Verilog-A model: Analog pipeline (S&H)





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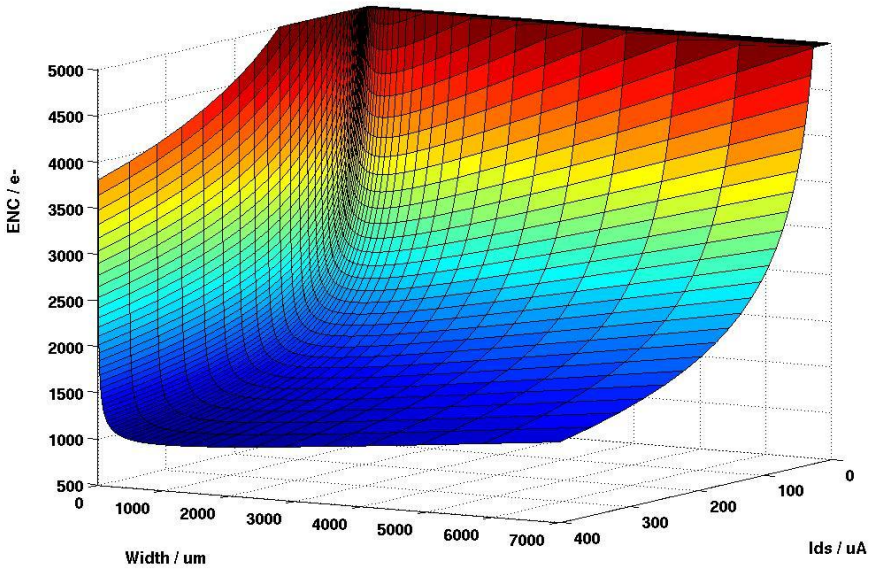
Noise analysis: Input PMOS

Unknown values

$$ENC = \sqrt{ENC_c^2 + ENC_I^2 + ENC_{Rs}^2 + ENC_{Rp}^2} < 1000e^-$$

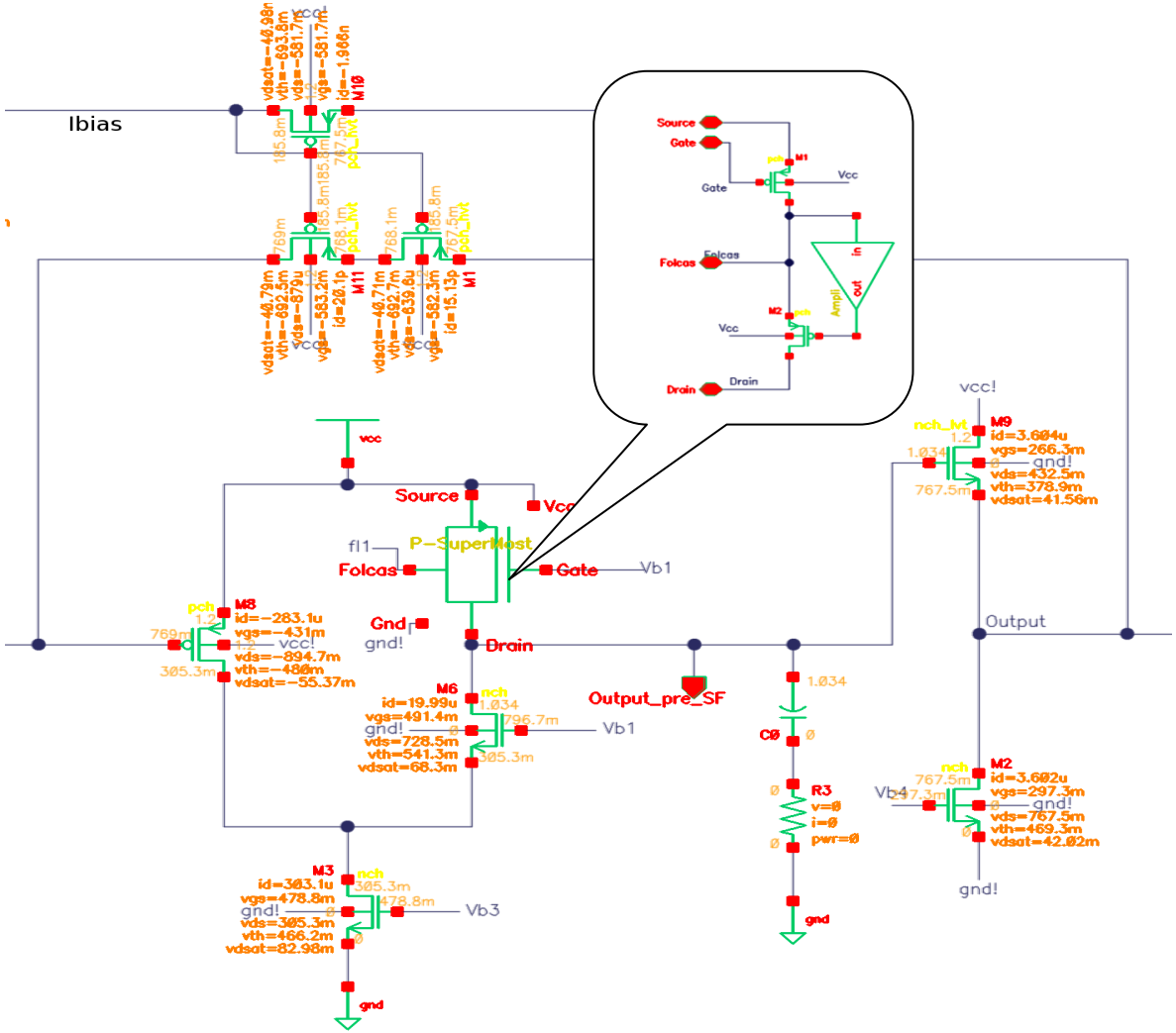
$$ENC_c = A + B.C_d < 400e^-$$



L(µm)	I_{ds}(µA)	A(e^-)	B(e^-)	ENC(e^-)20@pF	W_{opt}(µm)	Pow(µm)	IF
0.25	100	47	26.2	570	624	120	0.27
0.25	200	40	19.1	422	781	240	0.42
0.25	300	37	15.9	355	890	360	0.56
0.25	500	34	12.7	288	1046	600	0.79
0.5	100	71	28.1	633	493	120	0.7
0.5	200	63	20.8	479	613	240	1.12
0.5	300	59	17.6	410	694	360	1.49
0.5	500	54	14.3	340	808	600	2.13
0.75	100	94	29.8	689	428	120	1.25
0.75	200	84	22.4	532	528	240	2.02
0.75	300	79	19.1	460	594	360	2.70
0.75	500	74	15.7	387	683	600	3.90
1	100	115	31.4	743	385	120	1.89
1	200	104	23.8	581	470	240	3.10
1	300	98	20.4	507	525	360	4.16
1	500	92	17.0	596	596	600	6.11

Matlab used to dimension input PMOS transistor.

Pre-amplifier design: Folded cascode with gain-boosting



Power supply:
1.2V

Power consumption:
< 380 µW

Noise @ 2µs shaping time:
A ~ 35,7 e-
B ~ 16,5 e-/pF
[< 400 e- (20pF)]

Full scale:
100 MIP

Charge gain:
~ 6.5 mV/MIP

Amplifier:
Gain ~ 69 dB
3dB-BW: ~ 55kHz
PM ~ 66 º

* 1 MIP = 24000 e-

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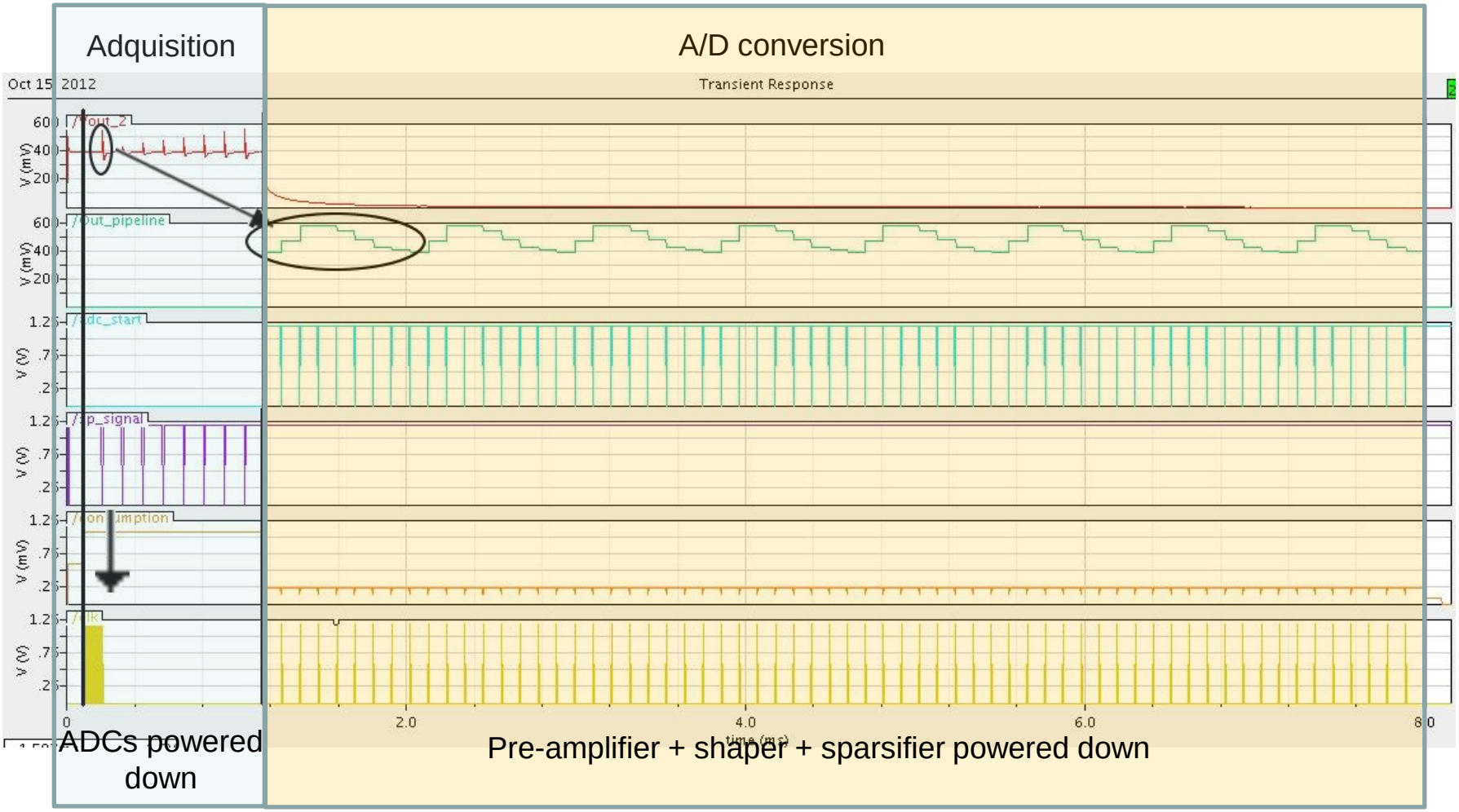
Adquisition
A/D conversion
Oct 15 2012
Transient Response
/vout_2
/vout_pipeline
/adc_start
/sp_signal
/consumption
/clk
V (mV)
V (V)
0
2.0
4.0
6.0
8.0
time (ms)
ADCs powered down
Pre-amplifier + shaper + sparsifier powered down

Conclusions

- Verilog A model of a complete channel designed for architectural exploration:
  - Extraction of main blocks requirements.
  - 10 – 100 faster than spice model
  - Less accurate but useful to speed up verification of 256 channel chip design
- Initiated the design on 65nm TSMC, with synergies with concurrent designs:
  - Designed pre-amplifier at transistor level
  - Silicon proved auxiliary modules: current source, DAC, temperature sensor.
- Dynamic power management under study. How this might affect power supply? Help needed.
- Resources are very limited and implication of other groups is necessary (LPNHE, g-2@JPARC. …)