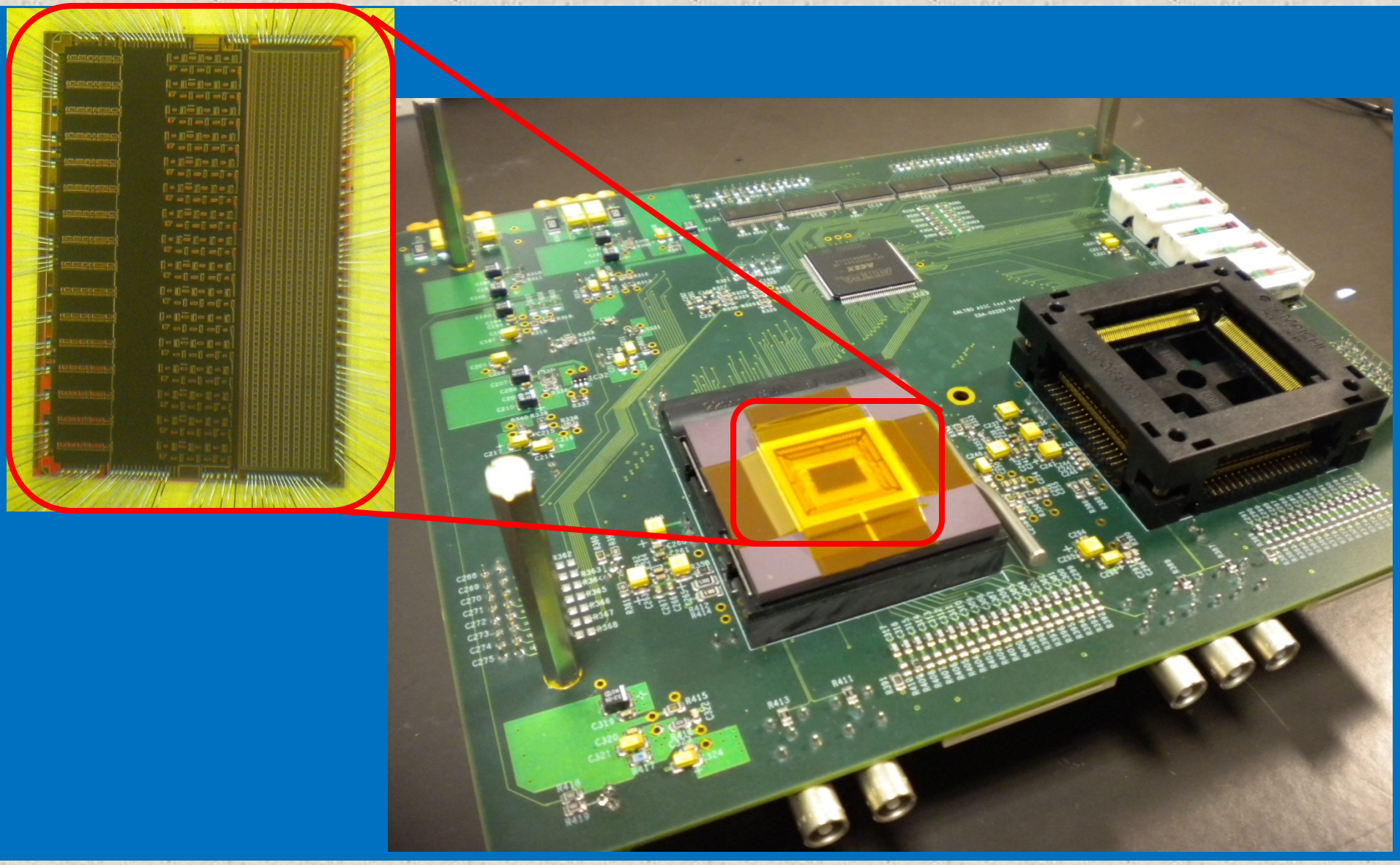
Noise and power pulsing measurements on the Super-Altro chip for gaseous detectors



Super-Altro Team

People:

Luciano Musa … S-Altro Specifications and Architecture
Paul Aspell … Coordinator of Demonstrator ASIC Design
Hugo França-Santos … ADC
Eduardo Garcia … Digital Signal Processing & Control
Massimiliano De Gaspari … Front-end, Integration, Tests

Organization:

CERN European Organization for Nuclear Research
Geneva, Switzerland

Presented at:

Linear Collider WorkShop
University of Texas at Arlington
October 24th, 2012

Outline

1. **Motivations and requirements for the project**

2. **System architecture:**
   - **Pre-amplifier shaper (PASA)**
   - **ADC**
   - **Digital Signal Processor (DSP)**

3. **Tests:**
   - **Gain**
   - **Noise**
   - **DSP**
   - **Power / power pulsing**

4. **Conclusions**

Super-Altro requirements

Applications:

Linear Collider TPC, CLIC/ILC: pads as small as 1x4mm^2, beam pulses.
Tests of GEM and MicroMegas.

S-ALTRO requirements:

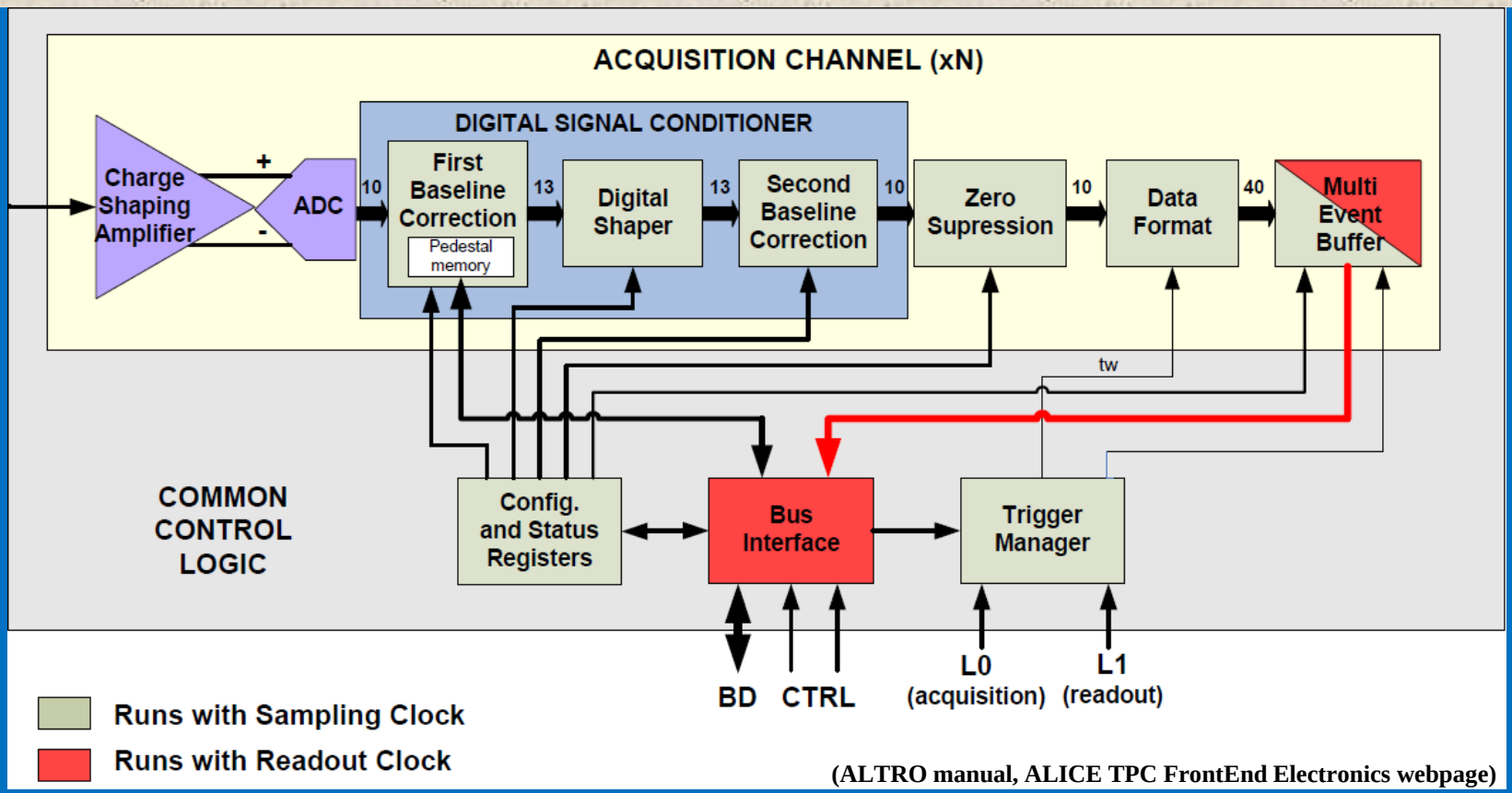
Provide signal charge, channel number and a time stamp.
Data processing of 100μs of data sampled at 10MHz (25μs @40MHz).
Small size.
Handling signals of both polarities, variable gain and shaping time.
10bit, 40MHz sampling.
Advanced DSP capabilities and zero suppression.
Power pulsing capability.

Goal: **to demonstrate integration per channel of a low-noise programmable analog front-end, an ADC and Digital Signal Processor in a single chip.**

Architecture: based on existing PASA + ALTRO electronics for the ALICE TPC.

Technology: CMOS 130nm.

System architecture

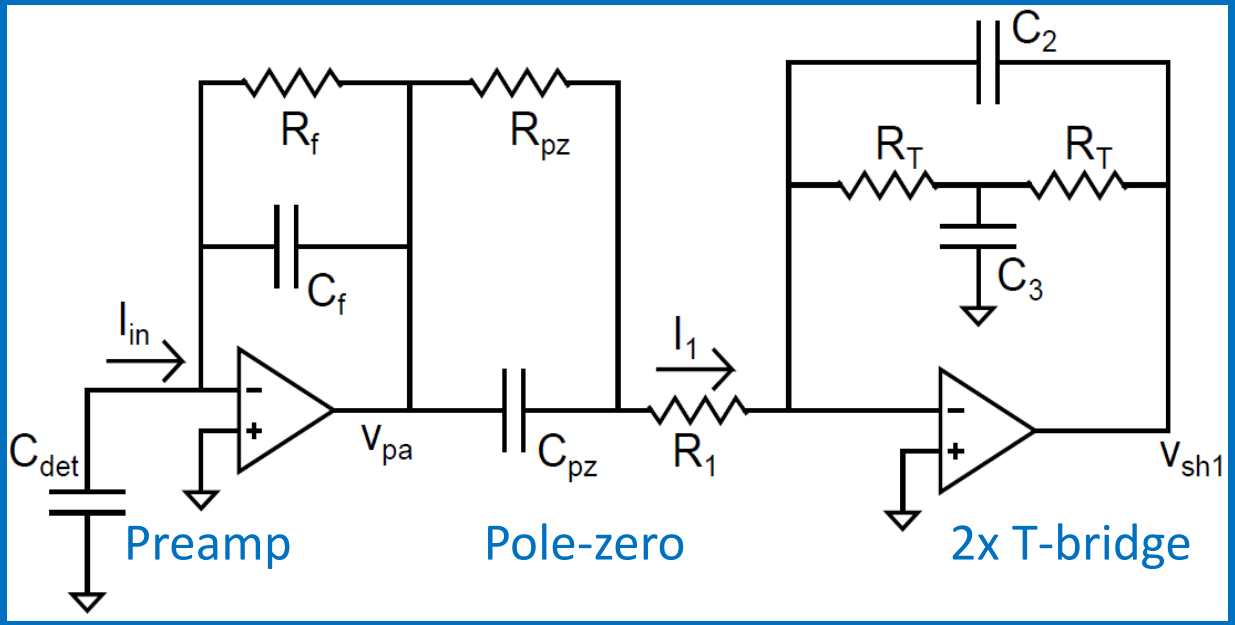


(ALTRO manual, ALICE TPC FrontEnd Electronics webpage)

Level 1: Starts the data acquisition.
Level 2: Validates data from previous L1.
Sampling clock : max 40MHz. Readout clock : max 80MHz.

PreAmplifier/Shaper (PASA)

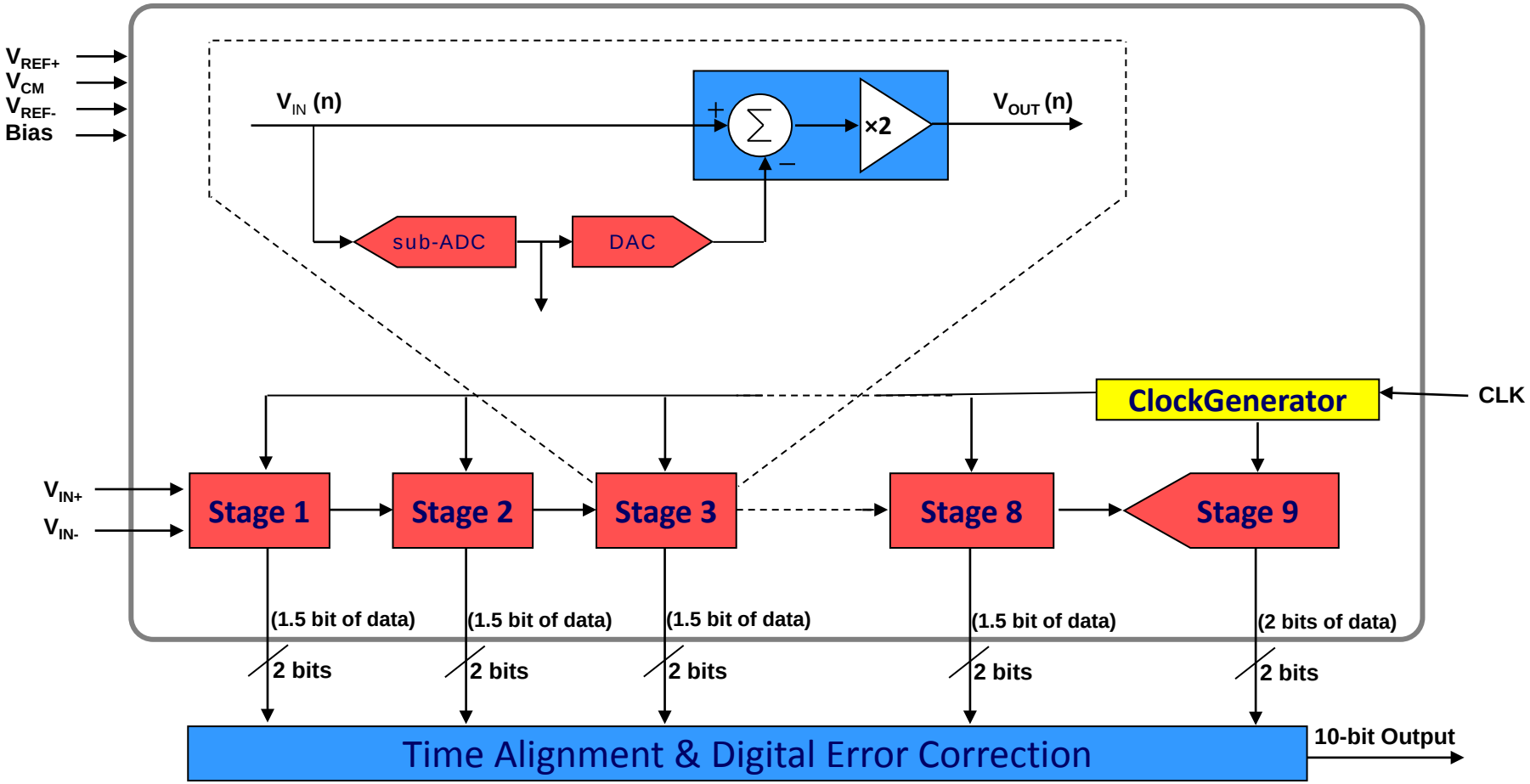
Based on the CERN PCA16 Prototype (G. Trampitsch).
Single-ended input, differential output.
4th order CR-RC4 filter.



Programmability options:
- **Polarity switch**
- **Shutdown switch**
- **Gain control (2 bits: 12-15-19-27mV/fC)**
- **Peaking time control (3 bits: 30-60-90-120ns) for GEM tests**
- **Bias decay (analog)**

Size: 1100μm X 210μm.

Pipeline ADC

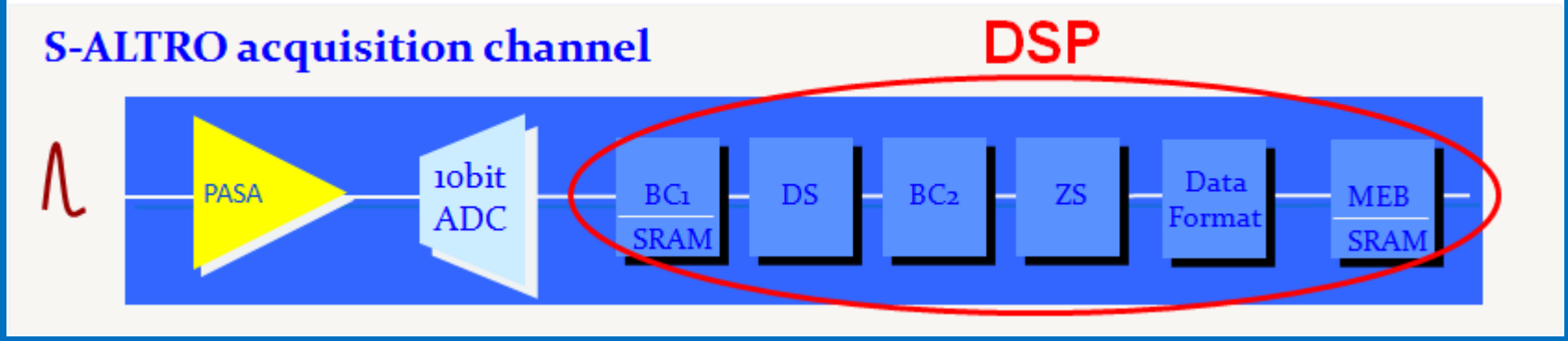


CERN ADC prototype (H. França-Santos):
8x 1.5-bit stages (redundancy) + 1x 2-bit flash ADC.
10bit, 40MHz, 1.5V supply, 34mW power, 1.5x0.5mm^2 area.

TWEPP 2009 proceedings pp452-456

DSP functions

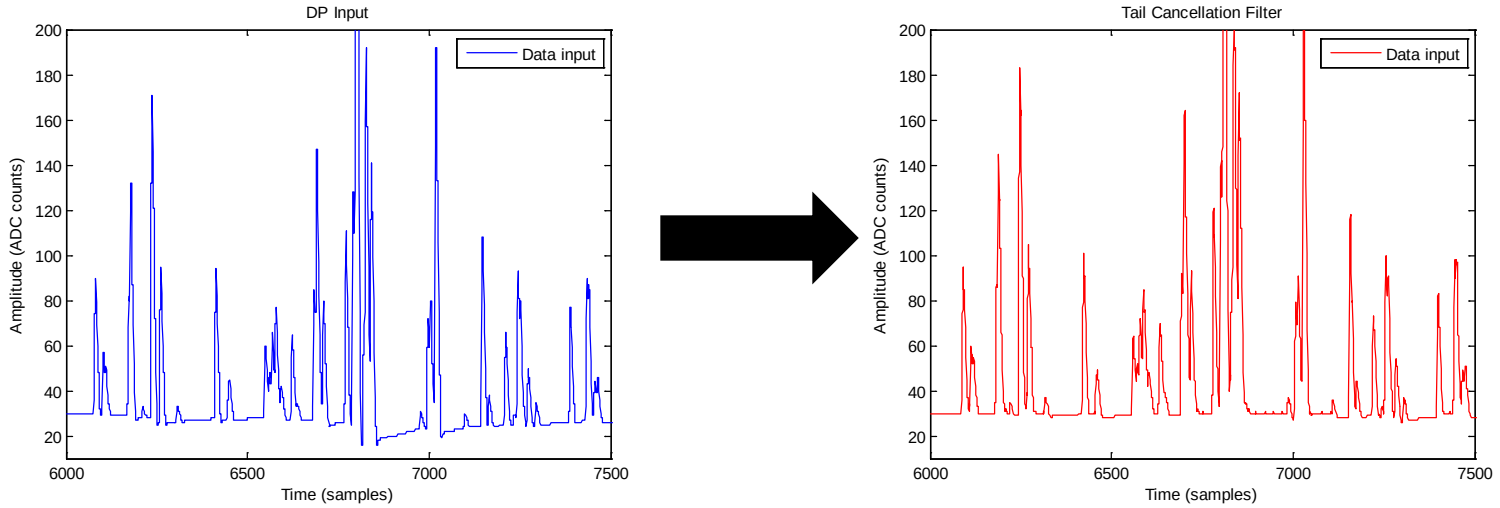
E. Garcia PRIME 2009 proceedings pp28-31



Baseline Correction 1	**Removes the systematic offsets that are introduced due to clock noise pickup and switching of the gating grid of the detector.**
Digital Shaper	**General-purpose digital shaper. Example: remove the distortion of the signal shape due to long ion tails.**
Baseline Correction 2	**Reduces non-systematic baseline movements based on a moving average filter.**
Zero Suppression	**Removes samples that fall below a programmable threshold.**
Data Format	**Converts the 10bit data stream into 40bit words including time stamp.**
Multi-Event Buffer	**In order to reduce the dead time of the system, data are saved in a memory for later readout.**

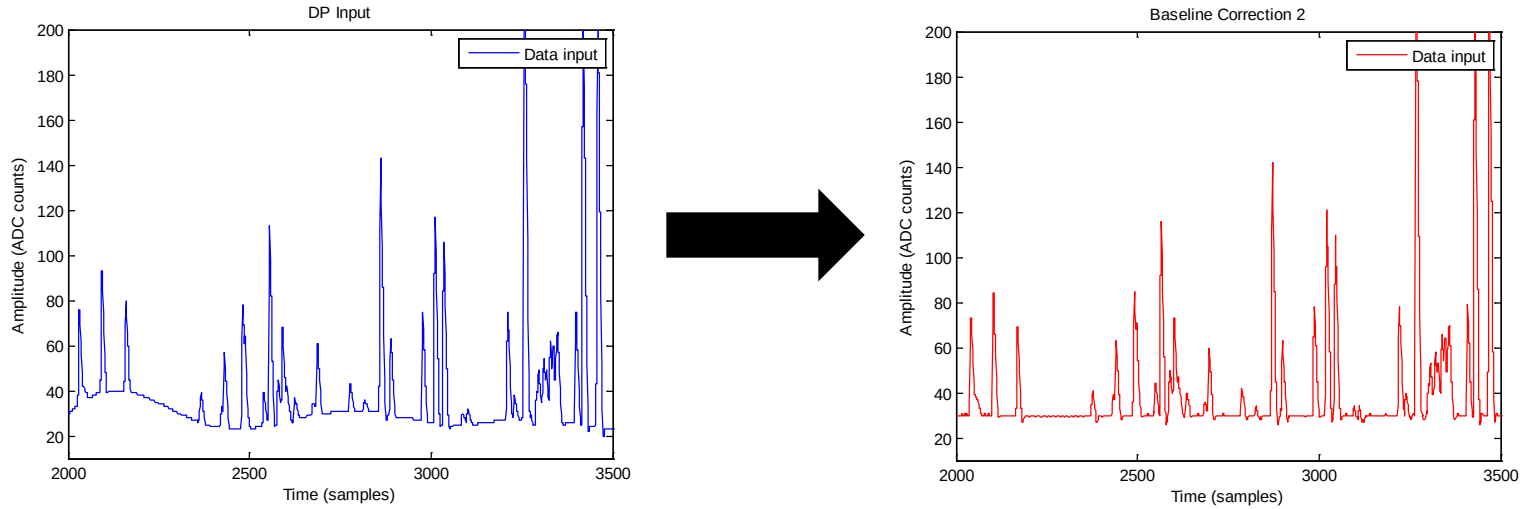
Digital Shaper simulation

DS example test: removing the undershoot of the analog pulse.

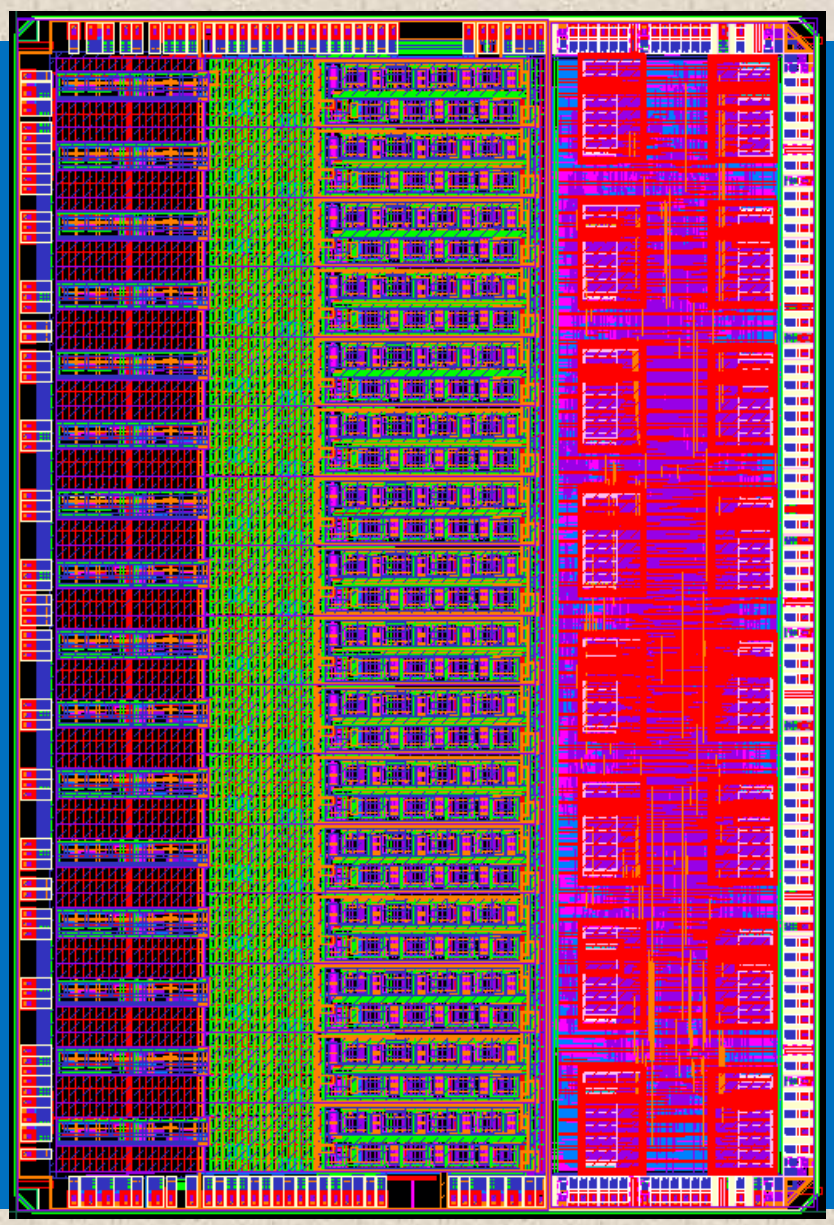


Baseline Correction 2 simulation

BC2 example test: a baseline fluctuation during the acquisition.



Layout



Size: 5750µm x 8560µm (49.22mm^2)

Submitted July 2010

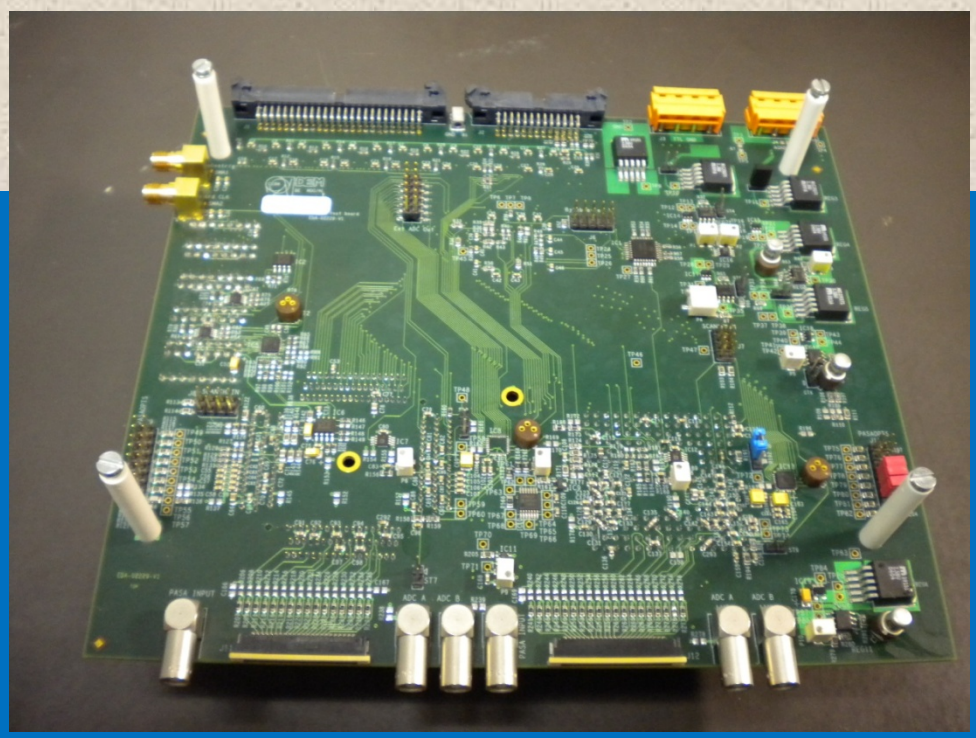
Packaged in 2 different packages:

PGA180 for testing purposes

QFP208 for applications

+ naked dies available

Tests



Test conditions:

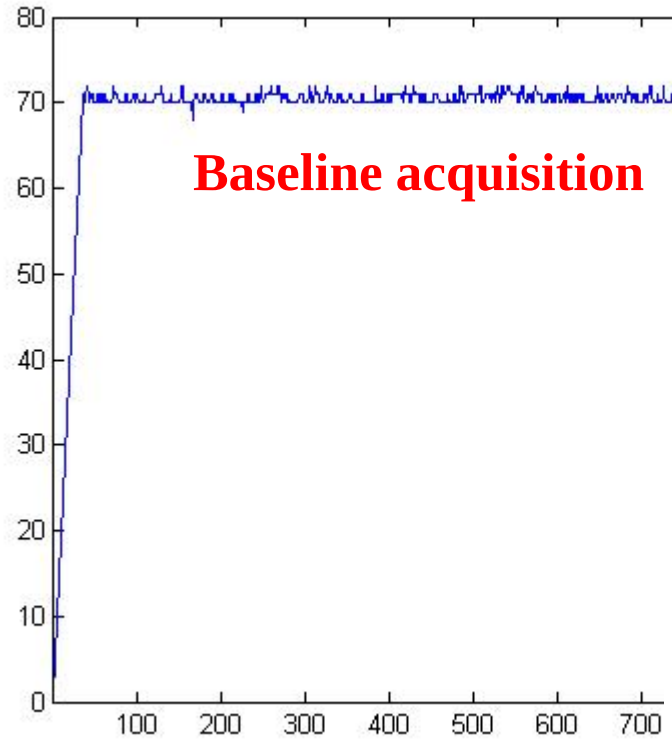
- **Sampling clock frequency 10-20-40MHz, readout clock 40MHz.**
- **Chip PGA3: the inputs of the PASA are not bonded. This avoids noise injection from the ground plane of the test board.**
- **Chip PGA4: all inputs bonded.**

Shutdown / power pulsing tests controlled using the Board Controller FPGA:

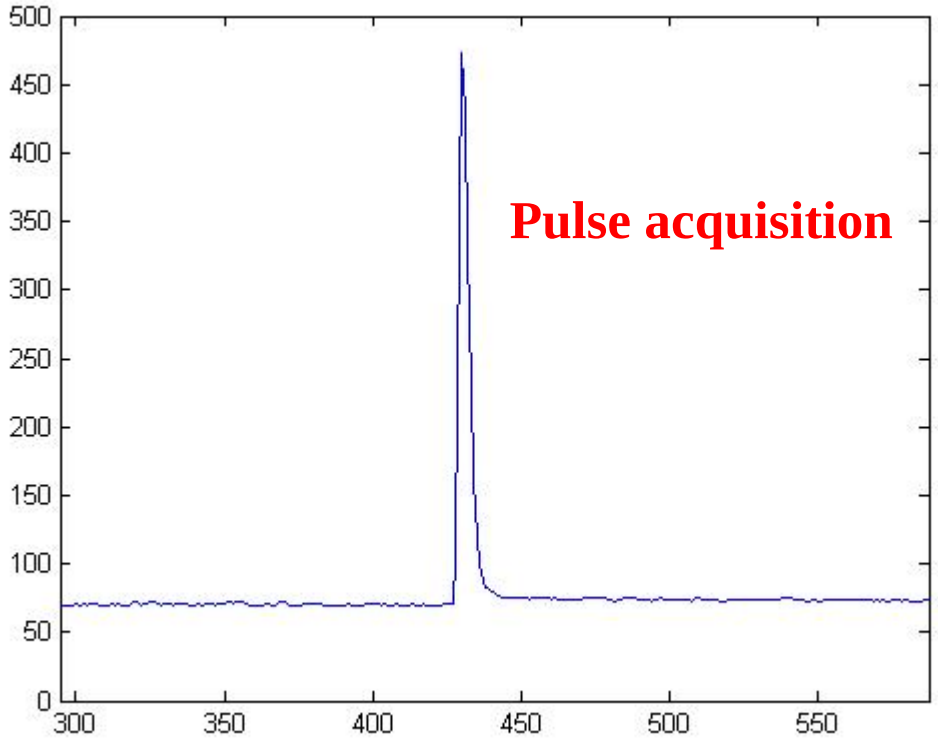
- **PASA shutdown feature**
- **ADC bias resistor switch**
- **Removal of the sampling and/or readout clock (enable lines)**

Example acquisitions

Examples of acquisitions with PASA gain=12mV/fC, shaping time=120ns, input cap 1.8pF, sampling clock frequency = 20MHz

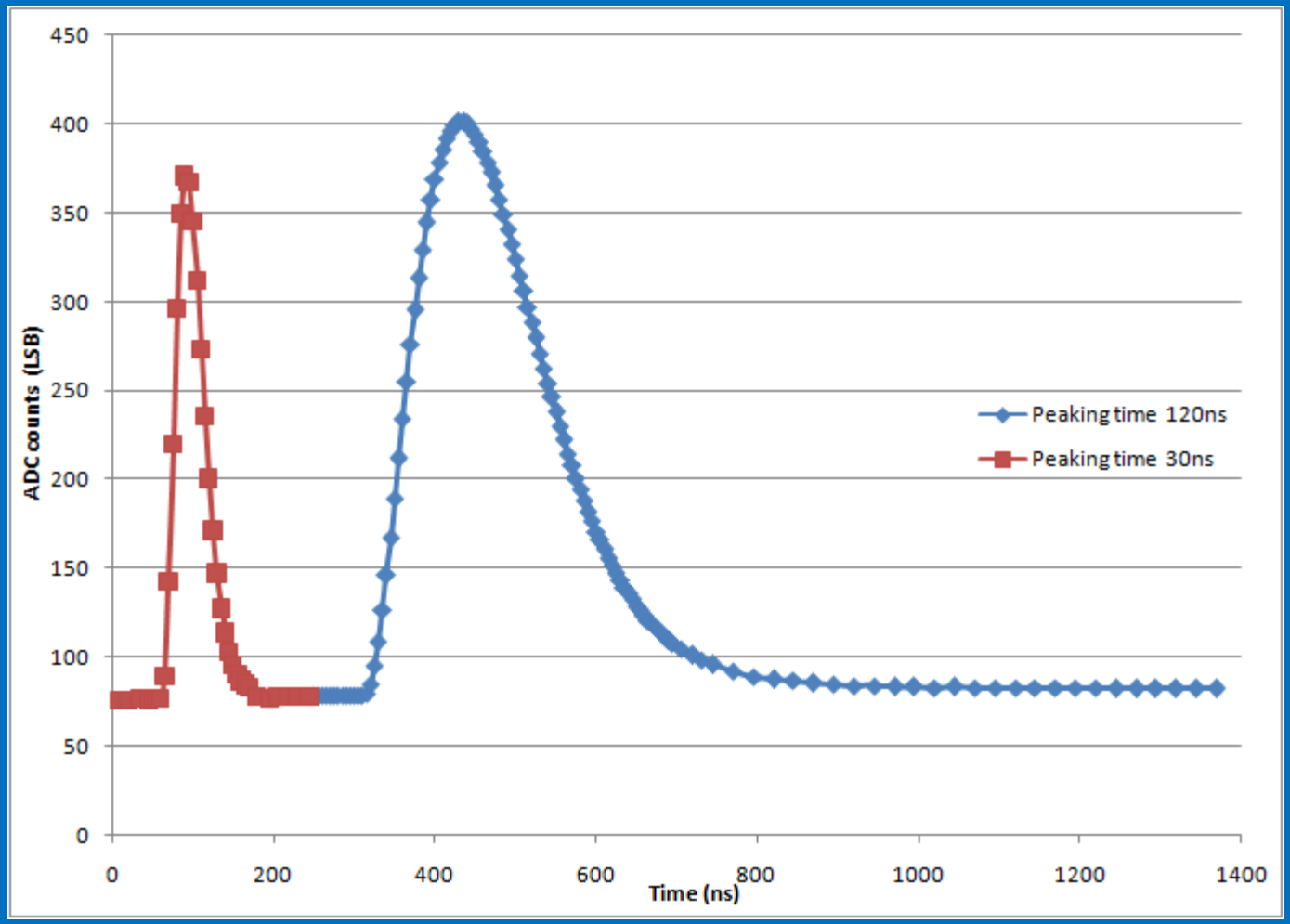


Baseline acquisition



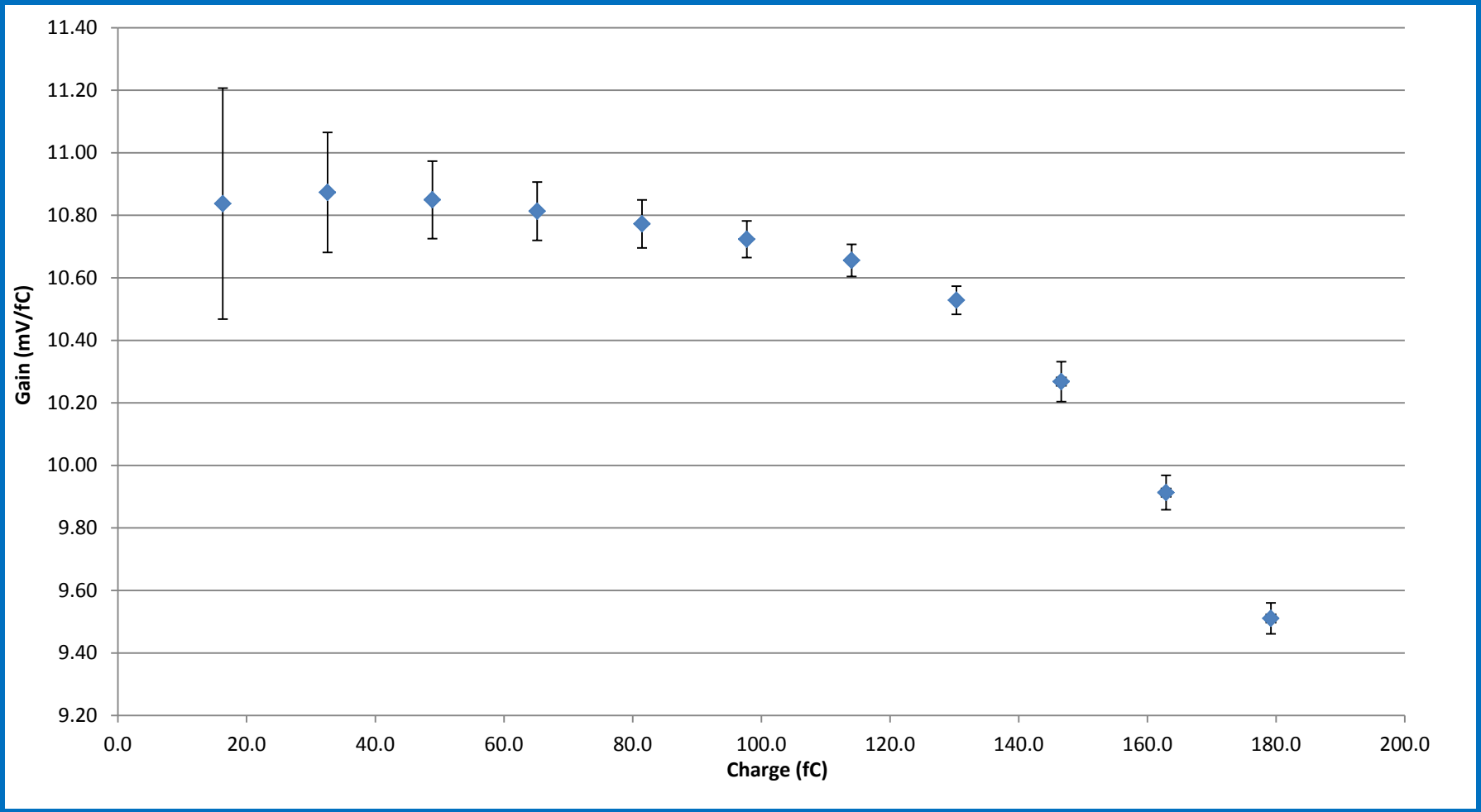
Pulse acquisition

Acquired pulses



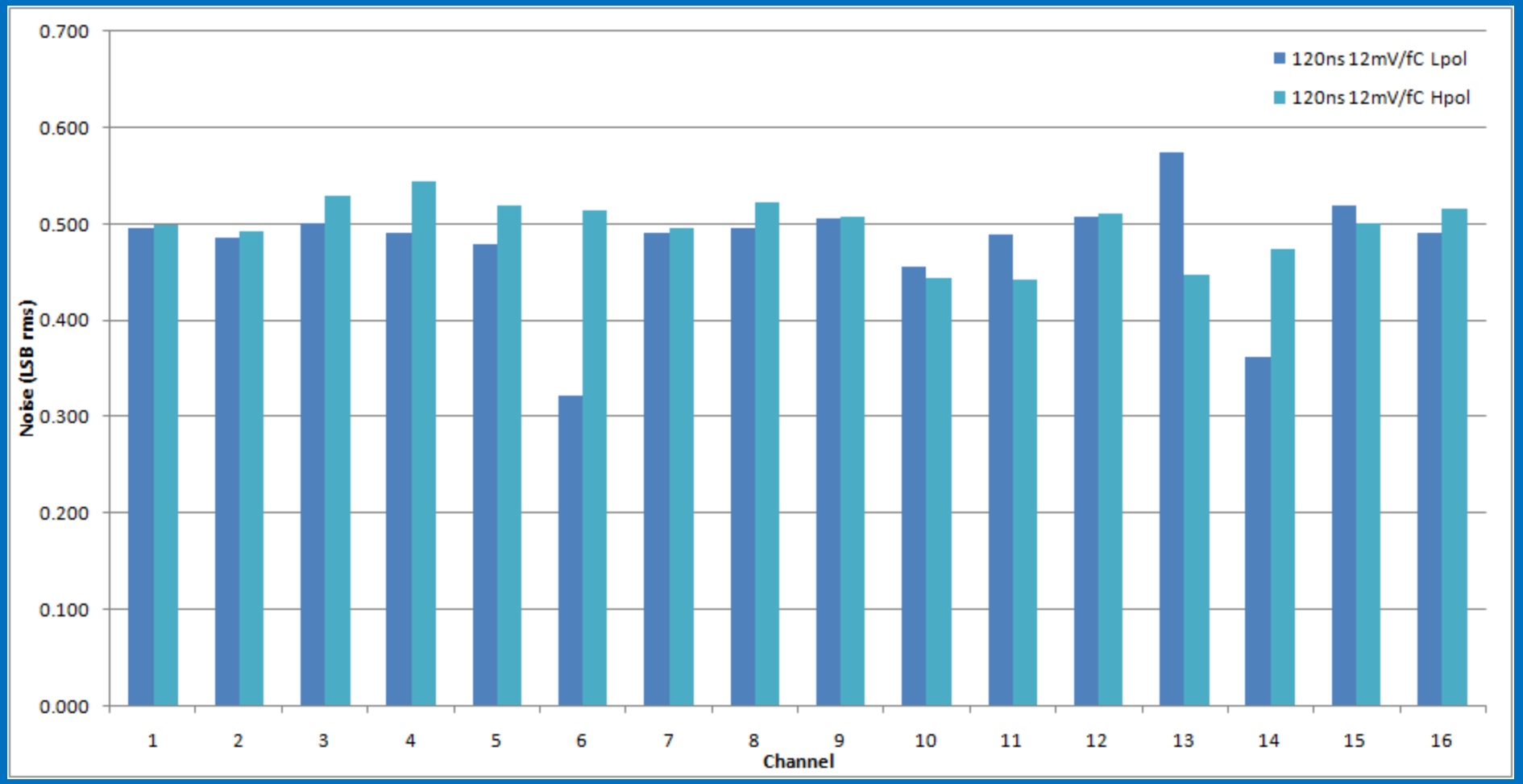
Examples of acquisitions at 30ns and 120ns shaping time.
Sampling frequency 40MHz. Signal scan with a granularity of 5ns.

Gain measurement



PASA configuration: 12mV/fC, 120ns, Low polarity.
Measured gain: 10.6mV/fC ±1.4%

Baseline noise: open analog inputs



PGA3: inputs not bonded

Noise constant across channels

Noise summary

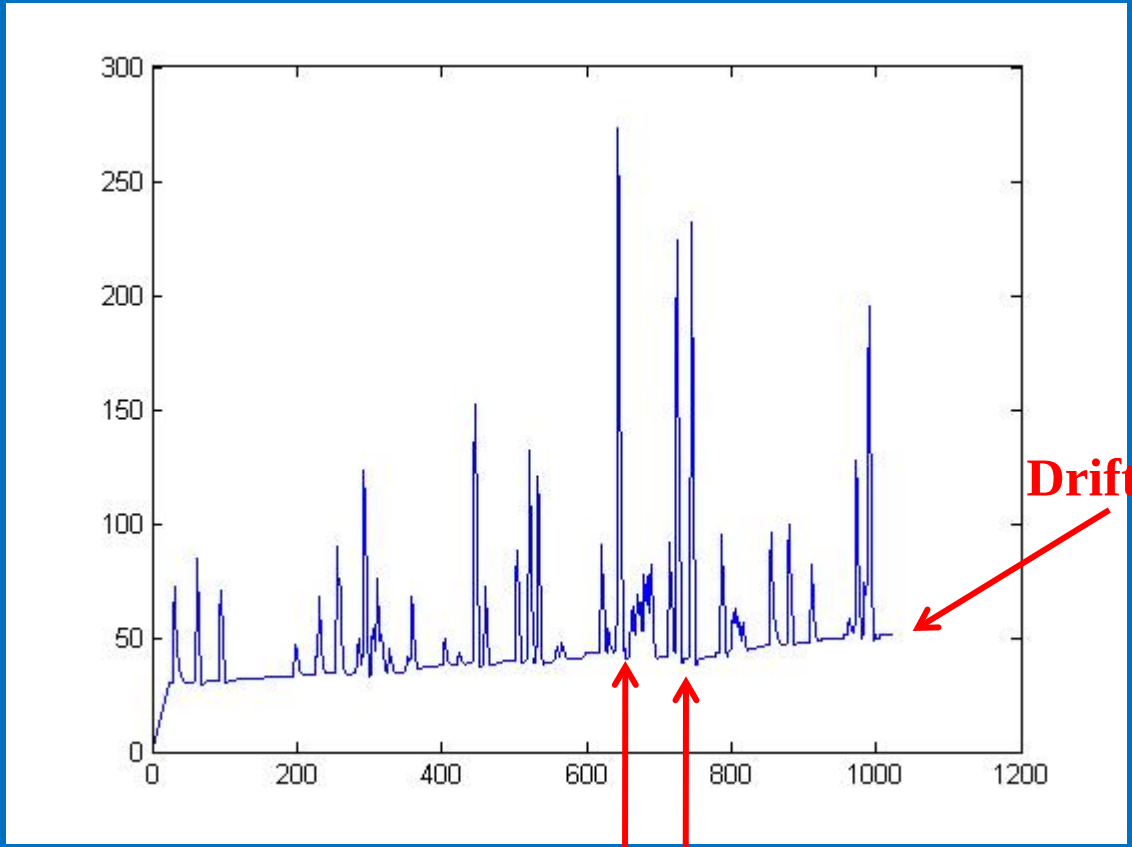
Analog inputs	PASA conf:	120ns L 12	120ns L 27	30ns L 12	30ns L 27	120ns H 12	30ns H 12
Open	Noise e^-	547	316	641	370	574	625
Bonded	Noise e^-	809	649	1796	1768	770	1587

Measured baseline noise averaged over 16 channels.

Shaping 30-120ns, Gain 12-27mV/fC, signal polarity H/L.

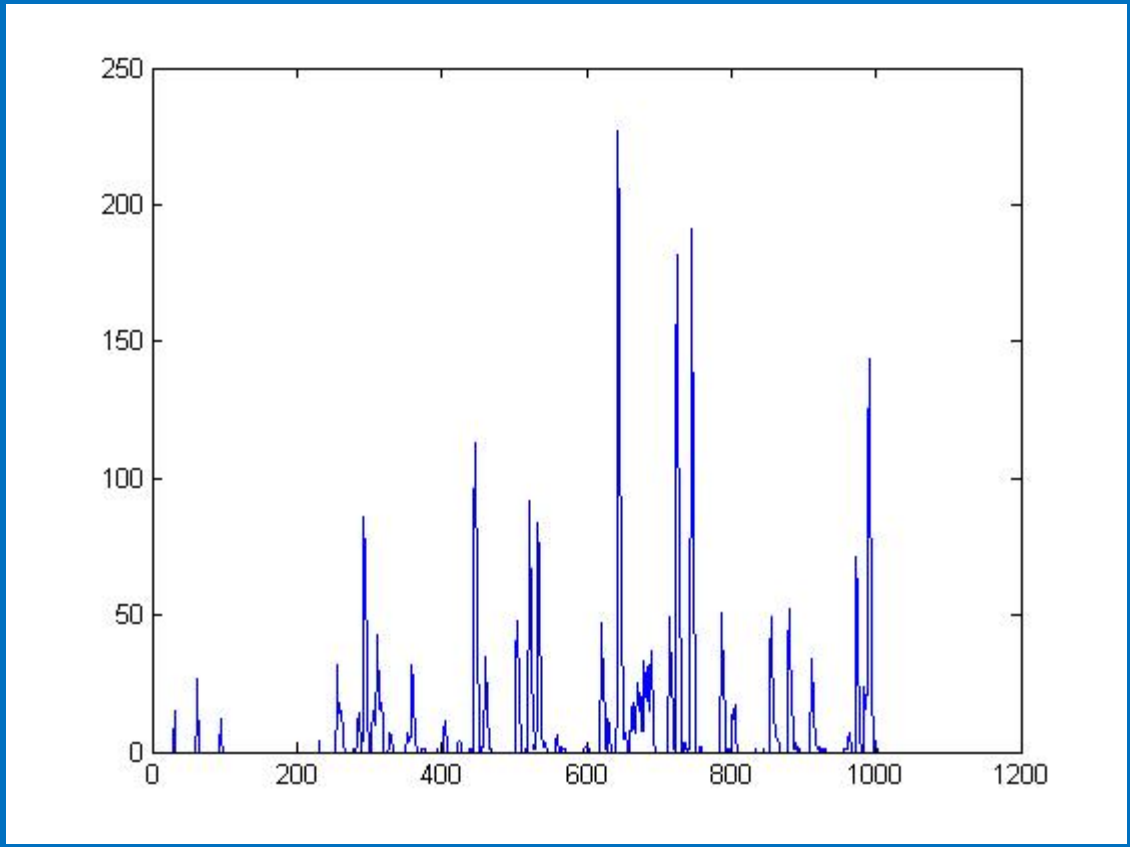
DSP tests 1

Known pattern written in the Pedestal Memory (Baseline Correction 1) and used as test input



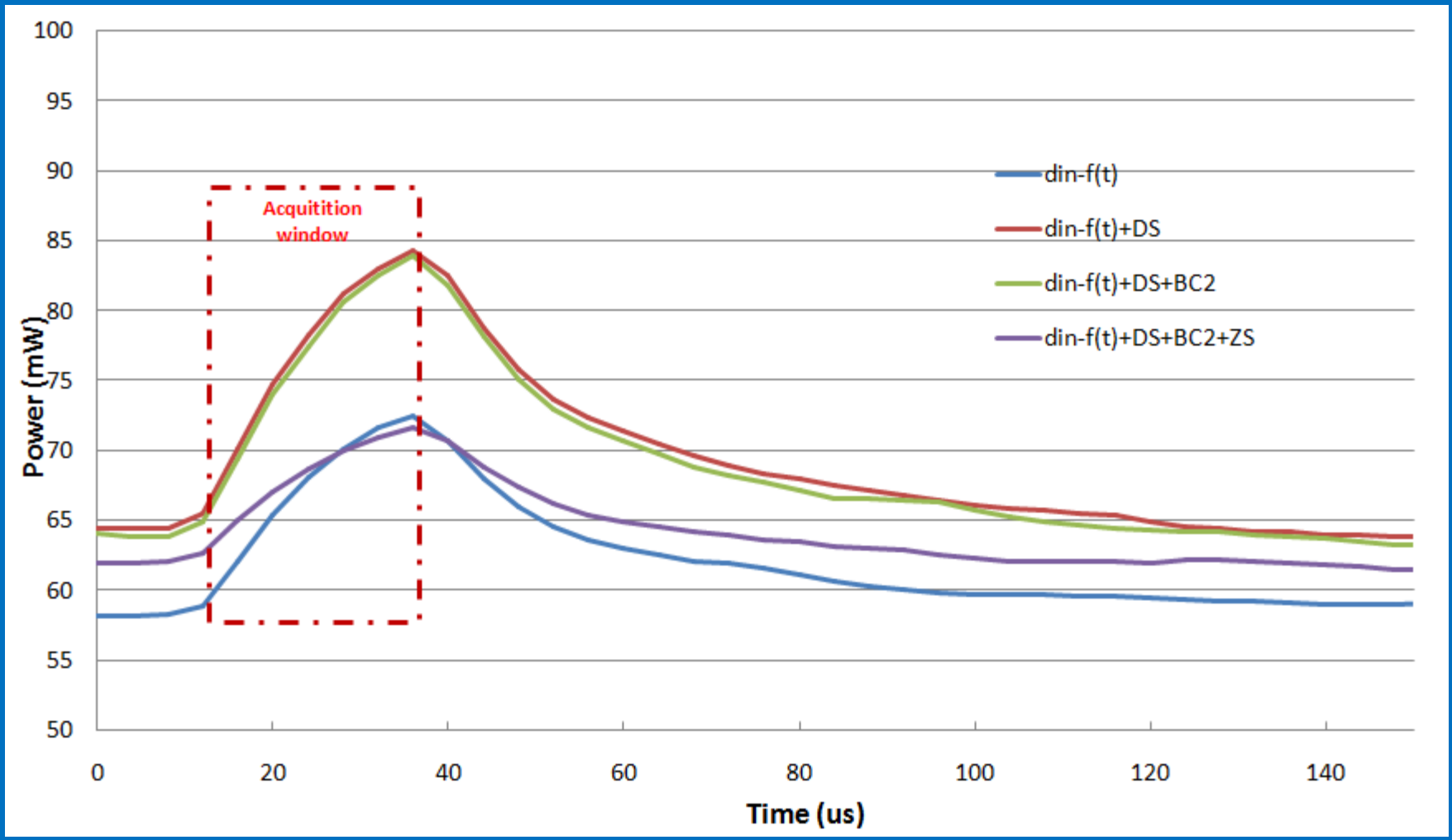
Emulates the pattern produced by a real detector

DSP tests 2



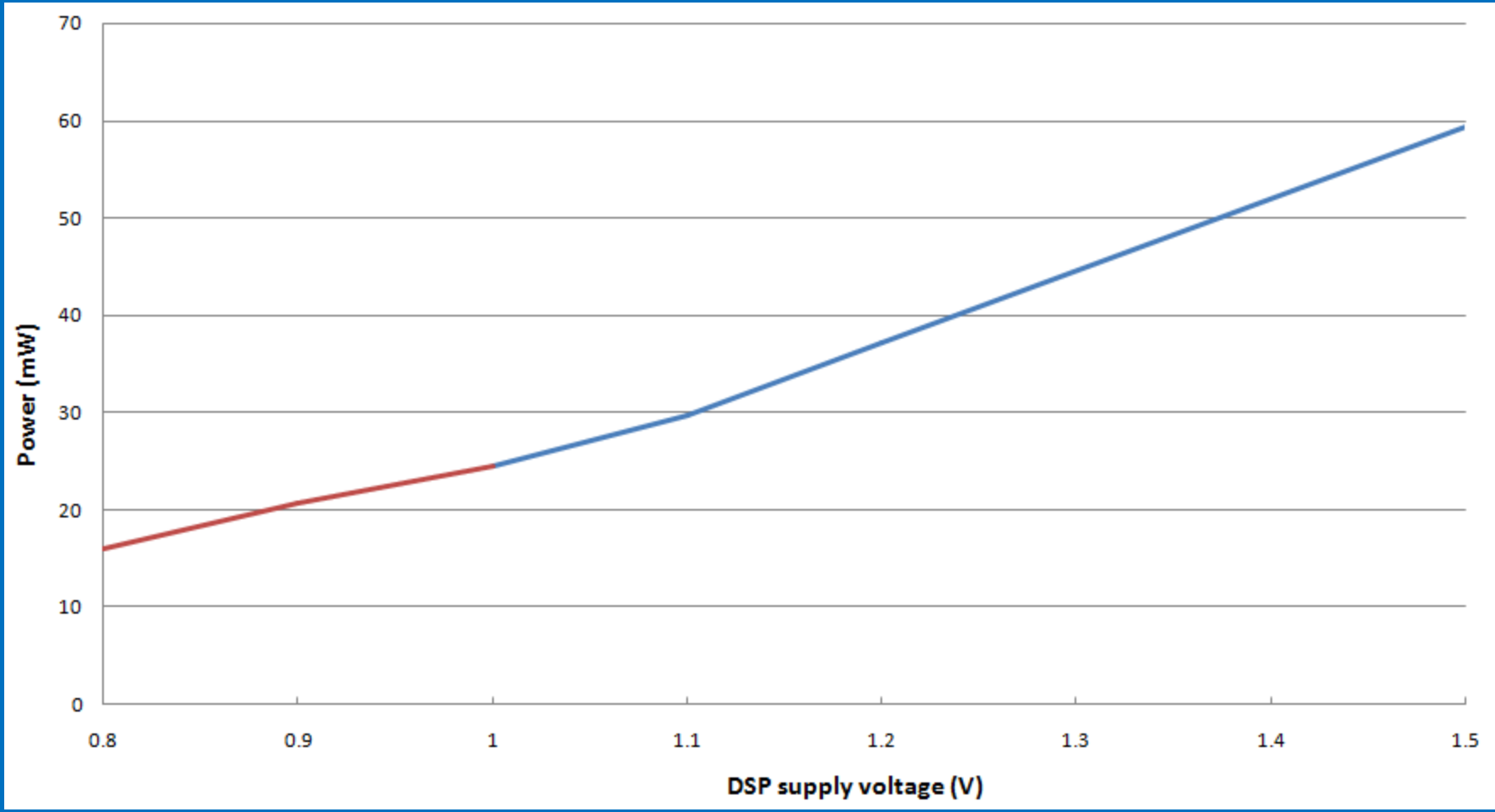
The DSP removes offsets, undershoots, baseline drifts

Power consumption DSP 1



Power consumption of the DSP when acquiring at 40MHz sampling frequency. Different DSP functionalities included.

Power consumption DSP 2

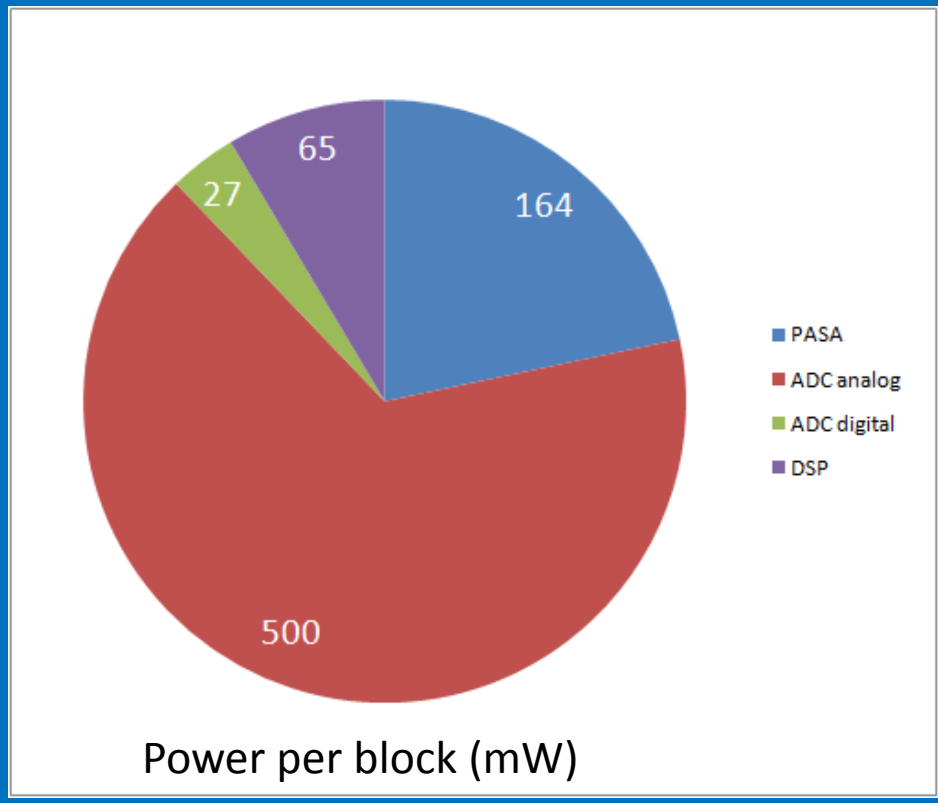


Power consumption of the DSP at different supply voltages.
Efficient operation down to 1V supply.

Power consumption

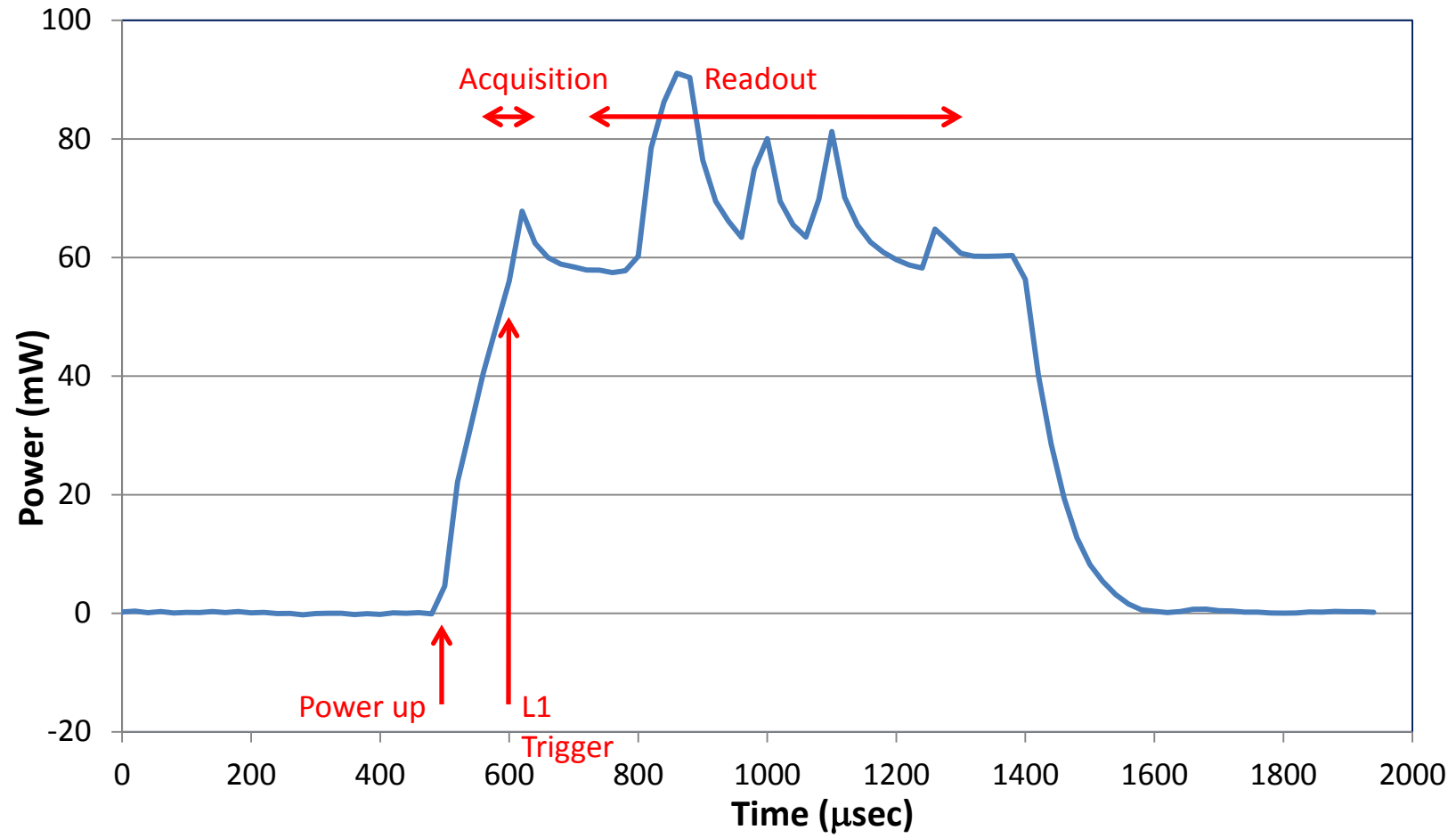
Each block can be switched off independently, and without removing the supply voltage.
PASA and ADC: remove the bias voltages.
DSP: remove the sampling/readout clock.

	40MHz operation	Smart shutdown
PASA	10.26mW/ch	132µW/ch
ADC analog	31.28mW/ch	430µW/ch
ADC digital	1.71mW/ch	≈0
DSP	4.04mW/ch	10µW/ch



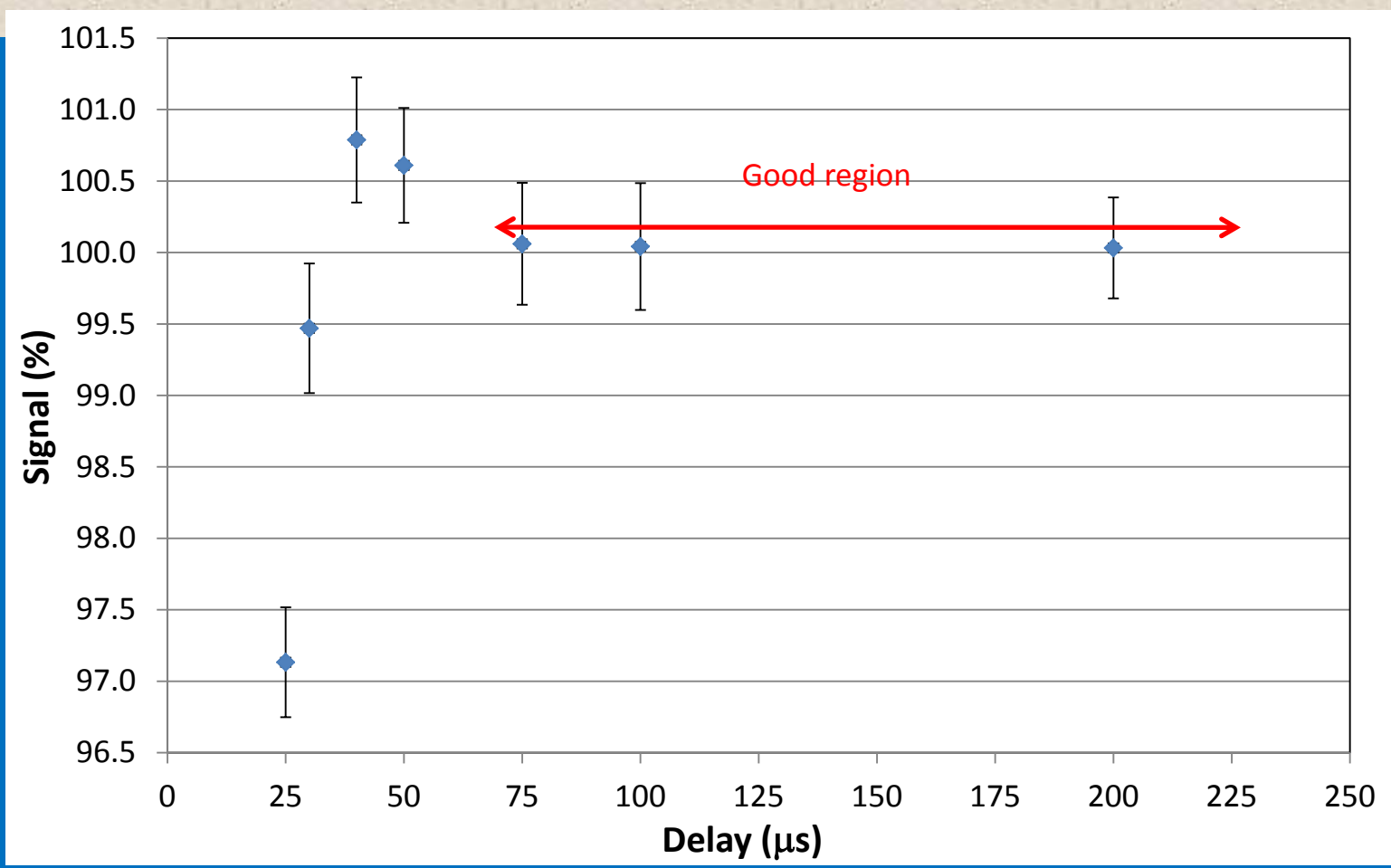
Power consumption: 47.3mW/ch, 757mW total @40MHz.

Power pulsing cycle



Power consumption of the DSP during a power pulsing cycle.
Minimum delay between power up and L1 trigger has to be measured.
Readout time is determined by the test setup (RCU) → minimum PP cycle ≈1ms.

Wake-up time



A test pulse is injected after power up; the amplitude of the pulse is monitored with different delays between power up and L1.
Plot of signal amplitude with PP vs signal amplitude in continuous mode.
100µs delay gives good results: difference with continuous mode <1 LSB.

Power pulsing results

	Shutdown (mW)	Power pulsing cycle (μJ)
PASA	2.12	145.2
ADC analog	6.88	421.1
ADC digital	0.01	22.9
DSP	0.16	58.3
Pads	≈0	6.9
Total	9.2	654.3

Power pulsing cycles are repeated at a frequency of 50Hz (Duty≈1/20).

P_{CLIC}=9.2mW+50Hz*654.3μJ=41.9mW

Power reduction by a factor 18.1 (continuous mode: 757mW).

In the ILC 50Hz case:

P_{ILC}=9.2mW+5Hz*654.3μJ=12.5mW (reduction: 60.6).

Conclusions and Outlook

- **The 16 channel Super-ALTRO Demonstrator has been designed, prototyped and tested successfully!!**
- **The chip is already usable for the Linear Collider TPC prototype.**
  The area is 3.07mm^2/channel (LCTCP requirement: <4mm^2)
- **Using appropriate design techniques, integration of low-noise analog components and digital functions is possible with little effect on noise performance.**
- **Power pulsing approach has been demonstrated effective in reducing the power consumption, while preserving the performance.**

- **The Super-ALTRO Demonstrator opens possibilities of design optimization for lower power and higher number of channels.**
- **The system can be used for detector tests, e.g. using GEM readout.**
- **Since integration has been proved, the next steps should attack the power consumption of the ADC.**

Thanks for your attention!

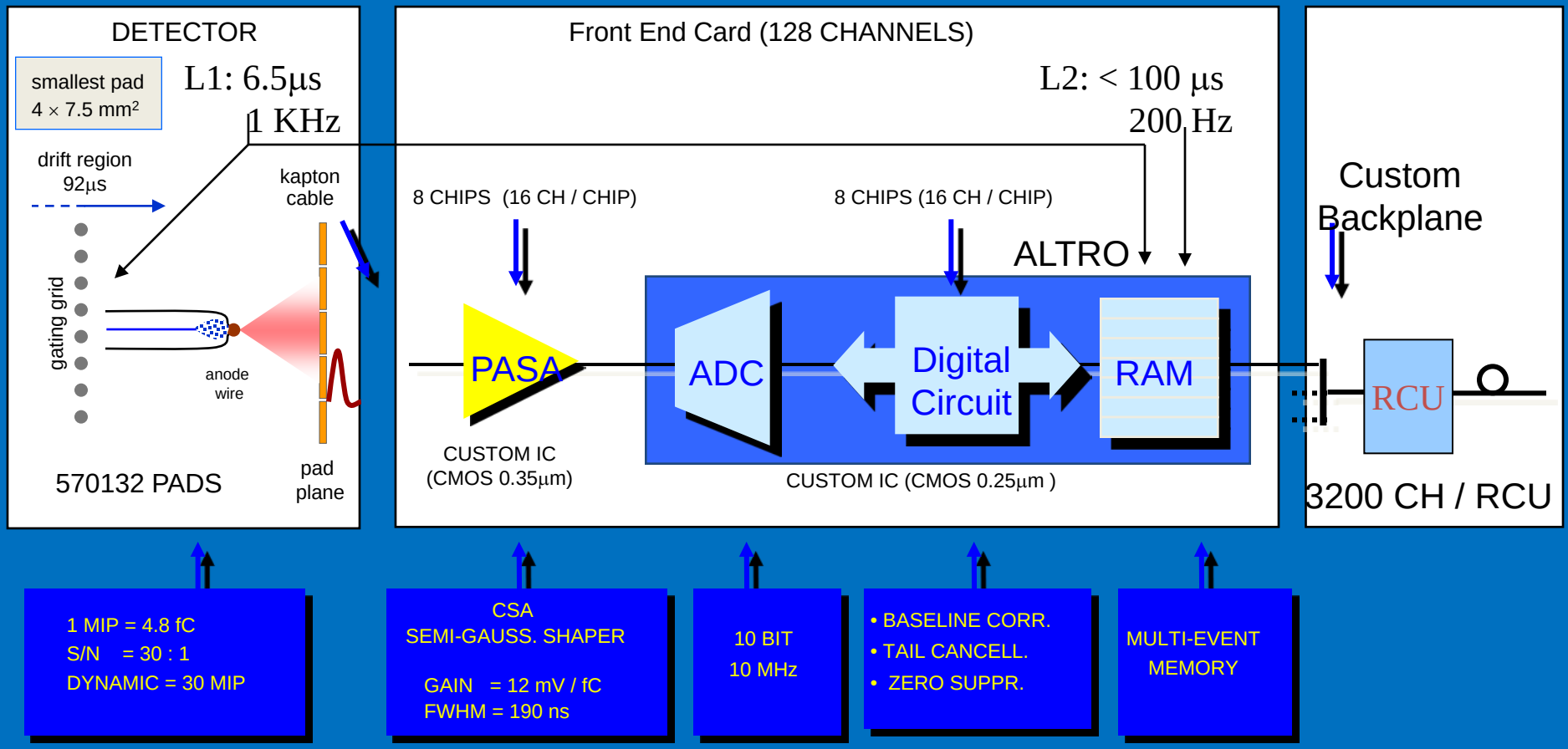
- **The 16 channel Super-ALTRO Demonstrator has been designed, prototyped and tested successfully!!**
- **The chip is already usable for the Linear Collider TPC prototype.**
  The area is 3.07mm^2/channel (LCTCP requirement: <4mm^2)
- **Using appropriate design techniques, integration of low-noise analog components and digital functions is possible with little effect on noise performance.**
- **Power pulsing approach has been demonstrated effective in reducing the power consumption, while preserving the performance.**

Ref:

LC note (http://www-flc.desy.de/lcnotes) LC-DET-2012-077 (pre-print).
"Super-Altro 16: a Front-End System on Chip for DSP Based Readout of Gaseous Detectors" accepted for publication in IEEE Trans Nucl Sci.

Back-up slides

Alice TPC: ALTRO

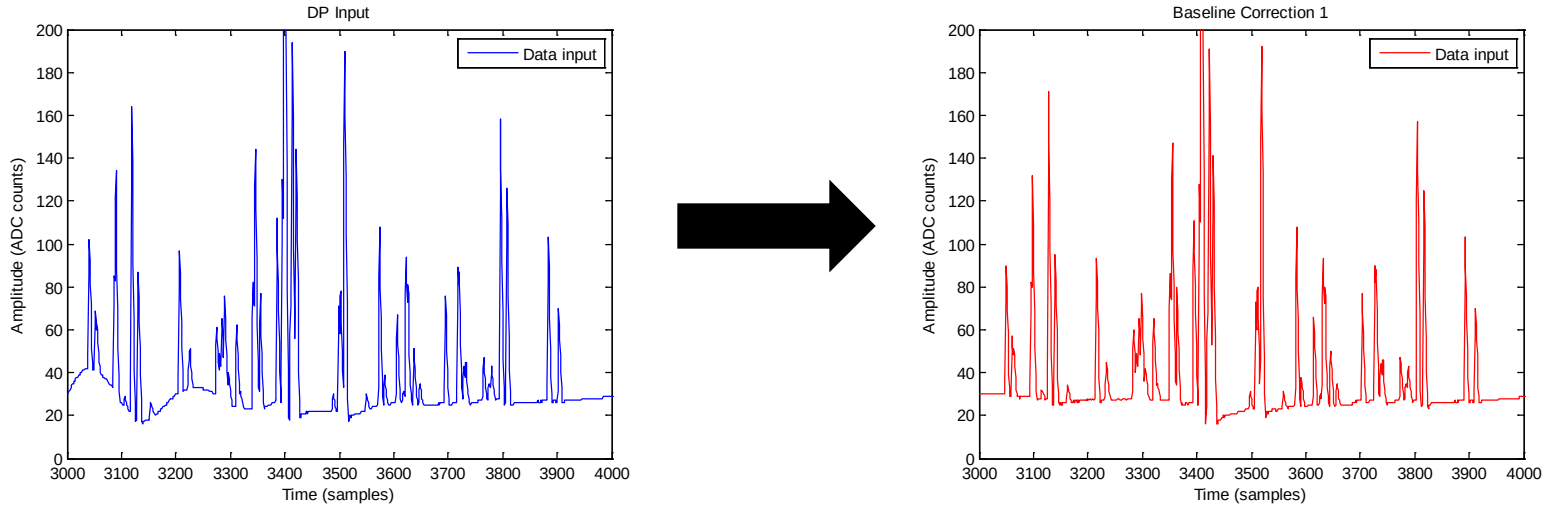


PreAmplifier Shaping Amplifier = PASA
ALice Tpc Read Out = ALTRO
Two-chips system, 4x7.5mm² pads

IEEE Trans Nucl Sci Vol50 Num6 2003 pp2460-2469
Nucl Instr Meth A Vol535 2004 pp500-505

Baseline Correction 1 simulation

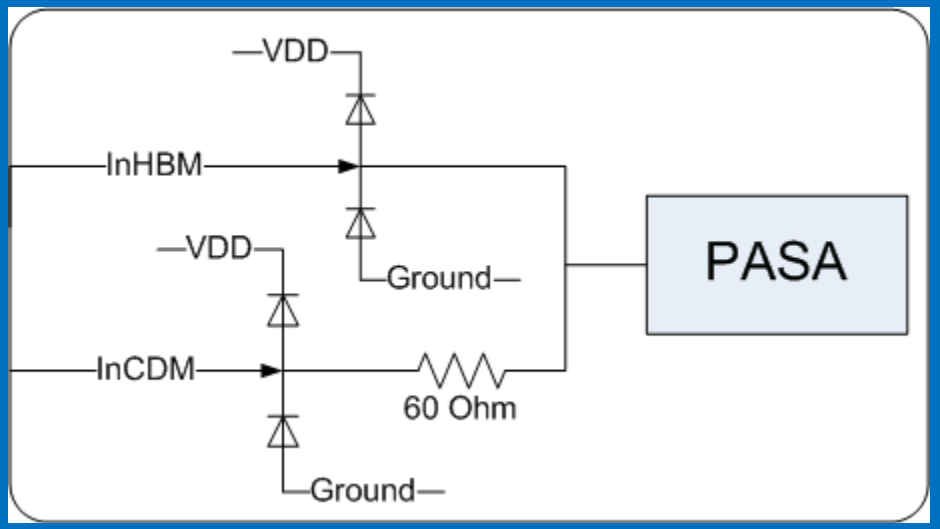
BC1 example test: subtract a systematic pattern.



PASA: ESD protections

Each PASA has two input pads in parallel (only one bonded):

- **Simple double diode protection scheme (Human Body Model)**
- **Structure with series resistor for enhanced protection (Charged Device Model)**

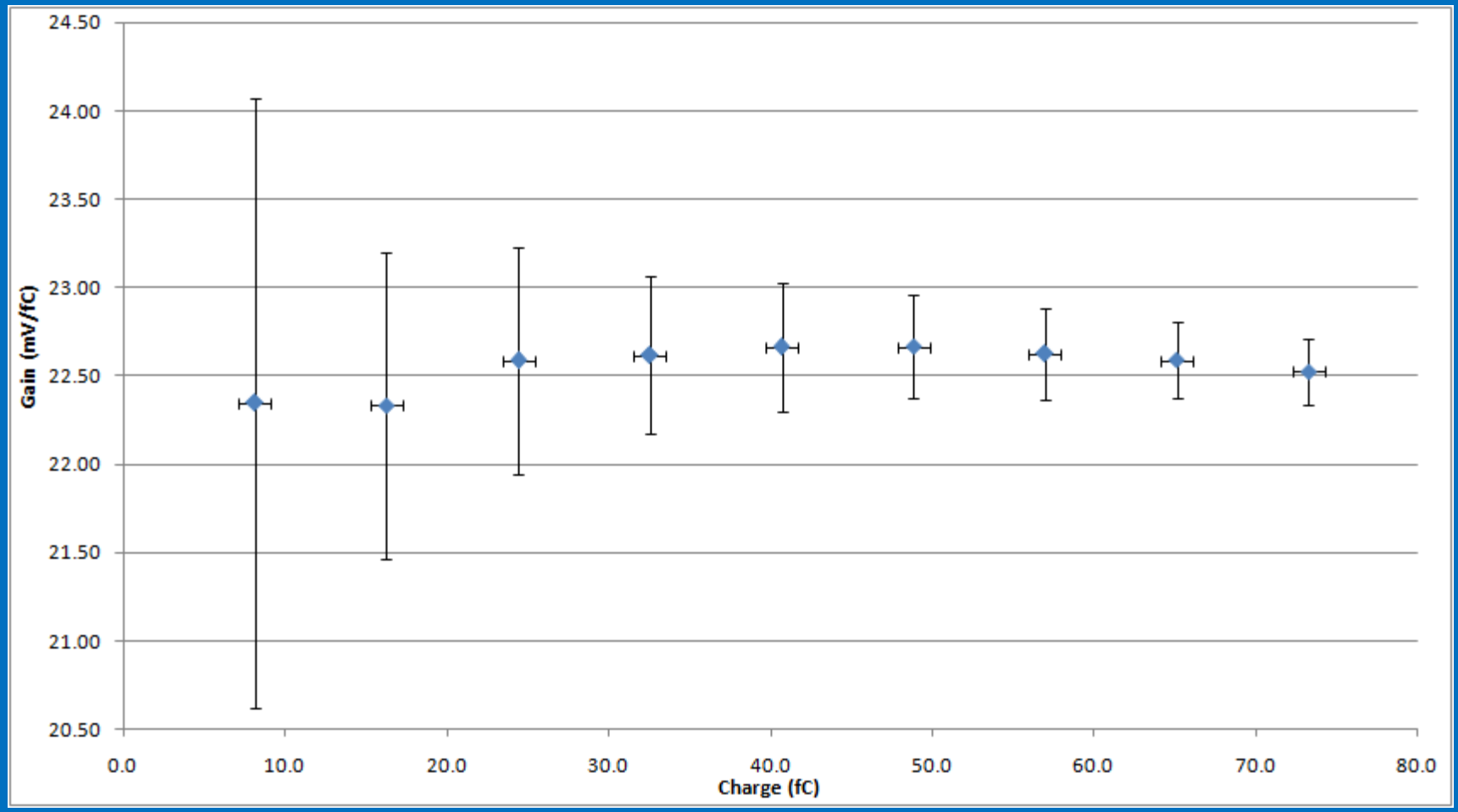


Drawback: the series resistor adds noise to the input signal.

PASA noise: 300e^- @ 10pF detector capacitance

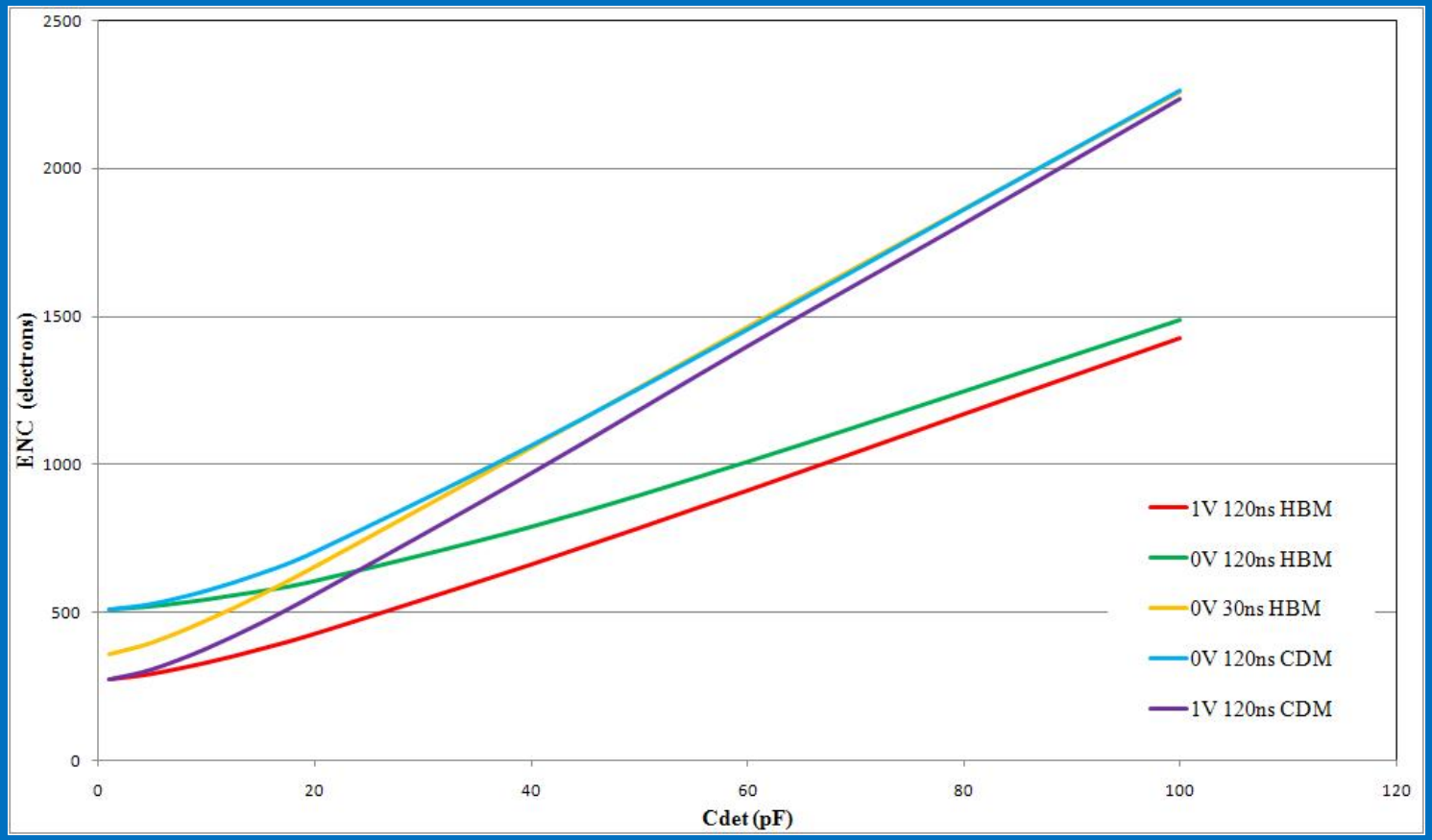
Noise increase (simulated): 20-30%

Gain measurement 2



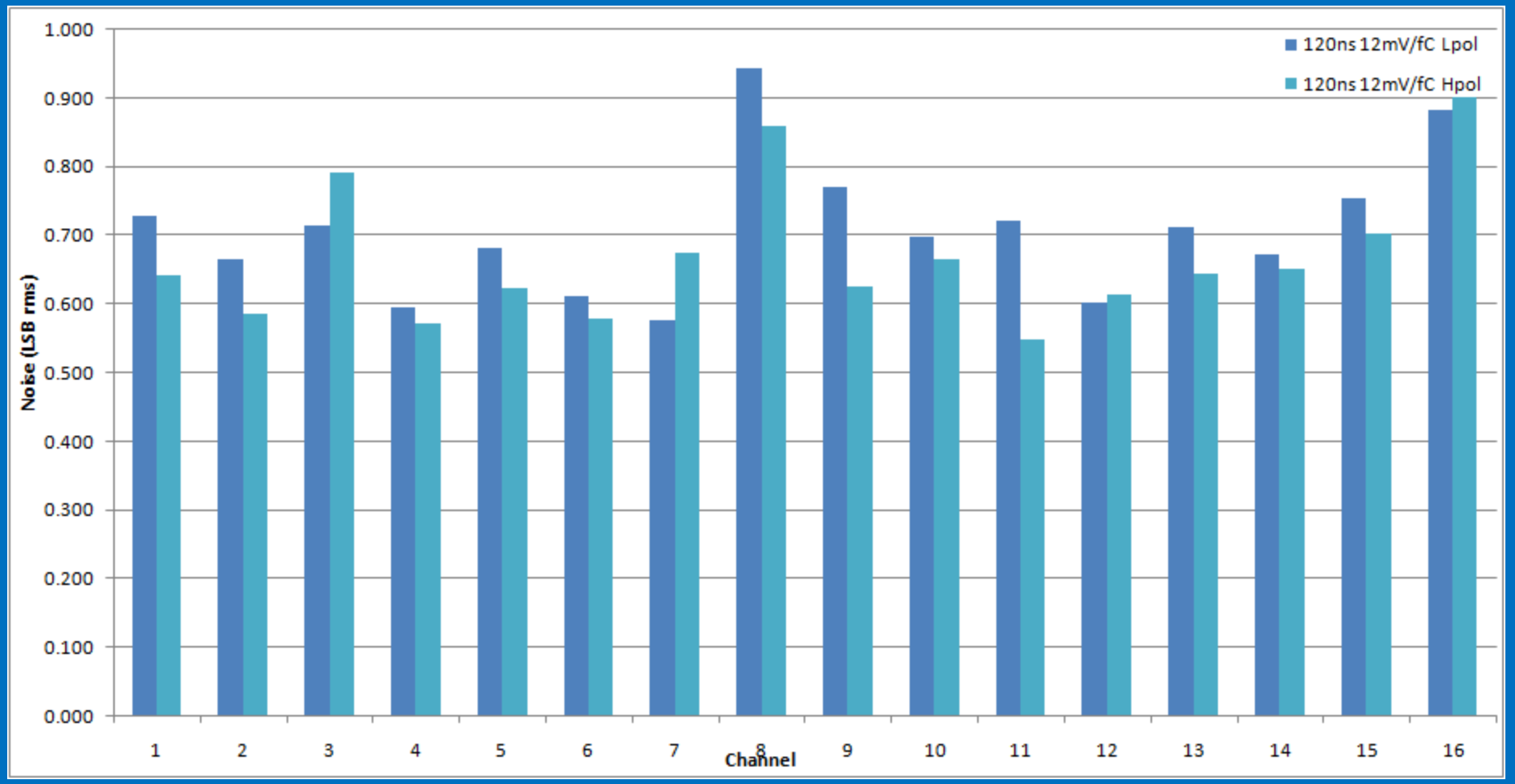
PASA configuration: 27mV/fC, 30ns, Low polarity.
Measured gain 22.5mV/fC±0.7%

PASA: Equivalent Noise Charge



Simulations: dependency of the noise on detector capacitance, shaping time, feedback resistance, and type of ESD protection

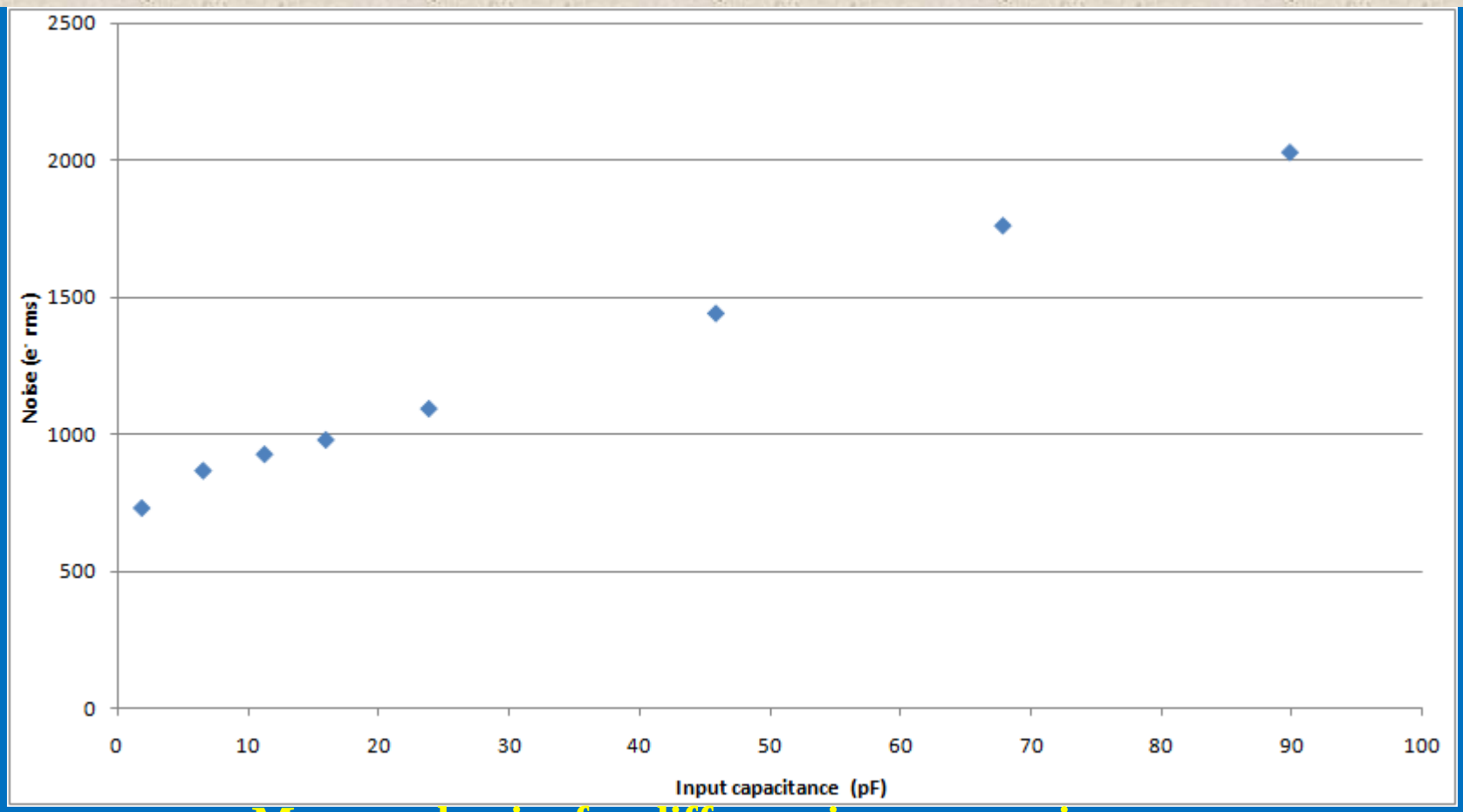
Noise: PGA4



PGA4 inputs bonded

Noise variation with the channel number

Noise: PGA4

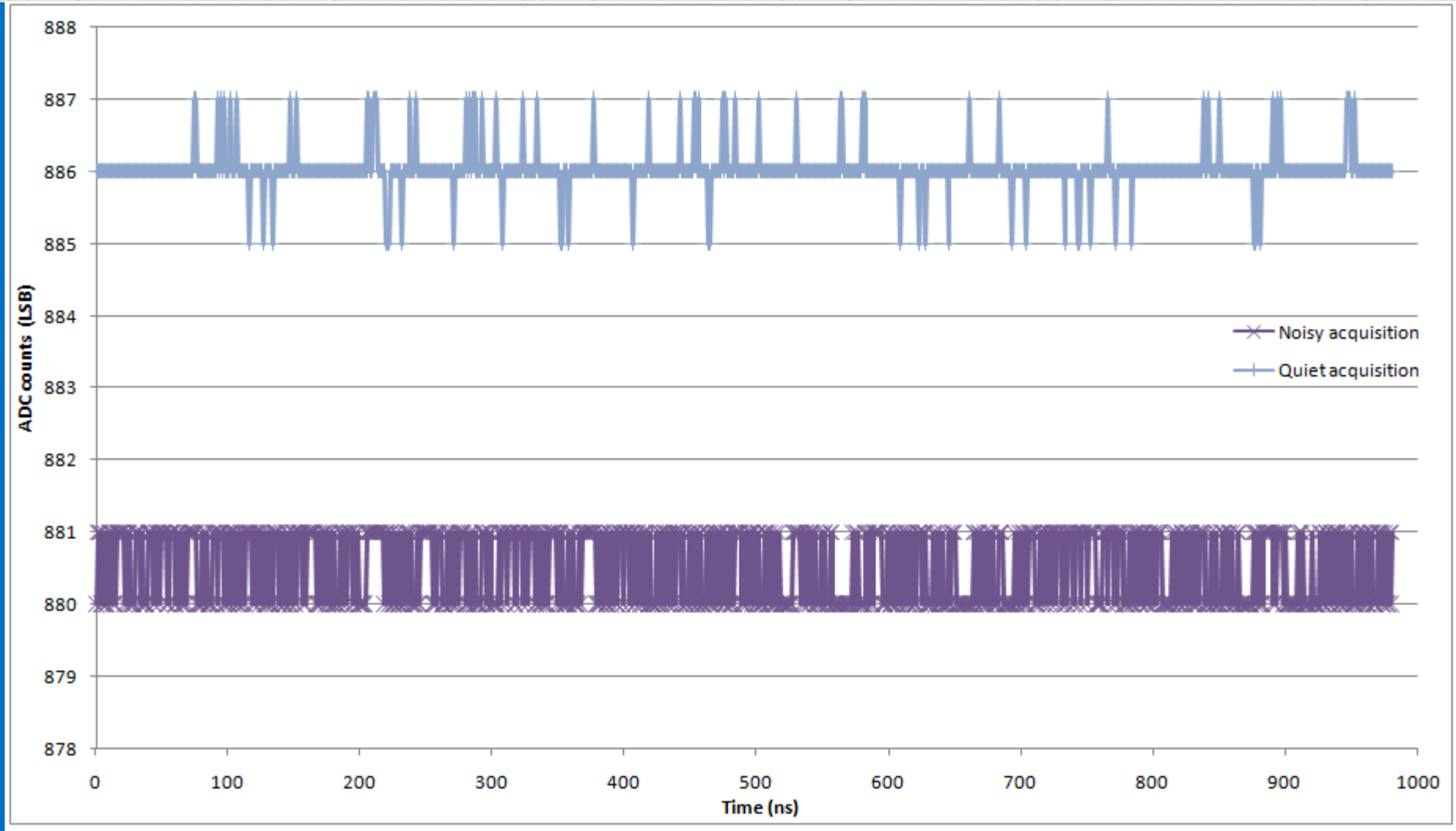


Measured noise for different input capacitances.

PGA4, Channel 0, 120ns, 12mV/fC

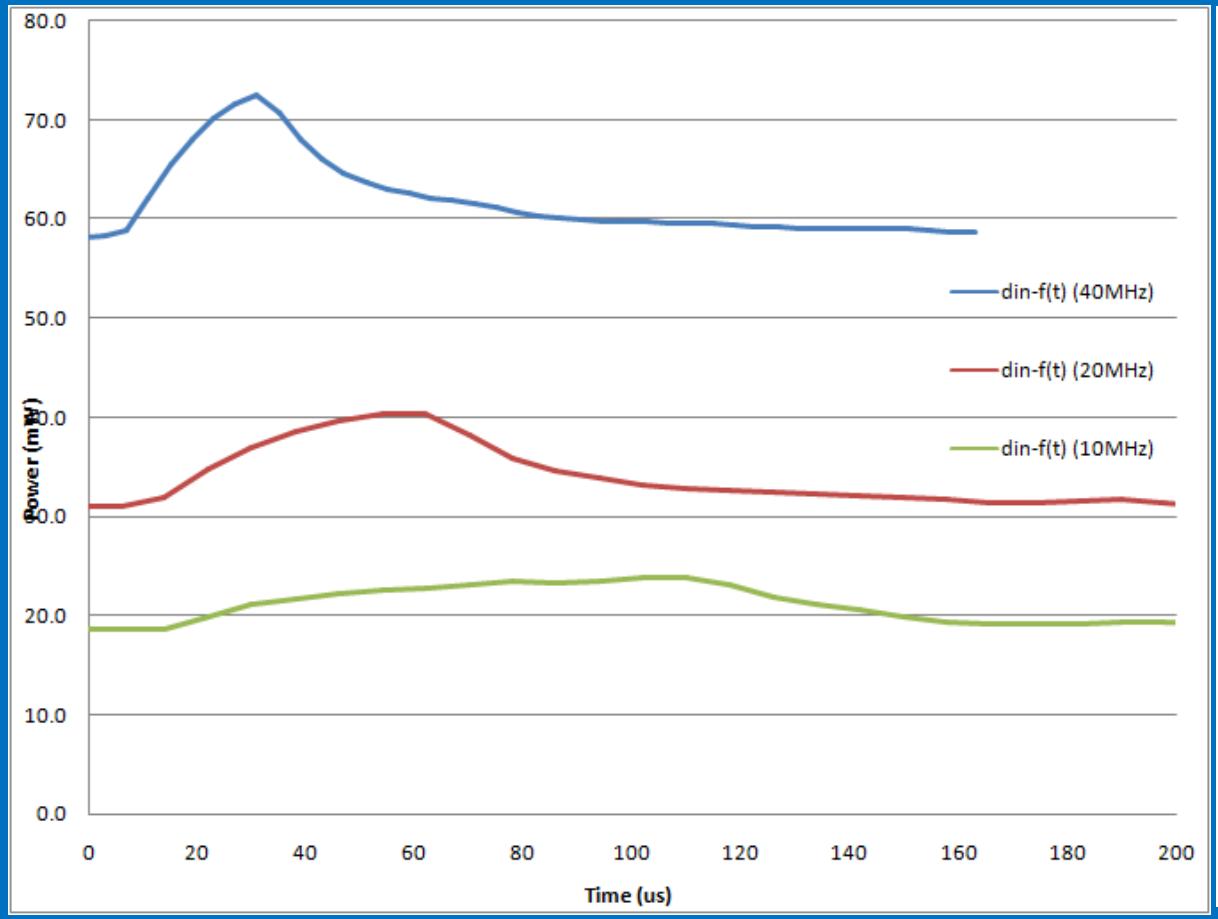
Slope: 15e$^-$/pF

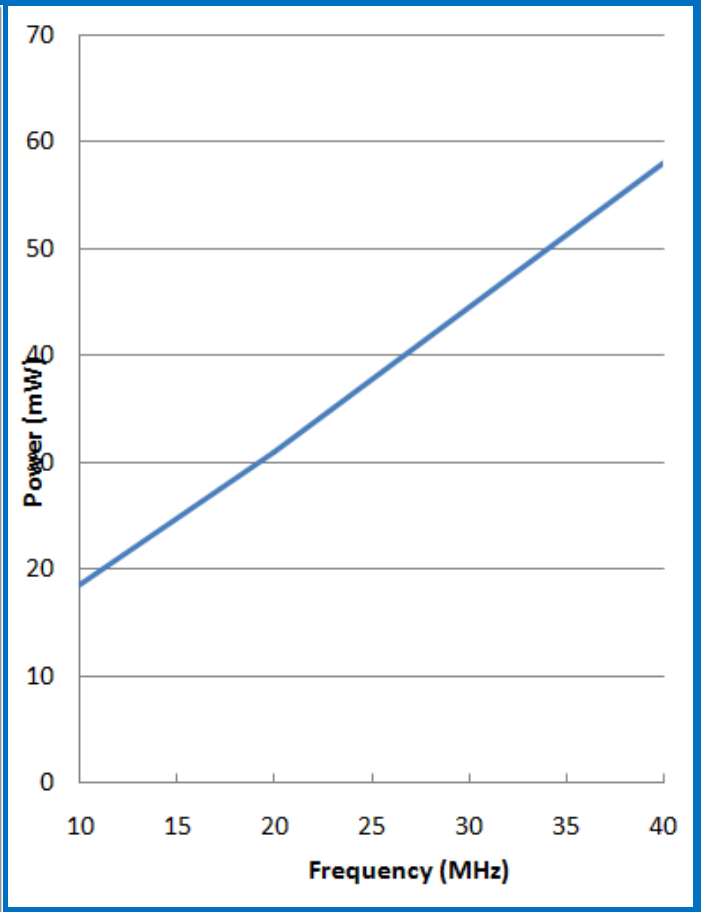
Noise: quantization



The influence of the ADC quantization on noise.

Power consumption: DSP





Power consumption of the DSP for different sampling clock frequencies.
DSP configuration: (Data In) – (Look-Up Table).

Zero Suppression example