Vertex-Detector R&D for CLIC

LCWS 2012

October 23, 2012
Arlington, Texas

Dominik Dannheim (CERN)
for the CLIC Physics and Detector study

Outline

- Vertex-detector requirements
- Background conditions
- Simulation layouts
- Readout-technology R&D
- Sensor-simulation studies
- Power delivery / power pulsing

More on CLIC vertex R&D in following talks:

- Massimiliano De Gaspari: Hybrid pixel readout chips
- Fernando Duarte Ramos: Mechanics & cooling

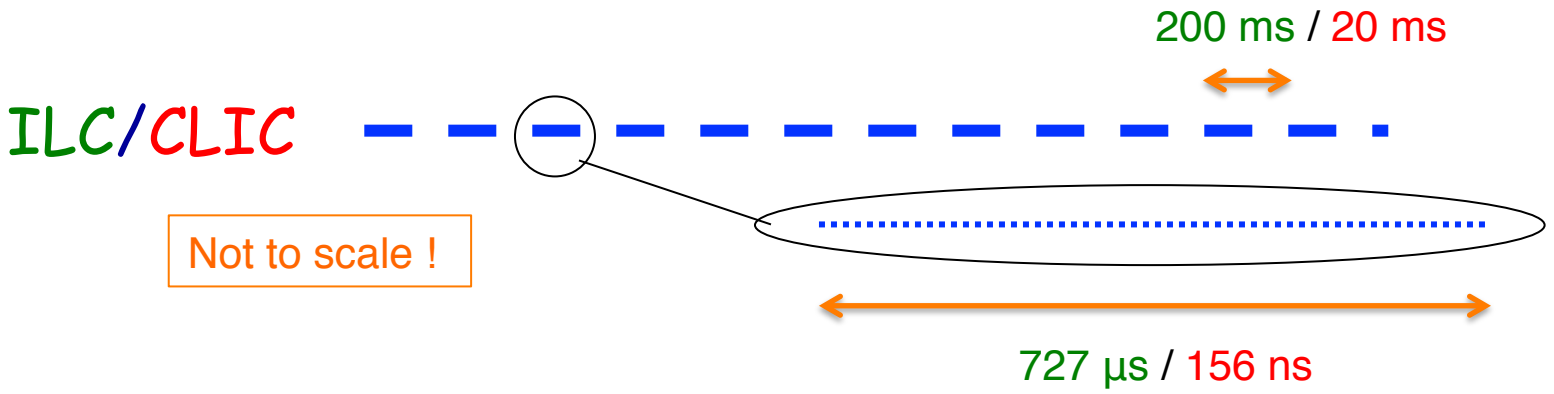
ILC and CLIC machine environment

	ILC at 500 GeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	$2x10^{34}$	$6x10^{34}$
BX separation	554 ns	0.5 ns
#BX / train	1312	312
Train duration	727 µs	156 ns
Train repetition rate	5 Hz	50 Hz
Duty cycle	0.36%	0.00078%
σ_x / σ_y (nm)	474 / 6	≈ 45 / 1
σ_z (µm)	300	44

drives timing requirements for detectors

very small beam sizes

ILC ESD-2012/2 / CLIC CDR

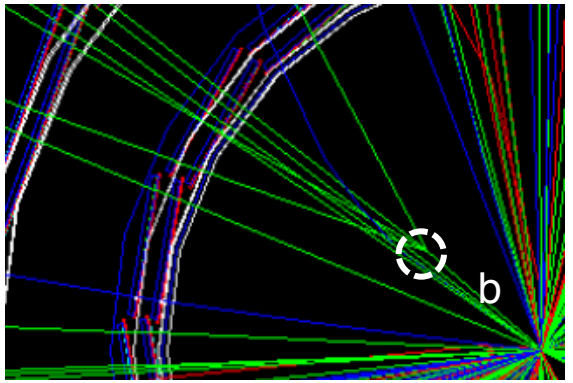


CLIC vertex-detector requirements

- Integral part of tracking systems (in particular for low p_T)
- Efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \approx 5\mu m \quad b \approx 15\mu m$$



→ Good single point resolution: σ_{SP}~3 µm
→ Small pixels ~25x25 µm, analog readout
→ Low material budget: X ≲ 0.2% X_0 / layer
→ Corresponds to ~200 µm Si, including supports, cables, cooling
→ Low-power ASICs (~50 mW/cm²) + air-flow cooling

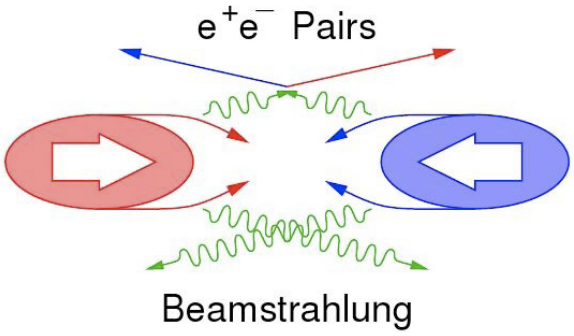
- 156 ns bunch trains, 20 ms gaps → trigger-less readout, pulsed powering
- Time stamping with ~10 ns accuracy, to reject background (see following slides)
→ high-resistivity sensors, fast readout
- B = 4-5 T → Lorentz angle becomes important
- Full coverage down to low polar angles θ_{min}~7° → Barrel + EC geometry

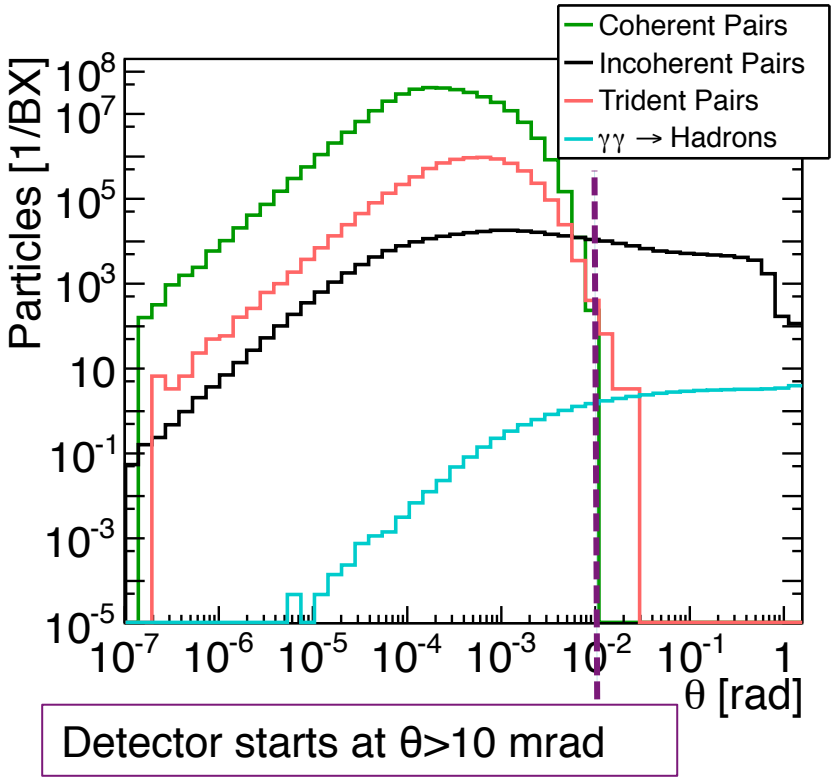
- To date: no technology option available fulfilling all requirements

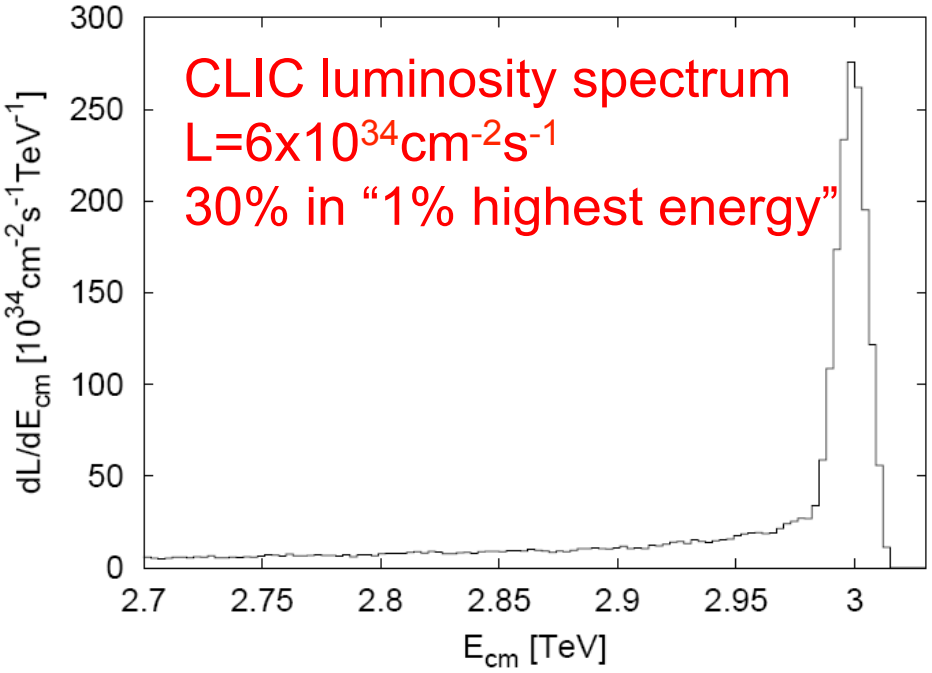
→ Simulation studies: impact of layout on performance
→ R&D on sensors & readout
→ Integration/Assembly + power-pulsing + cooling studies

Beam-induced backgrounds

e^+e^- pairs and $\gamma\gamma \rightarrow$ hadrons at $\sqrt{s}$=3 TeV





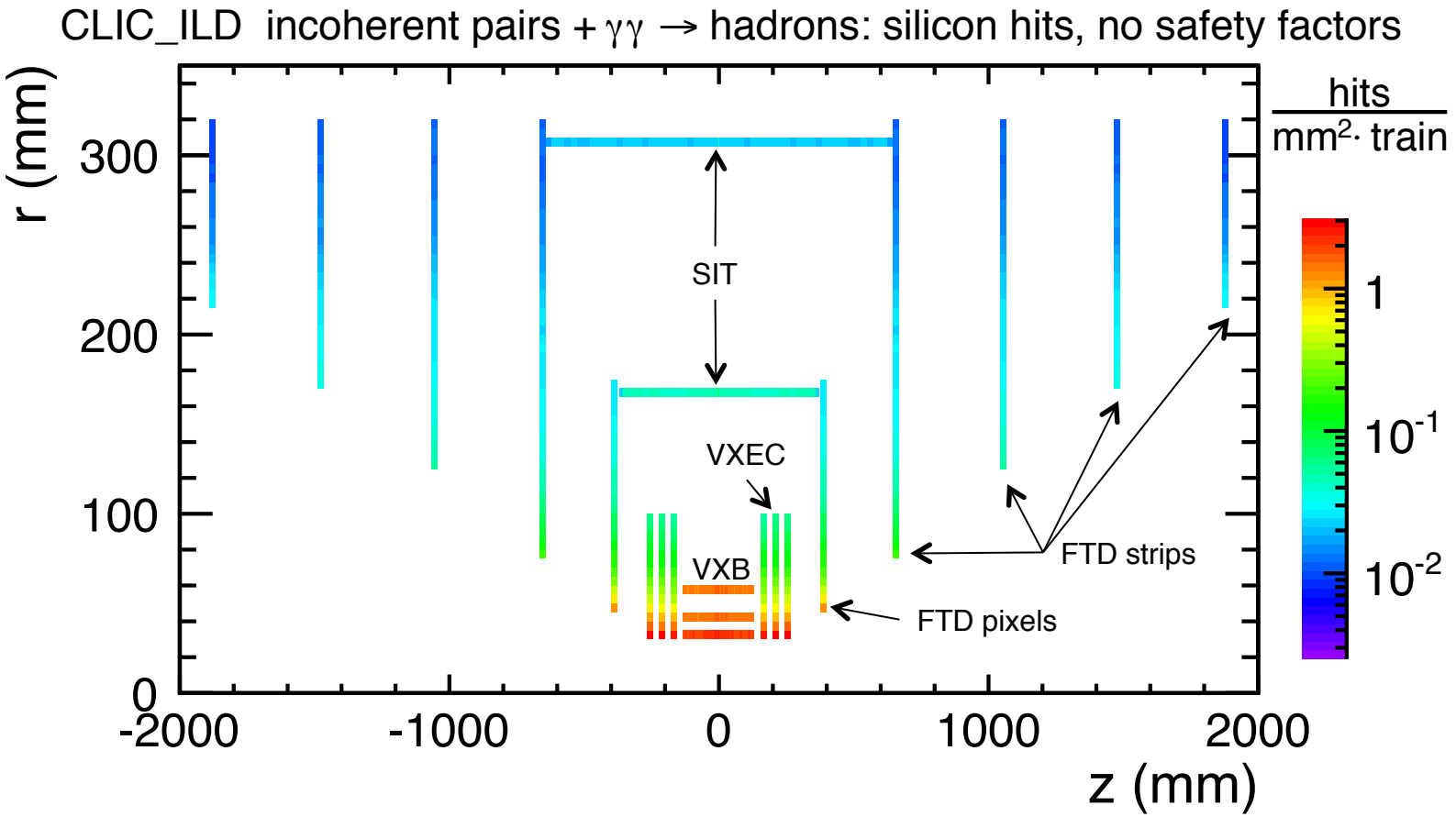


Main backgrounds in inner detectors:

- **Incoherent e^+e^- pairs**: 60 particles / BX
- **$\gamma\gamma \rightarrow$ hadrons**: 54 particles / BX

→ Need **pile-up rejection**

Backgrounds in inner tracking region



- Large hit rates in vertex and forward regions:
  - 2-3% maximum pixel occupancy / train (incl. clustering + safety factors)

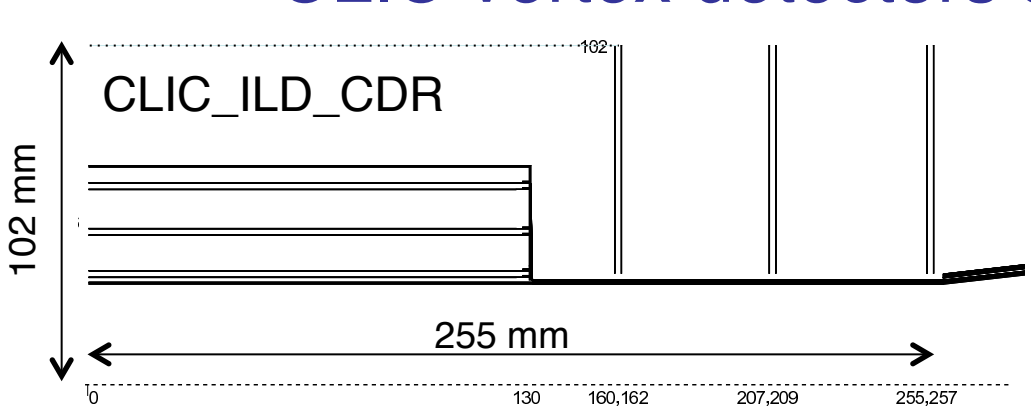
  → Constrains inner radius of beam pipe

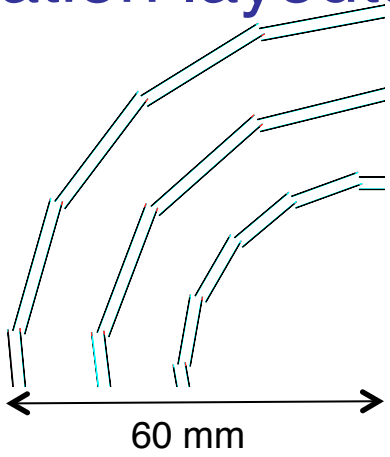
  → Drives design of forward region

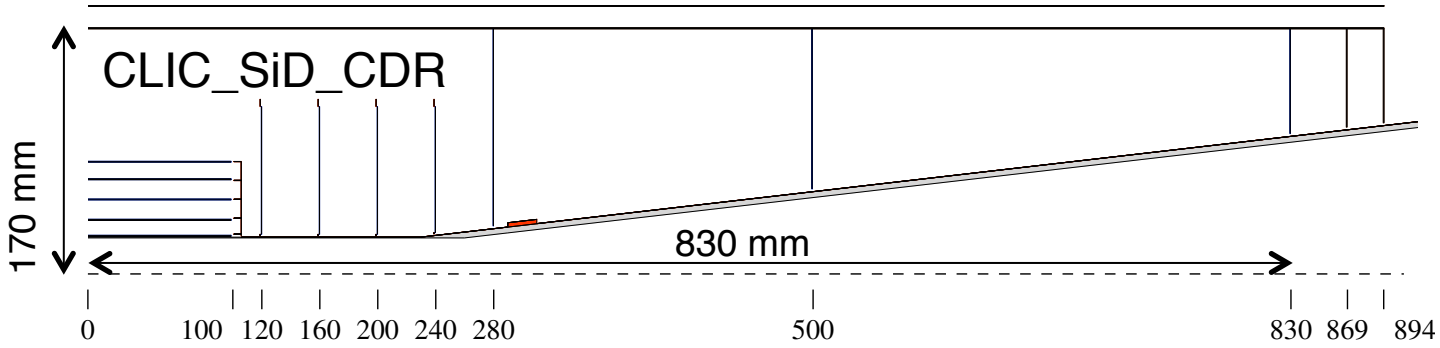
- Moderate radiation exposure:
  - NIEL: < 10^{11} $n_{eq}/cm^2/y$
  - TID: < 200 Gy / year

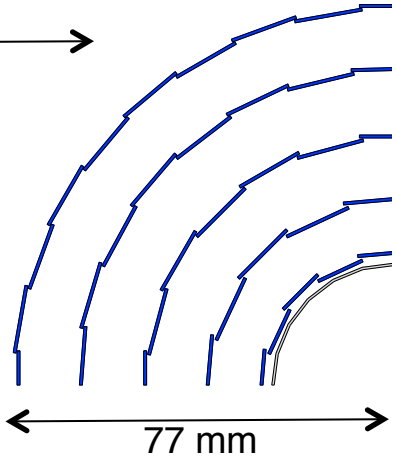
  (~10^4 below LHC!)

CLIC vertex detectors simulation layouts





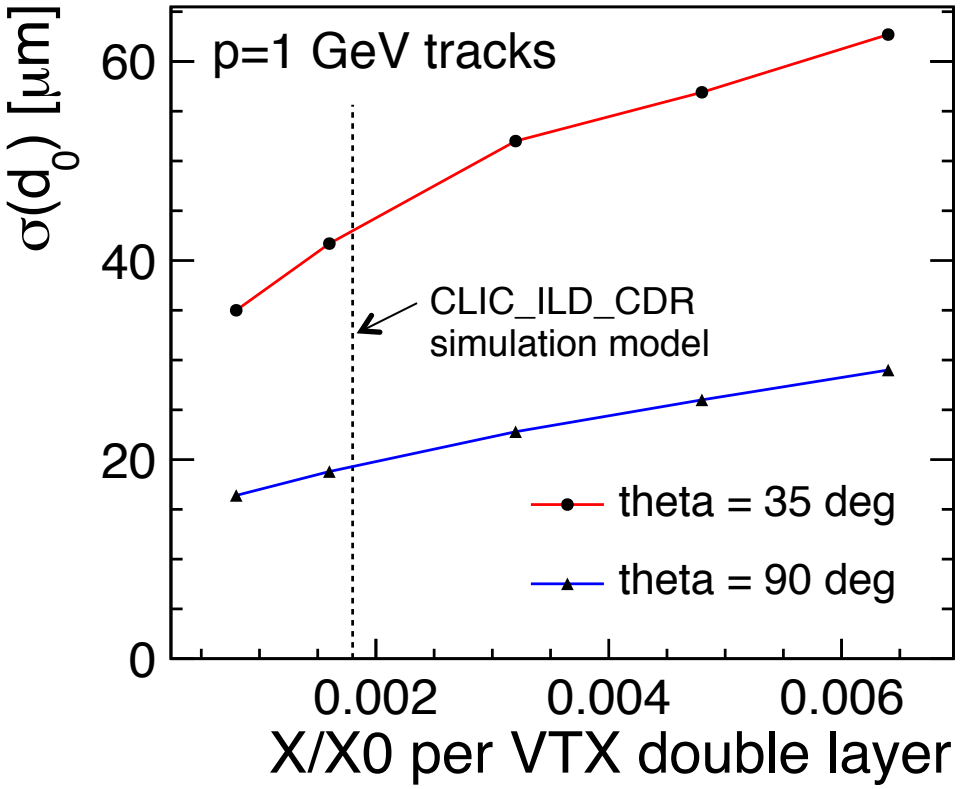




	CLIC_ILD_CDR	CLIC_SiD_CDR	CMS
Material X/X0 (90°)	~0.9% (3x2 layer)	~1.1% (5 layer)	~10% (3 layer)
Pixel size	20 x 20 μm^2	20 x 20 μm^2	100 x 150 μm^2
# pixels	2.03 G	2.76 G	66 M
Time slicing resolution	~10 ns	~10 ns	<~25 ns
Avg. power/pixel	<~0.2 μW	<~0.2 μW	28 μW

Vertex-detector performance

d_0: distance of closest approach to interaction point in R-phi plane
→ d_0 resolution closely linked to heavy-flavor tagging performance
→ main benchmark parameter for vertex detector performance

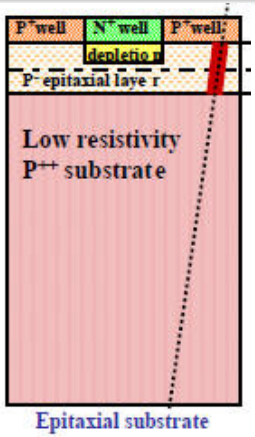


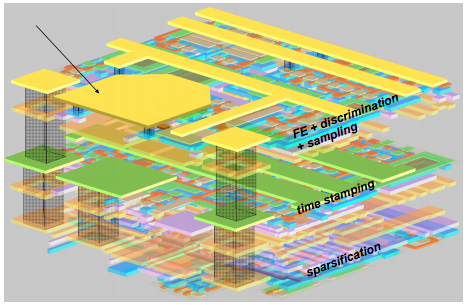
- Simulation models reach required performance
- Sensitivity to changes in design parameters:
  - Material budget
  - Single-point resolution
  - Distance to IP

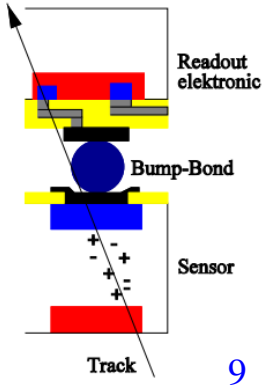
→ Parametric studies

Pixel-detector technologies

	Monolithic CMOS	3D-integrated	Hybrid pixel
Examples	DEPFET, FPCCD, MAPS, HV-CMOS	SOI, MIT-LL, Tezzaron, Ziptronix	Timepix3/CLICpix
Technology	Specialised HEP processes, r/o and sensors integrated	Customized niche industry processes, high density interconnects btw. tiers	Industry standard processes for readout; depleted high-res. planar or 3D sensors
Interconnect	Not needed	SLID, Micro bump bonding, Cu pillars	
granularity	down to 5 µm pixel size		~25 µm pixel size
Material budget	~50 µm total thickness achieveable		~50 µm sensor + ~50 µm r/o
Depletion layer	partial	partial or full	full → large+fast signals
timing	Coarse (integrating sensor)	Coarse or fast, depending on implementation	Fast sparsified readout, ~ns time slicing possible
R&D examples	ILC, ALICE, RHIC	ILC, HL-LHC	CLIC, ATLAS-IBL, HL-LHC







Medipix/Timepix hybrid r/o chip family

Chip	Year	Process	Pitch [μm²]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm IBM CMOS	55x55	∫TOT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm IBM CMOS	55x55	γ counting	Sequential (full frame)	Medical
Timepix3	2013	130 nm IBM CMOS	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	Medical, HEP
Smallpix	2013	130 nm IBM CMOS	~40x40	TOT + ToA, γ counting + ∫TOT	Sequential (data comp.)	Medical, HEP, XFEL
CLICpix demonstrator	2013	65 nm TSMC	25x25	TOT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
CLICpix	~2015	65 nm	25x25	TOT + ToA	Sequential (data comp.)	CLIC vertex detector

TOT: Time-Over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time stamping

- Taking advantage of smaller feature sizes:
  - Improved noise performance
  - Increased functionality and/or
  - Reduced pixel size
- Details in following talk by Massimiliano De Gaspari

Sensor simulation and digitization

Unprecedented combination of sensor+readout features:

- Thin sensors (~50 µm)
- small pitch (20-25 µm)
- fast shaping (<~50 ns)

→ Need to investigate:

- Charge rise time, collection efficiency, sharing between pixels, signal/noise
- Dependence on momentum, angle, E- and B-field

- Validation in test beam

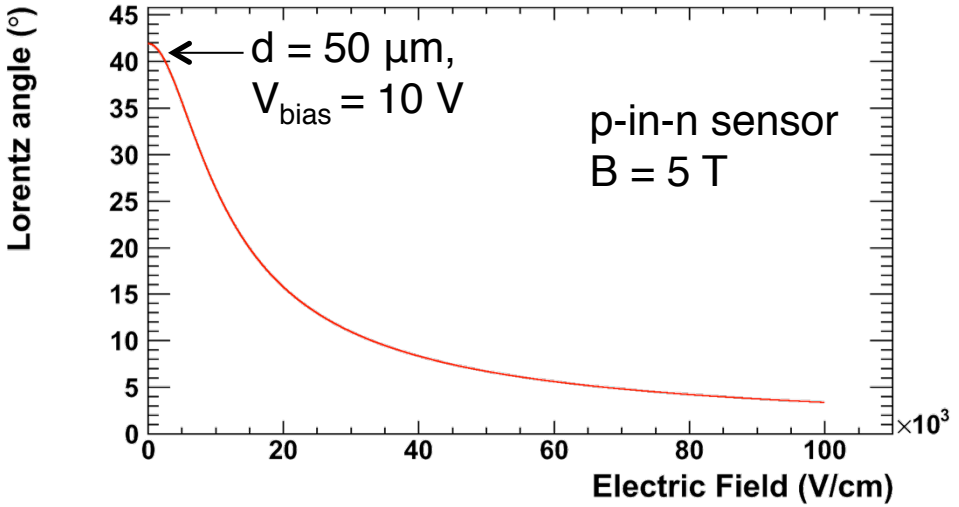
Simulation frameworks for pixel detectors:

- **Detailed TCAD simulation of thin pixel sensors**:
  Slow analytical approach, useful for tuning of simpler models
- **Monte-Carlo Charge Transport coupled to Static TCAD simulation**:
  ~fast, can be coupled to GEANT4, comparison with test-beam data
- **Geant4 simulation + Digitization model (Mokka / SLIC):**
  Fast, used for physics studies, needs calibration for sensor + r/o

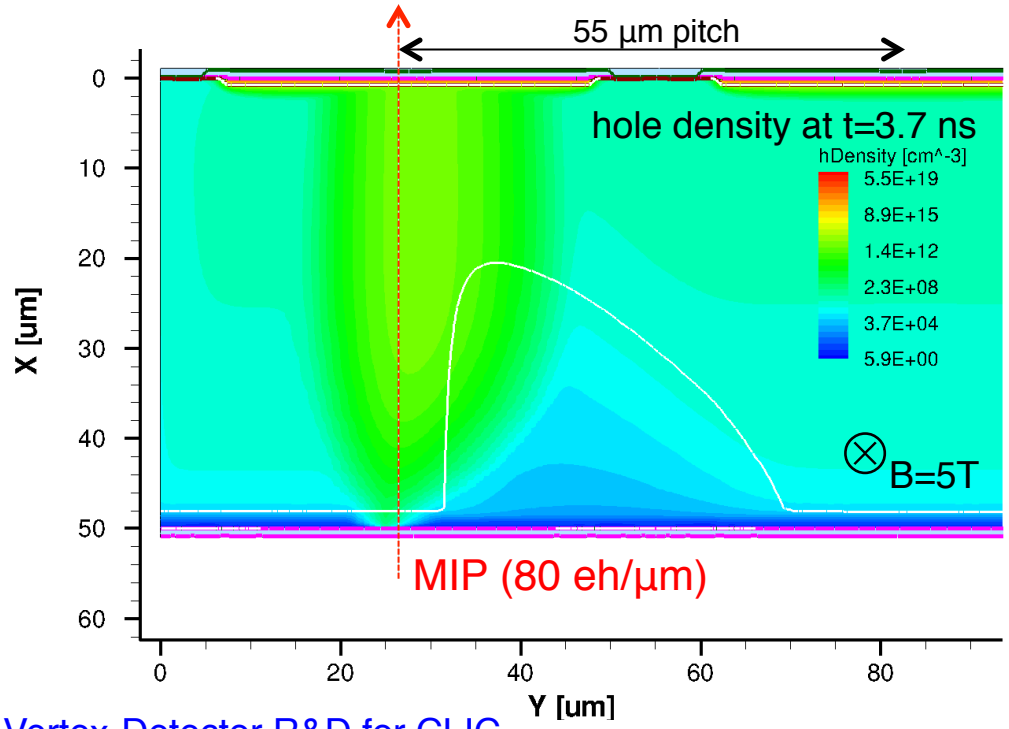
Silicon device simulation with TCAD

Example:
Hybrid detector with Timepix readout

p-in-n sensor (10 kΩcm)
50 µm thickness → V_{dep}~1 V
55 µm readout pitch
V_{bias}=10 V → E~2000 V/cm
Magnetic field: 5 T
→ θ_L~40°



- Spread of charge cloud due to Lorentz-angle effect
- Effect more pronounced for e^-
- Can be partially compensated by rotation of sensors with Lorentz angle
- Over-depletion reduces effect



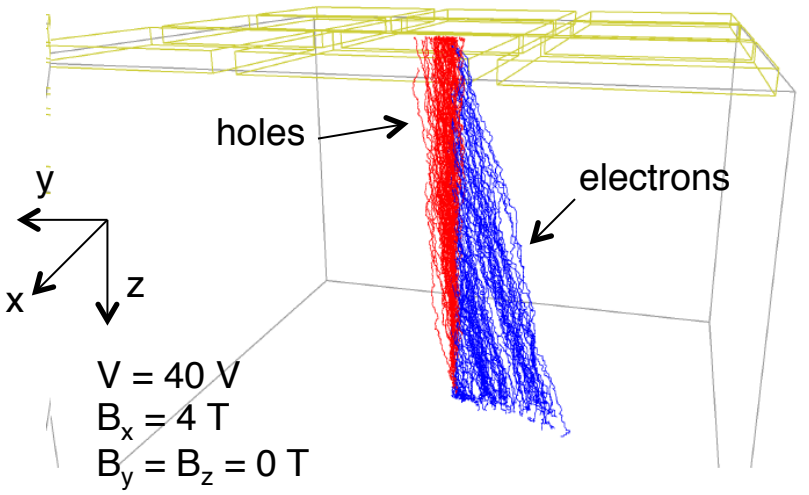
Monte-Carlo simulation of Charge Transport

- Simulate carrier drift in E+B field
- E-field from TCAD (previous slide)
- Takes into accout diffusion, mobility, trapping, repulsion

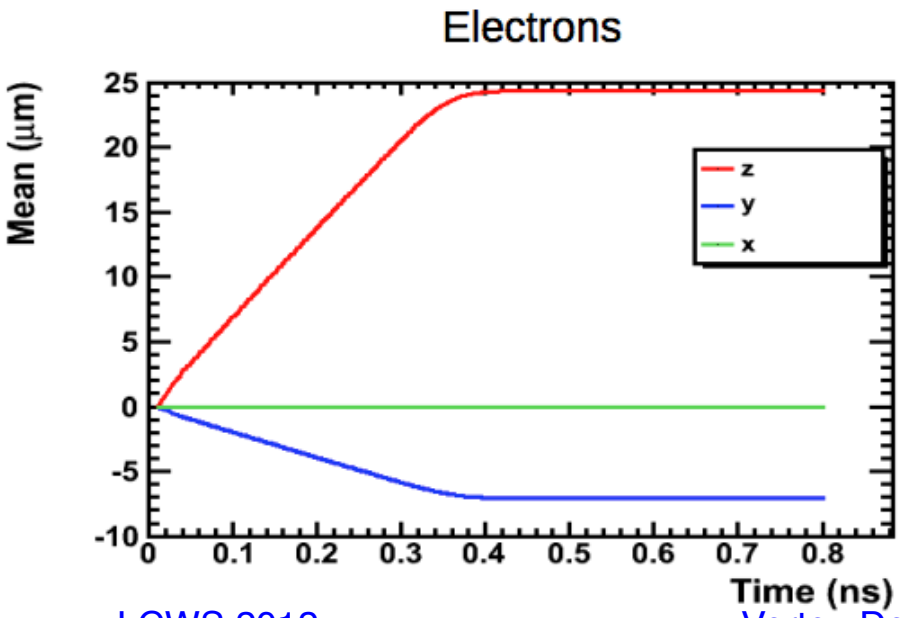
- Validation and simulation tuning in CERN SPS test-beam campaign (Timepix-based hybrid planar pixel sensor)

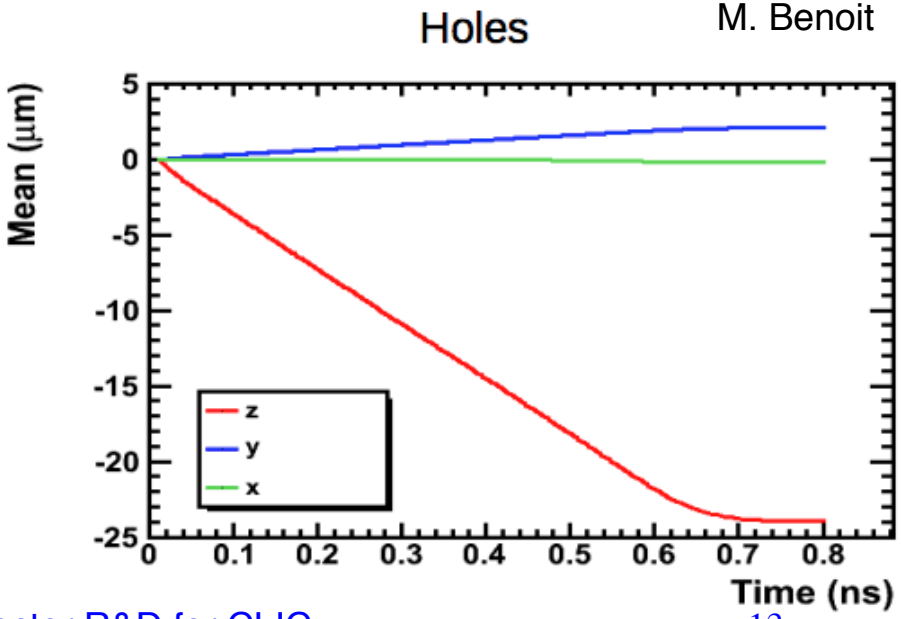
- Results will be implemented in Geant4-based full-detector simulation frameworks

Carrier drift in 50 µm thick fully depleted sensor:



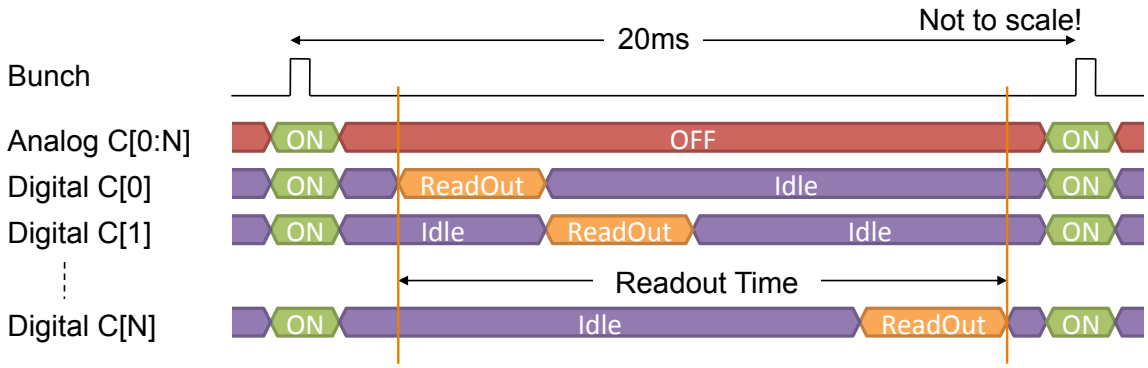
M. Benoit





CLICPix power-pulsing requirements

- Overall power budget (driven by air-flow cooling): $P_{avg} \sim 50$ mW / cm^2
- Estimation of power consumption for analog and digital blocks of CLICPix readout chip
- Based on measurements with 65 nm test-chip and projections from current Timepix
- Power pulsing with On/Idle/Off states, to reduce average power

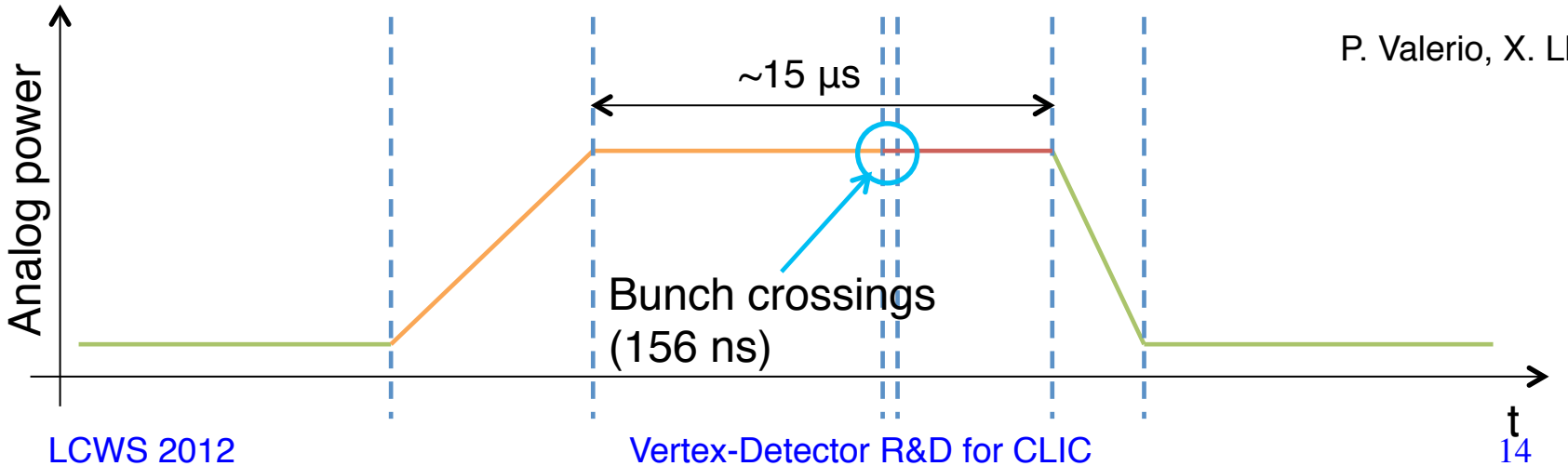


- Very small duty cycle for analog power
  → Favors local energy storage

Bunch Train (3.0 W/cm²)	
Pixel Analog	ON
Pixel Digital	ON
Periphery Analog	ON
Periphery Digital	ON
IO LVDS Pads	OFF

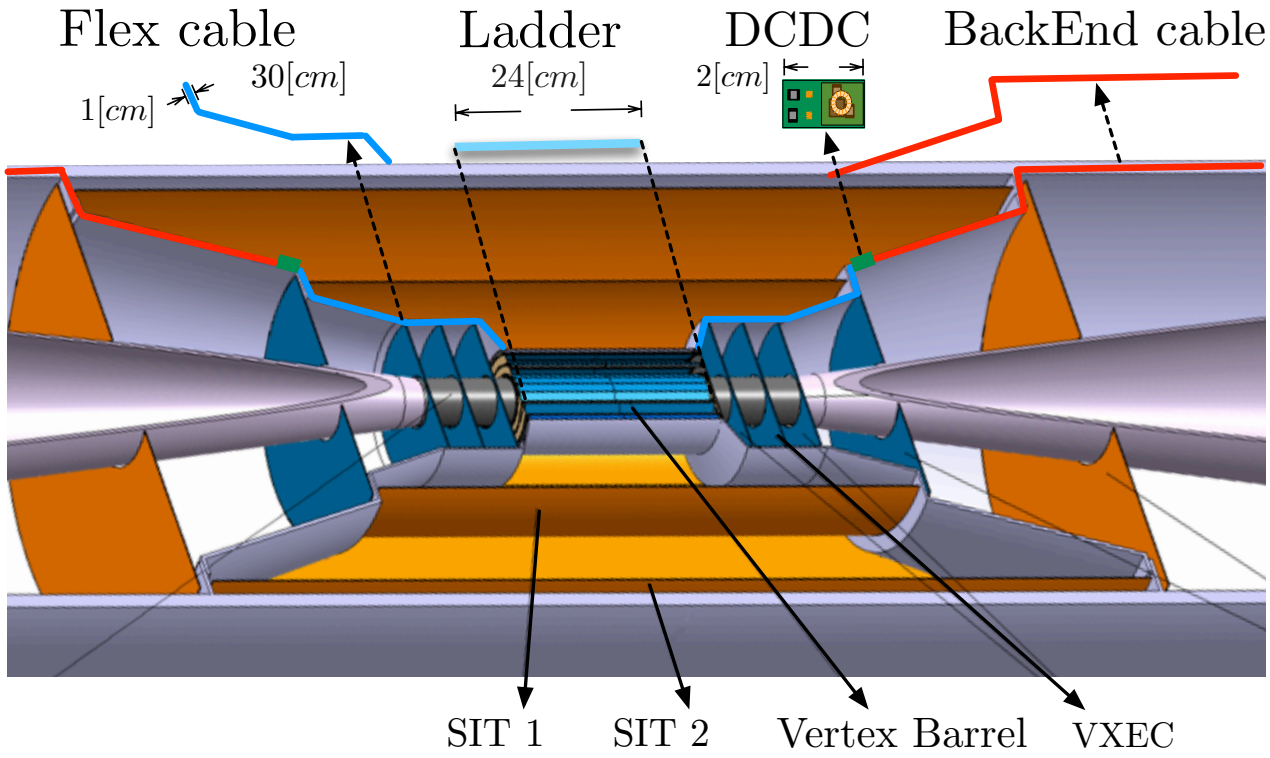
Chip Readout (360 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	ON
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	ON

Idle (7.8 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	Idle
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	OFF

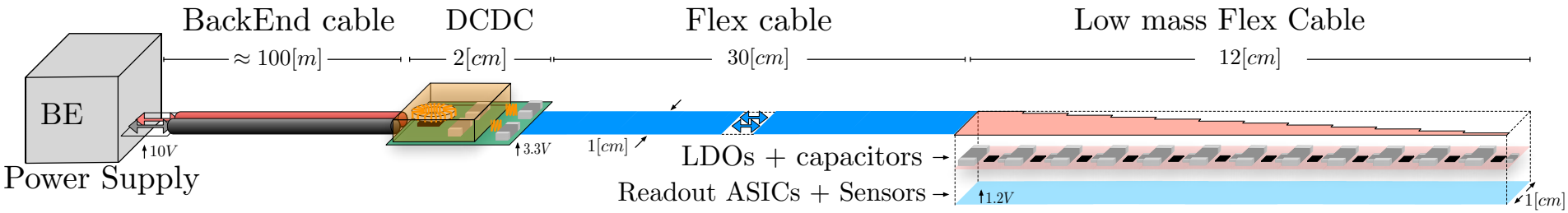


P. Valerio, X. Llopart

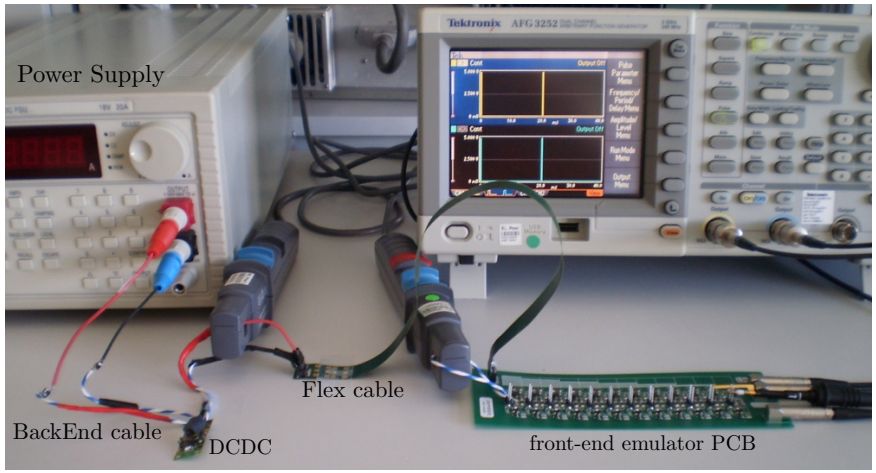
Power-pulsing and power-delivery scheme

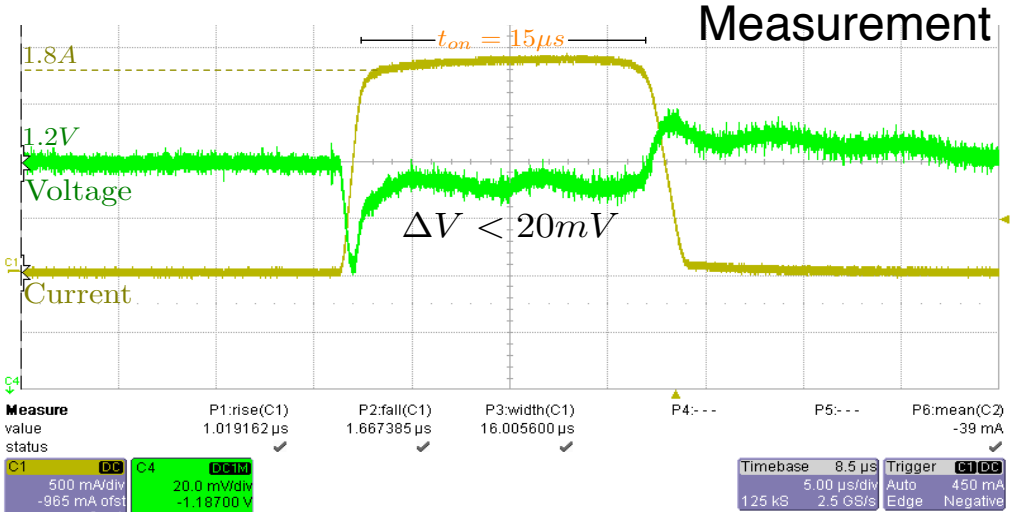


- DC/DC converters outside pixel-sensor area
- Flexible Kapton cables with Al conductor for power delivery
- Power pulsing, to reduce average power consumption
- local energy storage and voltage regulation with Si capacitors (~10 µF/chip) and LDO regulators



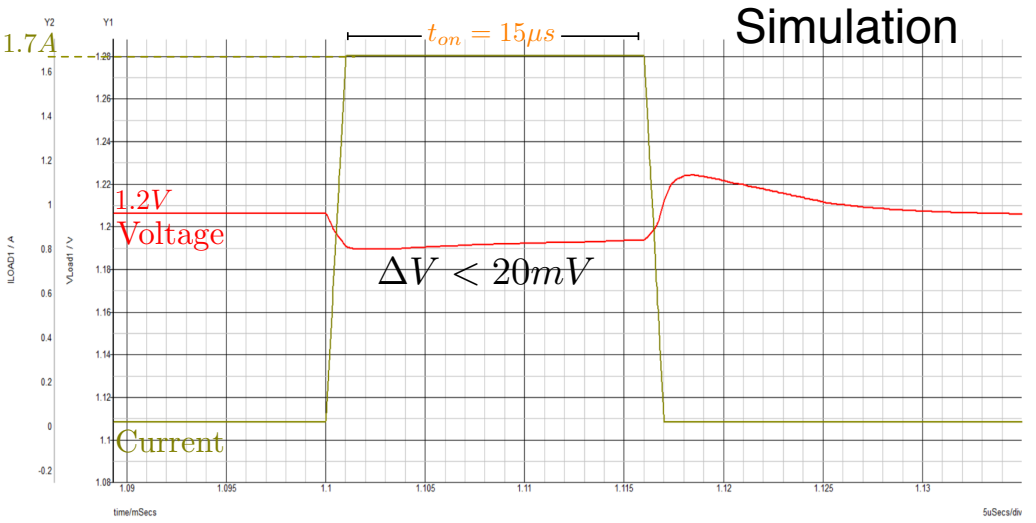
Power-pulsing and power-delivery tests





Test setup with active loads emulating analog pixel F/E:

- Equivalent thickness cable+LDO+cap.: 0.145% X0 / layer in vtx region
- Power pulsing at 50 Hz
- Load current of 2 A (half ladder) during 15 µs
- Monitor load voltages and currents
- Observed ripple ΔV< 20 mV, acceptable for CLICPix
- Agreement between measurement and simulation



C. Fuentes, G. Blanchot

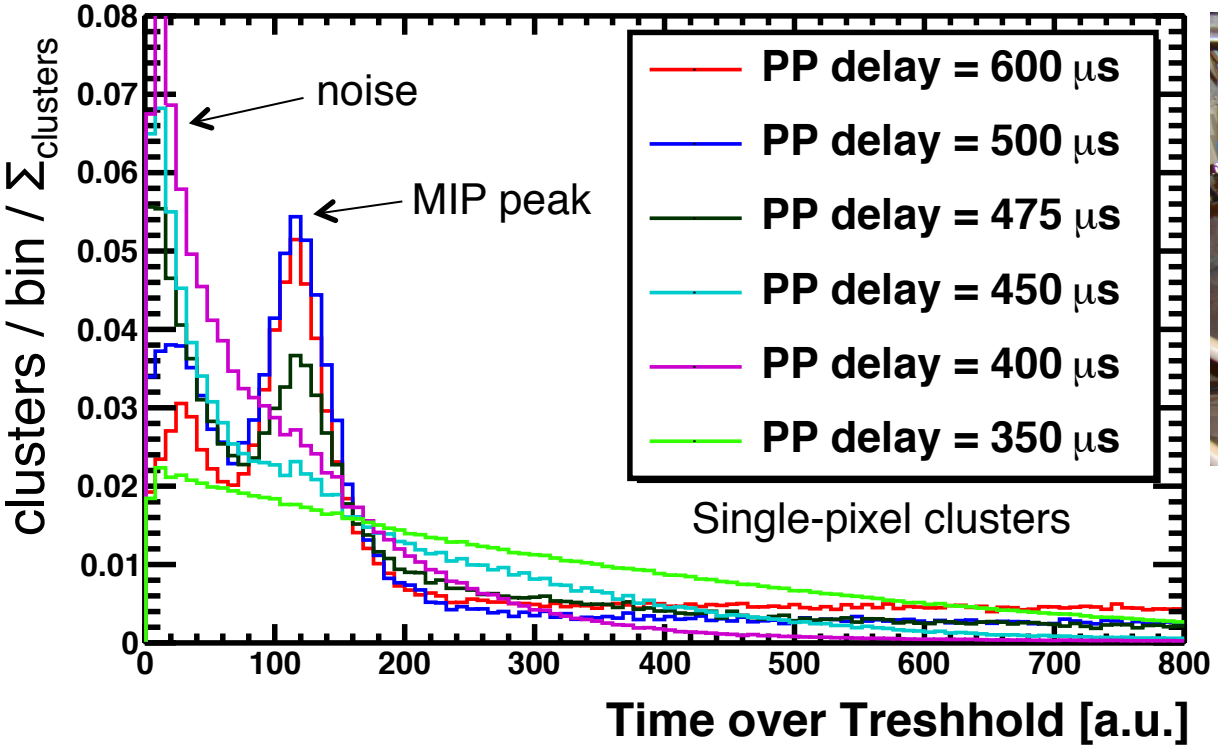
Power-pulsing in test beam

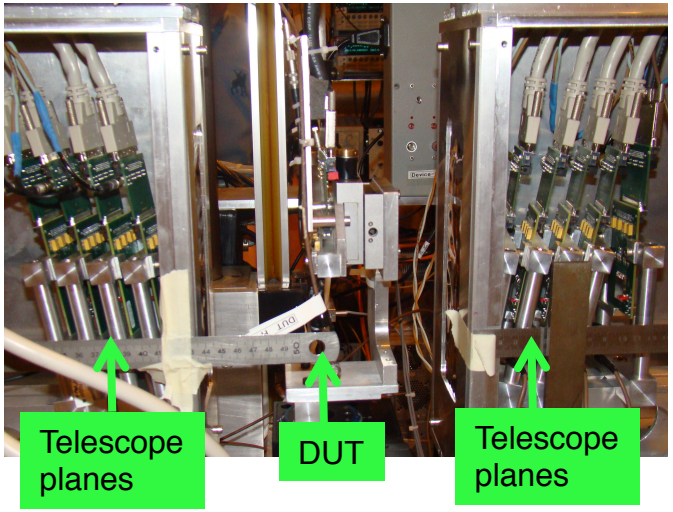
Power Pulsing with Timepix:

- Not designed for power pulsing, single bias line for all pixel rows
- But possibility to switch on/off all preamps through bias DAC

CERN SPS test-beam campaign in June 2012:

- Power pulsing of the Chip and operation in sync with LHCb/Timepix tracking telescope
- Shutter-based readout for 25 µs
- Adjustable delay between power-on and shutter-start times





- Fully efficient after ~600 µs
- Similar results obtained with source in laboratory and in simulation

M. Benoit

Summary / conclusions

- CLIC environment + physics requirements pose challenging demands on vertex-detector systems
- Presented initial layout proposals meeting those demands
- Examples for active R&D on:
  - Sensor + readout technologies
  - Silicon simulations
  - Power-delivery and power pulsing
- More details in CLIC vertex-detector working group presentations: http://indico.cern.ch/categoryDisplay.py?categId=2843 and in CDR: http://lcd.web.cern.ch/LCD/CDR/CDR.html

Backup slides

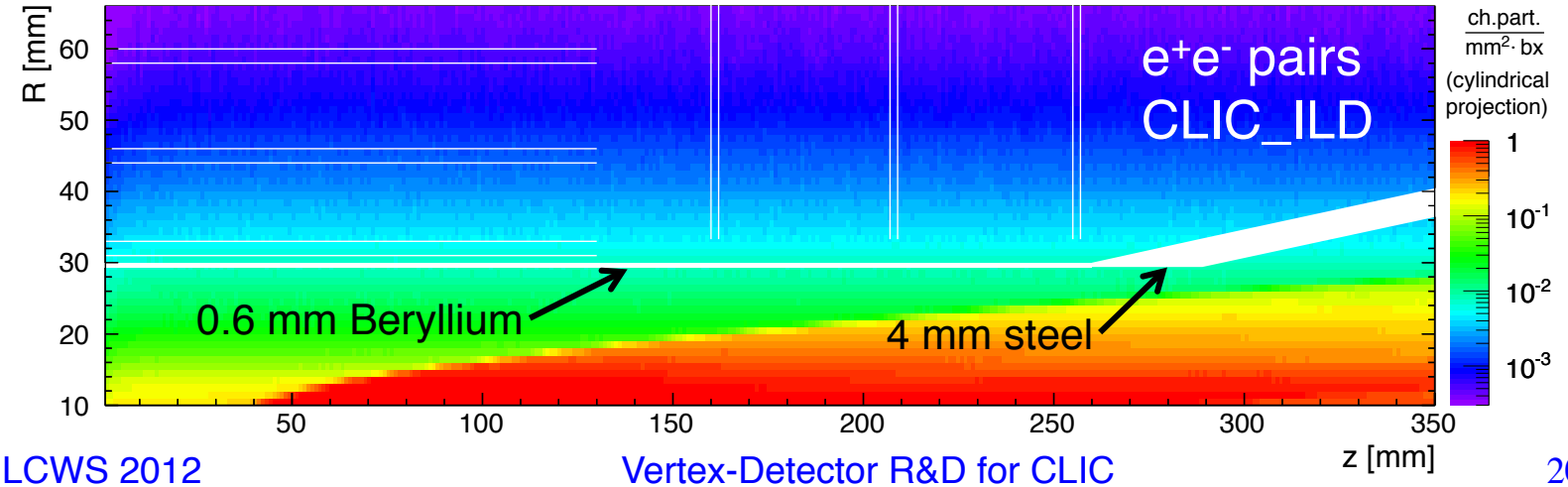
Beam pipe

Requirements for beam pipe:

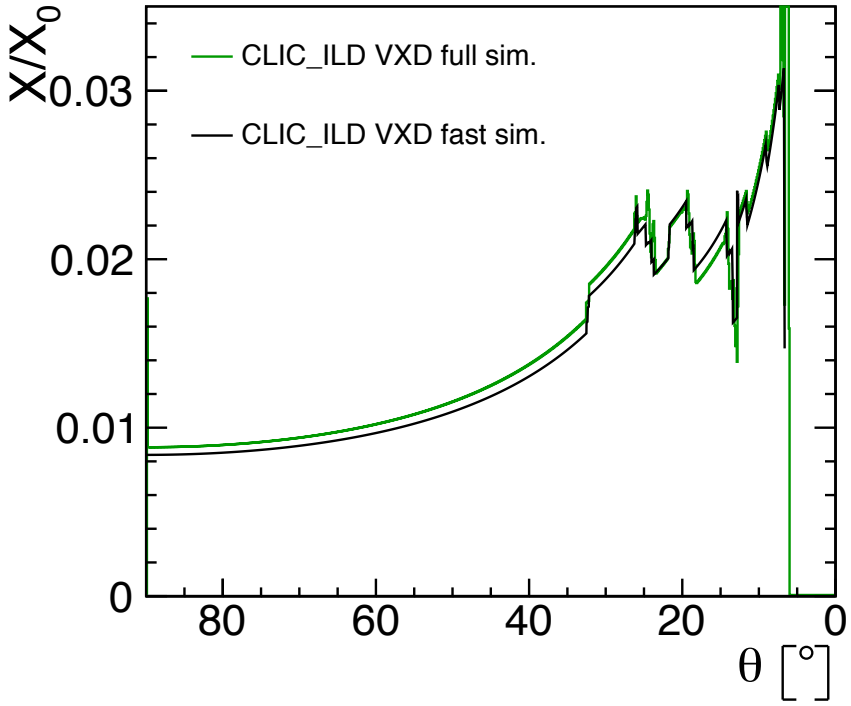
- Provide good vacuum → leak tightness
- Minimise multiple scattering → small amount of material in central part
- Allow for placement of Si layers close to IP → small radius
- Stay outside region of high background occupancy → lower limit on radius
- Shield against back scatters from forward region → thick conical part outside VTX acceptance

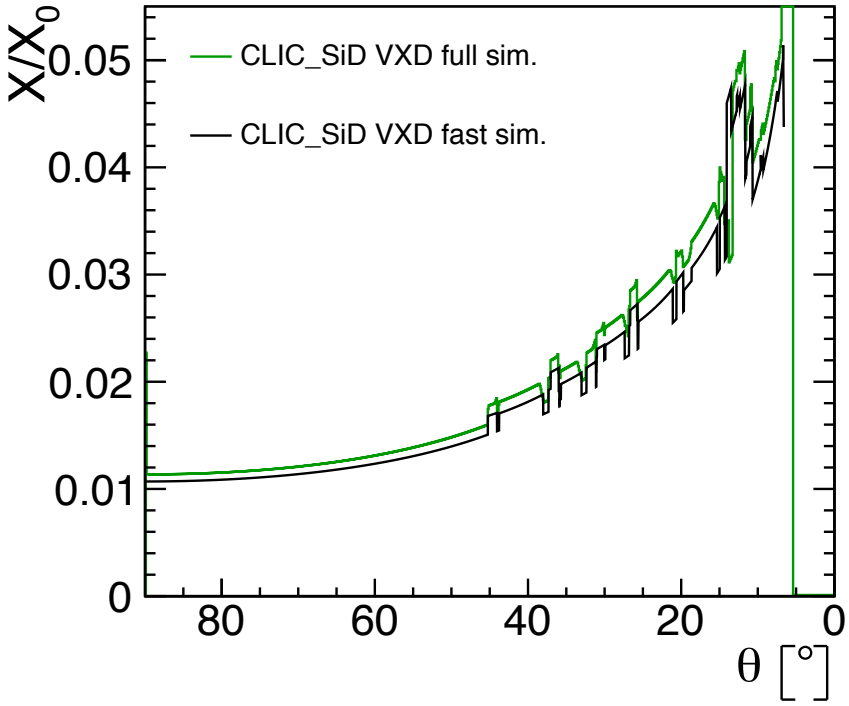
Implementation in simulations:

- Central Beryllium part:
  - CLIC_ILD: d=0.6 mm, R=29.4 mm (B=4 T)
  - CLIC_SiD: d=0.5 mm, R=24.5 mm (B=5 T)
  - Safe w.r.t. backgrounds, vacuum collapse, leak tightness (D0, CDF experience in run II)
  - Unlike ILC: no extra shielding, due to low expected levels of incoh. synchrotron radiation (t.b.c.)
- Forward conical part:
  - 4 mm iron, to shield against back scatters from forward region
  - Pointing to interaction point → no extra material inside tracking acceptance



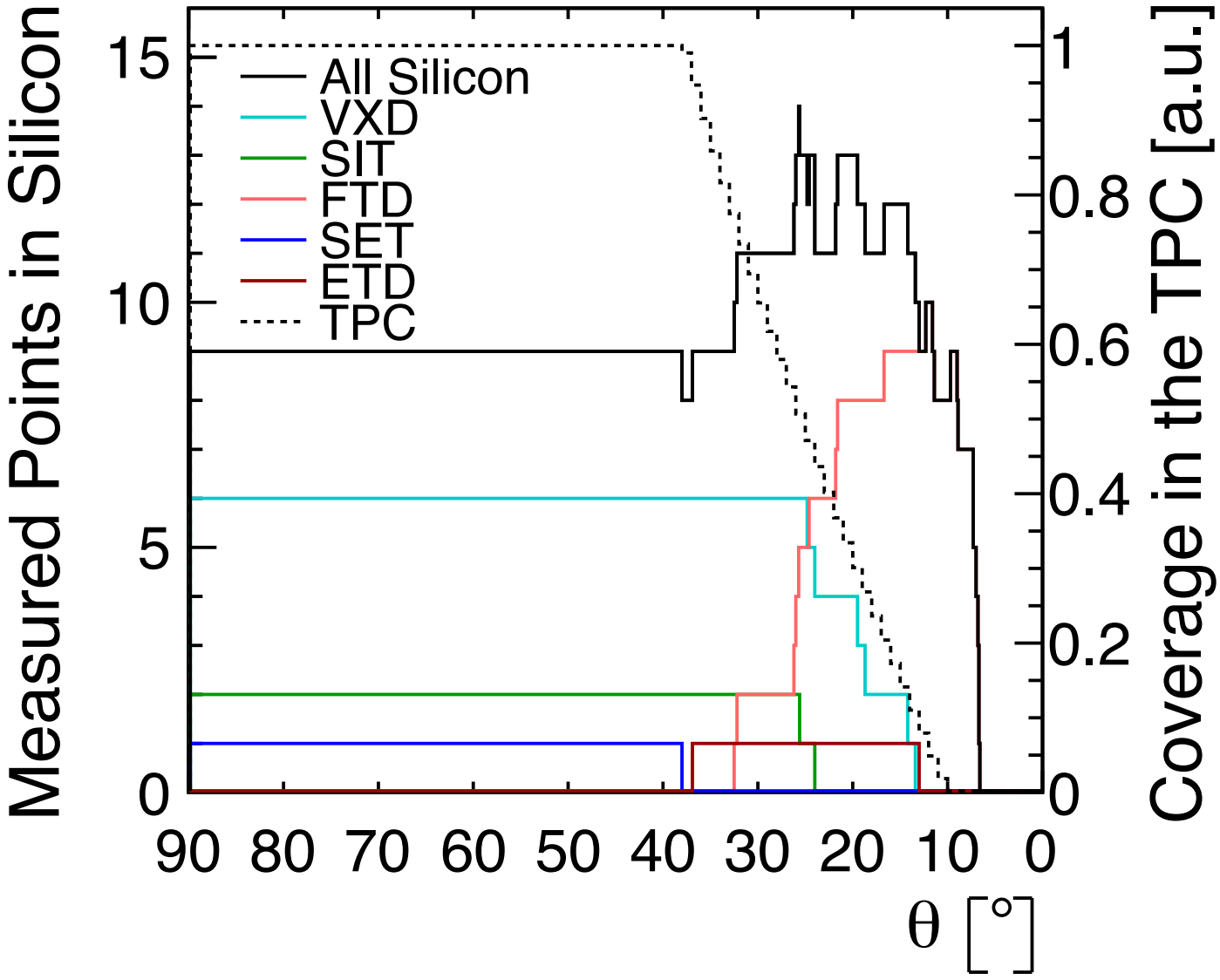
Material budget vertex region





- Integrated amount of material seen by particles originating from the IP:
  $X/X_0 \sim 1\%$ (at $\theta=90^o$, averaged over ϕ)
- Good agreement full / fast simulation
  (fast simulation has only ideal cylinders and disks, no module overlaps)

Angular coverage CLIC_ILD tracking



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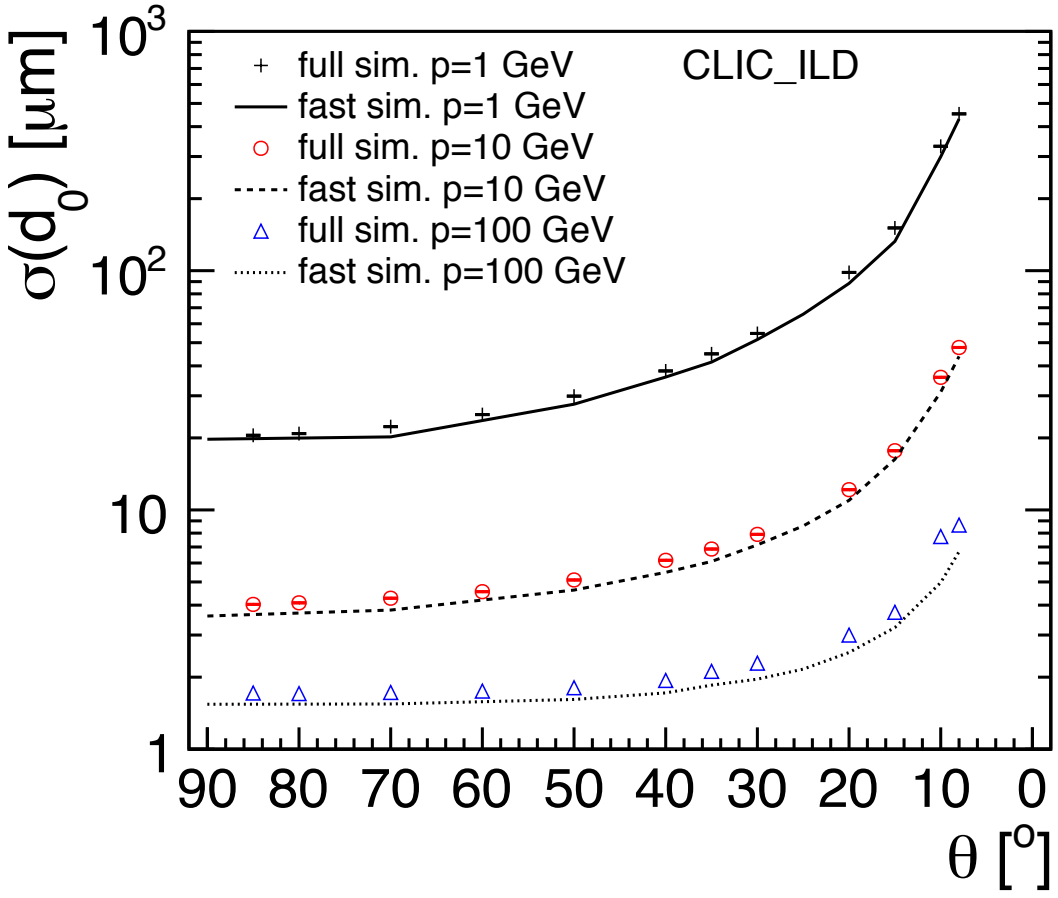
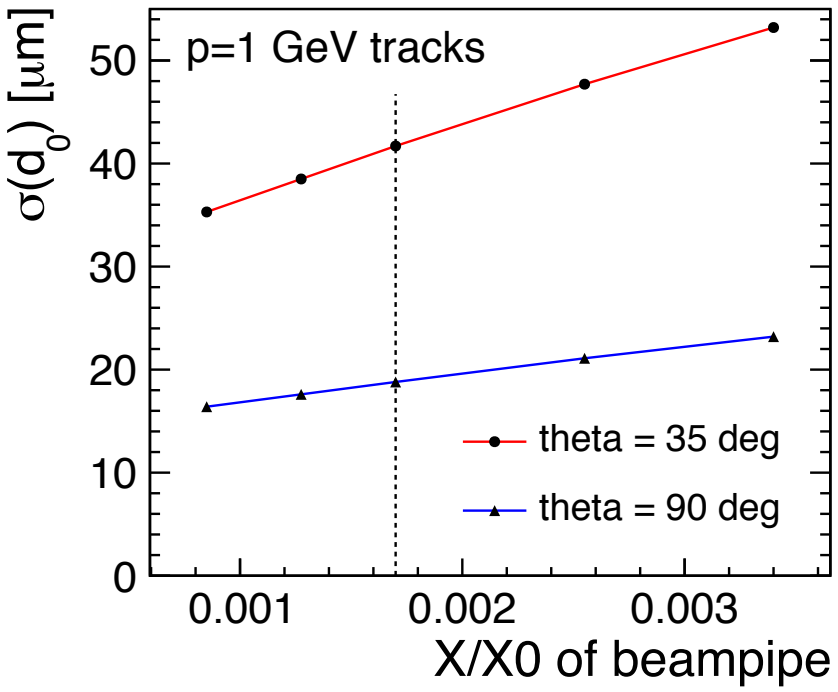
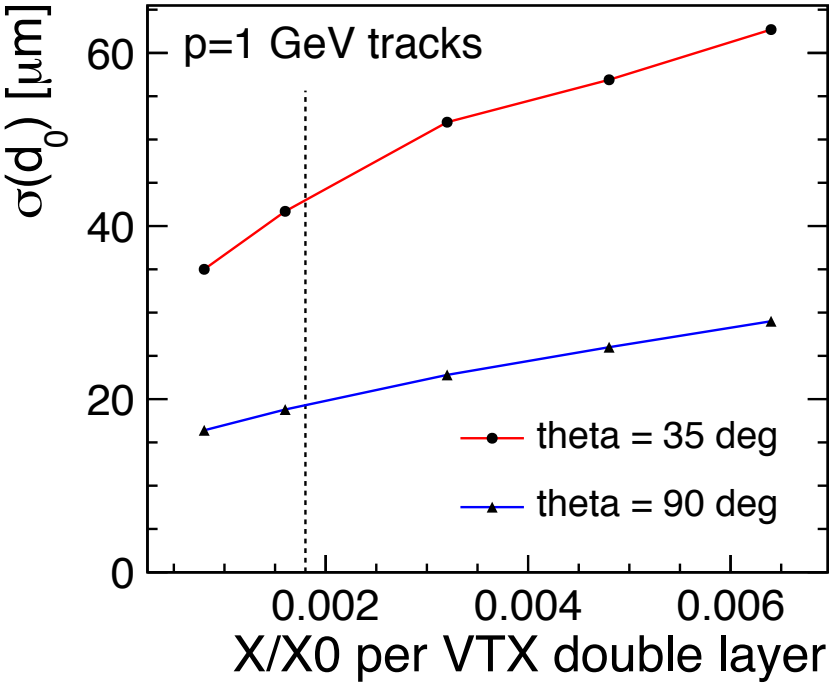


- Simulation models reach required performance
- Sensitivity to changes in design parameters:
  - Single-point resolution
  - Distance to IP
  - Material budget

→ Parametric studies

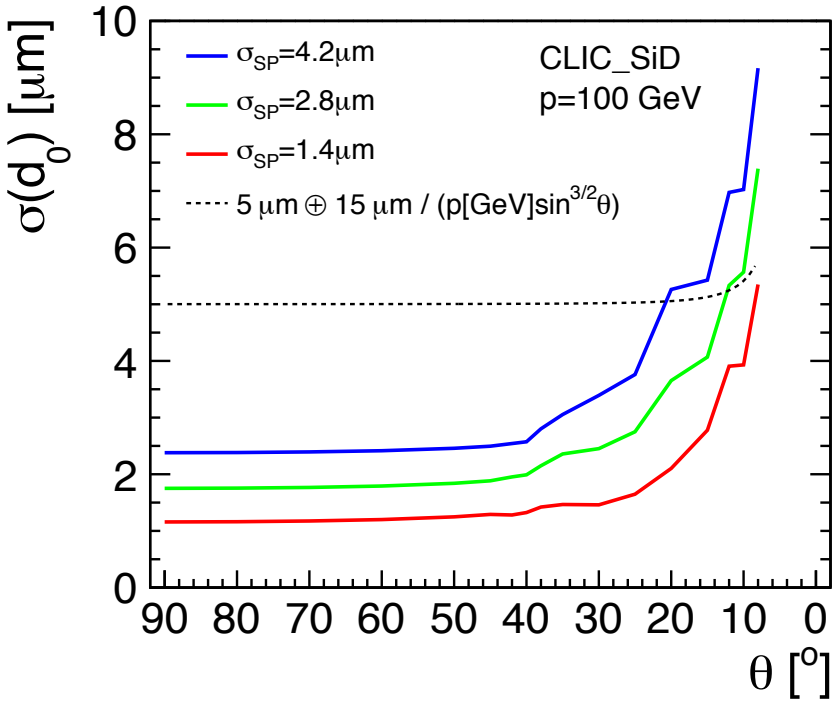
Dependence on material

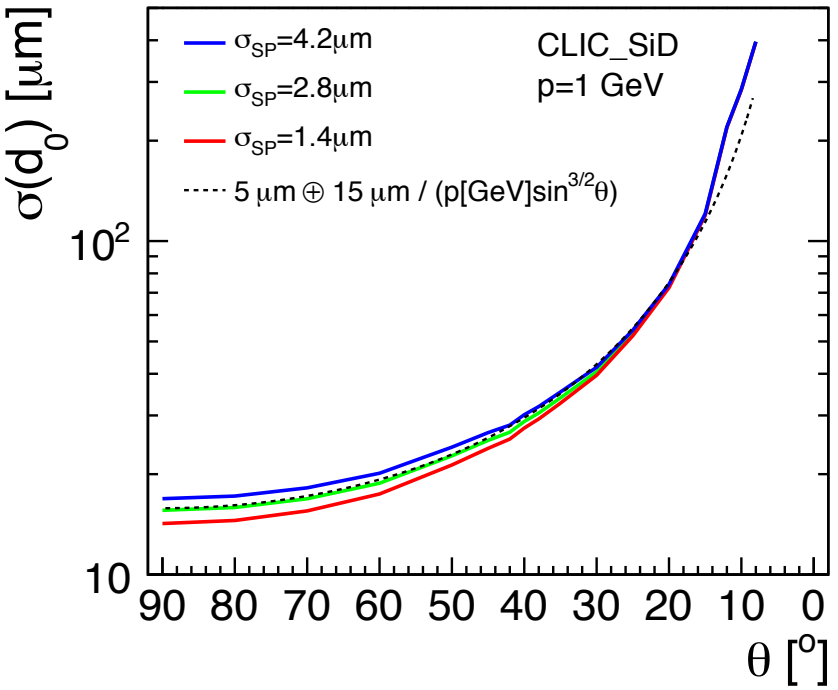




- Studied sensitivity of d_0 resolution for low momenta on material in beampipe and silicon pixel layers of CLIC_ILD
- Doubling beam-pipe thickness → ~20% worse resolution at 90°
- Doubling material in silicon layers → ~20% worse resolution at 90°
- Steeper slope in forward region

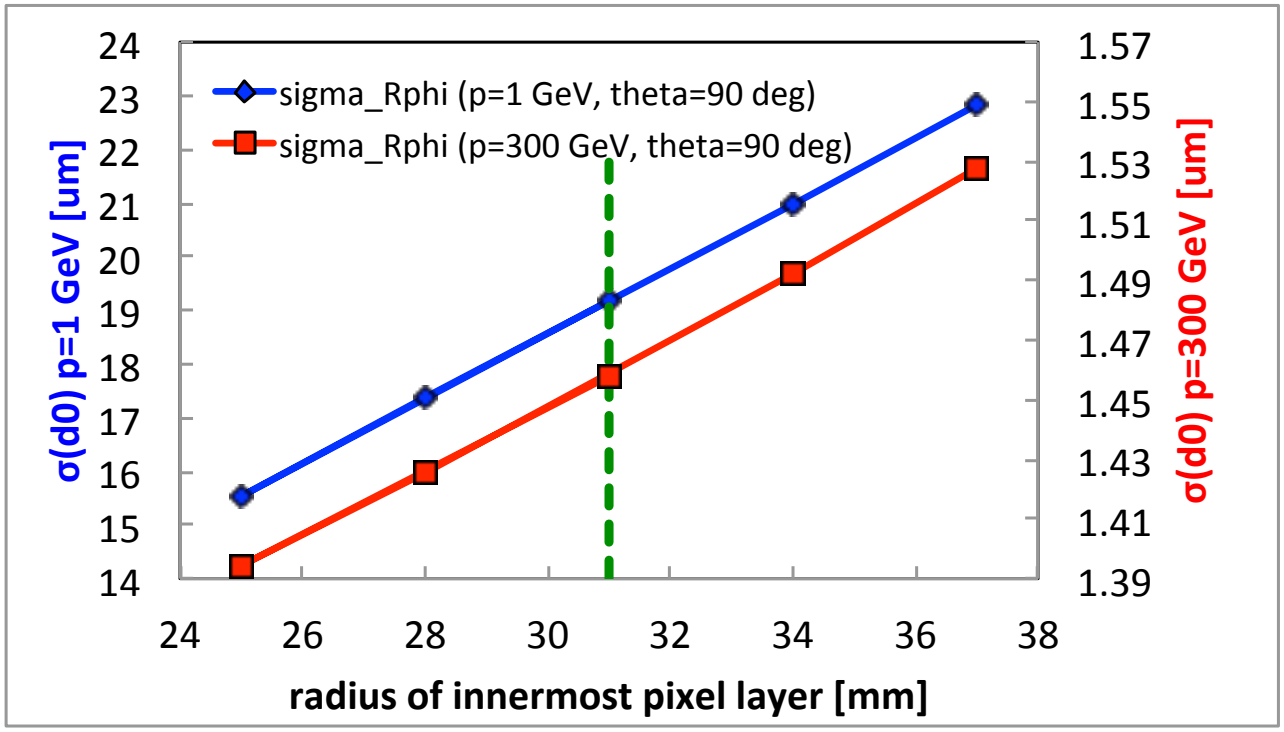
Dependence on single-point resolution





- Varied single-point resolution by +- 50% (~ pixel sizes 10x10, 20x20, 30x30 μm²)
- Observed change in d_0-resolution:
  - +- 40% for p = 100 GeV
  - +- 15% for p = 1 GeV
- Resolution close to or better than target values for all cases
- Pixel size is also constrained by:
  - Expected background occupancy
  - Ability to separate adjacent tracks in dense jets

Dependence on distance to IP



- Varied distance to interaction point, by changing radii of beam pipe and barrel vertex layers in CLIC_ILD model
- Observed change in d_0-resolution:
  - 3.2% / mm for high momenta (parameter 'a')
  - 0.8% / mm for low momenta (parameter 'b')
- Distance to interaction point is constrained by direct hits from incoherent pairs

Signal rise time

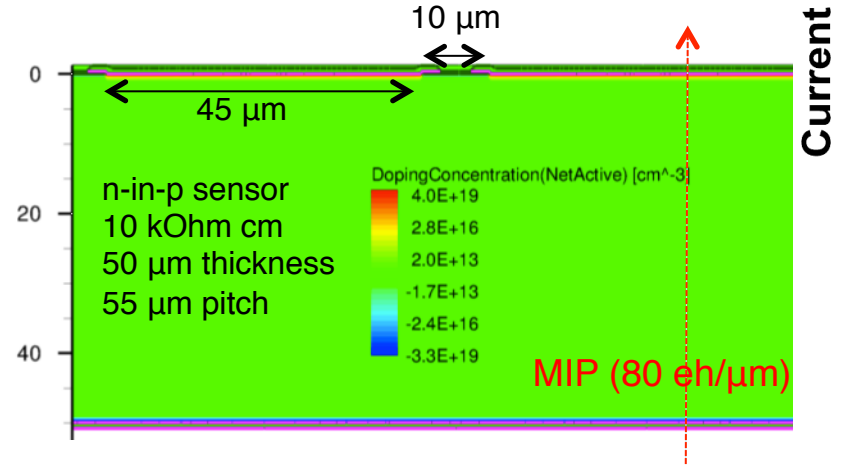
- Need time-stamping precision of ~10 ns, to suppress beam-induced backgrounds

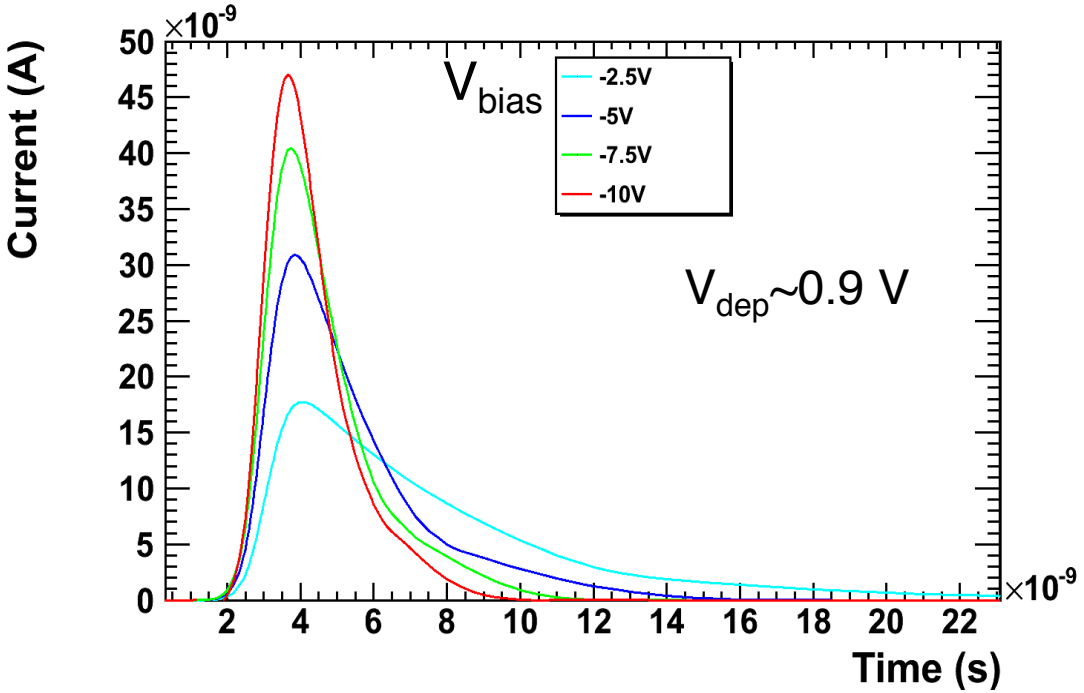
→ Peaking time in sensor should be <<10 ns, to optimize S/N and reduce effect of time walk

- electron collection faster than holes → favors n-in-p sensors

Example:

- 55 x 55 µm^2 pixels
- 50 µm thinned n-in-p sensor, ρ=10 kOhm cm
- ~2 ns peaking time with weak dependence on V_{bias}
- For higher V_{bias} better S/N expected after shaping, due to higher peak value; also less time walk due to reduced dispersion





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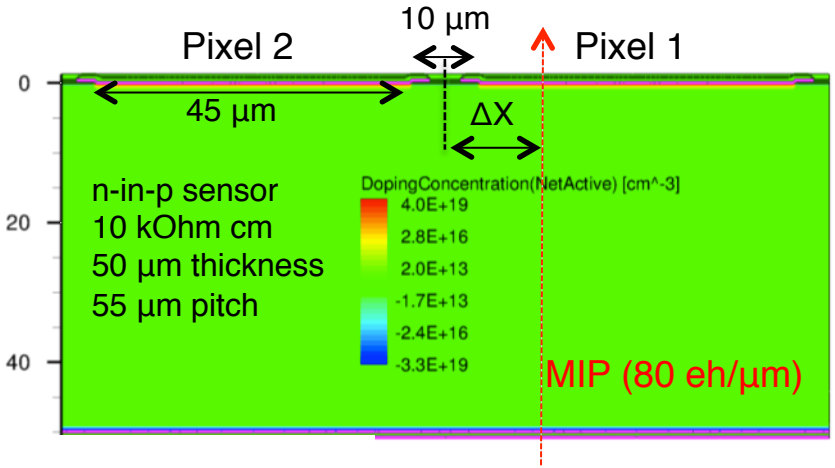
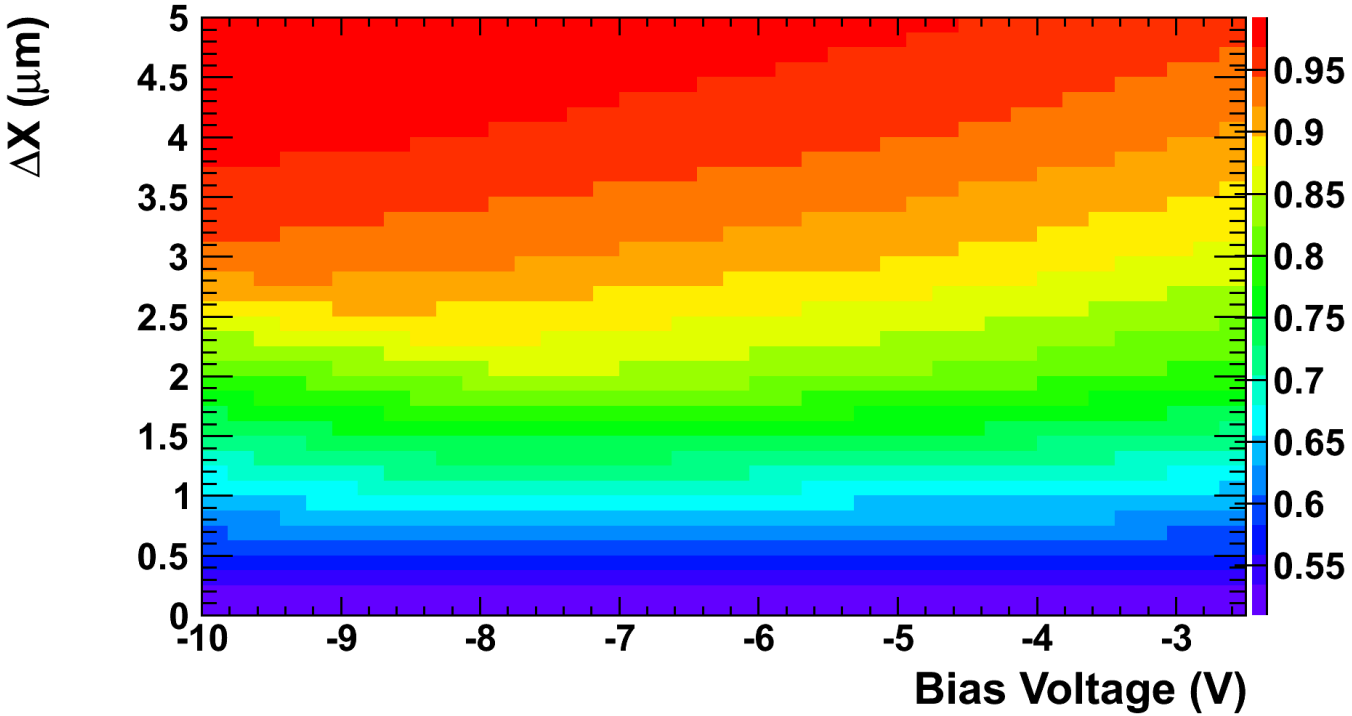
Charge sharing

- Charge spread in sensor leads to sharing of charge between neighboring pixels
- Over-depletion increases E-field, thereby reduces charge spread and charge sharing
- Charge sharing can improve resolution through interpolation (with analog readout)
- However: signals below threshold are lost





Fraction of total signal collected in pixel 1

M. Benoit

Hybrid approach: R&D examples

- Thinned high-resistivity fully depleted sensors
  - Several producers for ~50 µm thick silicon sensors (e.g. IZM, Micron, CNM, VTT)
  - Handling + flip-chip bonding is a concern, in particular for larger structures

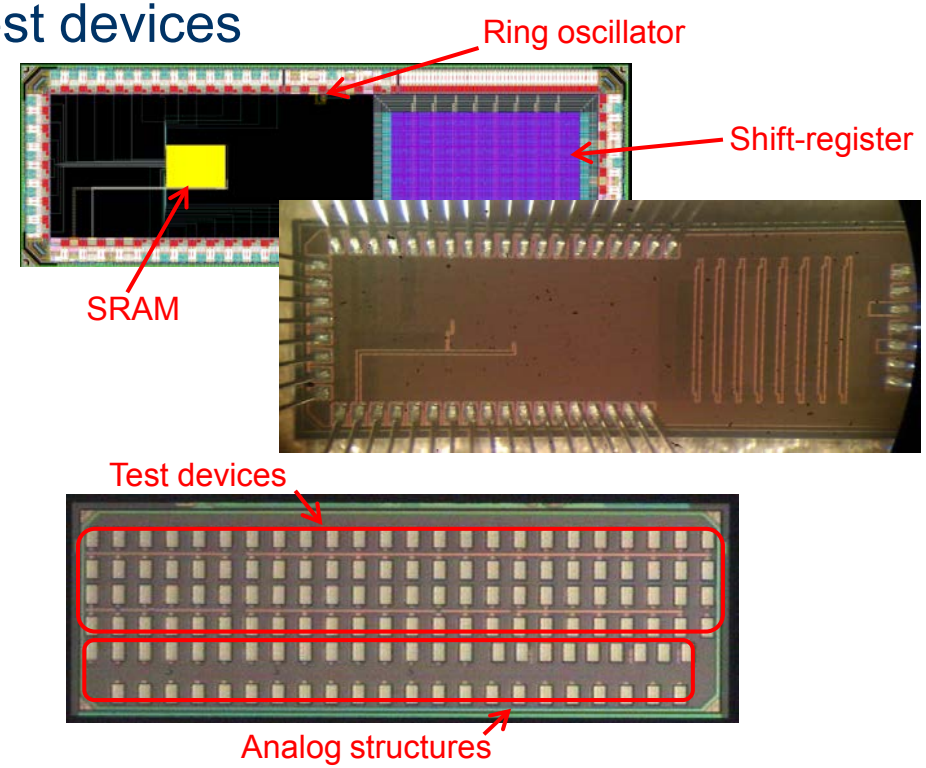
- Fast, low-power readout ASICs in Very-Deep-Sub-Micron (VDSM) technology
  - Timepix3 2013: 130 nm IBM CMOS, 55 µm^2 pitch
  - SmallPix 2013: 130 nm IBM CMOS, ≤40 µm^2 pitch (medical applications, XFEL)
  - CLICPix ~2015: 65 nm, 25 µm^2 pitch

  → CLICPix demonstrator prototypes 2013: 64x64 pixel array
  - See talk on hybrid pixel readout chip developments by Massimiliano De Gaspari

- Low-mass interconnects and pixel connectivity
  - Micro bump bonding or Cu pillars for pixel interconnects
  - Through Silicon Vias (TSV):
    - fan out ASIC contacts to backside through vertical conducting channel
    - avoids dead areas from wire-bonding pads around the chips
    - Example: CEA-Leti via-last process with Medipix 3, prototypes under test
  - Lateral interconnectivity
    - Slim-edge/edgeless sensors
    - Stitching of neighboring chips

CLICPix 65 nm test structures

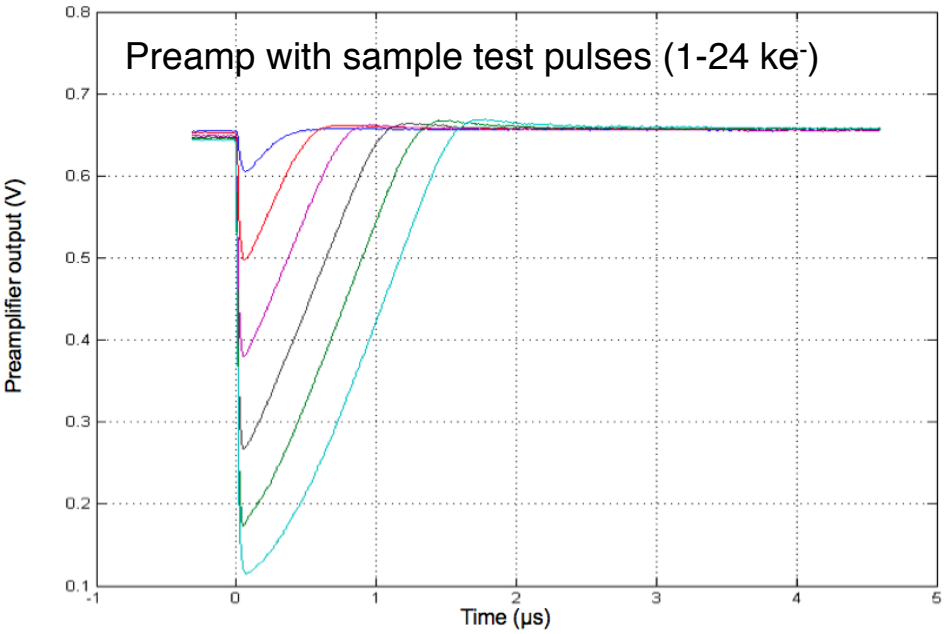
- Radiation and functional tests
- Total size: 3x4 mm
- Divided in three sub-chips:
- 1 chip for analog structures and test devices
  - 1 pad per multiple gates
  - Analog structures
- 1 chip w/ test structure/devices
  - 1 pad per gate
  - 142 total pins
- 1 chip for digital logic
  - 64 kbit Shift-register
  - 56kbit Memory
  - Ring oscillator (1025 gates)



P. Valerio

CLICPix 65 nm test structures

- 65 nm technology allows for performance improvements w.r.t. 130 nm:
  - Smaller pixel sizes (10-30% less area for analog part, 60% less for digital part)
  - More functionality in each pixel
  - Lower noise (due to lower capacitances)
- Analog+digital test structures (pixel sub-circuits) produced 2011 in 65 nm TSMC multi-project wafer run



- Results according to simulations
- Improved radiation tolerance w.r.t. 130 nm observed (TID up 200 Mrad and SEU)
- Results allow for projections to CLICPix performance (e.g. power consumption)

Preamp measurements:

	Simulations	Measurements
Rise time	50ns	65ns
Gain	30mV/ke⁻	29.1mV/ke⁻
Linearity	5% at 16ke-	5% at 15ke⁻
Noise	55e⁻	60e⁻ (70e⁻ for ELT channel)

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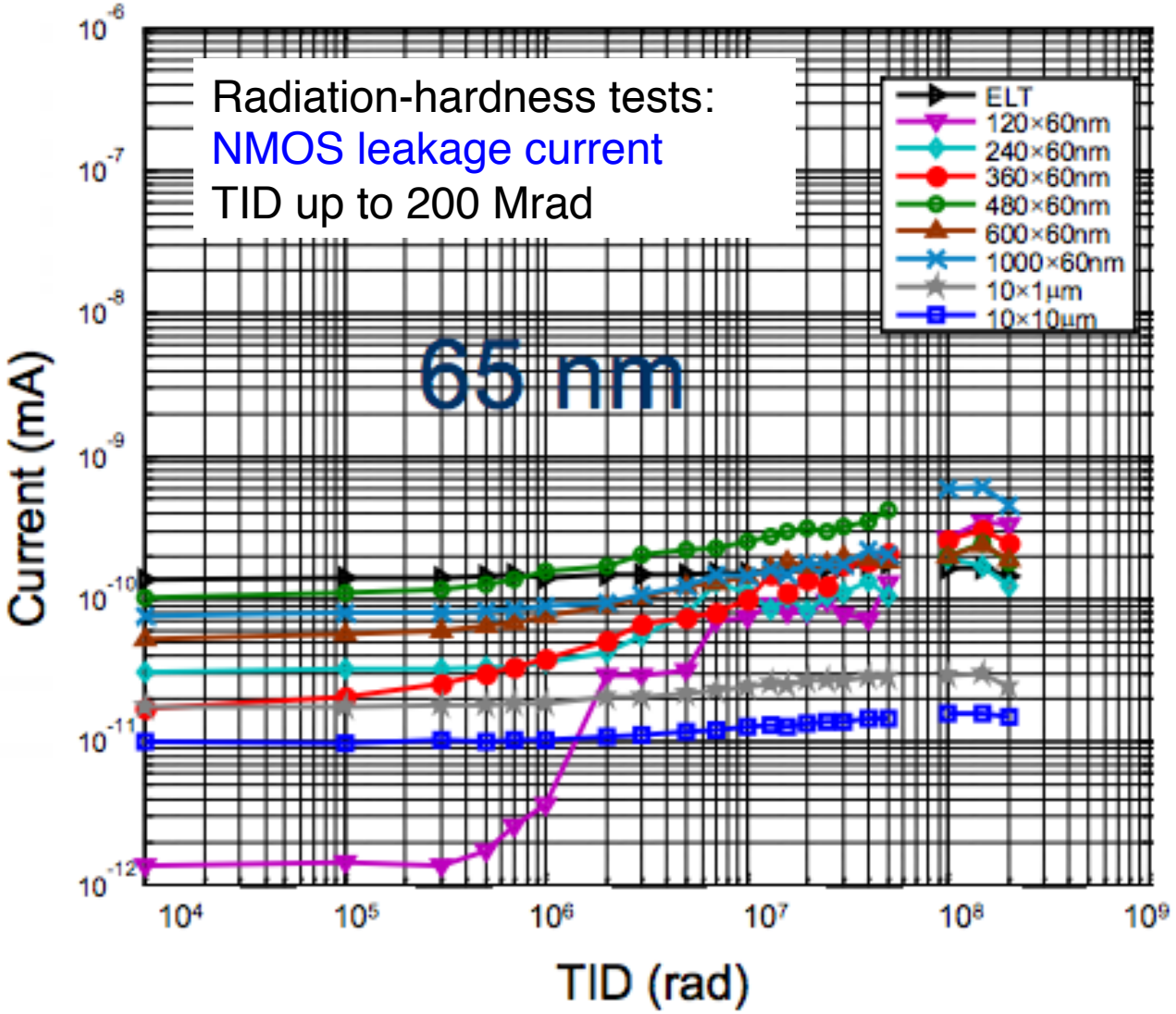
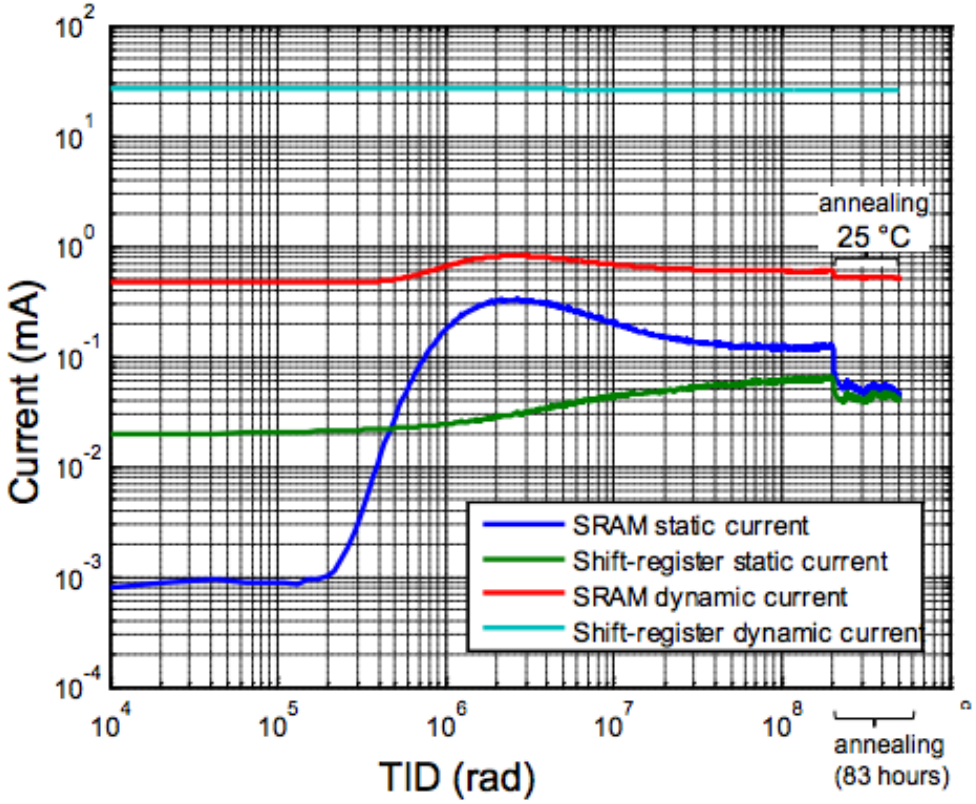
CLICPix 65 nm test structures: results



CLICPix 65 nm digital test structures

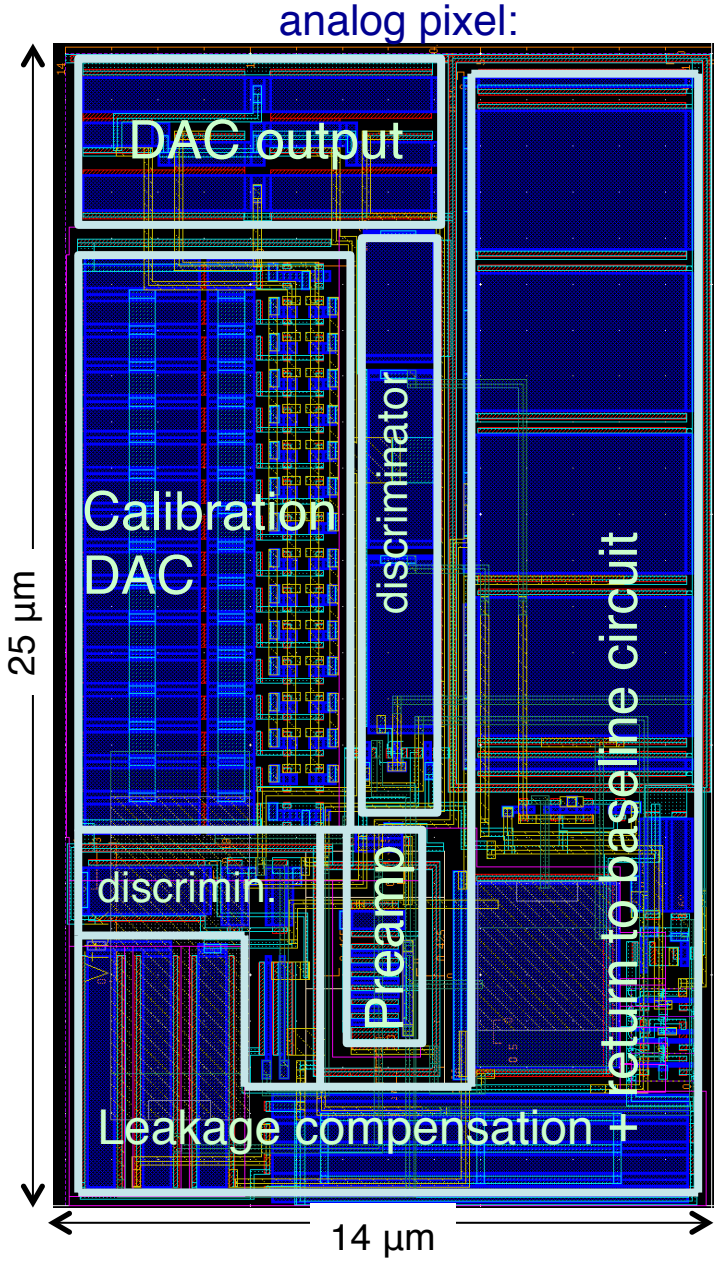


- Measured static and dynamic currents of SRAM and shift-register
  - Dynamic test run @ 30MHz
- SRAM static current increases by 300×
  - Dynamic current reflects this change with a small increase
  - Ultra-narrow devices are used in the SRAM from foundry (W=80nm)
  - Peak current at ~2-3 Mrad
- Shift-register static current changes very little
  - ~12.5 nW/MHz per D-FF
- Visible partial annealing effect at room temperature
  - Time constant ~ 1.5 hours

P. Valerio

CLICPix 65 nm demonstrator chip

- **65 nm CMOS**, targeted to CLIC vertex detectors
- **25 µm** pixel pitch
- simultaneous **4-bit TOA and TOT per pixel**
- **Photon Counting Mode** for threshold equalization
- Front-end **time slicing < 10 ns**
  (time-walk correction using TOT)
- Selectable compression logic:
  - Zero suppression
  - **cluster-based + column-based compression**
- Full chip r/o in less than 800 µs (for 10% occupancy) using a 320 MHz read-out clock
- P_{analog}~2 W/cm^2 (peak power)
- **power pulsing scheme** (Clock gating, power gating for analog part) → P_{avg}< 50 mW/cm^2
- Demonstrator chip designed with
  fully functional 64 by 64 pixel matrix
- **Submission November 2012**
  in TSMC Multi-Project Wafer run



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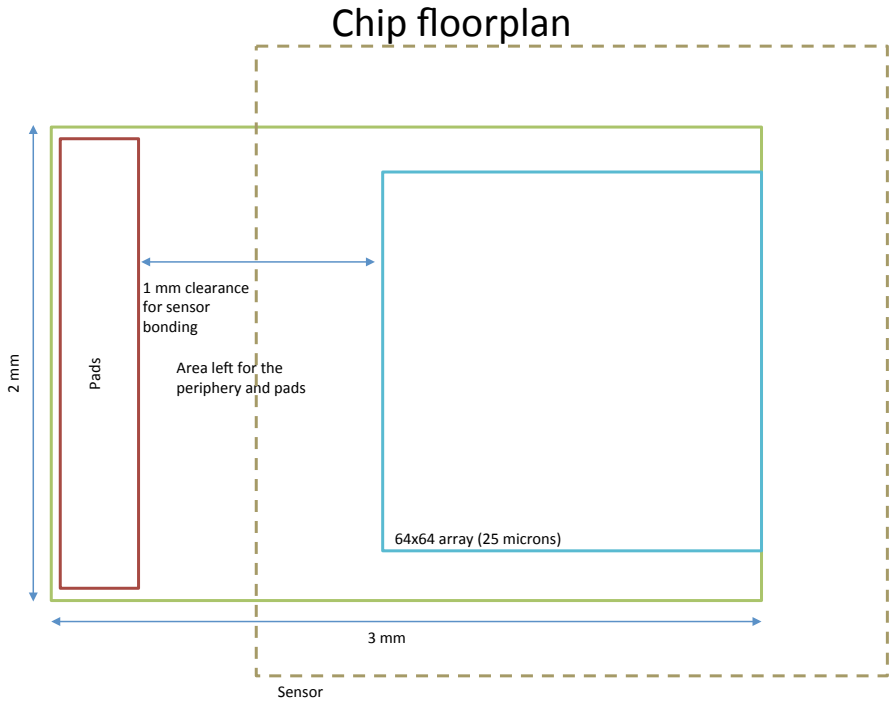
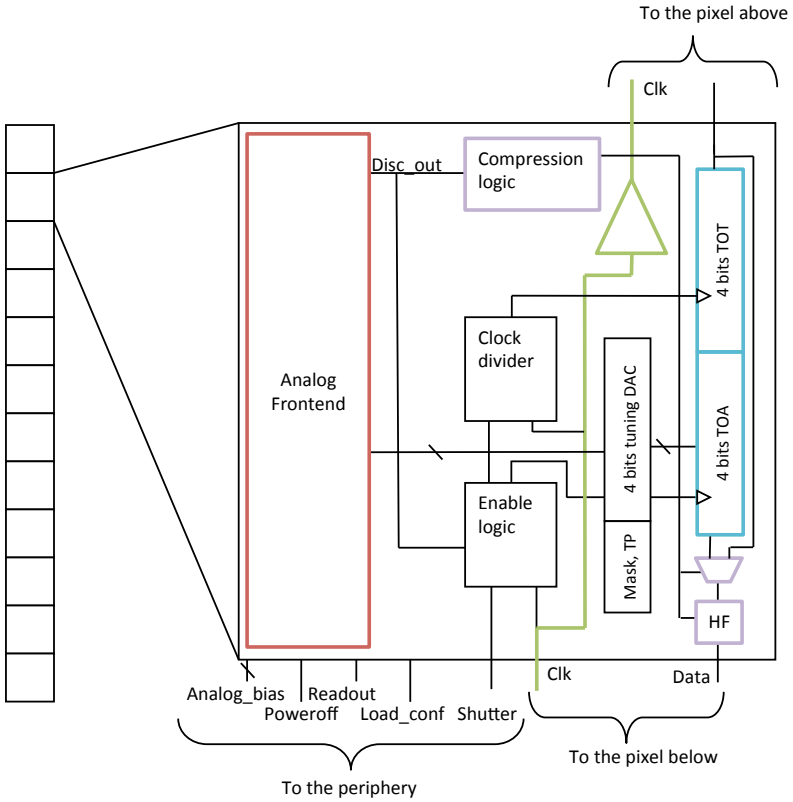
CLICPix 65 nm demonstrator chip

Demonstrator chip for next 65 nm MPWR

- First prototype with full pixel-readout functionality
- Submission end of 2012
- Includes 64 x 64 pixel array with 25 µm pitch
- Will try to (partially) bond to sensor



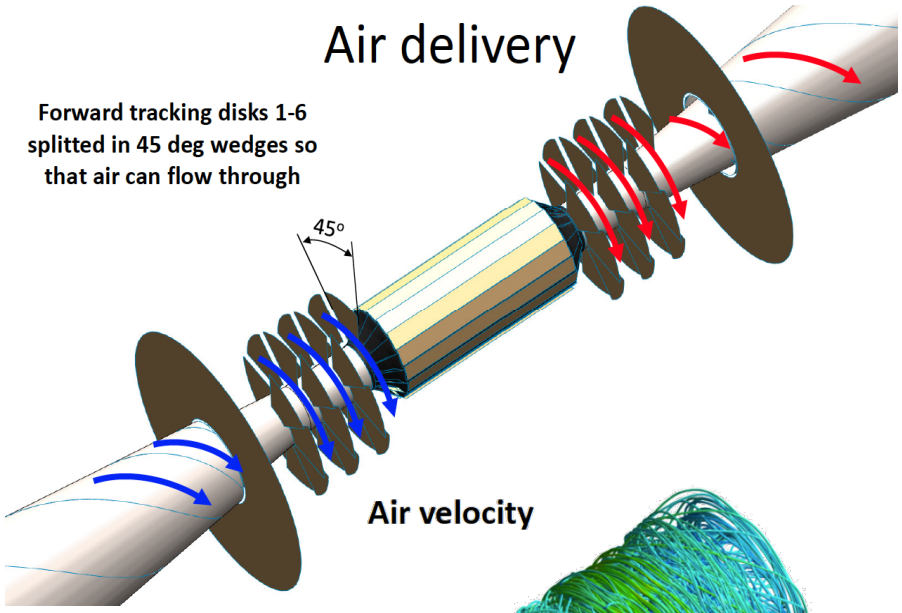


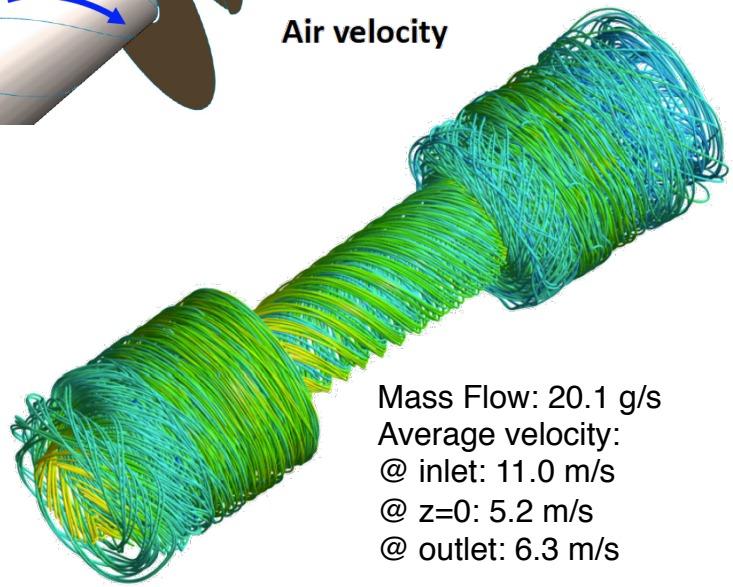
- simultaneous 4-bits TOA and 4-bits TOT measurements per pixel (100 MHz reference clock)
- Compression logic allows for sparse readout; Cluster-based compression is being evaluated
- Power saving techniques include clock gating when the pixel is not being read out and power gating (with an external signal) for the analog part when the chip is not acquiring data

P. Valerio, X. Llopart

Low-mass cooling

- P~500 W in vertex detectors (50 mW/cm^2)
- Need efficient cooling, meeting material budget requirements

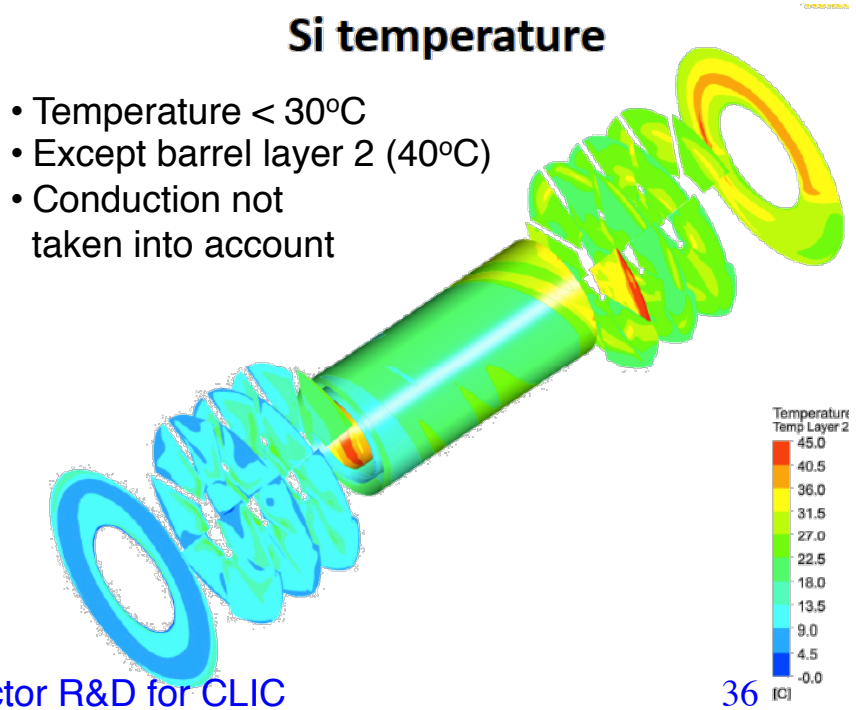




Mass Flow: 20.1 g/s
Average velocity:
@ inlet: 11.0 m/s
@ z=0: 5.2 m/s
@ outlet: 6.3 m/s

ANSYS finite element simulation of air-flow cooling:

- Spiral disk geometry
  → allows for air flow into barrel
- Sufficient heat removal
- See talk on vtx mechanics + cooling by Fernando Duarte Ramos



- Temperature < 30°C
- Except barrel layer 2 (40°C)
- Conduction not taken into account