

LCWS12 Arlington
October 22-26, 2012

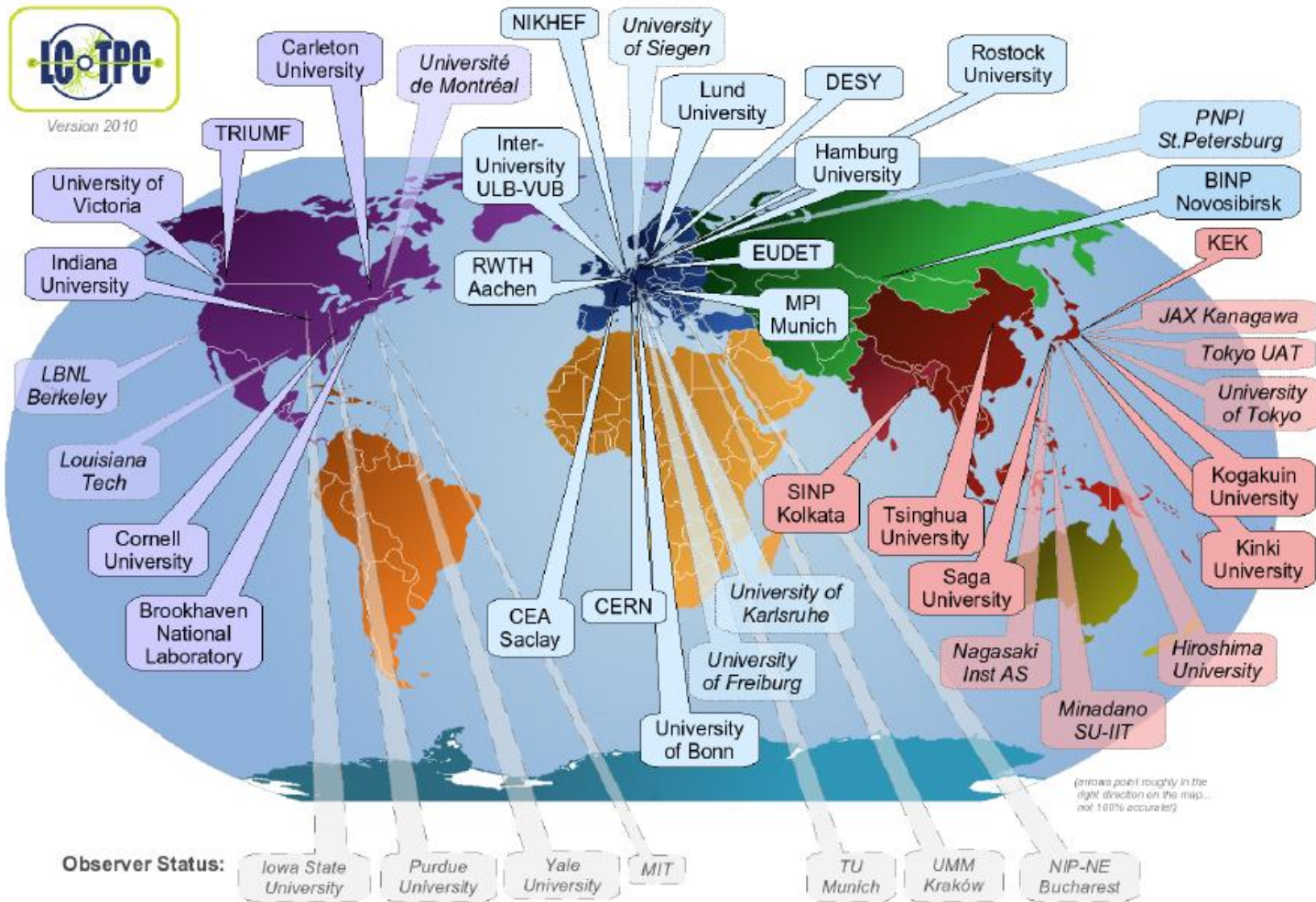


RESULTS OF A BEAM TEST OF A LARGE MICROME GAS TPC PROTOTYPE WITH 6 MODULES



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A. Robichaud, J. Timmermans, W. Wang

All the R&D is gathered in LCTPC



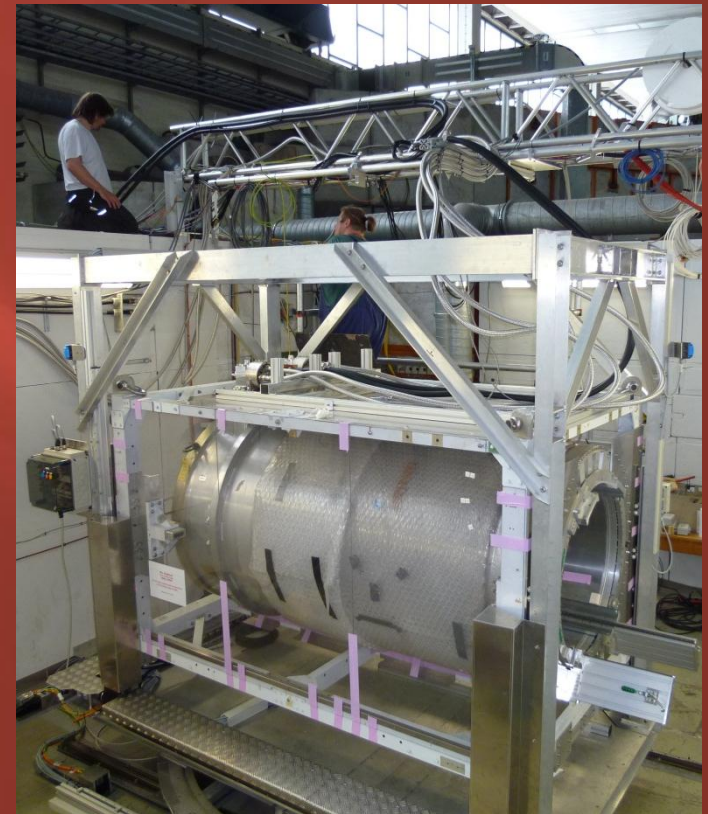
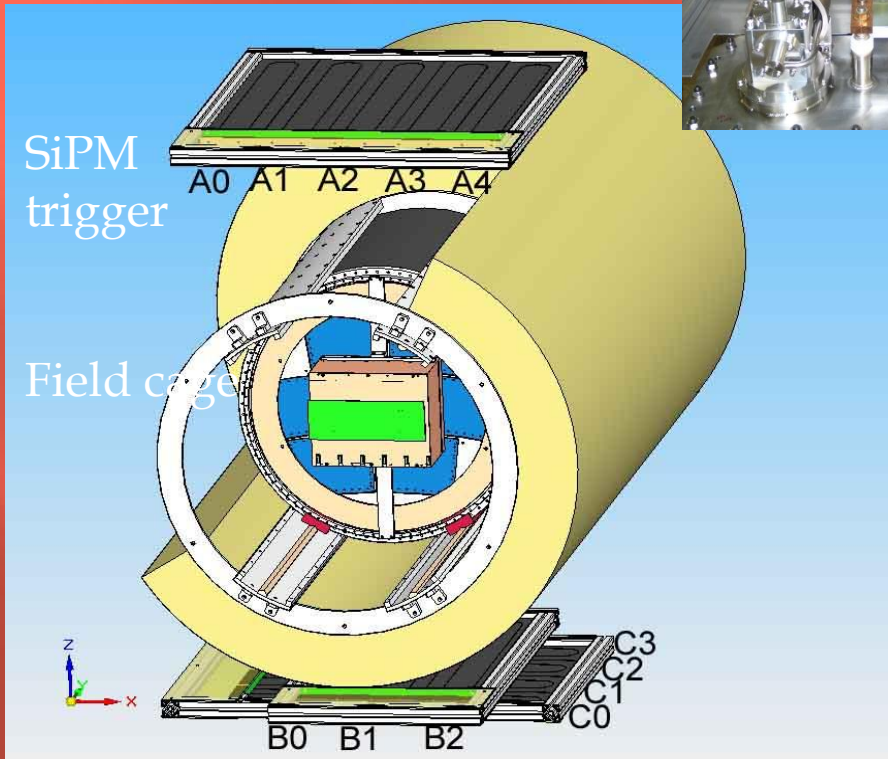
38(*) member + 7 observer institutes from 12 countries

(*) 25 signed the MOA

www.lctpc.org

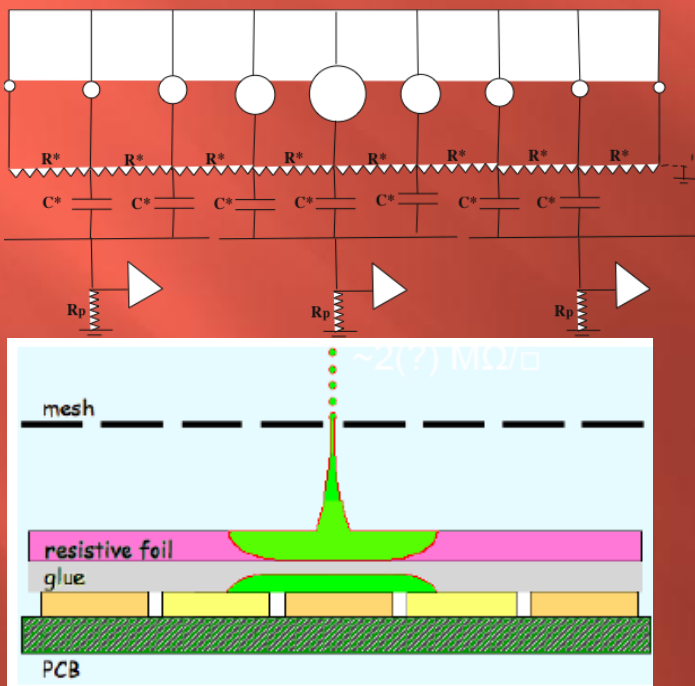
The EUDET test setup at DESY

The EUDET (FP6) setup at DESY is operational since 2008
Upgraded within AIDA (FP7): autonomous magnet with 2
cryo-coolers since July



Charge spreading by resistive foil

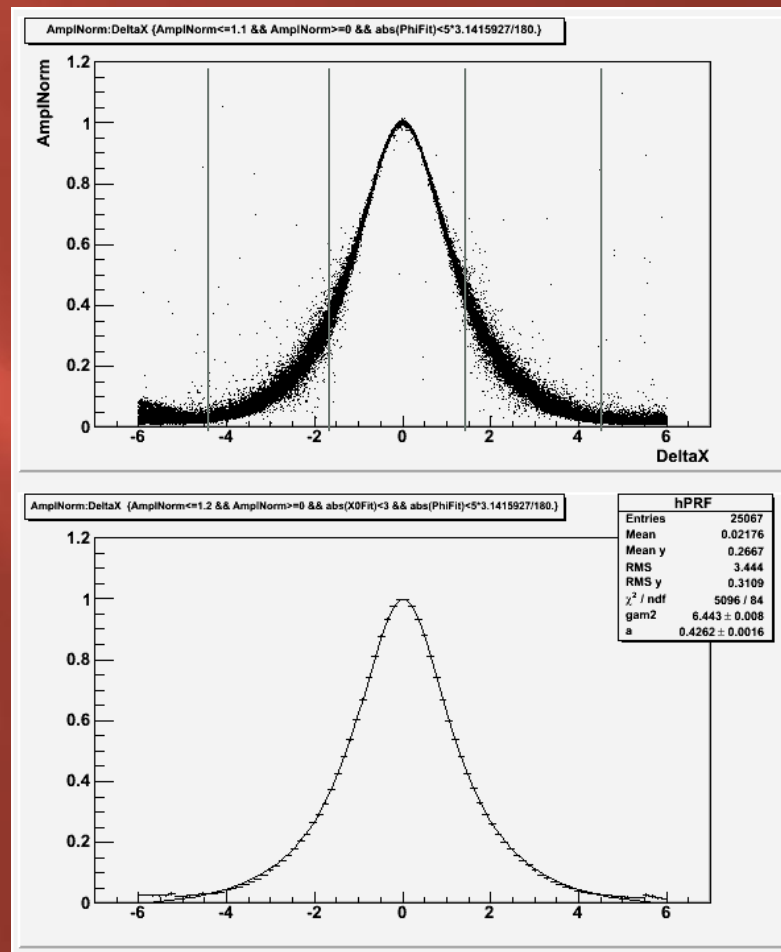
Resistive coating on top of an insulator:
 Continuous RC network which spreads the charge from $\sigma(\text{avalanche}) \sim 15\mu$ to mm:
 matching pad width improves position sensitivity



M. Dixit, A. Rankin, NIM A 566 (2006) 28

PAD RESPONSE: Relative fraction of 'charge' seen by the pad, vs $x(\text{pad}) - x(\text{track})$

$Z=20\text{cm}$, 200 ns shaping



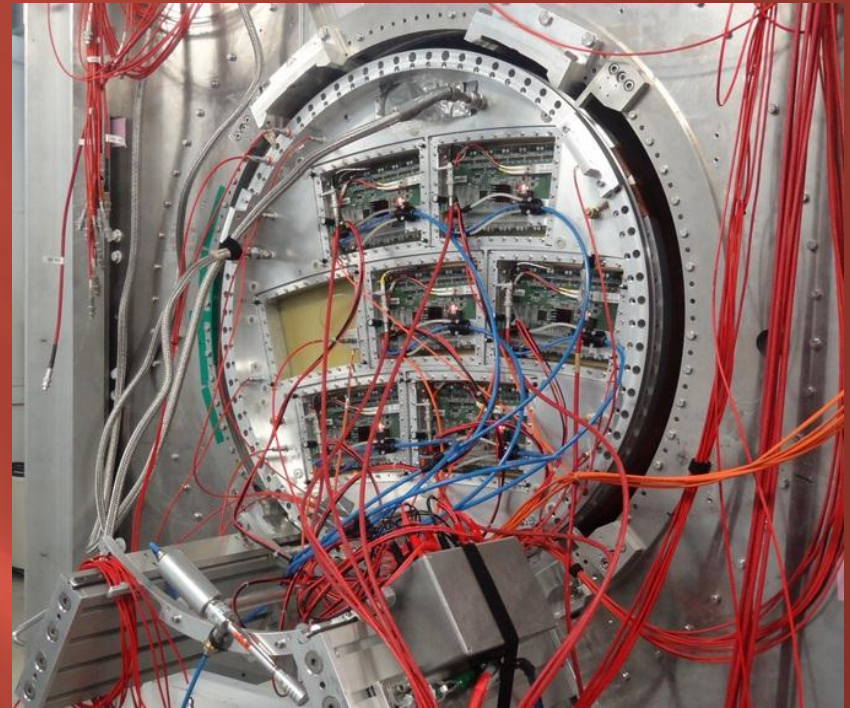
$x(\text{pad}) - x(\text{track})$ (mm)

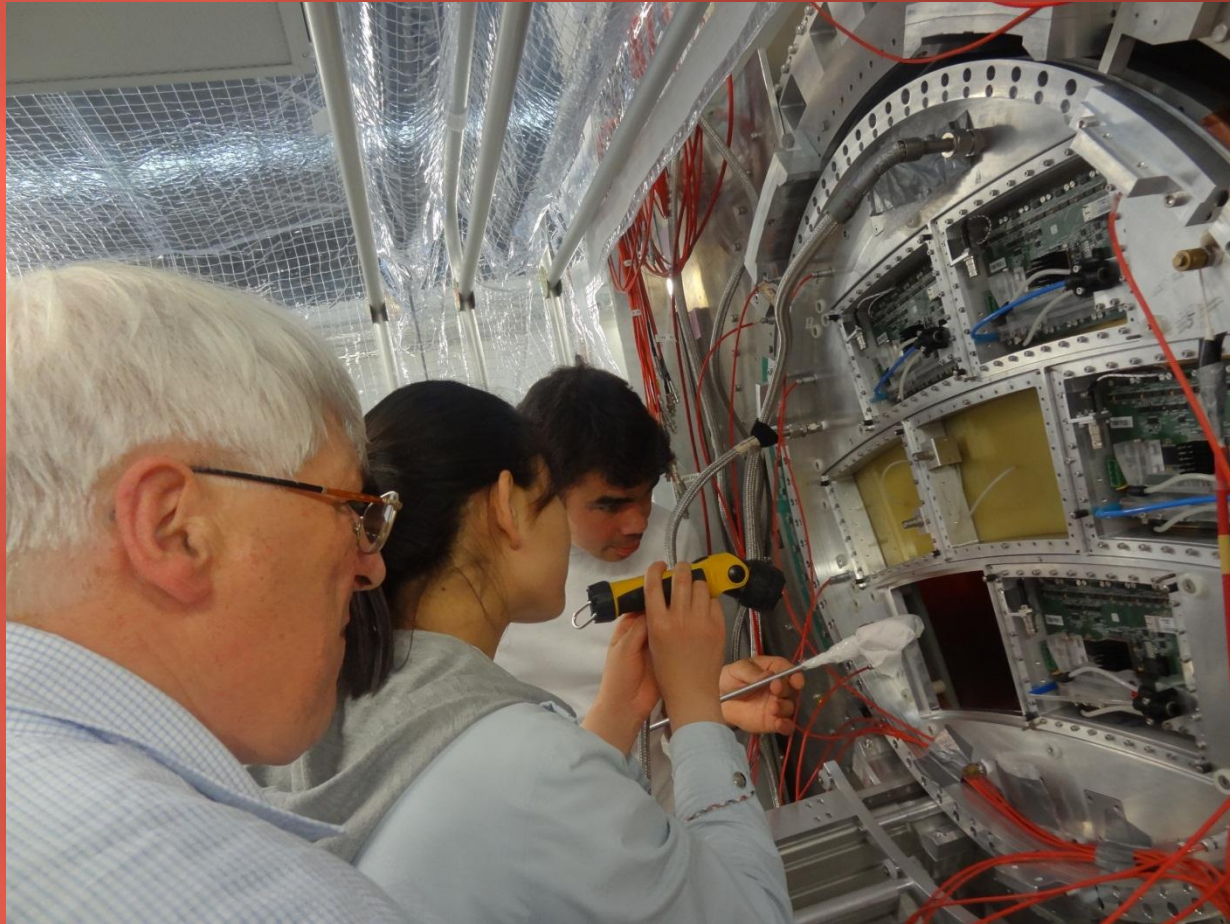
Integrated electronics

- New detector : new routing to adapt to new connectors, lower anode resistivity ($3 \text{ M}\Omega/\text{sq}$), new res. foil grounding on the edge of the PCB.
- New 300 points flat connectors (zero extraction force)
- New front end: keep naked AFTER chips and remove double diodes (count on resistive foil to protect against sparks)
- New Front End Mezzanine (FEMI)
- New back-end for up to 12 modules
- New DAQ, 7-module and more compact format
- New trigger discriminator and logic (FPGA).

The multi-module configuration allows new studies :

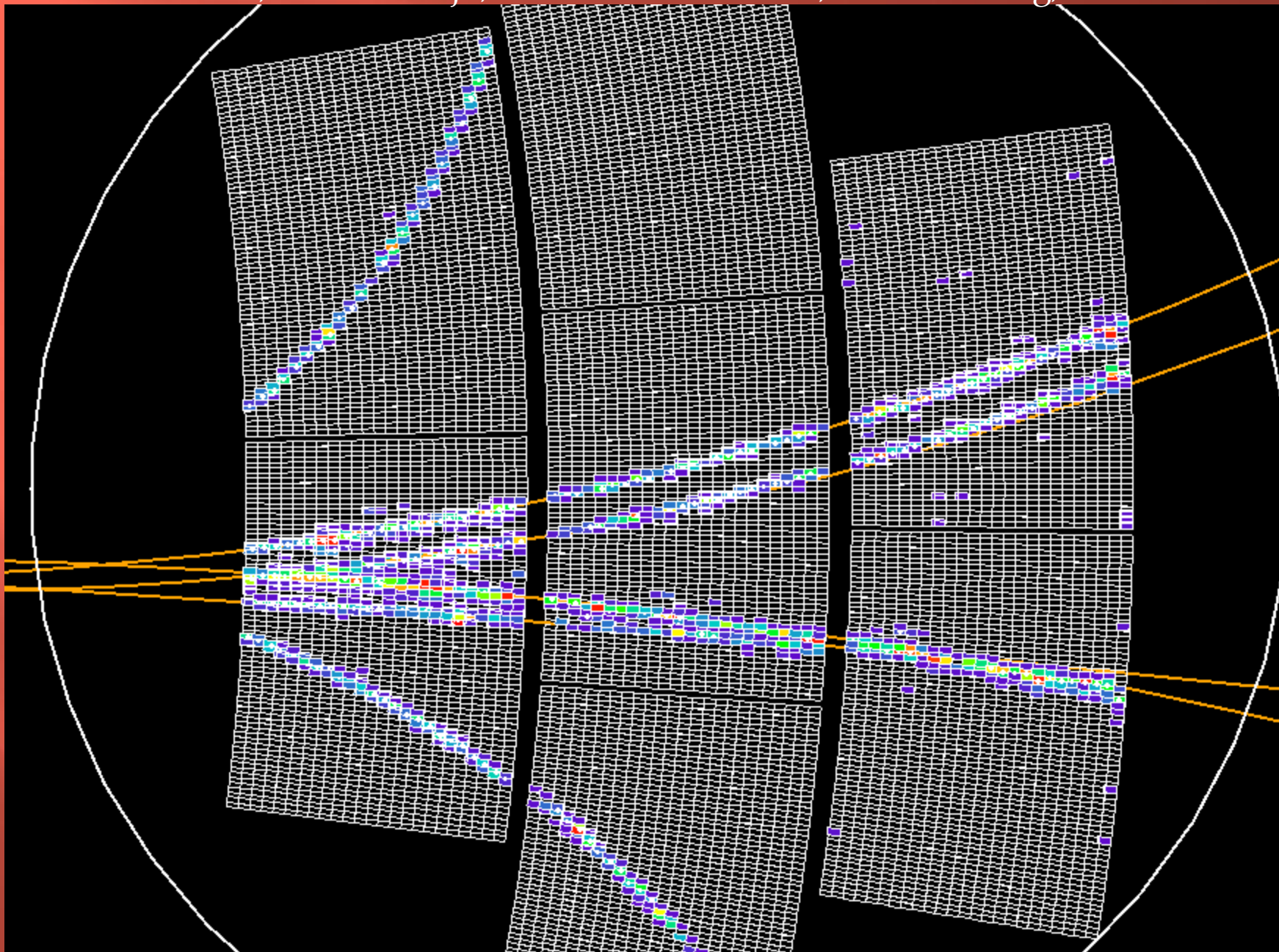
- Performance in cracks
- Module misalignment
- distortions



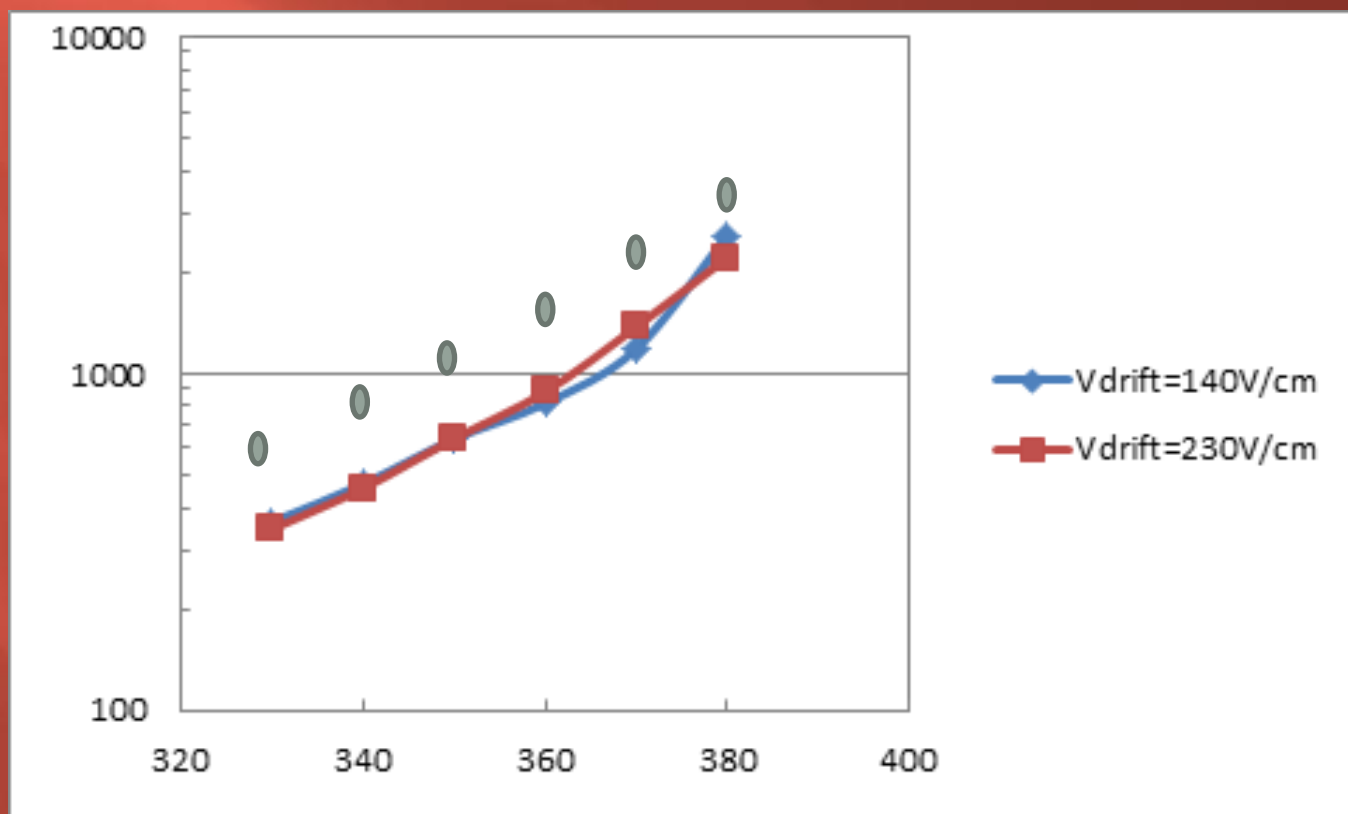


Smooth data taking in July, with over 1 000 000 evts. Air cooling and temperature control. However 6 modules only, 2 of them prototype or pre-serie, imperfect contacts

Thanks to Bo Li, Keisuke Fujii, Gilles de Lentdecker, M. Killenberg,...

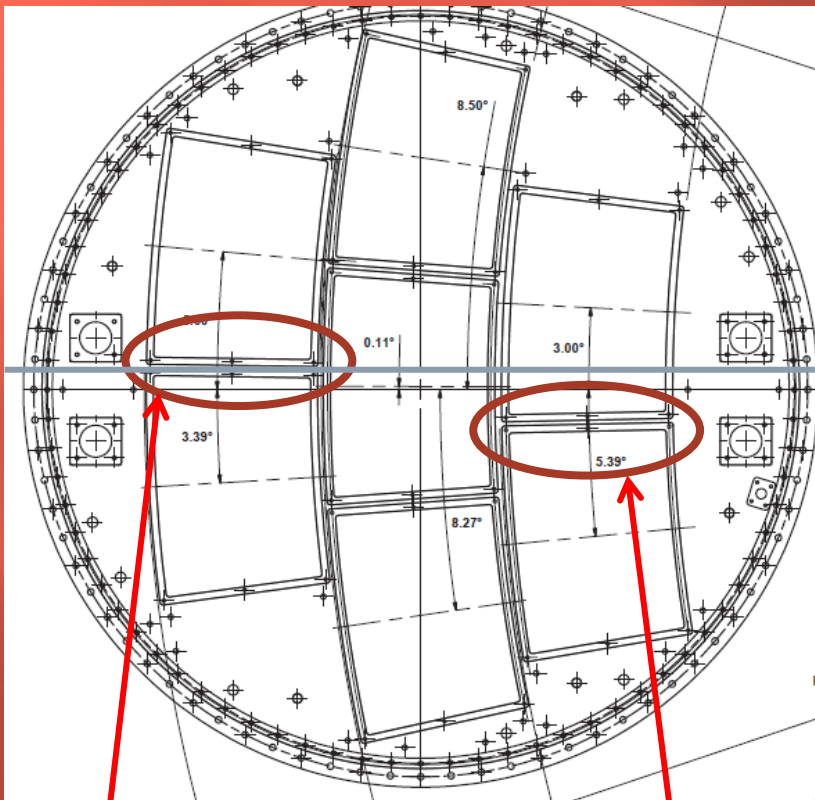


Effective gain vs mesh voltage is measured by using the fitted MPV of the (Landau) distribution of the measured charge. It compares well with direct gain measurements with a ^{55}Fe source on a detector without resistive foil (x2 lower)



Crack scan

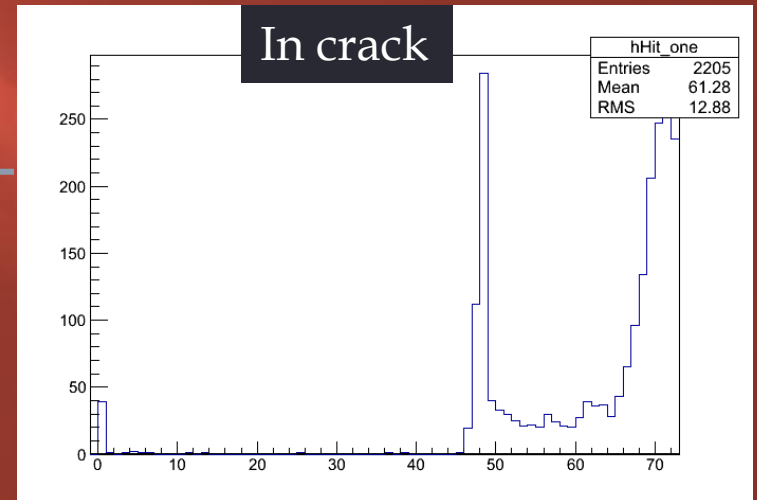
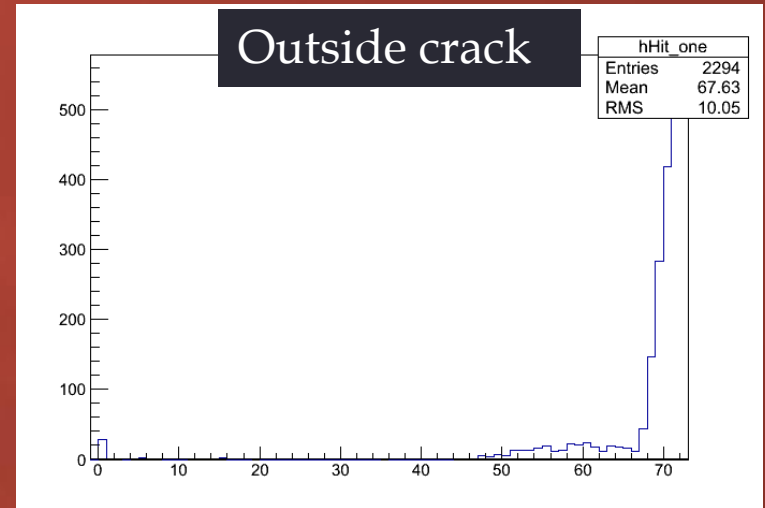
Study the hit reconstruction efficiency at or near the crack: take data with beam, moving by steps of 2mm



Upper crack

Lower crack

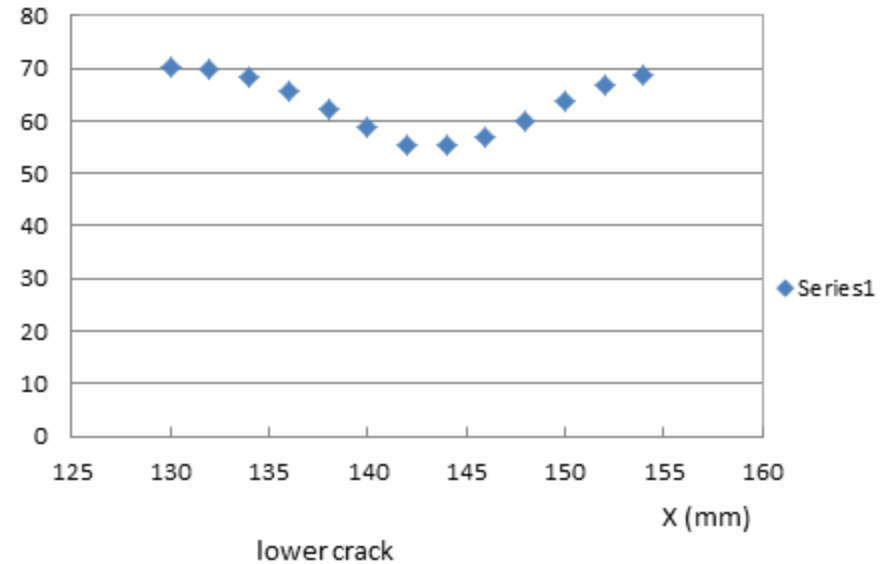
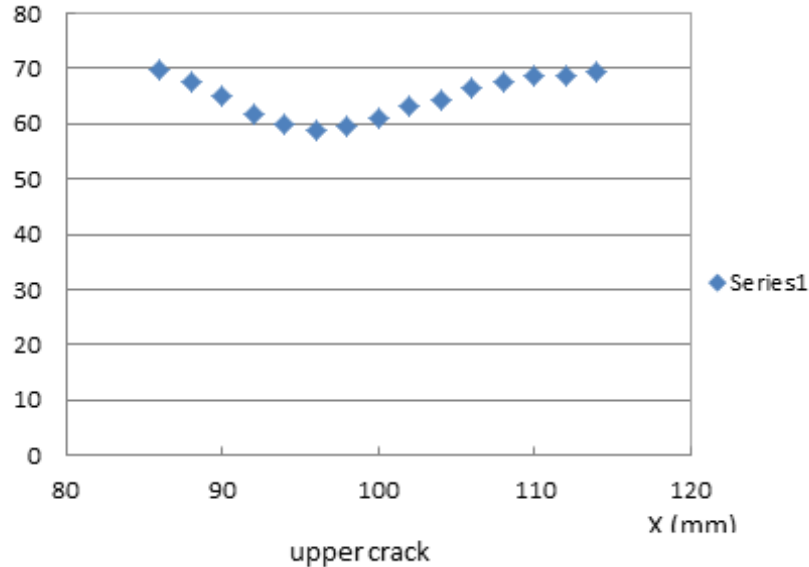
Beam
direction



Padrow number (3x24=72)

Hits with ADC>150, 1-track evts

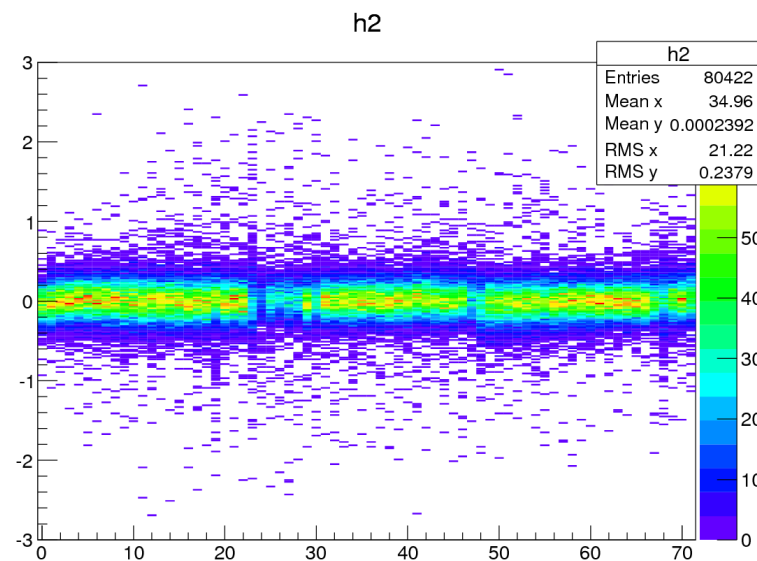
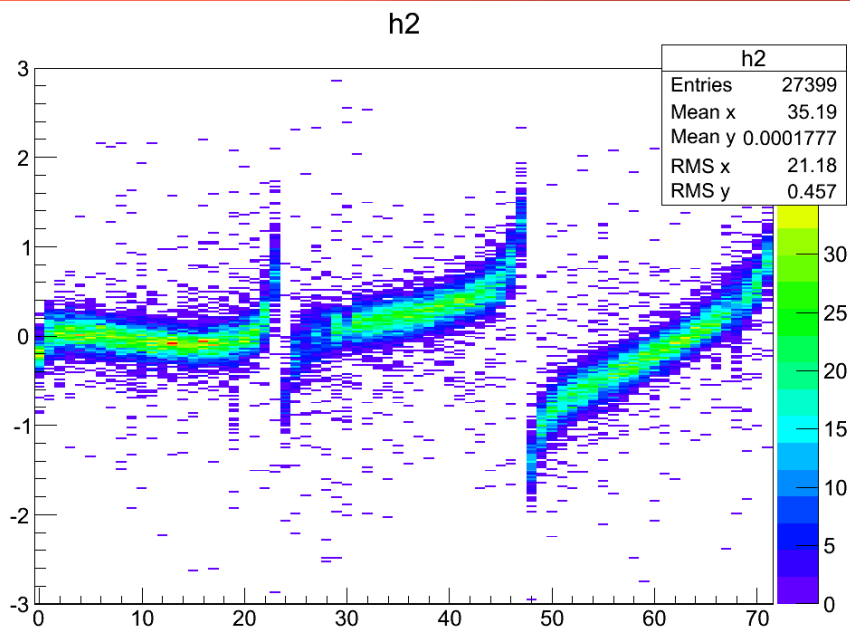
Crack scan



Number of hits vs x

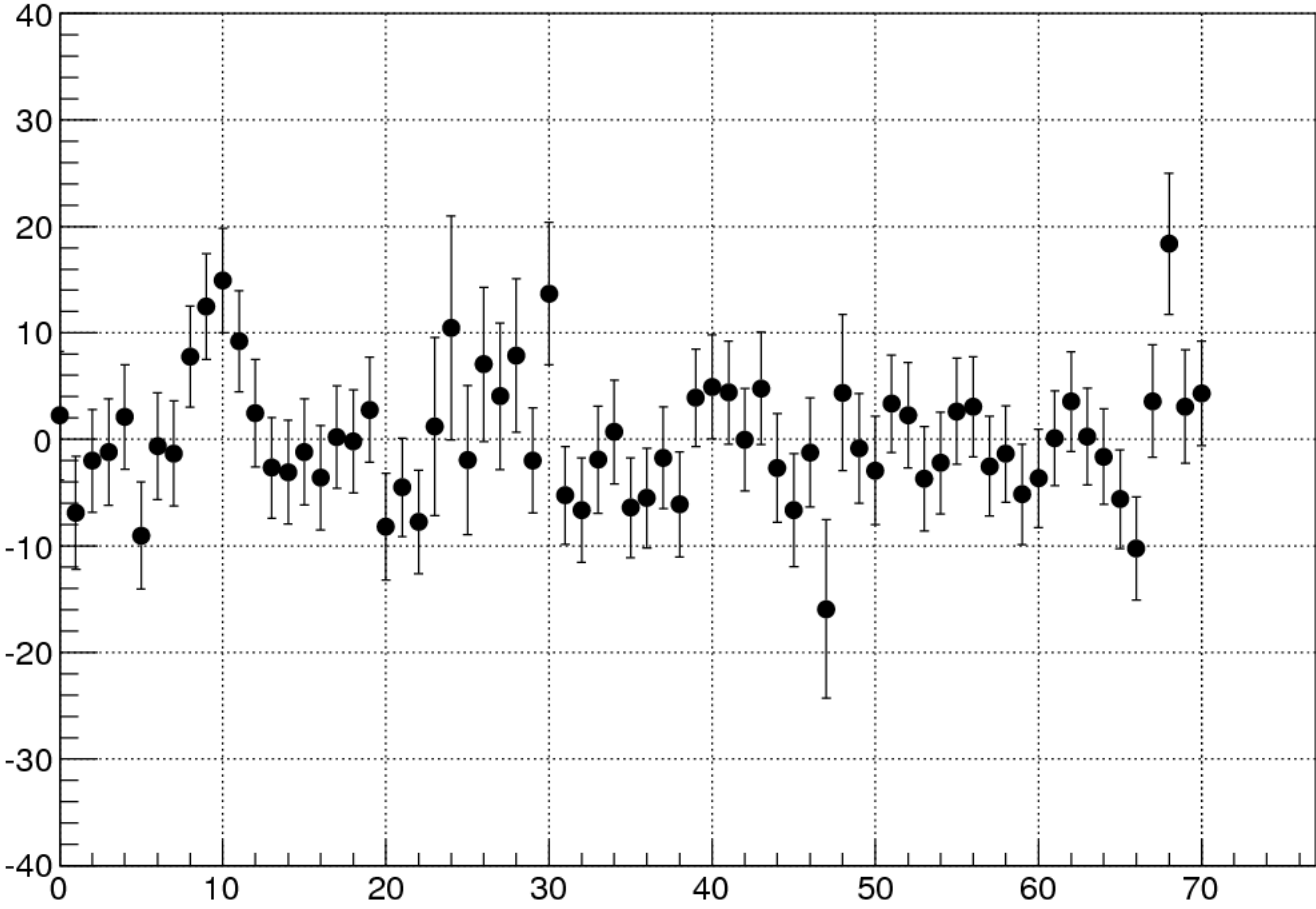
Effect of cracks is felt in an area $\sim 1\text{cm}$ around.
In the worst case, 50% of the hits are lost

Brute force alignment

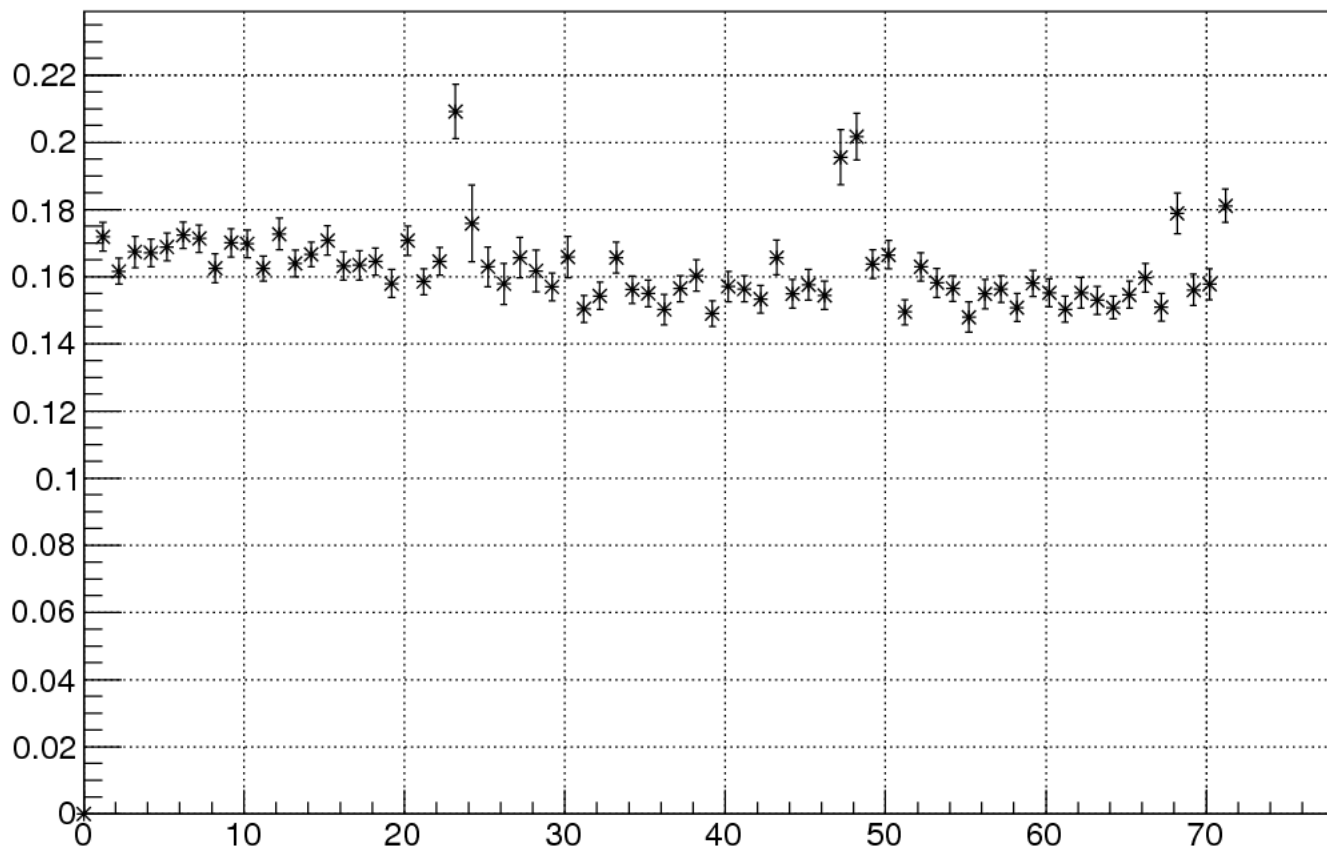


ROW NUMBER : $3 \times 24 = 72$
Displacement in mm

Residual Means

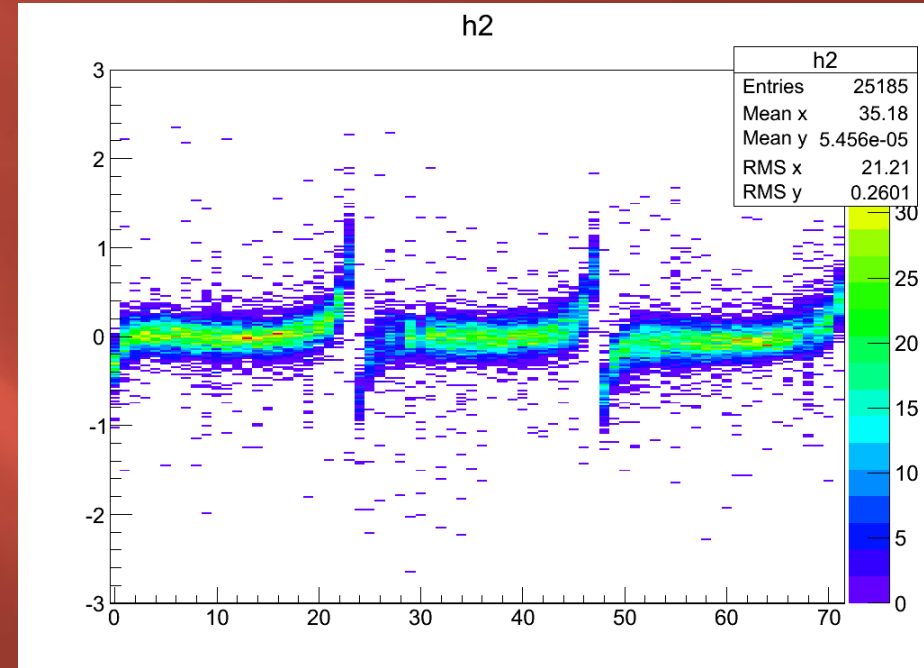
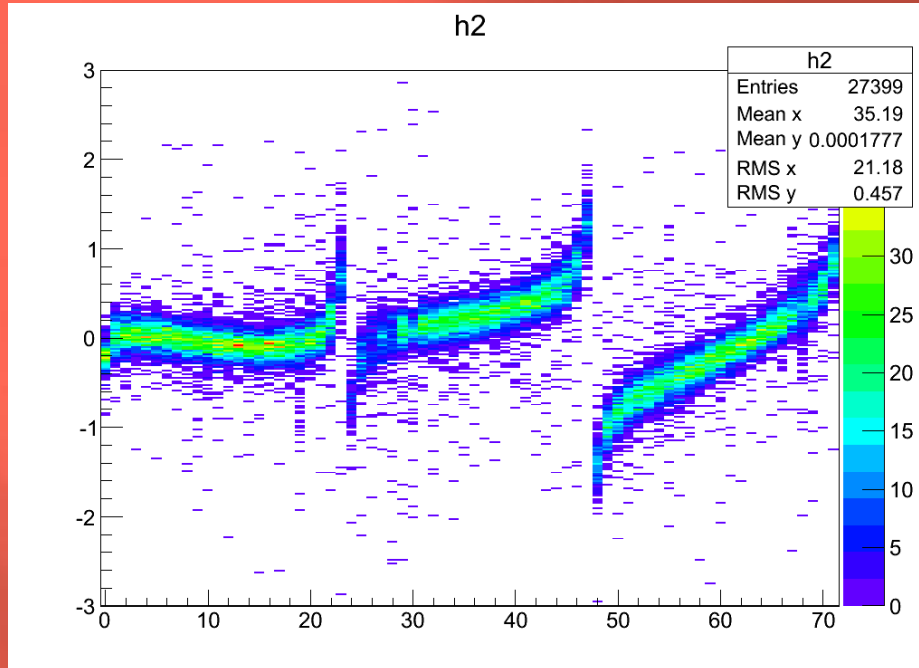


Residuals for rows



Alignment

Z=10cm



Fitted displacement :

Rotation :

$\delta\phi = -1.7$ mrad, 3.7 mrad and 8.4 mrad

Translation:

$\delta x = -54$ μm , 180 μm and 278 μm

After alignment : only distortions remain (probably ExB effect)

Maximum effect of distortions $400\mu\text{m}$

On-going electronics developments

GdSP : gaseous detector signal processing (or Go digital as Soon as Possible)
CERN-based collaboration lead by Paul Aspell, including Saclay: F. Guilloux and E. Delagnes, continuing S-ALTRO evolution.

Common development for CMS GEM μ -chambers and LC TPC. Recently considering ALICE upgrade (GEM TPC and μ chambers).

Main developments : 130 nm technology, 64 or 128 channels, low noise and ultra-low consumption, many power domains to ease power switching

First Si test to be submitted in February 2013 (AIDA)

Goals for the FE: for 10 pF detector capacitance and 100 ns peaking time
ENC < 900 e- and power < 1mW/ch

Front End specifications

From Paul
Aspell

| Parameter | VFAT2 (IBM 0.25) | SALTRO (IBM 0.13) | VFAT3 / GdSP (IBM 0.13) |
|-----------------------------------|--|---|----------------------------|
| Linear range | + - 12fC | 150fC | Max 200fC |
| Input capacitance (pF) | 20 | 0-20 | 5 - 10 - 30 - 60 |
| Noise | $\sim 500e^- \oplus 40-60e^-$ /pF @ 25ns | $\sim 650e^- \oplus 15e^-$ /pF @ 120ns | < SAltro /VFAT |

Starting from data measured on ABCN (130nm design by Jan Kaplon for ATLAS SCT):

** 800 e- @ 5pF, $t_p=22ns$, 100 μ W*

** assuming serie noise only + strong inversion for the input transistor*

→ we can hope 530 e- @10pF, $t_p= 100ns$, 200 μ W

→ Ultra Low power low noise design seems feasible (cf slide 6)

| Parameter | VFAT2 | SALTRO | VFAT3 / GdSP |
|-------------------------------|---------------------------------------|--------|--------------|
| Power (mW/channel) | 1.5 (IBM 250nm) (incl. comparator) | 10 | << 1 |

Proposal for CFE

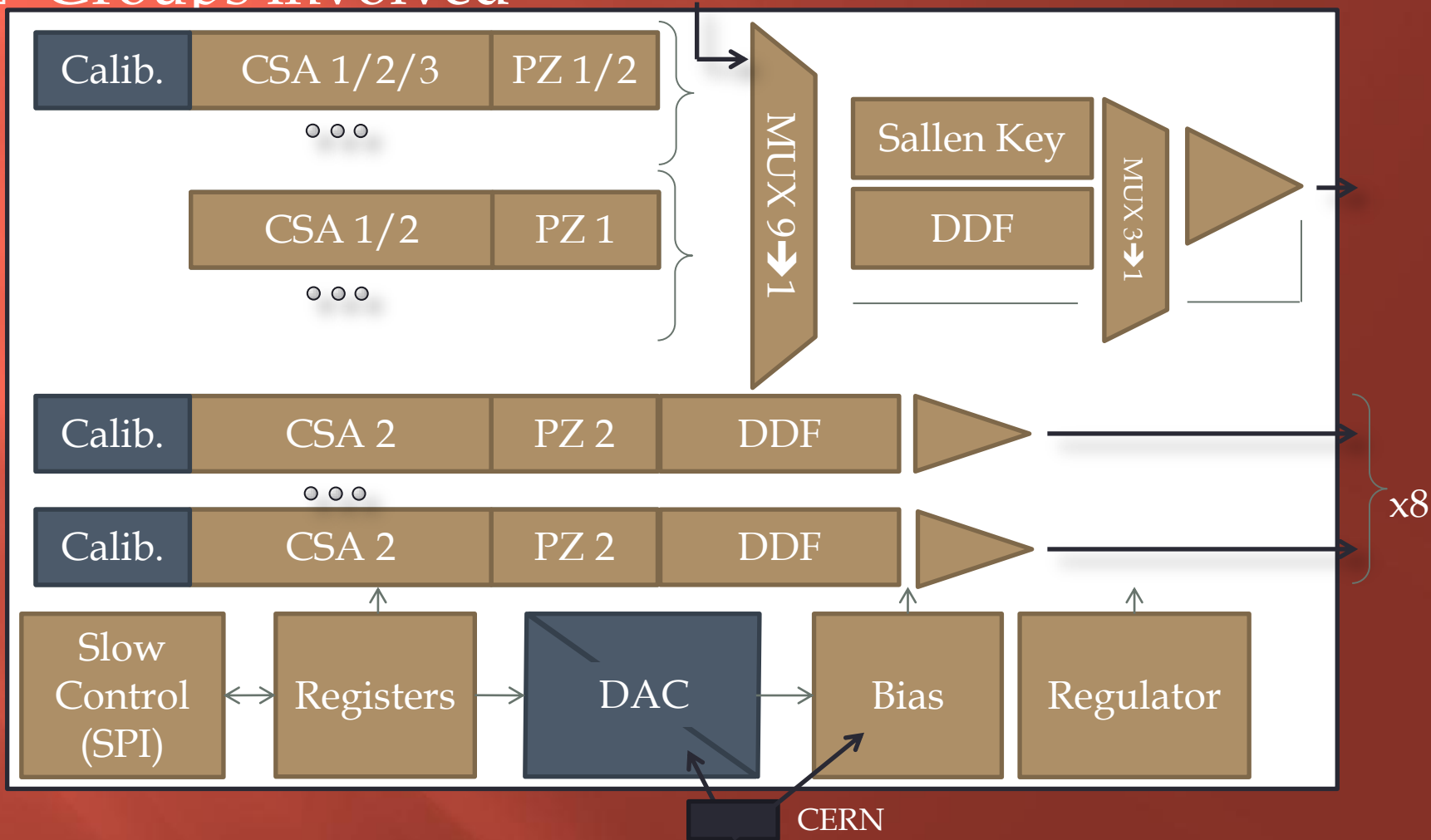
Groups involved



CEA-IRFU



INFN-BARI



Summary

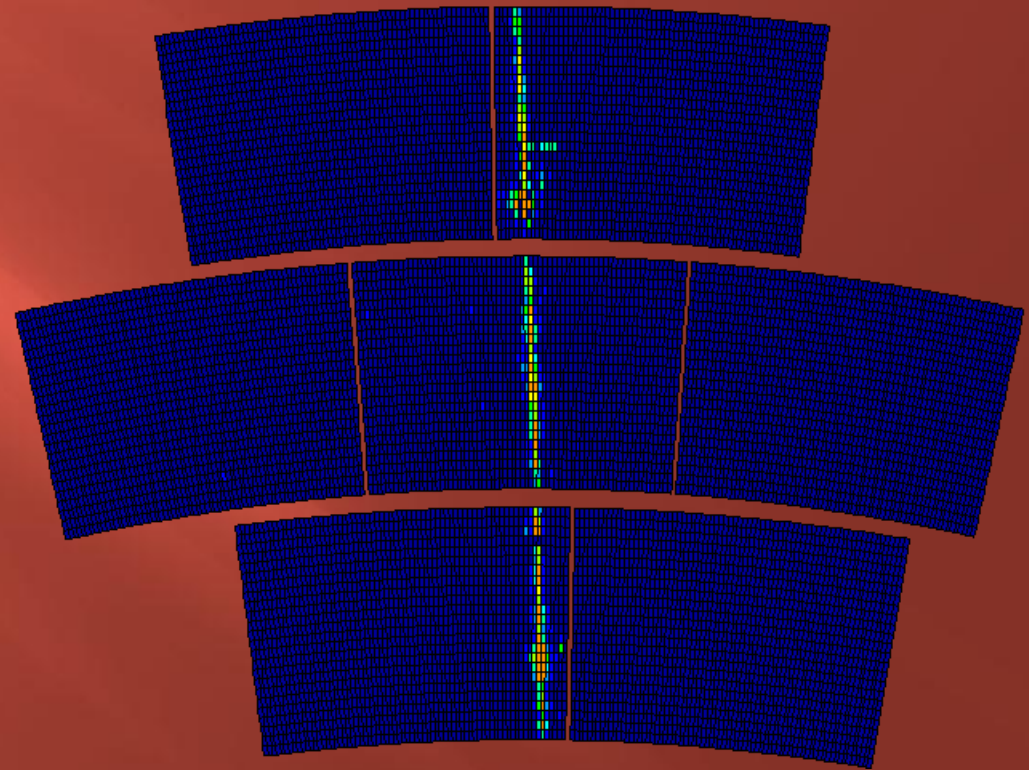
Successful test of 6 modules at a time

- Most integration questions addressed
- Improvements needed in contacts of the flat connectors
- Multi-modules aspects addressed: alignment, reconstruction

Next step: 7 modules high quality test, full calibration on the test bench, detailed analysis in 2013-2014

R&D projects: thinner meshes, other charge dispersion devices (ceramic with ruthenium oxide).

Then a larger module with smaller pads for the inner wheel.



Thanks to our DESY colleagues, especially Ralf Diener, Christophe Rosemann and Felix Müller