Hybrid pixel readout chip developments in view of the Linear Collider

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Outline

- Introduction.
- Timepix3 (TPC readout, Vertex Detector for LHCb, dosimetry, general purpose).
- SmallPix (Vertex Detector, dosimetry, general purpose).
- CLICpix prototype (Vertex Detector readout for CLIC).
- Summary.

Introduction

The CERN Medipix team is designing hybrid pixel readout chips, interesting for the CLIC Vertex Detector.

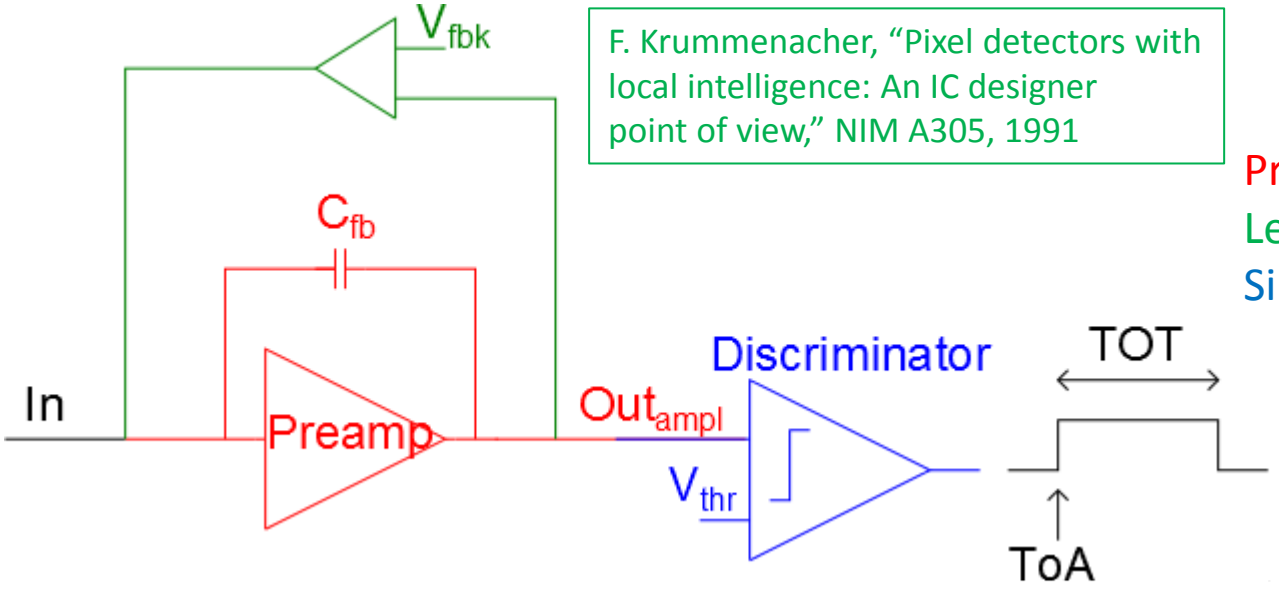
Ultimate CLIC Vertex Detector specifications:

- 25x25μm^2 pixels
- Time-Over-Threshold (4bits), Time of Arrival (4bits)
- Input charge range 1ke^--45ke^-
- 10ns time slicing
- Thickness 0.1% of the radiation length
- Power (including 50Hz pulsing) 50mW/cm^2
- Readout in 800μs (25 chips in 20ms)

These specifications are very demanding.
The R&D path to fulfil them passes through some intermediate steps:

1. Timepix3
2. SmallPix
3. CLICpix prototype

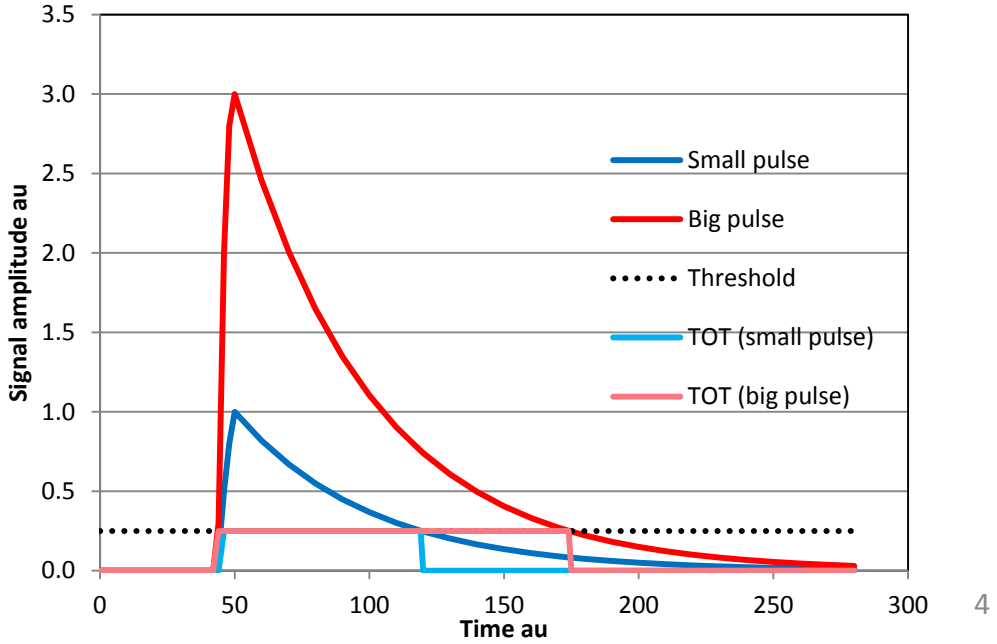
Front-End architecture in use



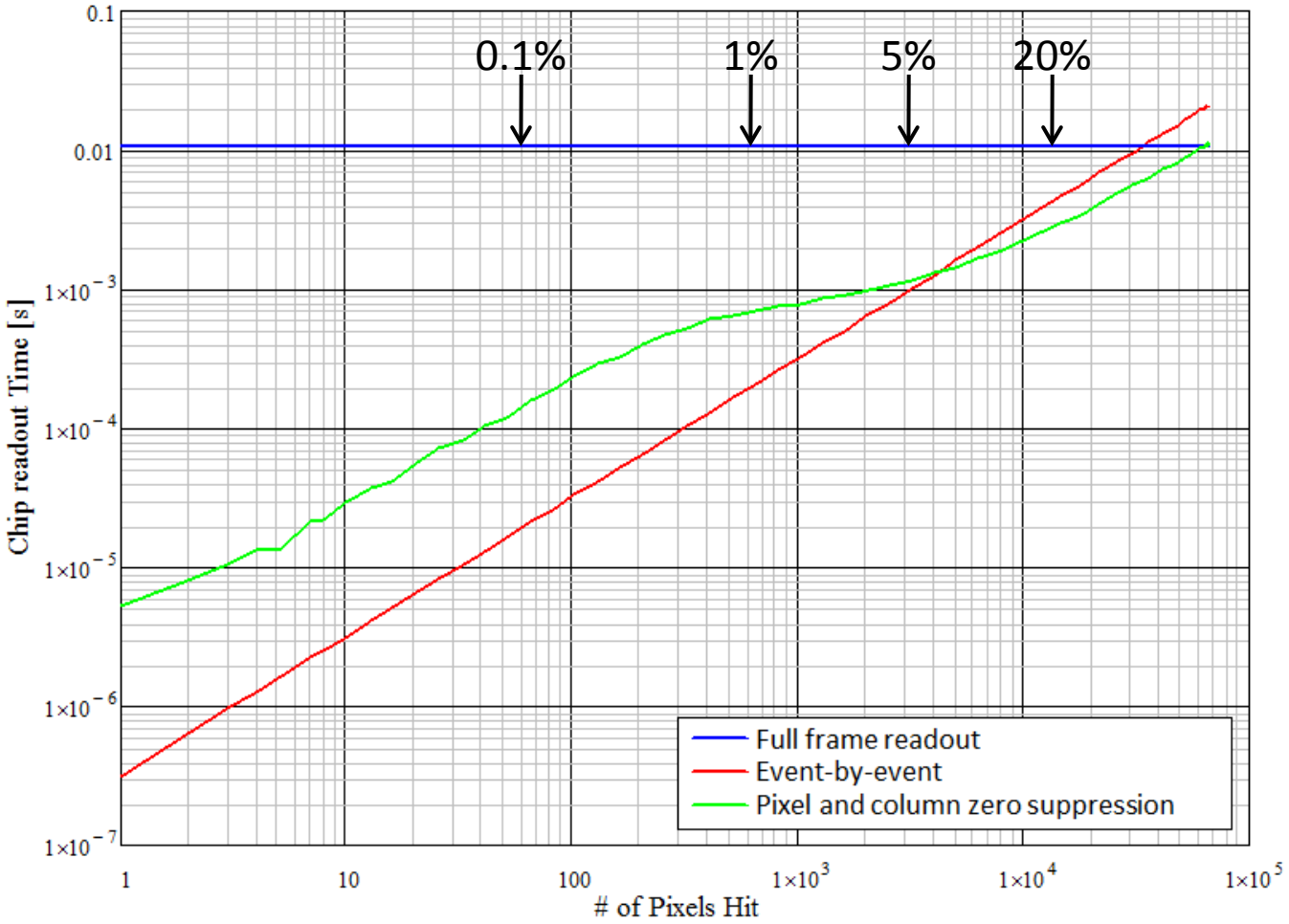
F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view," NIM A305, 1991

Preamplifier
Leakage current compensation
Single-threshold discriminator

The output of the discriminator is used to measure Time-Over-Threshold (proportional to the energy deposited in the pixel) and/or Time of Arrival (time stamping of the hit).



Readout speed (power) vs occupancy



Similar to:
Medipix3
Timepix3
SmallPix,
~CLICpix

X. Llopart

Simulation with 100MHz clock, 256x256 pixel matrix, 16 bits/pixel, randomly distributed hits.
Full frame: 256x256x16 bits are read out.
Event-by-event: at each pixel hit, 16bits for the pixel address and 16bits of content are read out.
Zero suppression: columns and pixels not containing data are skipped.

Timepix3

What TP3 is:

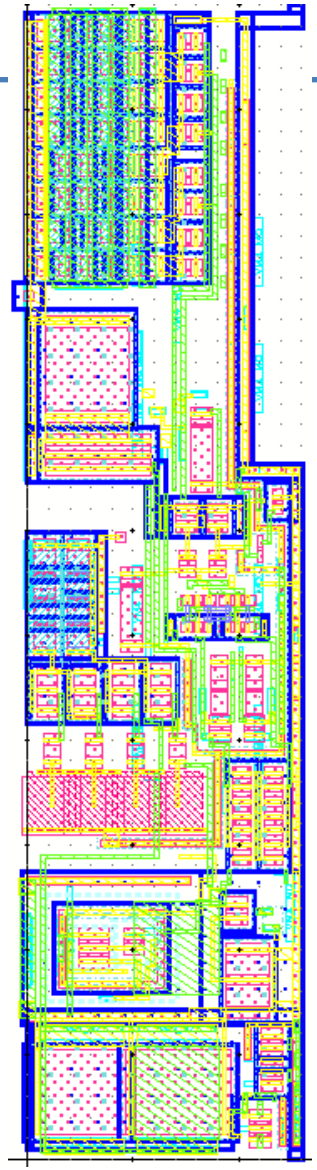
- 256x256 pixels of 55x55µm^2.
- 130nm CMOS technology.
- Simultaneous 10-bits TOT and 14-bits ToA measurements.
- Design effort between CERN, Bonn University and Nikhef.

What's new:

- 4 additional bits may be available for ToA if time stamping with a precision of 1.56ns is required.
- Data-driven readout: dead-time free, for a maximum hit rate of 20Mhits/s /cm^2.
- Shutdown/wake-up features for power pulsing tests on a full system.

Status:

- Specifications frozen.
- Analog pixel, digital pixel, periphery designs advanced.
- Integration of the different parts starting Nov 2012.



Analog Pixel
55x14µm^2

Timepix3: front-end requirements

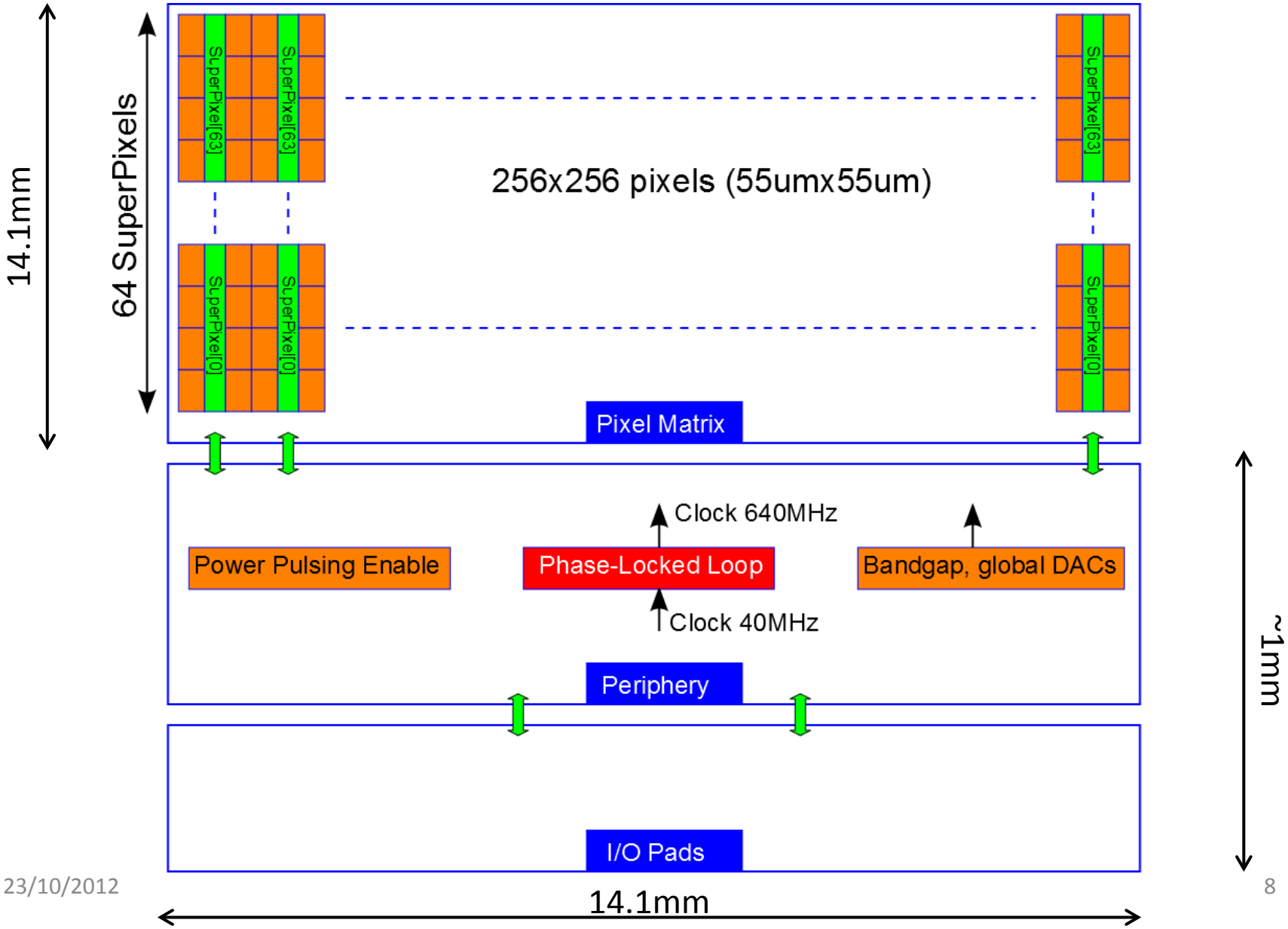
- Target: noise + pixel-to-pixel mismatch = ~90e^-, which would give minimum detectable charges around 500e^-.
- Amplitude linearity NOT required: only Time-Over-Threshold relevant

  → TOT monotonicity desired for large positive charges up to 300kh^+:

  circuit techniques to achieve this are under investigation.
- 4bit pixel DACs to equalize thresholds (compensate pixel-to-pixel mismatches).
- Target Time-to-Peak: 25ns.
- Target power consumption: 12μW/pixel.
- Simulations so far: 7.4μA/pixel@1.5V=11.1μW

  3μA preamplifier
  4μA discriminator
  0.4μA pixel DAC

Timepix3: floorplan

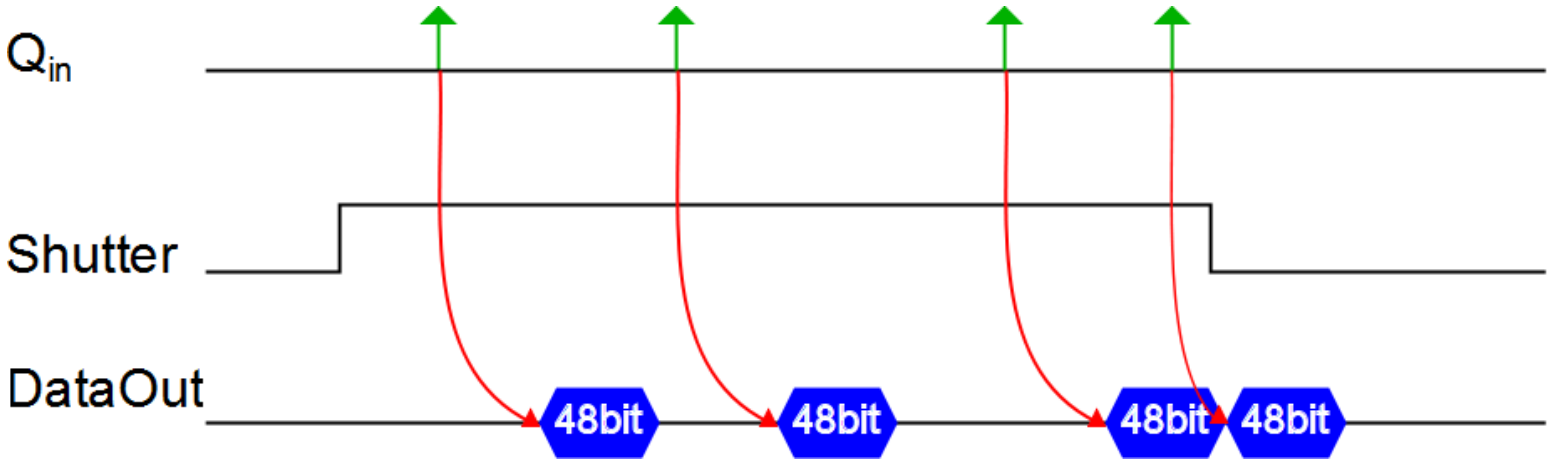


Timepix3: digital requirements

- Simultaneous ToA & TOT measurement: 10bit TOT@40MHz, 14bit ToA@40MHz.
- A Phase-Locked Loop (PLL) in the periphery provides an additional, higher-frequency clock. Target frequency up to 640MHz → additional 4bits for fine ToA@640MHz measurement.
- Packet-based readout with pixels active during readout: small readout associated dead-time of 375ns (for pixel data transfer into the SuperPixel)

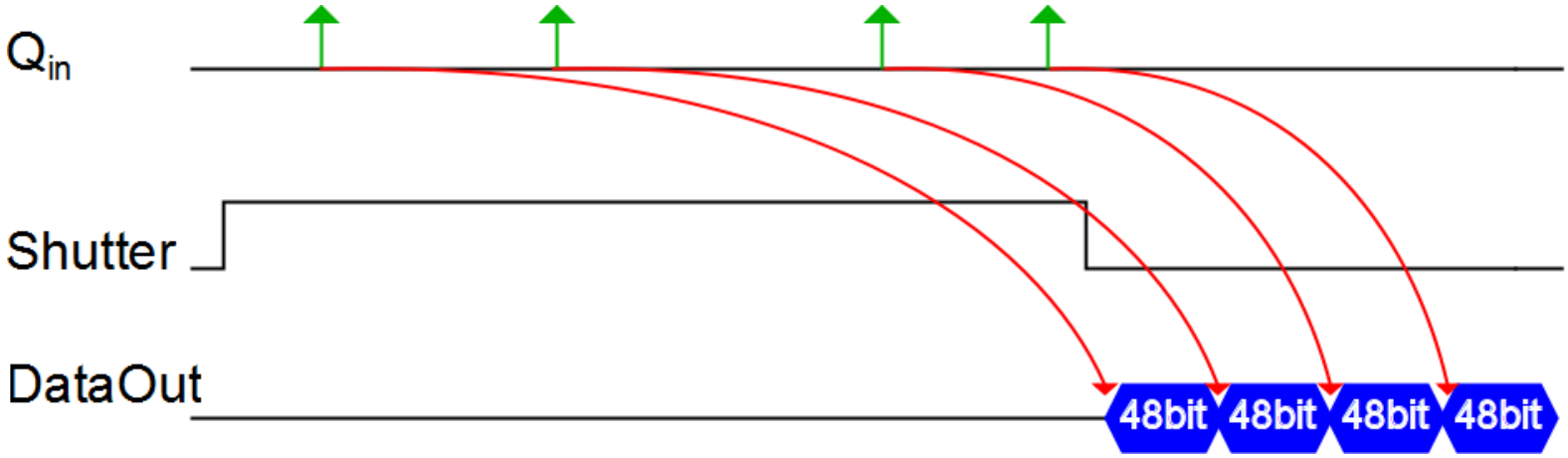
  → Maximum dead-time free hit rate: 20Mhits/s /cm² (expected for randomly distributed hits).
- Periphery: power pulsing enable for the front-end, controlled by an external pin.
- Static leakage power minimized with a high-density low-power cell library (already used in Medipix3).

Timepix3: readout modes



Data-driven readout mode.

X. Llopart



Sequential Read/Write mode.

Timepix3: power consumption

Preliminary power consumption estimations:

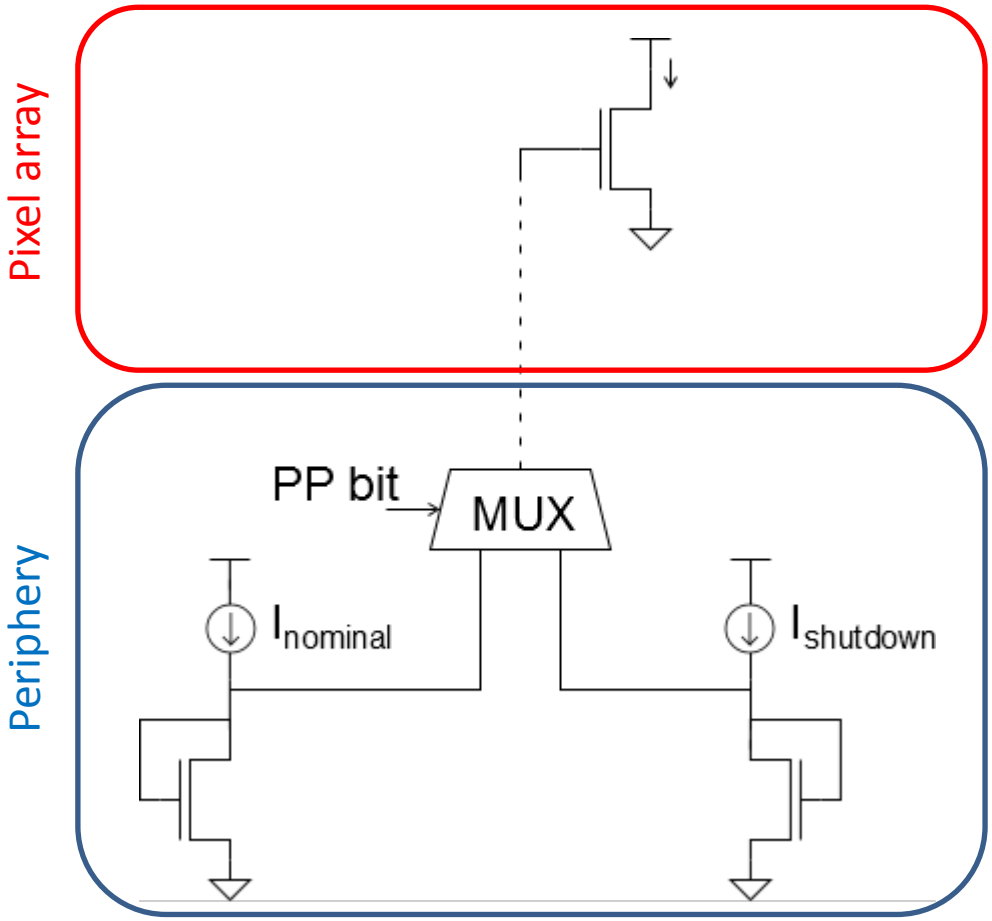
- Simulated analog power consumption ~11.1μW/pixel.
- Digital power depends on how many pixels are active (hit).
- Simulation assumption: 5000 pixels active, 1000 SuperPixels active.
- Data acquisition @ 40MHz, data-driven readout.
- Total simulated power consumption in the order of 886 mW/cm^2.
- Some blocks (IO block, PLL …) not yet included in this simulation.

T. Poikela

Timepix3: analog power pulsing

Implementing power pulsing for the analog pixel:

- DACs in the chip periphery are duplicated, thus providing two different biasing levels.
- Multiplexers in the periphery select which current should be mirrored in the pixels.
- The Power Pulsing bit (external line) toggles dynamically the current consumption of preamplifiers and discriminators in the pixel array.
- The transition times shutdown/power-up are independently programmable between 800ns and 1.28ms.



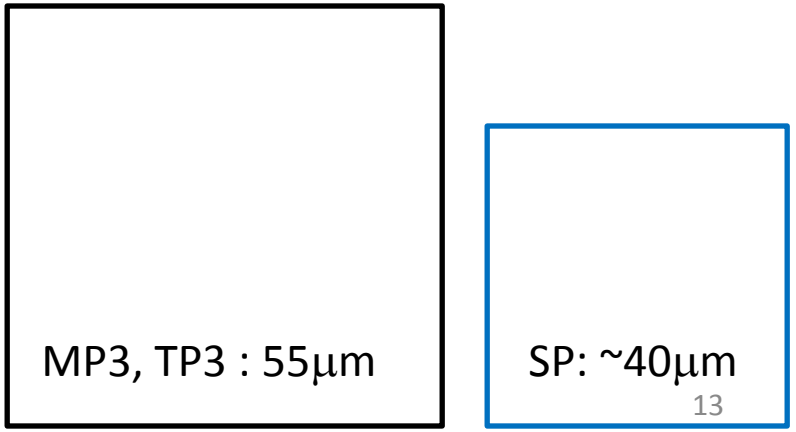
SmallPix

Main goals of the project:
• Decrease the pixel size, as compared to Timepix3 or existing chips (Medipix3), whilst providing TOT and ToA measurement.
• Create a full array of pixels (250k, if possible), suitable to system tests, including power pulsing.

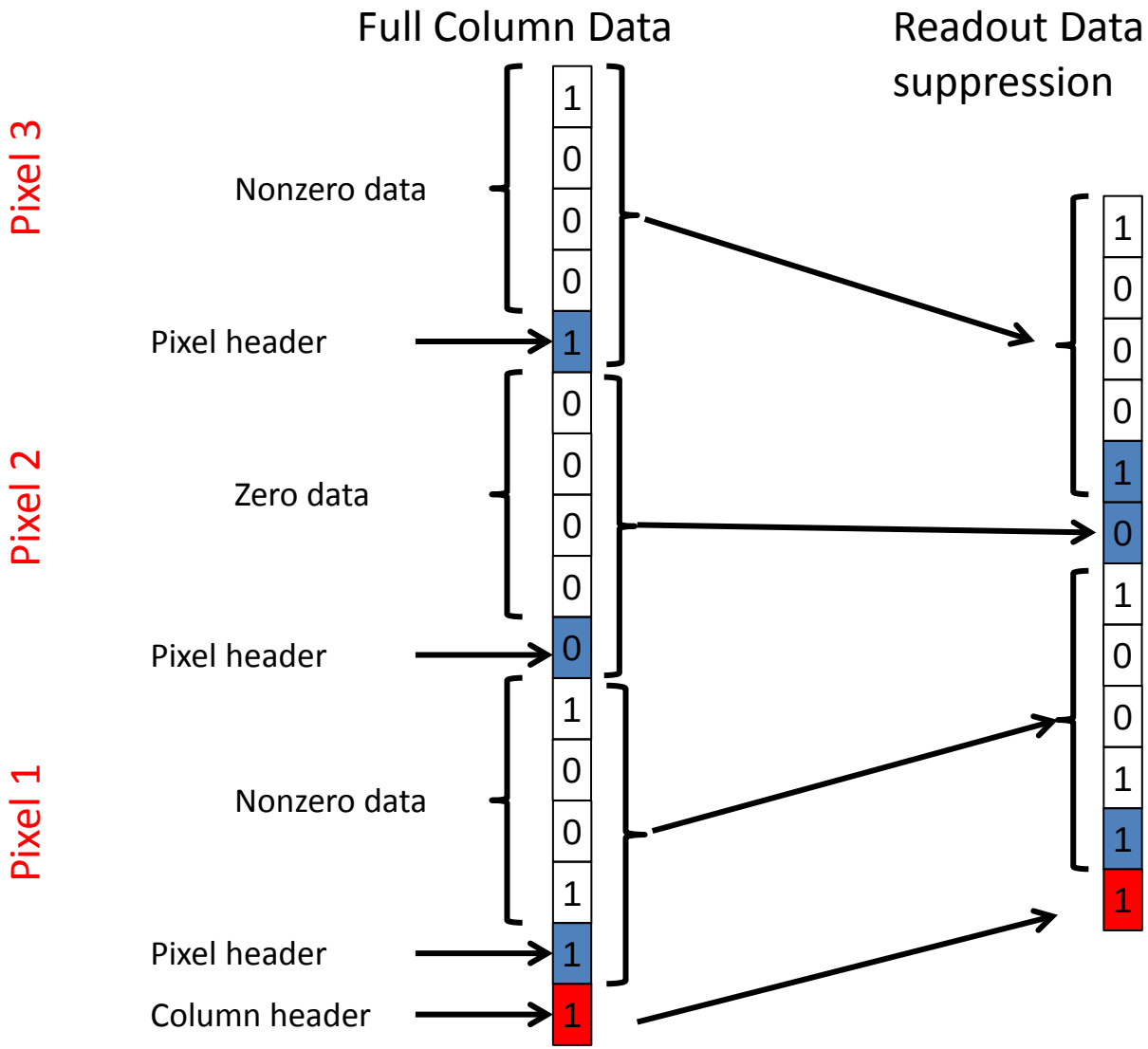
Technology: CMOS 130nm.

Main features (feasibility studies ongoing):
• Front-end design shared with Timepix3, with different form factor.
• Fast-OR to generate a trigger, fast reset.
• Data compression (zero suppression) per pixel and per column.
• Implementation of 2x2 superpixels to share resources is being considered.

Status of the project:
• Front-end under development (same as Timepix3).
• Specifications in definition phase.



SmallPix: Data Compression algorithm



R. Ballabriga

SmallPix pixel architecture

On-pixel (digital) functionalities reduced, as compared to Timepix3 ➔ smaller area.

Two modes of operation are being considered:
- TOT + ToA
- ITOT + PC

Frame-based readout.

Preliminary area estimation:

TOT+ToA	10+10bits	12+12bits	14+14bits
Analog area		730μm^2	
Digital area	580μm^2	640μm^2	710μm^2
Total size	36x36μm^2	37x37μm^2	38x38μm^2

Estimation based on Timepix3 analog front-end and Timepix1 logic (using the High-Density library of Medipix3).

➔The final pixel pitch may be about 40μm.

➔Aim at 250k pixels in a large area in the order of 400mm^2.

CLICpix prototype

P. Valerio

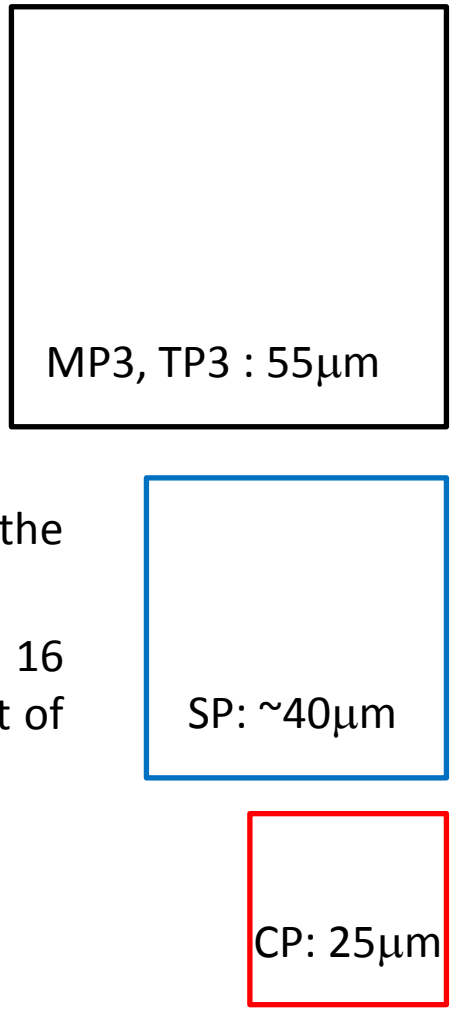
Goals of the project:

- Demonstrate feasibility and functionality of pixels as small as 25x25µm^2.
- Measure power consumption during power pulsing.

Technology: CMOS 65nm, required by the short pixel pitch specification.

Main features:

- Simultaneous 4-bit ToA and TOT measurement @100MHz.
- Photon Counting mode available for calibration purposes.
- Front-end timing accuracy <10 ns (time walk can be corrected using the TOT measurement).
- 3-level zero suppression implemented in each pixel, in clusters of 16 pixels and in each column, aiming at the ultimate CLIC target readout of a full chip in <800µs (for 10% occupancy).
- Power pulsing features.



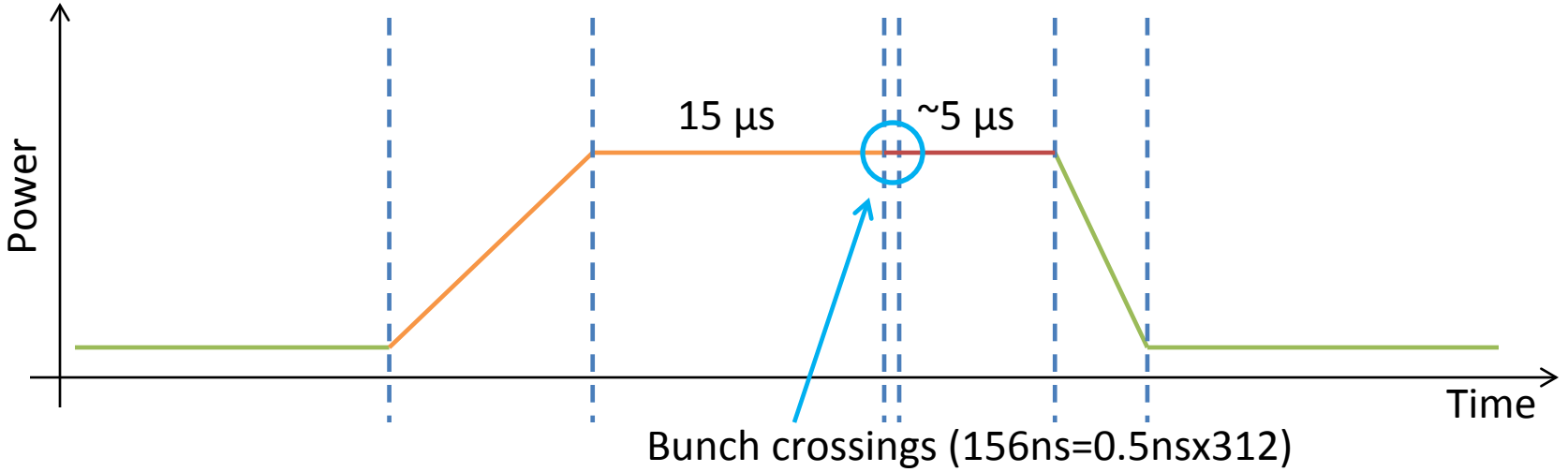
CLICpix power budget

- Analog pixel: ~5.4μA @ 1.2V = 6.5μW/pixel

  → ~1-2W/cm^2 if run continuously
- Power pulsing scheme: target power consumption <50 mW/cm^2

  → air cooling
- Analog power ON and power OFF implemented one column at a time, with a programmable delay between columns.

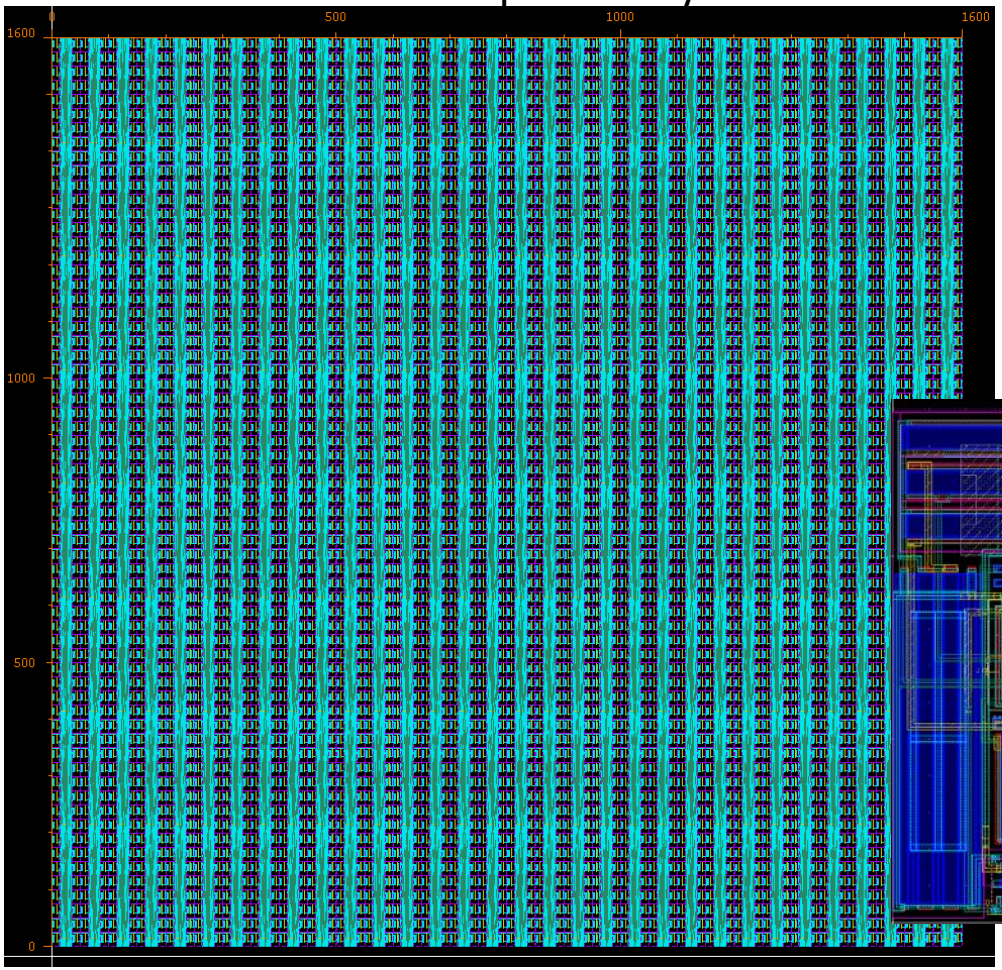
  Transitions independently programmable from 320 ns to 80 μs.
- Wake-up time ~15μs.



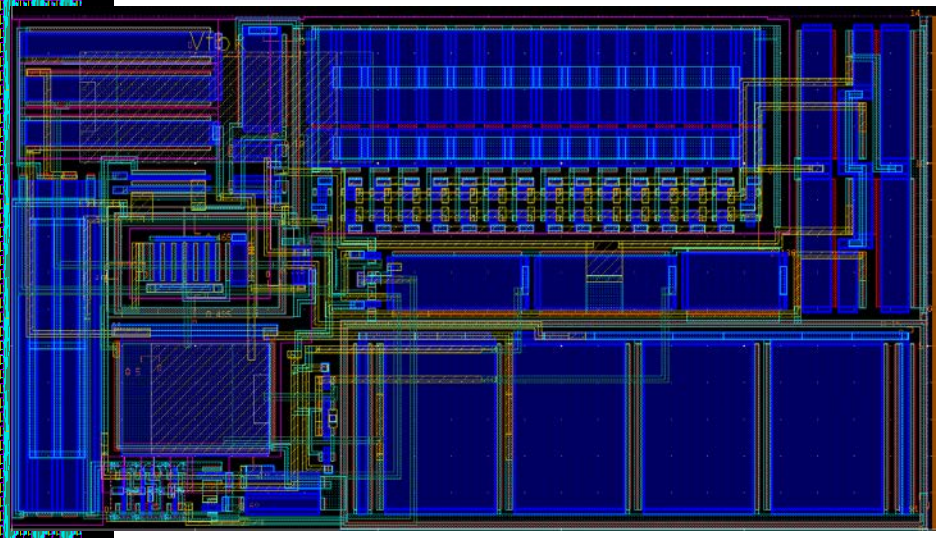
- Digital pixel implemented using low-power components.
- Clock gating for the digital parts.

CLICpix status

1.6x1.6mm^2 pixel array.



25x14μm^2 analog pixel.



Some test structures were already submitted, fabricated and tested in 2011.
CLICpix prototype submission scheduled in November 2012 with a Multi-Project Wafer run.

Summary

	Timepix3	Smallpix	CLICpix prototype
Technology	130nm	130nm	65nm
Pixel size	55x55μm^2	~40x40μm^2	25x25μm^2
Analog/digital	730/2300μm^2	~730/710μm^2	350/275μm^2
Chip area	210mm^2	~400mm^2	5.4mm^2 (pixel array 2.56mm^2)
#pixels/chip	256x256 (65k)	~250k	64x64 (4k)
Functionality	TOT 10bit, ToA 14+4bit or ITOT 14bit, PC 10bit	ToA+TOT or PC+ITOT	ToA 4bit, TOT 4bit or PC 4bit (only for calibration)
Measurement clock	40MHz	tbd	100MHz
Readout clock	160MHz	tbd	320MHz
Readout mode	Data Driven or Sequential	Sequential	Sequential
Power pulsing	YES	YES	YES
Data Compression	Per pixel (sparse readout)	Per pixel, per column	Per pixel, per cluster, per column

TOT= Time-Over-Threshold
ITOT=Integral TOT
ToA= Time of Arrival
PC= Photon Counting

Thanks for your attention!

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