Low mass, low power vertex detector for an ILC experiment based on μs fast CMOS pixel sensors adapted to 1 TeV running conditions

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- Sensor design : coll. with IRFU-Saclay -

- Ladder design : PLUME coll. - STAR coll. - ALICE coll. - CBM coll.

Univ. Texas/Arlington – 23 Octobre 2012

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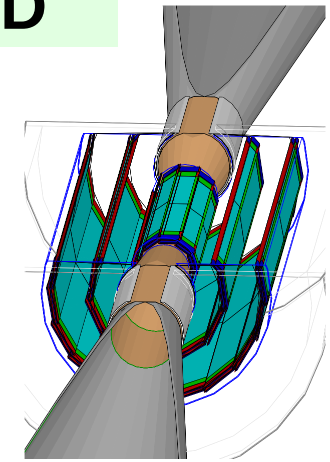
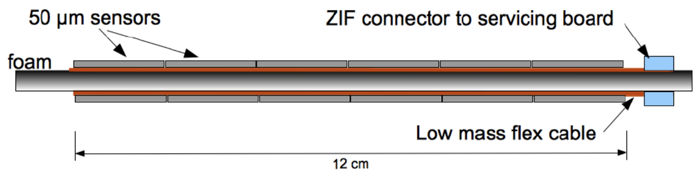
CMOS Pixel Sensors for the ILD-VXD

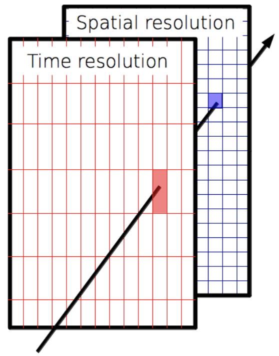


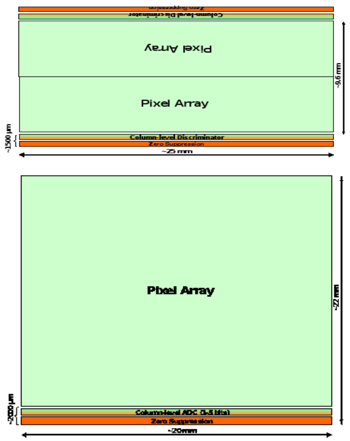
- **Two types of CMOS Pixel Sensors (CPS):**
  - ⁂ **Inner layers** ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm
  - ⁂ **Outer layers** ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⁂ Total VXD instantaneous/average power $<$ 600/12 W (0.18 μm process)



- **2-sided ladder concept for inner layer :**
  - ⁂ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)

    & *E*longated pixels (16×64/80 μm^2) on external ladder face ($t_{r.o.} \sim$ 10 μs)



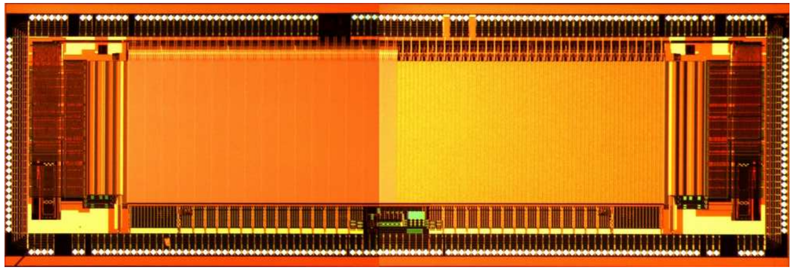


- **Sensor final "500 GeV" prototypes :** fab. in Winter 2011/12
  - ⁂ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷
    - ↪ one side : 256 pixels (16×16 μm^2)

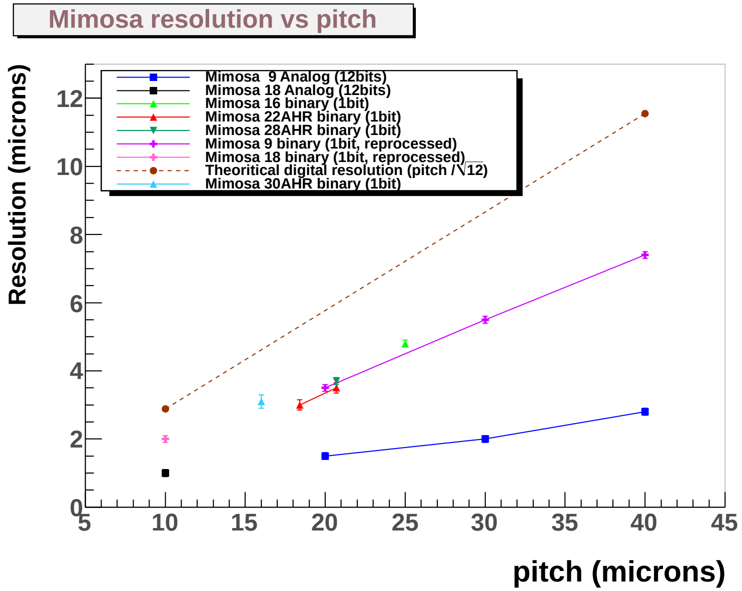
      other side : 64 pixels (16×64 μm^2)
  - ⁂ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC
  - ⁂ prototypes still fabricated in 0.35 μm process (cost issue)

CMOS Pixel Sensors: Status of Baseline Devt

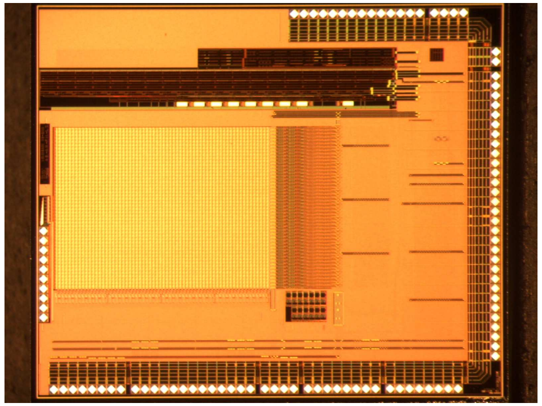
- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷



  - ⋇ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⋇ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⋇ columns length $\simeq$ final sensor (4-5 mm long)
  - ⋇ **high resolution side : pixels of 16$\times$16 μm^2 $\Rrightarrow$ expect $\sigma_{sp} < 3\ \mu m$**
    - 128 columns (discri) & 8 col. (analog) of 256 rows
    - read-out time $\lesssim$ 50 μs
  - ⋇ **time stamping side : pixels of 16$\times$64 μm^2 $\Rrightarrow$ $t_{r.o.} \sim$ 10 μs**
    - (expect $\sigma_{sp} \sim$ 6 μm)
    - 128 columns (discri) and 8 col. (analog) of 64 rows
    - lab tests positive : N $\sim$ 15 e$^-$ ENC & discri. all OK for $t_{r.o.} = 10\ \mu s$
  - ⋇ beam tests (CERN-SPS) in July '12 $\Rrightarrow$ σ_{sp} ▷ ▷ ▷



- **MIMOSA-31: prototype for ILD-VXD outer layers**



  - ⋇ pixels of 35$\times$35 μm^2 (power saving) ▷ ▷ ▷
  - ⋇ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    - $\hookrightarrow$ expect $\sigma_{sp} \lesssim$ 3.5 μm
  - ⋇ $t_{r.o.} \sim$ 10 μs (1/10 of full scale chip $\rightarrowtail$ $\sim$ 100 μs)
  - ⋇ beam tests (DESY) in Q1/2013 $\Rrightarrow$ σ_{sp}, ϵ_{det}, fake rate

Evolving towards an Optimal CMOS Process

- **Motivation: 0.35 μm process used up to now does not allow to fully exploit the potential of CPS**
- **Main limitations of presently used 0.35 μm CMOS fabrication process:** (not restricted to ILC specs)

CMOS process fab. parametres	**In-pixel circuitry**	**Read-out speed**	**Power consum.**	**Insensitive areas**	**TID ($\triangleright$ ILC)**	**Data throughput**
Feature size	X	X	X	X	X	
Planar techno.	X	X	X		x	
Nb (metal layers)	X	X		X		
Clock frequency				X		X

- **Moving to a 0.18 μm imaging CMOS process (Tower/Jazz SC):**
  - ⋇ Deep P-well (quadruple well techno.) $\Rrightarrow$ in-pixel discriminators
  - ⋇ 6 metal layers (instead of 4) $\Rrightarrow$ in-pixel discriminators, avoids insensitive zones
  - ⋇ Epitaxial layer : high-resistivity ($\triangleright$ 1 k$\Omega \cdot cm$), ”18 μm thick”
  - ⋇ Stiching $\Rrightarrow$ multi-chip slabs

  $\Rrightarrow$ process very well suited to the VXD specifications

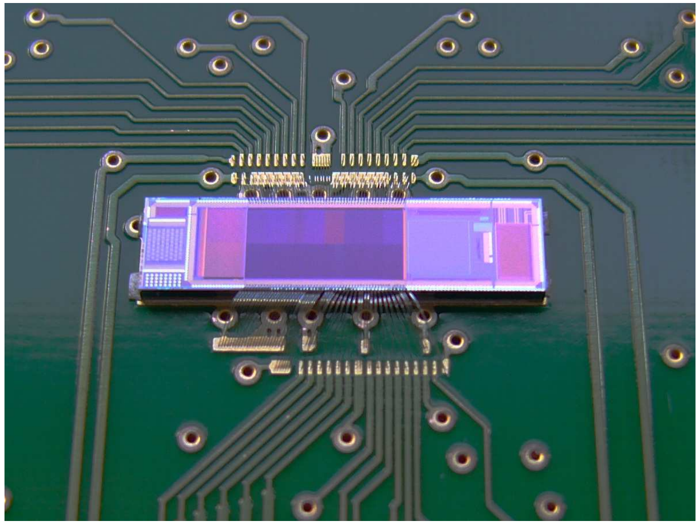
- **Prototyping started in Summer 2011, driven by ILD-VXD, CBM-MVD, ALICE-ITS, SuperB-SVT**

  Main objective: assess CCE & N $\rightarrowtail$ SNR $\rightarrowtail$ ϵ_{det}, radiation tolerance (T),

  $\triangleright$ $\triangleright$ $\triangleright$ use of deep P-well, elongated pixels

0.18 μm Technology Prototyping

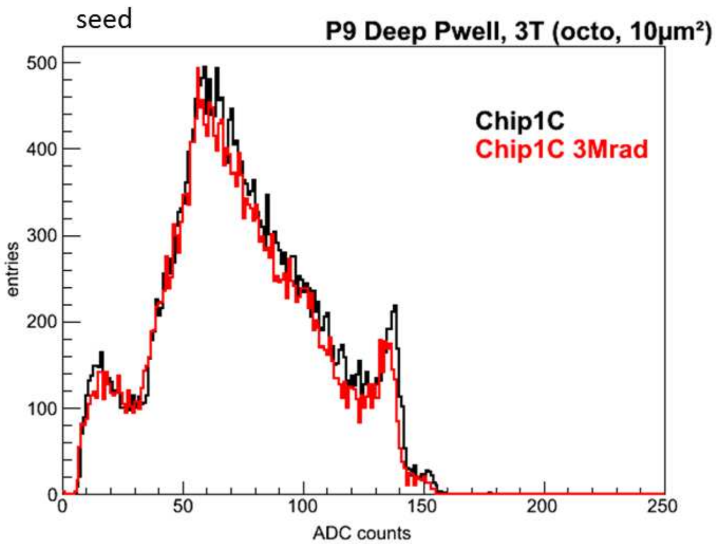
- **MIMOSA-32 : technology exploration**
  - ⋇ fabricated in Winter 2011/12 with high resistivity epitaxial layer
  - ⋇ various pixels : sensing syst., pre-ampli., elongated, etc.
  - ⋇ lab tests with ^{55}Fe source, t_{ro} = 32μs:
    - good charge collection efficiency observed (high-res epi)
    - no parasitic charge collection seen with Deep P-well
    - N $\sim$ 15-18 e^- ENC
    - irradiation up to 3 MRad has marginal impact

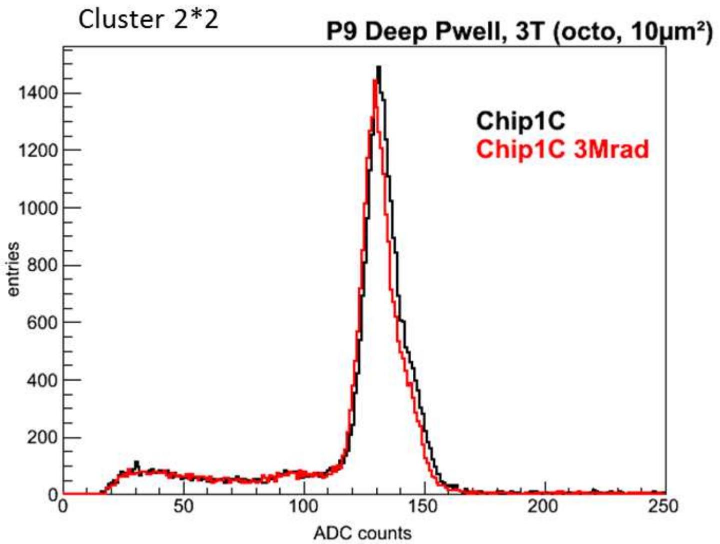


Charge collected from

5.9 & 6.5 keV X-Rays

(room temperature, 32 μs)





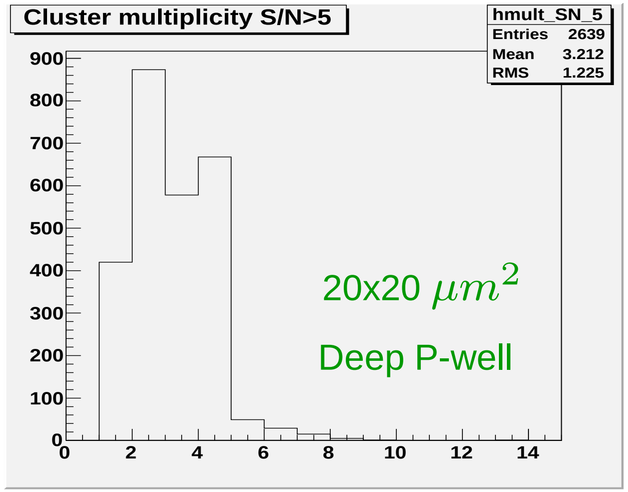
- **Test of in-pixel amplification not convincing** (reduced dynamics w.r.t. 0.35 μm technology)

  $\Rrightarrow$ New prototype (MIMOSA-32ter) fabricated $\longrightarrow$ Tests starting this week

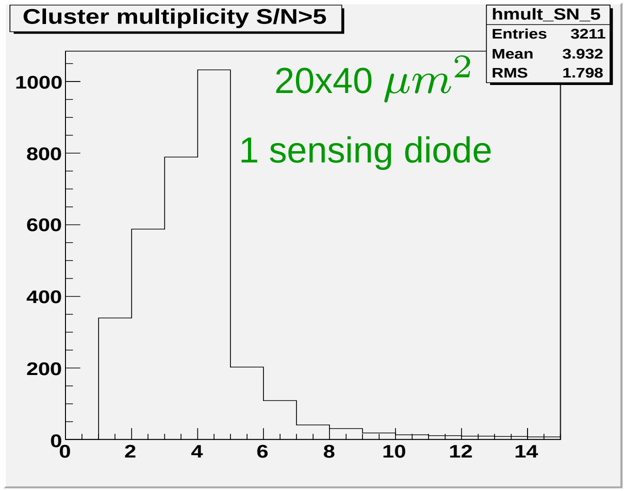
Cluster Multiplicities

- **Beam tests with 60-120 GeV negatively charged particles at CERN-SPS in Summer (T = 30°C) :**

- **Average cluster multiplicity (RMS):**
  - ⋇ 20x20 μm^2 pixels hosting a deep P-well
    - $\Rrightarrow$ average multiplicity = 3.2 (rms = 1.2)



  - ⋇ 20x40 μm^2 staggered pixels with 1 sensing diode
    - $\Rrightarrow$ average multiplicity = 3.9 (rms = 1.8)

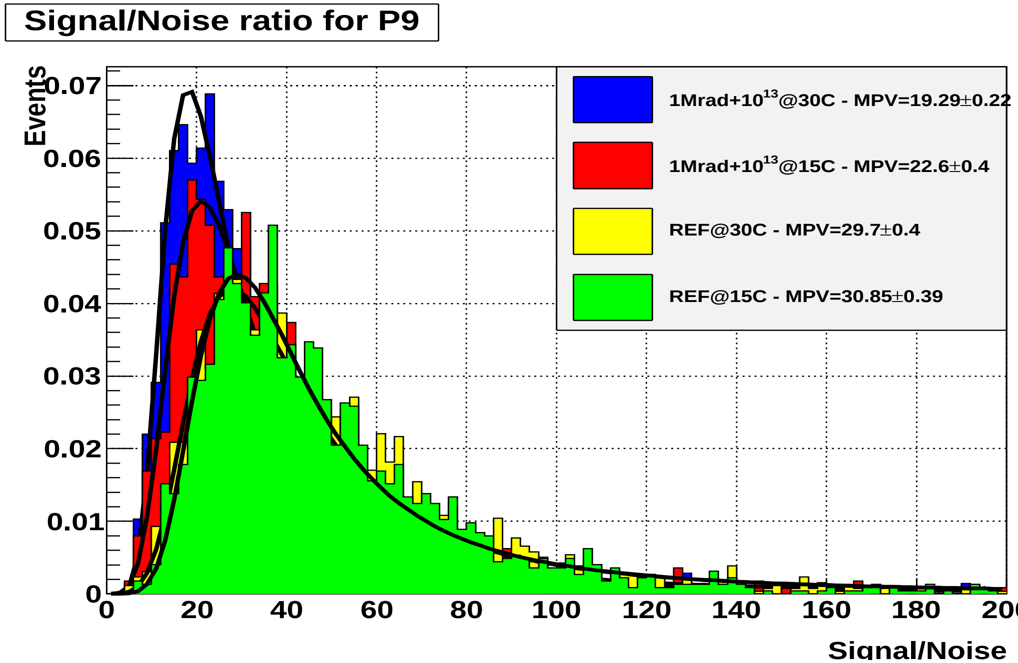


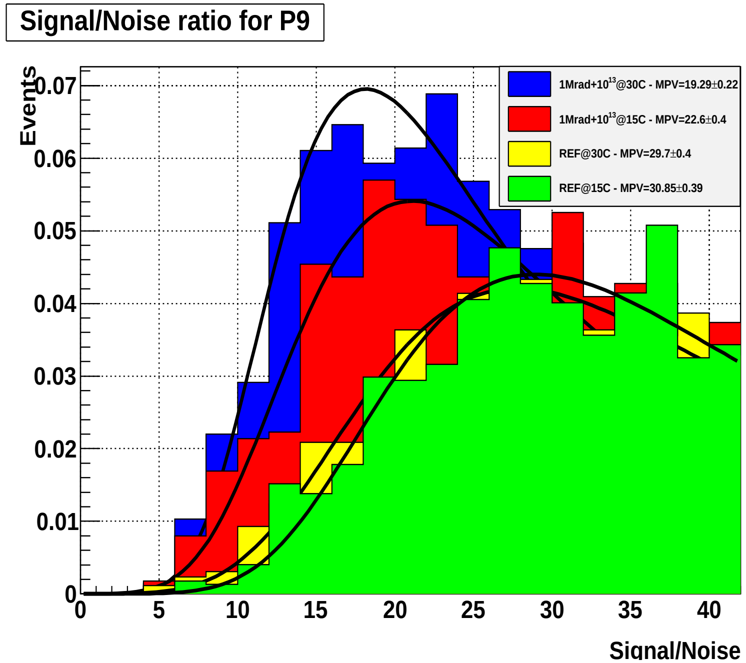
- **Measurement outcome :**
  - ⋇ evidence for high-resistivity epitaxial layer
  - ⋇ elongated (staggered) pixels exhibit marginal cluster extension

P9: Deep P-Well (3T)

- **Coolant temperature and (ALICE-ITS) radiation dose dependence:**

  ⋇ T = 15°C & 30°C ⋇ Doses: 1 MRad$\oplus 1 \times 10^{13}$n$_{eq}$/cm^2 $\equiv$ 10$\times$TID $\oplus$ 10$^2 \times$ TNID / ILC yr





- **SNR (MPV) and detection efficiency** *(stat. uncertainty only)*:

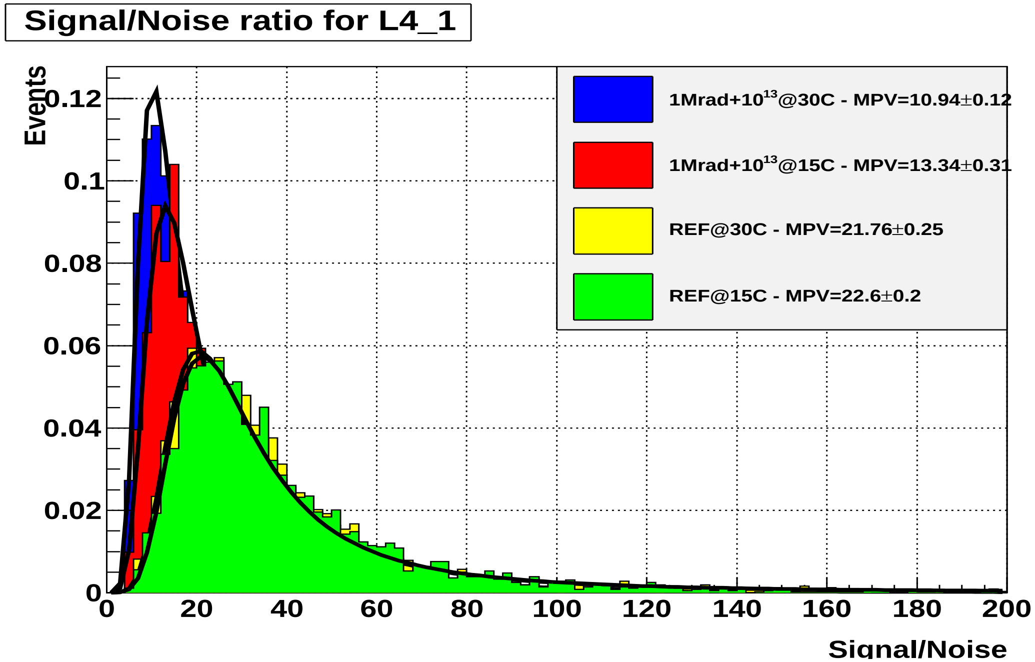
Irradiation Dose	SNR (MPV) 15°C	SNR (MPV) 30°C	Detection efficiency [%] 15°C	Detection efficiency [%] 30°C
0	*30.9 ± 0.4*	*29.7 ± 0.4*	*99.91 ± 0.06*	*99.7 ± 0.1*
1 MRad & 1$\times 10^{13}$n$_{eq}$/cm^2	*22.6 ± 0.4*	*19.3 ± 0.2*	*99.92 ± 0.08*	*99.87 ± 0.07*

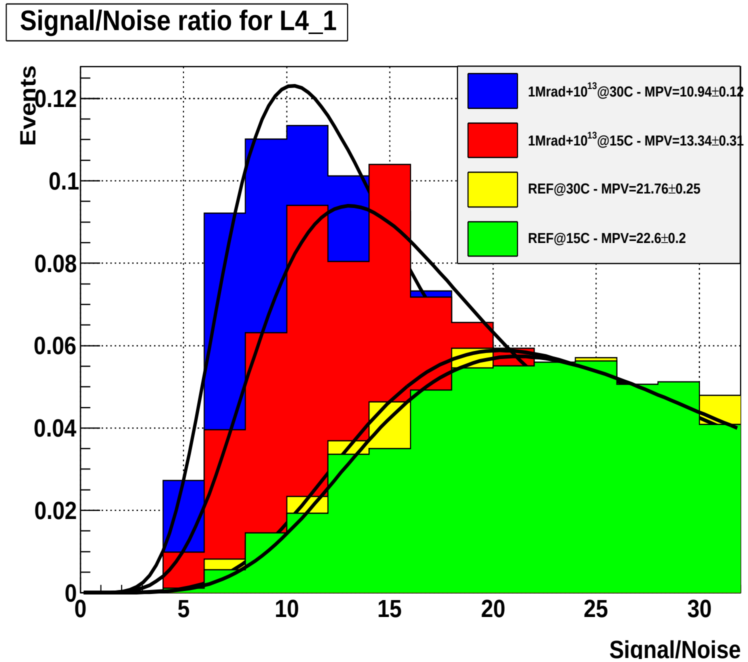
⇛ ILC radiation load has no effect

L4-1: 20x40 μm^2 (1 Sensing Diode)

- **Coolant temperature and (ALICE-ITS) radiation dose dependence:**

  ⁜ T = 15°C & 30°C ⁜ Doses: 1 MRad $\oplus$ $1\times10^{13}n_{eq}/cm^2 \equiv 10\times$TID $\oplus$ $10^2\times$ TNID / ILC yr





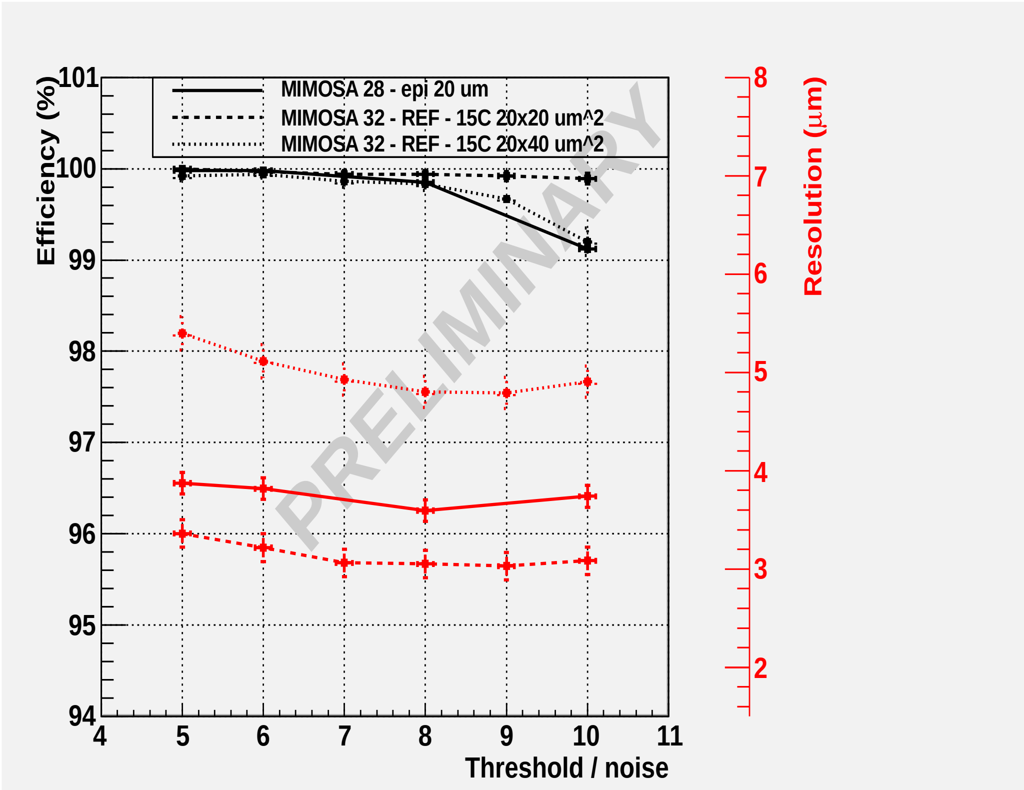
- **SNR (MPV) and detection efficiency** *(stat. uncertainty only)*:

Irradiation Dose	SNR (MPV) 15°C	SNR (MPV) 30°C	Detection efficiency [%] 15°C	Detection efficiency [%] 30°C
0	*22.6 ± 0.2*	*21.8 ± 0.3*	*99.86 ± 0.06*	*99.78 ± 0.08*
1 MRad & $1\times10^{13}n_{eq}/cm^2$	*13.9 ± 0.3*	*10.9 ± 0.1*	*99.51 ± 0.25*	*97.99 ± 0.25*

$\Rrightarrow$ ILC radiation load has no effect

Spatial Resolution

- **Beam test (analog) data used to simulate binary charge encoding :**
  - ⋇ Apply common SNR cut on all pixels using <N>
    - ↪ simulate effect of final sensor discriminators
  - ⋇ Evaluate single point resolution (charge sharing) and detection efficiency vs discriminator threshold for 20x20 μm^2 pixels and 20x40 μm^2 staggered pixels (1 sensing diode)



- **Comparison of 0.18** μm **technology (**$>$ **1** $k\Omega \cdot cm$**) with 0.35** μm **technology (**$\lesssim$ **1** $k\Omega \cdot cm$**)**
  (resp. pitch values: 20.7 μm and 20.0 μm)

- $\sigma_{sp}^{bin} \simeq 3.2 \pm 0.1\ \mu m$ (20x20 μm^2) AND $\simeq 5.4 \pm 0.1\ \mu m$ (20x40 μm^2)
  - ↪ expect $\sim$ 2.8 μm for 17×17 μm^2 pixels (ILD-DBD)

Read-Out Acceleration

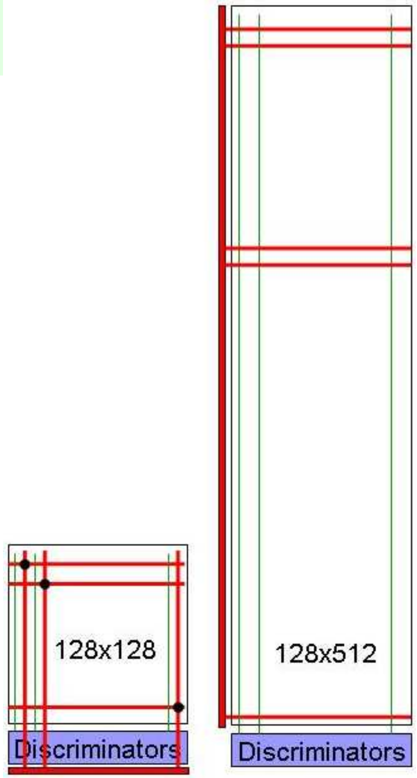
- **Motivations for faster read-out:**
  - ⋇ robustness w.r.t. predicted 500 GeV BG rate (keep small inner radius, no Anti-DID, ..)
  - ⋇ standalone inner tracking capability (e.g. soft tracks)
  - ⋇ compatibility with high-energy running: beam BG at $\sqrt{s} \gtrsim$ 1 TeV $\Rrightarrow$ beam BG ($\gtrsim$ 1 TeV) 3–5$\times$BG (500 GeV) ?

- **How to accelerate the elongated pixel read-out**
  - ⋇ elongated pixel dimensions allow for in-pixel discri. $\Rrightarrow$ $\geq$ 2 faster r.o.
  - ⋇ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⋇ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm process needed: 6-7 ML,, design compactness, in-pixel CMOS T, ...
  - ⋇ conservative step: 2 discri./col. **end** (22 μm wide) $\Rrightarrow$ simult. 2 row r.o.

- **Expected VXD performances at 1 TeV (and 0.5 TeV)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	Occupancy [%] 1 TeV (0.5 TeV)	Power inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (10 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

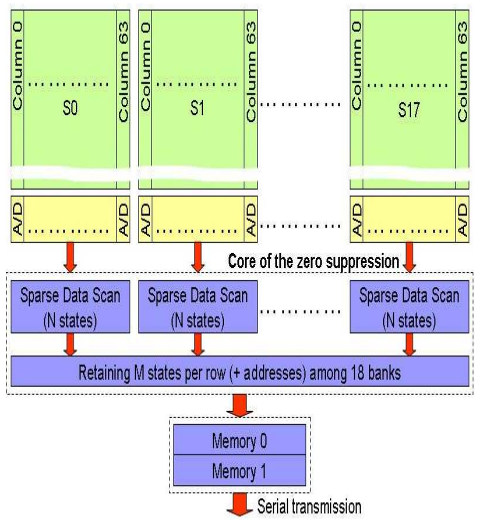
Next Steps of 0.18μm Architecture Prototyping

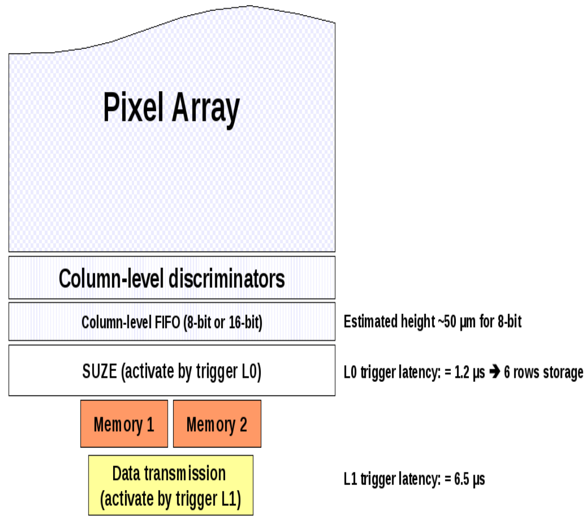


- **1st step : MISTRAL $\equiv$ MIMOSA FOR THE INNER SILICON TRACKER OF ALICE**
- **MIMOSA-22THR (Upstream part of sensor) :**
  - ⁜ Col. // pixel array with in-pixel ampli + pedestral subtraction (cDS)
  - ⁜ Each of 128 columns ended with discriminator + 8 columns without discri.
  - ⁜ Pixel array sub-divided in sub-arrays featuring different pixel designs (22$\times$22/33 μm^2)
  - ⁜ 2 options $\rightarrowtail$ submission in Decembre'12 :
    - ○ sgle end of column discriminator $\equiv$ translation of MIMOSA-22AHR (0.35 techno.)
    - ○ simultaneous 2-row encoding & 2 discriminators/column $\Rrightarrow$ twice faster
- **AROM-1 (Accelerated Read-Out Mimosa) $\Rrightarrow$ ASTRAL (2nd step)**
  - ⁜ in-pixel discri. & simultaneous 4-row encoding

    $\Rrightarrow$ 8 times faster than MIMOSA-22THR
  - ⁜ submission of 1st prototype in Q1-Q2/2013
- **SUZE-02 (Downstream part of sensor) :**
  - ⁜ $\varnothing$ μ-circuits & output buffers

    (extension of SUZE-01 with $\leq$ 4 rows simult. encoding)
  - ⁜ encode windows of 4 rows$\times$5 columns
  - ⁜ signal transmission at 320 MHz/cm
  - ⁜ submission in $\geq$ Decembre'12



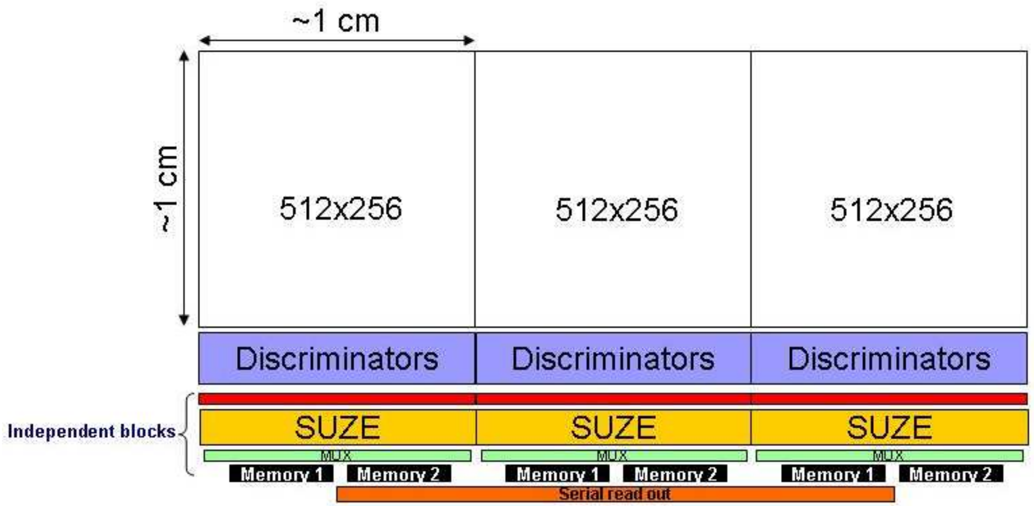


R&D Plans towards Final Sensor

- **FSBB (Full Scale Basic Block) : combining upstream and downstream chain elements**
  - ⋇ Composition:
    - Pixel array with $\sim$ final pixel design ($\sim$ 1 cm^2)
    - Final r.o. circuitry ($\emptyset$, filtering, data transmission, ...)
  - ⋇ Variants:
    - ALICE baseline (MISTRAL): 30 μs, 22$\times$33 μm^2 pixels, subm. Q4/2013
    - ALICE fast sensor (ASTRAL): 15 μs (can be $<$ 4 μs), same pixels, subm. Q4/2015
    - AIDA-BT: ???

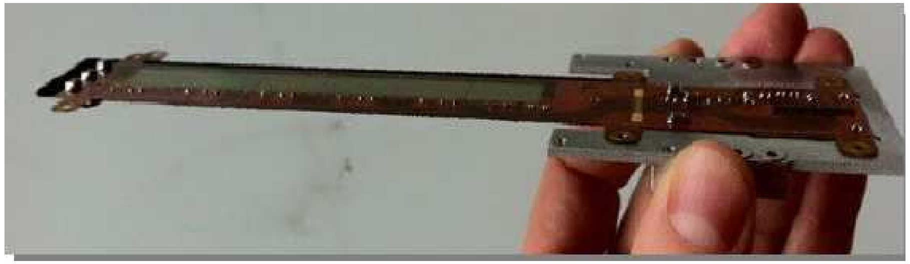
- **Final sensors for ALICE, CBM, AIDA, ...:**
  - ⋇ Composition :
    - 3 adjacent FSBB (1-sided read-out)

      or 2 rows of 3 FSBB (stitching, 2-sided r.o.)
    - Complemented with serial r.o. circuitry
  - ⋇ Submissions:
    - MISTRAL: 30 μs (15μs possible), subm. Q4/2014
    - ASTRAL: 15 μs ($\lesssim$ 2 μs possible) subm. Q4/2016
    - AIDA-BT: subm. 2015 (?)



Ultra-Light Ladder Developments

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**



⋇ *1st PLUME ladder prototype (0.6 % X_0)*

↪ *6 MIMO-26 (50 μm) on each side (8 Mpix, 2 Gb/s)*

⋇ *Preliminary results : no X-talk observed*

↪ *combined impact res. (20 % improvmt) & pointing resolution (2 mrad)*

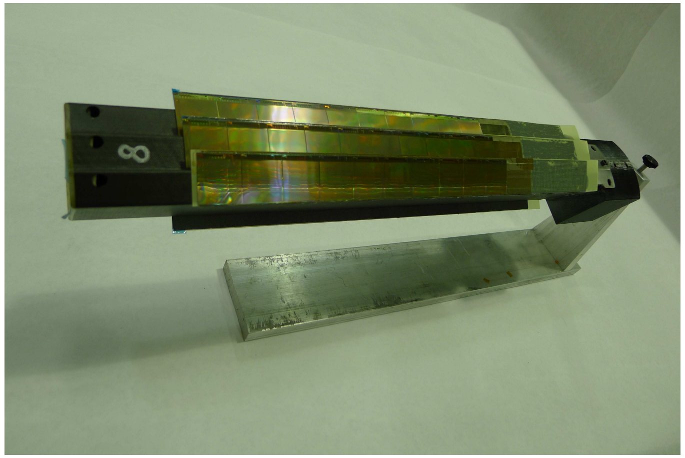
- **New PLUME proto. being fabricated with 0.35% X0** (X-section) ⟼ beam tests in 2013

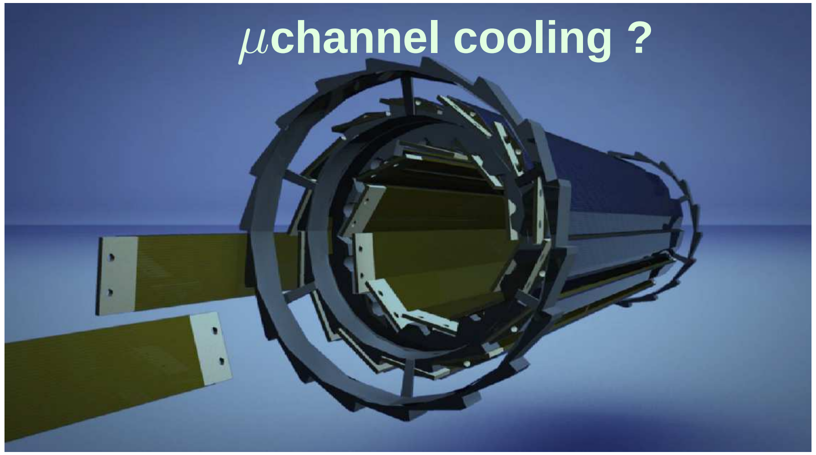
- **Other developments :**

⋇ *SERNWIETE : unsupported ladder with $<$ 0.15 % X_0 ⟼ operational prototype under evaluation*

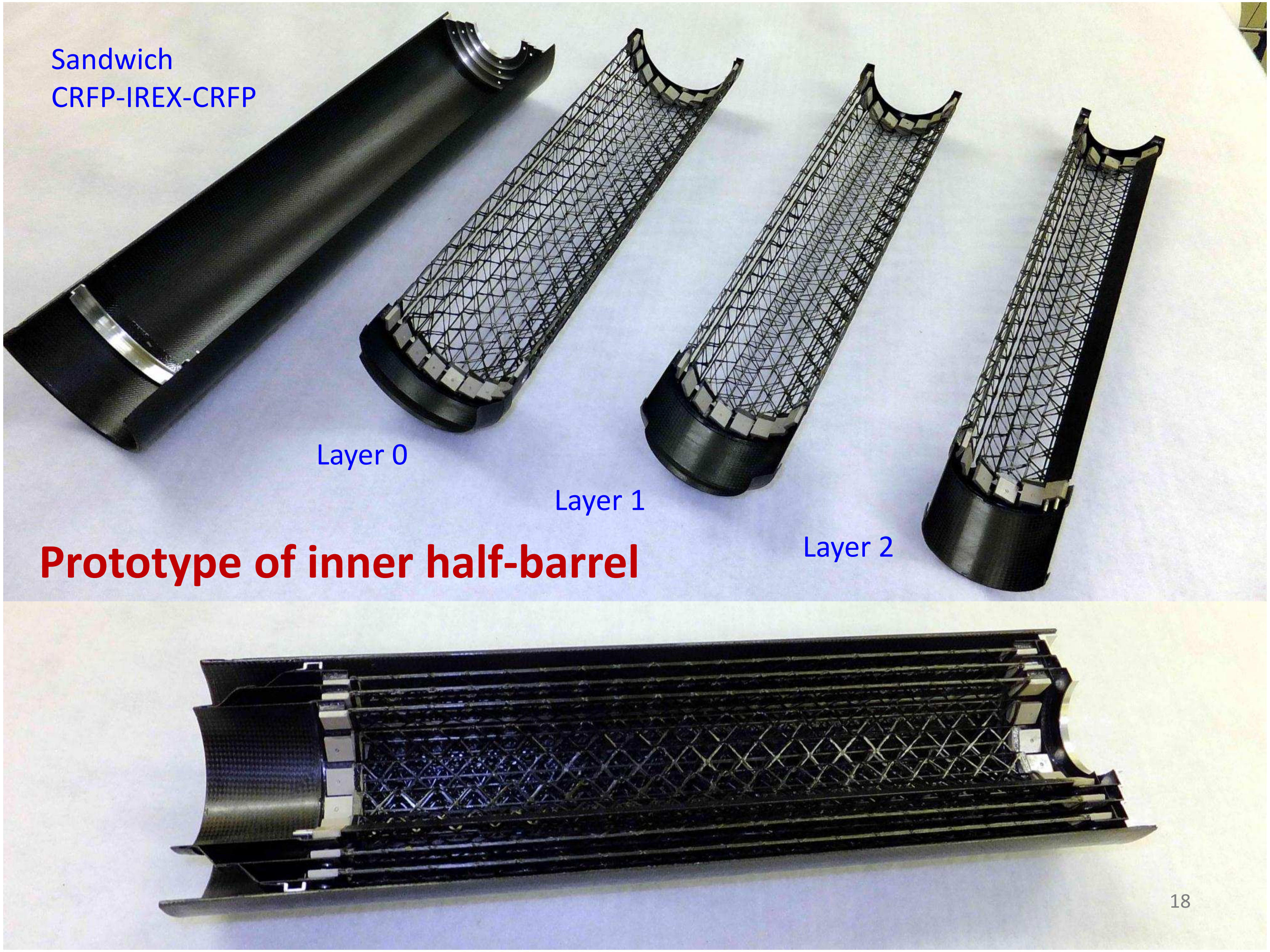
⋇ *STAR-PXL : under construction (0.37% X_0)*

⋇ *ALICE-ITS (0.3% X_0)*





ALICE-ITS Inner Barrel Prototyping



SUMMARY

- **CPS archi. ready to be adapted to all VXD sensor specs at $\sqrt{s}$ = 500 GeV (using 0.35 μm techno.):**
  - ○ innermost layer : $< 3\ \mu m$ and $\lesssim 10\ \mu s$ ○ outer layers : $< 4\ \mu m$ and $\sim 100\ \mu s$
  - ○ VXD power consumption : < 700 W (inst.) / < 15 W (average)
  - ▷ $\sim$ 0.3% X_0 double-sided ladders (PLUME like)
  - ▷ expect physics performance feedback from STAR-PXL (1st data taking in 2013)

- **Extension to 0.18 μm process under way, mainly motivated by 1 TeV running conditions :**

  $\Rrightarrow$ 1st CMOS technology allowing to come close to real CPS potential
  - ○ innermost layer : $< 3\ \mu m$ and $\lesssim 2\ \mu s$ ○ outer layers : $< 4\ \mu m$ and $\lesssim 10\ \mu s$
  - ○ VXD power consumption : < 600 W (inst.) / < 12 W (average)

- **0.18 μm CPS development sustained by ALICE-ITS, CBM-MVD, AIDA-BT :**
  - ○ 2012: validation of charge sensing properties
  - ○ 2013: validation of upstream and downstream sensor elements
  - ○ 2014: validation of complete sensor architecture with "1 cm^2" MISTRAL prototype
  - ○ 2015: pre-production of MISTRAL sensor for ALICE and CBM
  - ○ 2016: validation of complete sensor architecture with "1 cm^2" ASTRAL prototype
  - $\hookrightarrow$ **2017-19: adapt MISTRAL/ASTRAL to ILC vertex detector**

- **Accumulate experience on system integration aspects within STAR & ALICE environments**