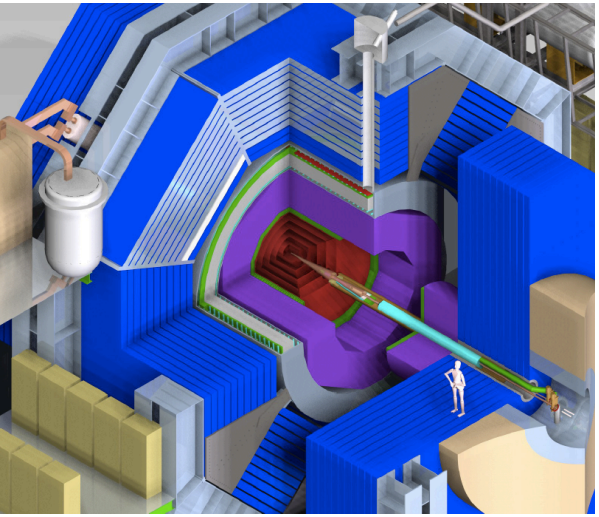
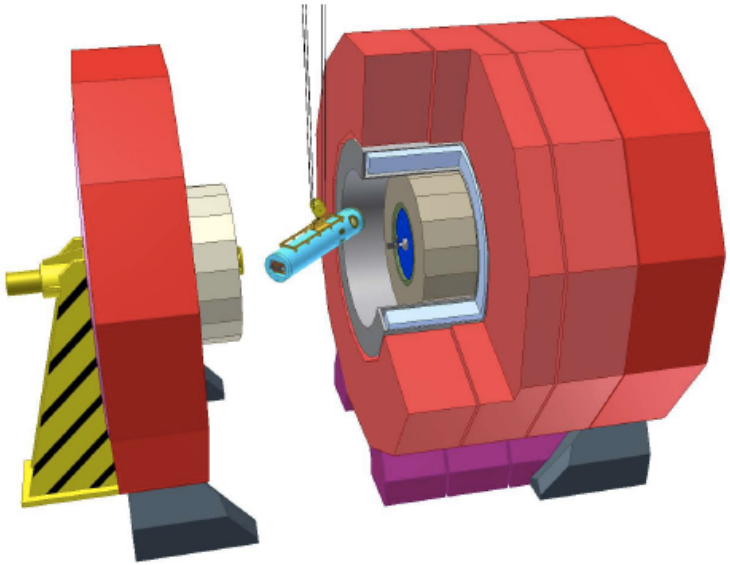
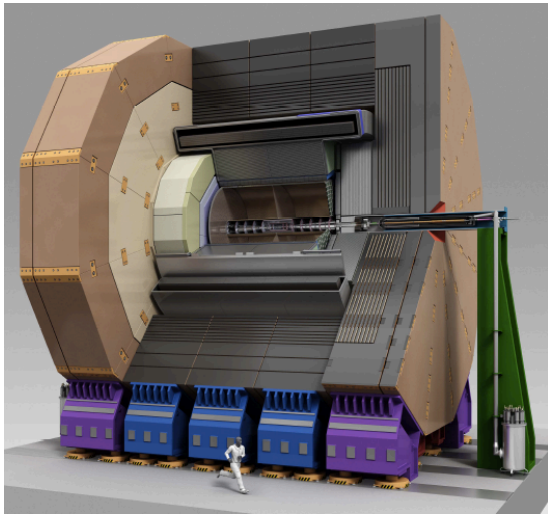
Recent advances in Linear Collider detector R&D

Lucie Linssen, CERN
with input from many LC colleagues

Recent advances in LC detector R&D

CALICE Calorimeter for ILC

LC TPC

FCAL Collaboration High precision design

SiD

clic

ilcILD.org

AIDA

Disclaimer:

Impossible to pay justice to the ongoing detector R&D in 25 minutes !

This talk concentrates on **recent 2011-2012** advances in detector **technology**

Collection of snapshots

Outline

- Linear collider detector requirements
- Vertex detectors
- Tracking
- Calorimetry (electromagnetic)
- Calorimetry (hadronic)
- Forward calorimetry
- Detector engineering
- Coil
- Summary and outlook

Detector performance requirements

High-precision physics calls for:

- Jet energy resolution of $\sigma_E/E \lesssim 3.5\%$ for jet energies from 100 GeV to 1 TeV ($\lesssim 5\%$ at 50 GeV);
- Track momentum resolution of $\sigma_{p_T}/p_T^2 \lesssim 2 \cdot 10^{-5}$ GeV^{-1};
- Impact parameter resolution with $a \lesssim 5$ μm and $b \lesssim 15$ μm GeV, where the resolution is expressed as:

$$\sigma_{d_0}^2 = a^2 + \frac{b^2}{p^2 \sin^3 \theta},$$

- Lepton identification efficiency better than 95% over the full range of energies;
- Detector coverage for electrons down to very low angles.

Additional requirement, due to experimental conditions:

- Manageable occupancies in the presence of beam-induced background
- Radiation hardness for forward calorimetry

Moreover, timing capabilities required for CLIC:

- All tracking detectors with ~10 ns time-stamping capability
- Time precision on calorimeter hits of ~ 1ns

Challenges in LC detector R&D

These requirements lead to the following challenges:

Vertex and tracker

- Very high granularity
- Dense integration of functionalities
- Super-light materials
- Low-power design + power pulsing
- Air cooling

ultra – light

Calorimetry

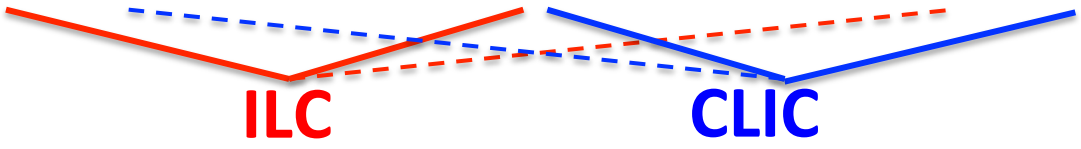
- Fine segmentation in R, phi, Z
- Ultra – compact active layers
- Pushing integration to limits
- Power pulsing

ultra – heavy and compact

Vertex detectors

Categories of candidate technologies

	Monolytic CMOS	(3D) integrated	Hybrid pixel
Examples	DEPFET, FPCCD, MAPS, HV-CMOS	SOI MIT-LL, Tezzaron, Ziptronix	CLICpix (TimePix3, Smallpix)
Technology	Specialised HEP processes, r/o and sensors integrated	Customized niche industry Processes with focus on Interconnectivity	Industry standard ASIC processes; HEP-specific high-resistivity sensors
Depletion layer	Partial	Partial or full	Full => large fast signals
Granularity	Down to 5 µm pixel size	Down to 5 µm pixel size	25 µm pixel size
Thickness	~50 µm total thickness achievable	~50 µm total thickness achievable	~50 µm sensor + ~50 µm r/o



Vertex detectors

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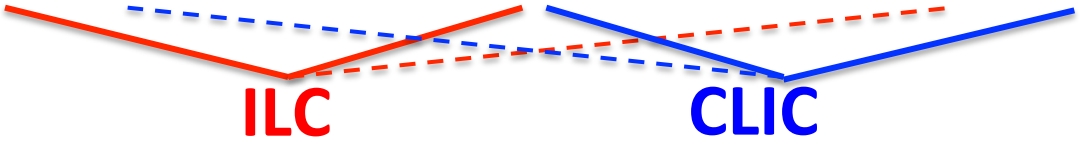
Technology	Specialised HEP processes, r/o and	Customized niche industry	Industry standard ASIC processes;

Smaller pixels

Thinner detectors

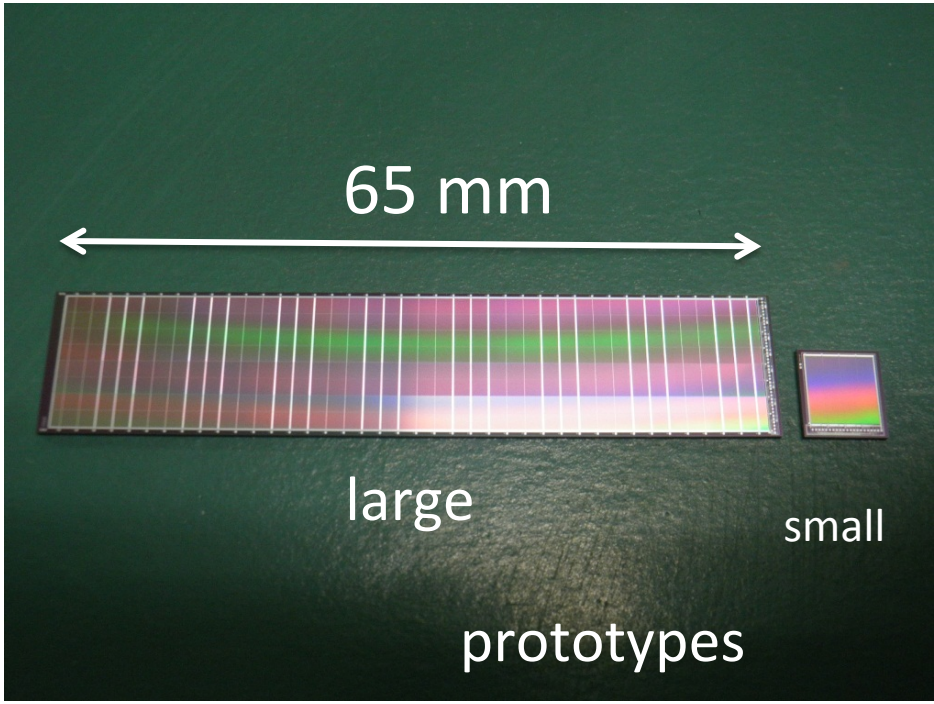
High level of pixel functionality

Fast time-stamping



Vertex detector: FPCCD (ILC)

- Design of **FPCCD** vertex detector
  - **~5 µm pixel for inner 2 layers** → sub - µm point resolution expected
  - **~10 µm pixel for outer 4 layers**
  - Acceptable pixel occupancy even with signal accumulation over 1 bunch-train
  - Relatively slow readout speed of ~10M pixels/s

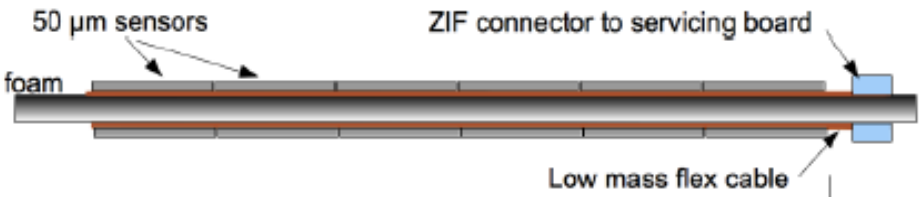


- **Recent highlight of sensor R&D**
  - **Small** (6 mm × 6 mm) **prototype**
    - 4ch (output nodes)/chip
    - All 6 µm pixels
    - It works!
  - **Large** (65 mm × 13.4 mm) **prototype**
    - Almost real size prototype for inner layers
    - 8ch/chip
    - 12 µm (2ch), 8 µm (2ch), and 6 µm (4ch) pixels
    - To be tested

Vertex det.: monolithic CMOS (ILC)

Monolithic sensor, CMOS process with high-resistivity epitaxial layer

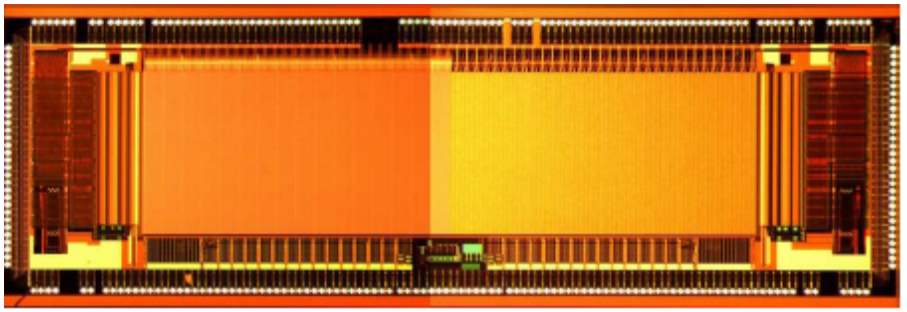
- Electronics integrated in pixel
- Correlated-Double Sampling (CDS) in pixel
- Rolling shutter read-out (coarse timing)
- Analog or digital readout possible



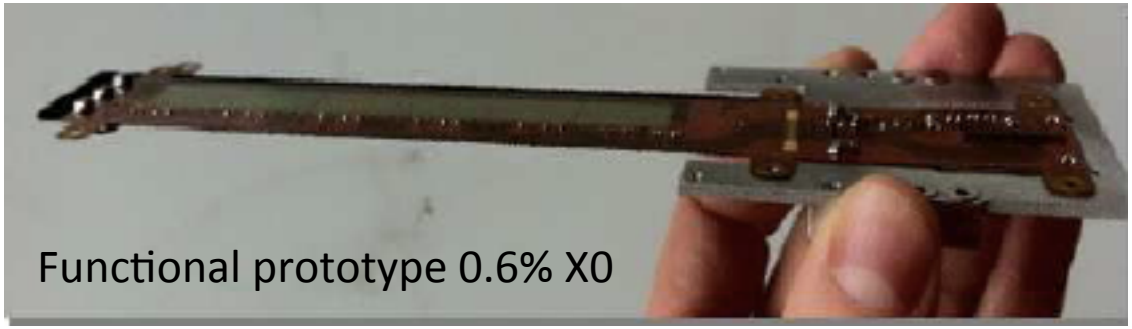
2 types of sensors for inner and outer layers

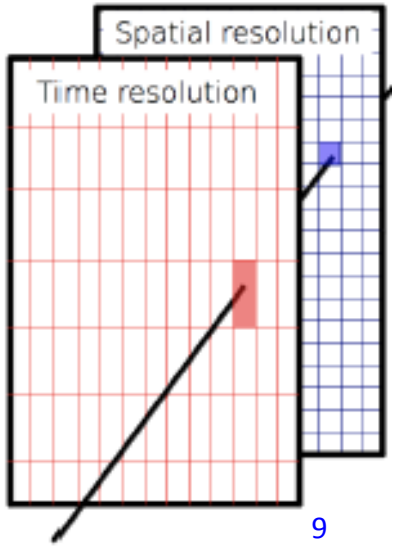
MIMOSA-30 : Dual sided readout out

- 1 side for spatial resolution (16x16 µm pixel),
- 1 side for timing (~10µs, 16x64 µm pixel)



MIMOSA-31 : Larger pixel for reduced power consumption (35x35 µm)





Further R&D: increased epitaxial layer, 180 nm CMOS, thinner assemblies

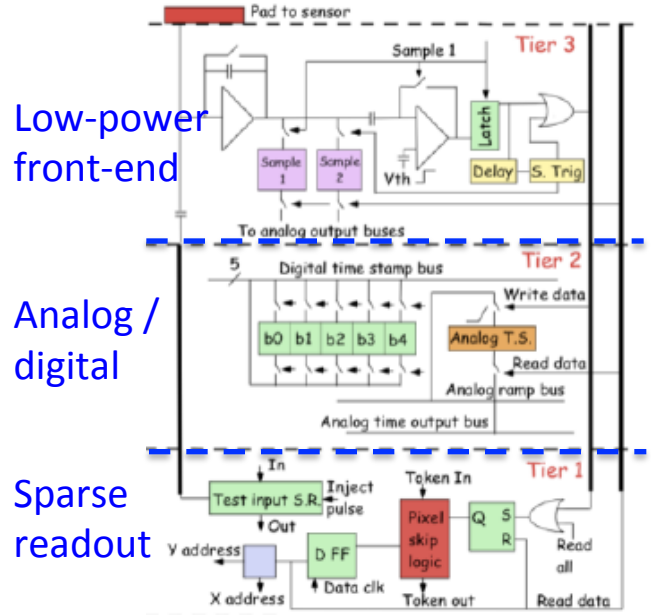
Vertex: VIP-3D / Chronopixel

3D - interconnect and active edge sensor development

Synergy with other projects (LHC upgrades)

3D multi-tier wafer assembly
For high-density functionality
Allows for optimal combination of processes: ASIC+sensor

Successful full VIP2b-3D 0.13 nm CMOS run at Tezzaron
Earlier 2D tests => good functionality
3D testing is underway

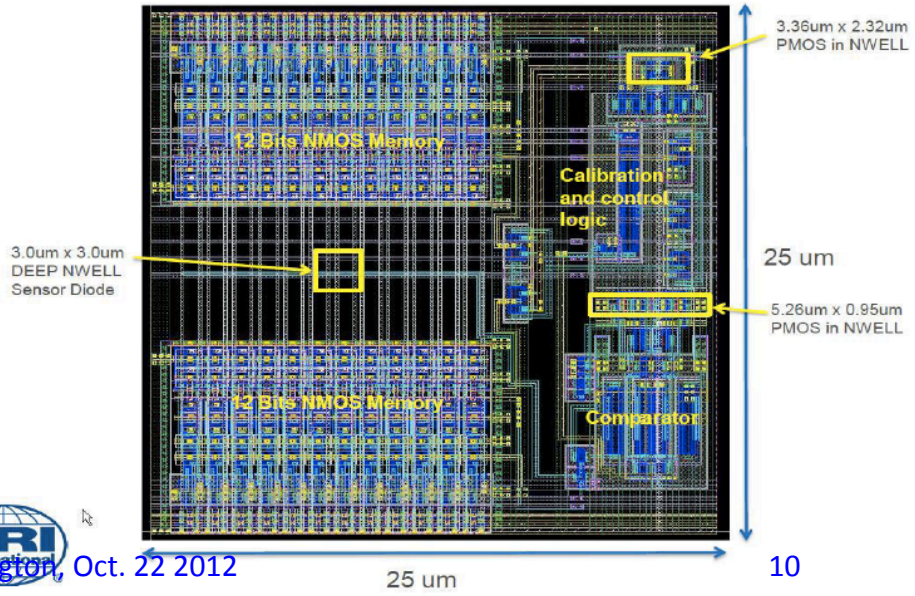


Chronopixel R&D

Monolithic-CMOS, with time-slicing ~10 µs
Ultimate design will require 45 nm technology
2nd prototype:

- Recently fabricated in 90 nm technology
- Pixel size 25*25 µm^2
- Implementing lessons from 1st prototype

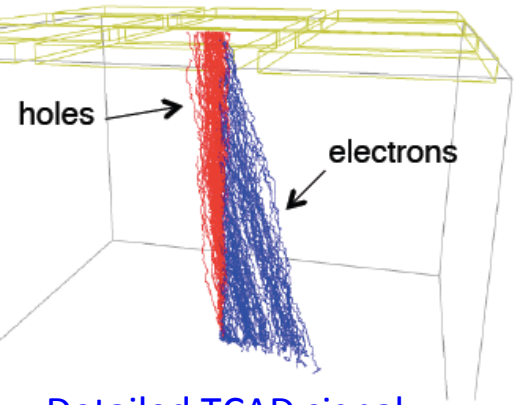
Received from foundry, June 2102.
Looking forward to results of ongoing tests



Vertex detectors: CLIC pixel R&D

Hybrid approach:

- Thin (~50 µm) sensors (e.g. Micron, CNM, VTT)
- Thinned High density ASIC in very-deep-sub-micron:
  - TimePix3, Smallpix <= R&D steps
  - CLICpix
- Low-mass interconnect
  - Micro-bump-bonding
  - Through-Silicon-Vias (R&D with CEA-Leti)
  - Chip-stitching
- Power pulsing and air cooling foreseen



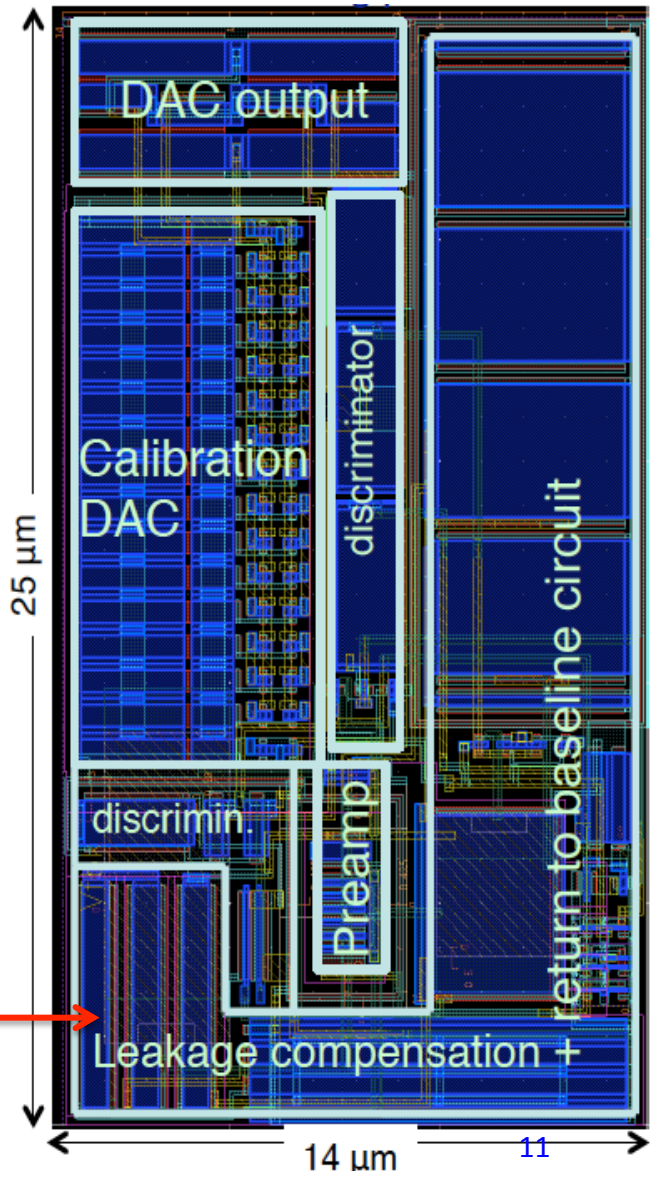
Detailed TCAD signal formation simulation

CLICpix

- 65 nm technology
- 25×25 µm^2 pixels
- 4-bit TOA and TOT information
  - 10 nsec time-slicing
- Power 2 W/cm^2 (continuous)
- With sequential power pulsing
  - 50 mW/cm^2

64×64 pixel demonstrator
Submission November 2012

Analog part of a CLICpix pixel



Vertex detector: Power pulsing

Vertex power pulsing design + first lab tests:

- With vertex analog powering in mind: ~2 A at 1.2 V for ~15 µs
- **Low-mass !**

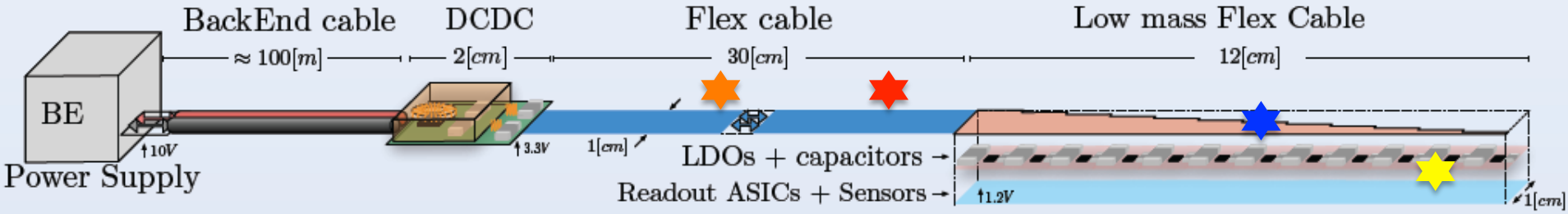
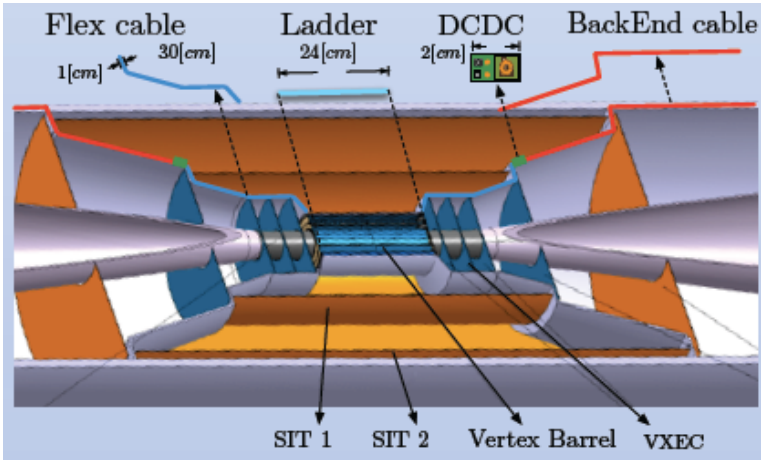


Figure: Half ladder proposed powering scheme

Emulation of: DC-DC converter + flex cable + (LDO/capacitors) + Pixel module

Equivalent 0.145% X0/layer in vertex region

20 mV Voltage ripple achieved



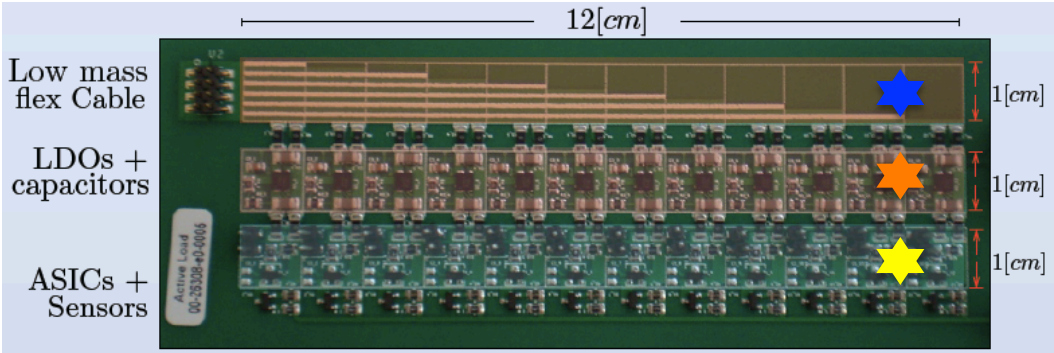
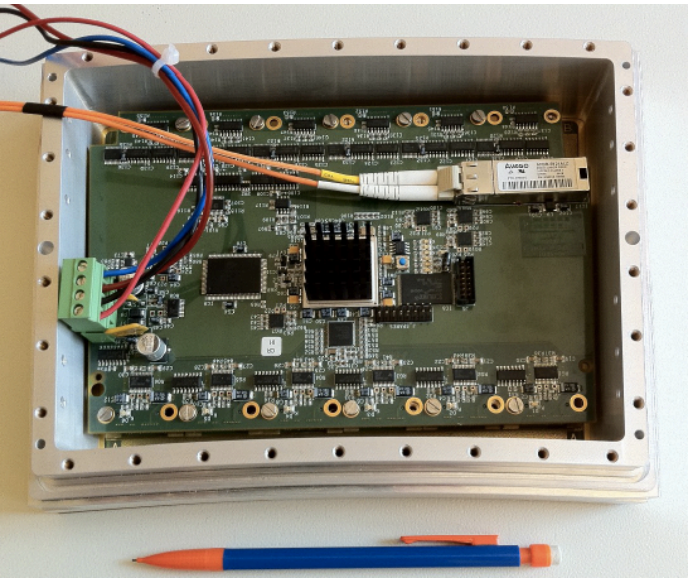
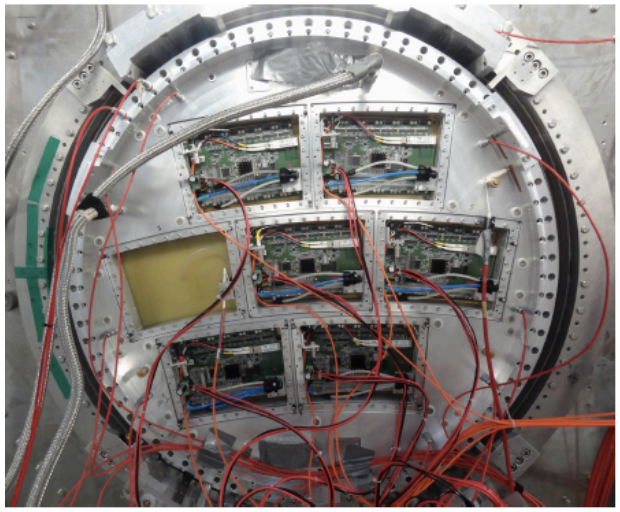


Figure: PCB that emulates the readout ASICs power consumption. It integrates the low mass flex cable, the array of LDOs and capacitors, and their interconnections.

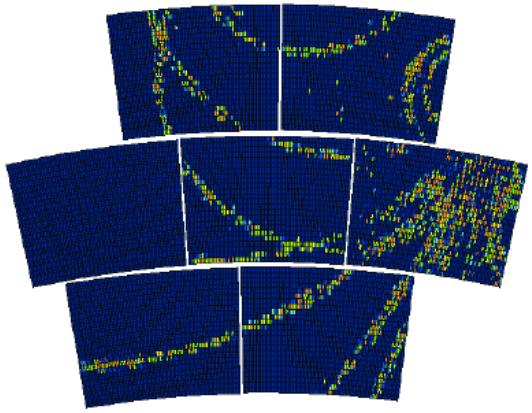
Figure: 30 cm long Flex cable

Tracking => TPC pad readout

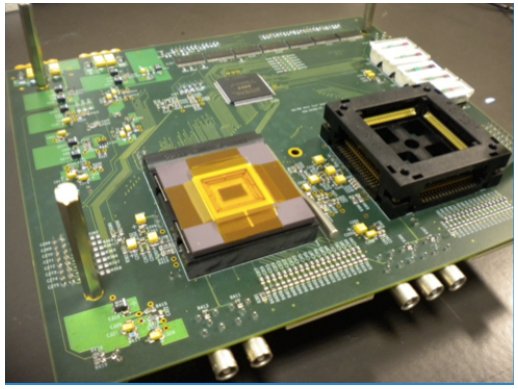




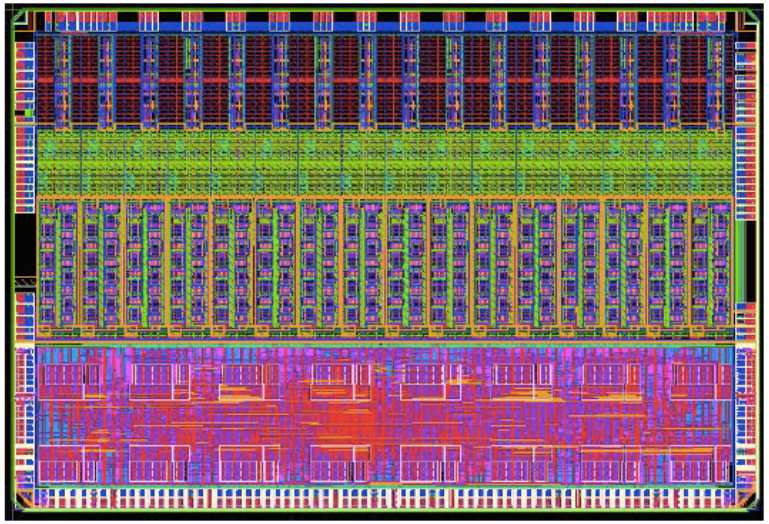
Cosmic muon shower



Six **highly integrated Micromegas** modules with resistive anode



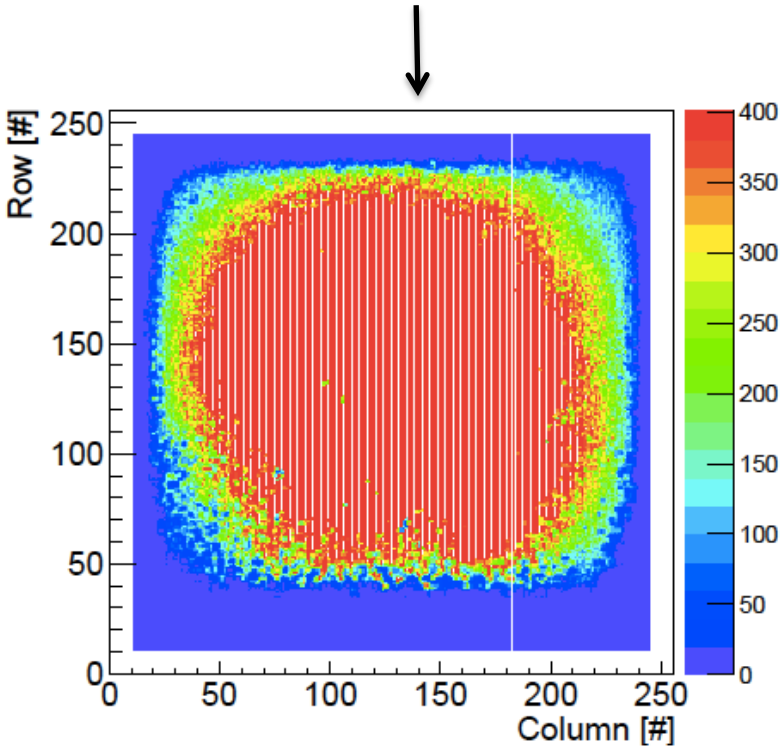
S-Altro16 (130 nm)
Highly integrated analog
+digital TPC readout chip
=> Fully tested and available



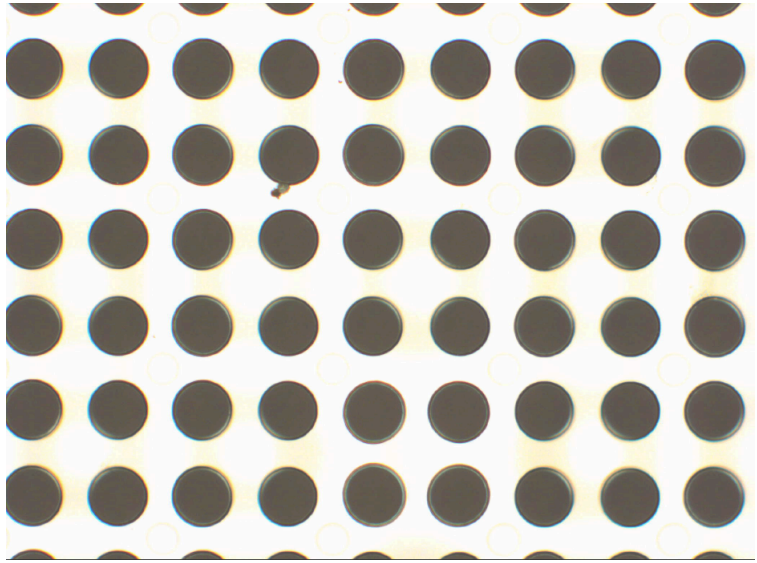
Power pulsing at 50 Hz => factor 18 gain in power

TPC => pixel readout

- **New Ingrid production** of one wafer (at IZM)
- Major improvement in the protection layer (Si-Nitride)
- All tested Ingrids have survived more than 5 weeks
  - even with high gain (i.e. more frequent sparking)
- Good signal uniformity, only very few closed holes



Source illumination near centre of the chip

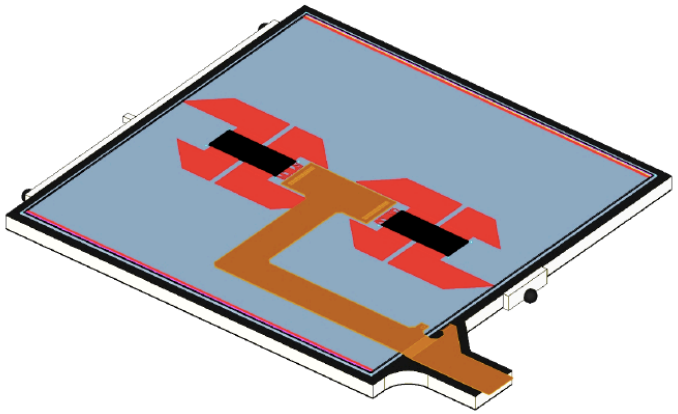


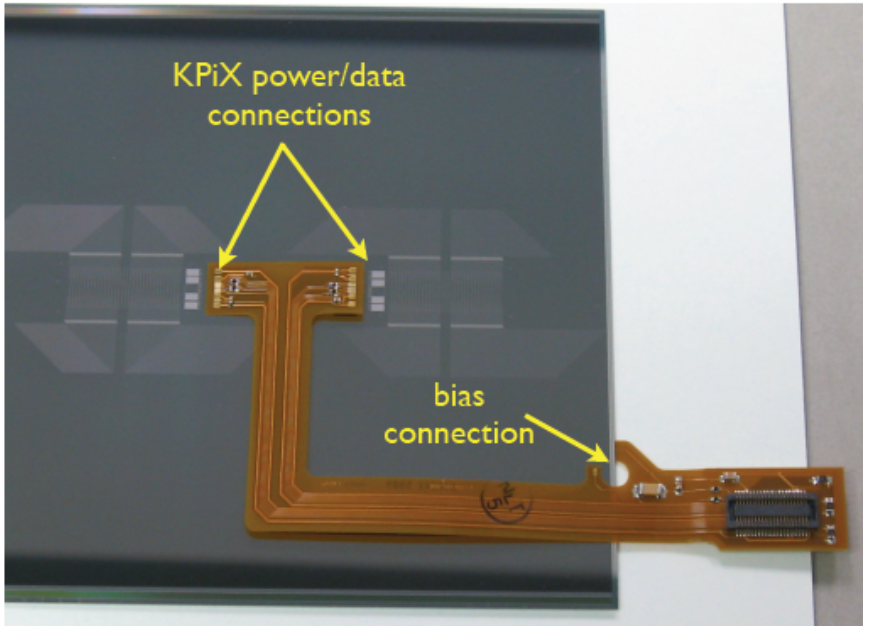
55 µm

Several other TPC R&D not covered here:
Double / triple GEM studies, Octopus etc

Tracking => “chip on sensor”

SiD tracker module





- 1024-channel KPIX chip is produced and tested
- Sensor with double metal-layer routing is available
- Kapton pig-tail available (bonding compatibility ….)

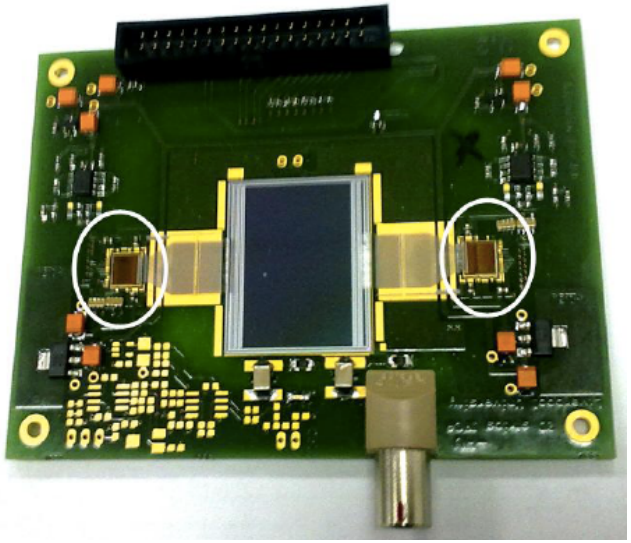
Pending possibilities to fully bond chip-on-sensor:
tests are ongoing, combining KPIX chip and new pigtail connection.

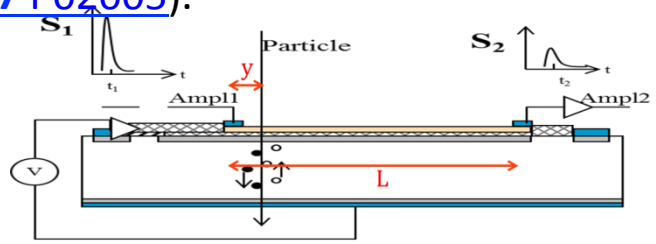
Tracking (strips)

Charge division for 2nd coordinate in microstrip silicon sensors

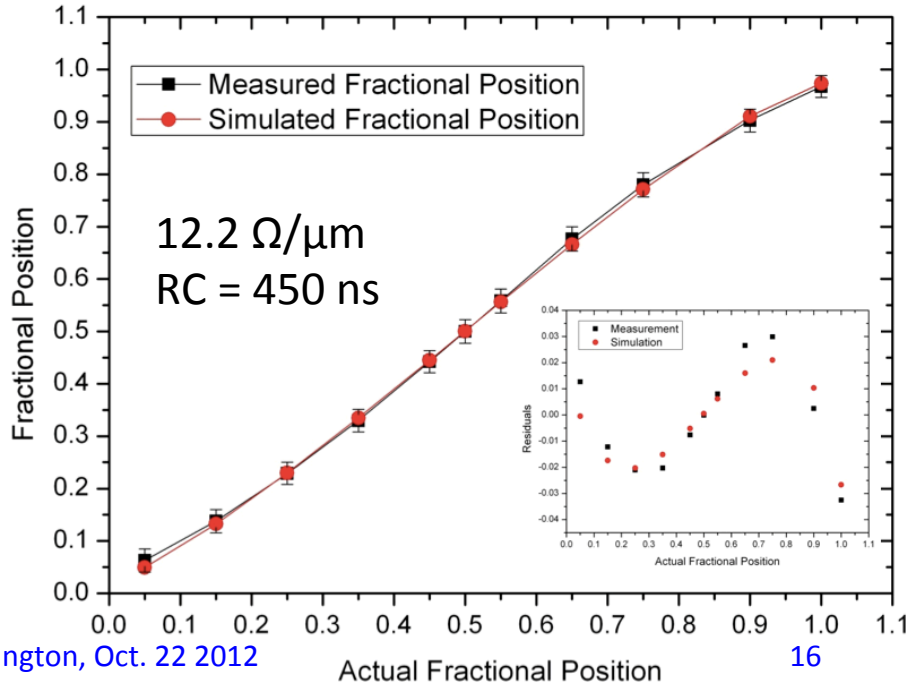
- Aim: determine the coordinate along the strip. Implemented with slightly resistive electrodes (doped polysilicon) => interesting for low-occupancy tracker regions
- **Position accuracy of a few percent of the microstrip length achieved**
- on the first prototypes (POLYSTRIPS sensors, 2012 *JINST* **7** P02005).

Strip: length 20 mm
width 20 µm
Pitches: implant 80 µm
readout 80 µm
Electrode: 12.2 Ω/µm (2.8 Ω/µm)

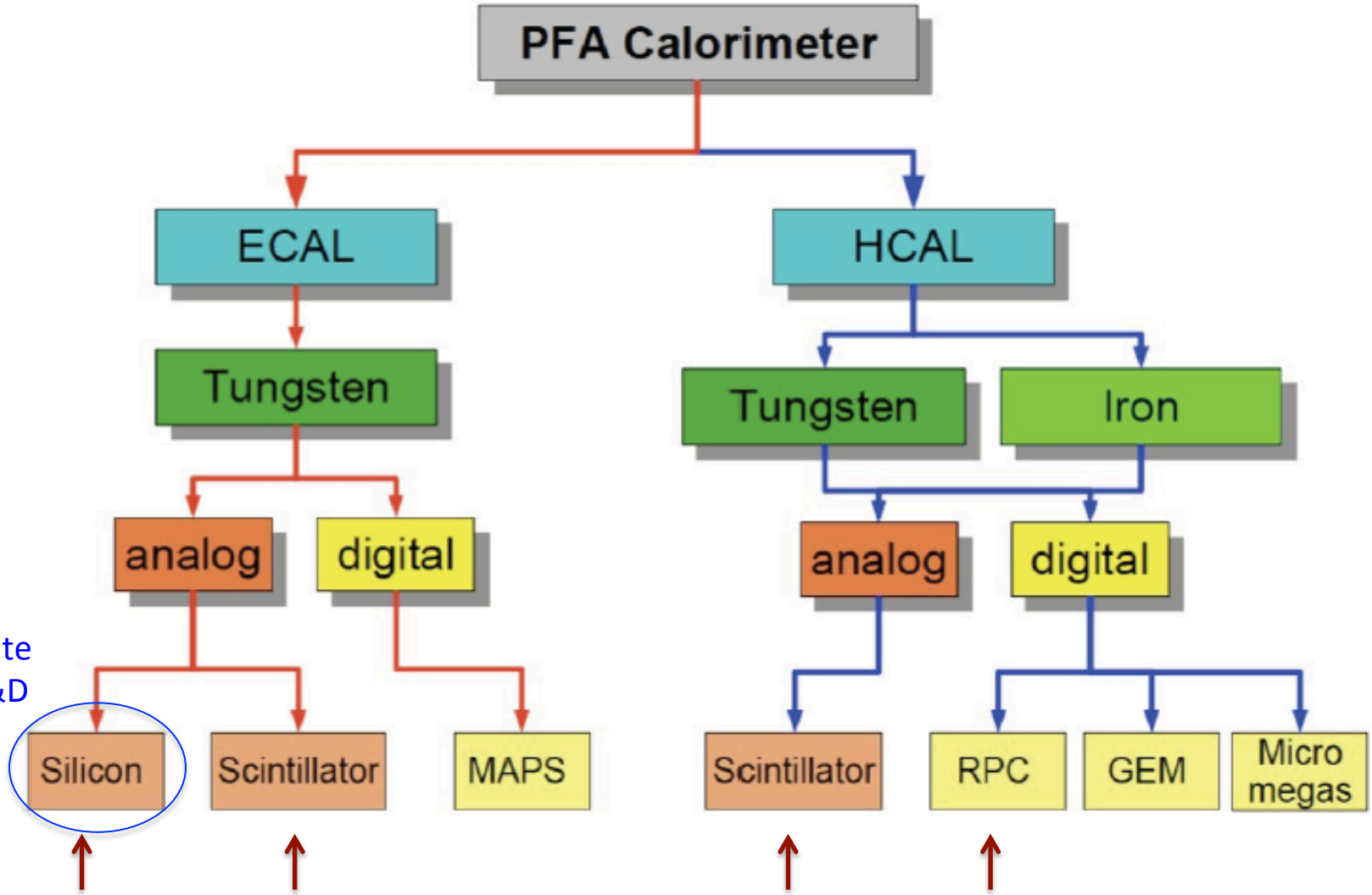




Fractional Position ≡ y/L = S2/(S1 + S2)



Calorimetry (CALICE)



also separate SiD R&D

With major technological prototypes in beam tests in 2011-2012

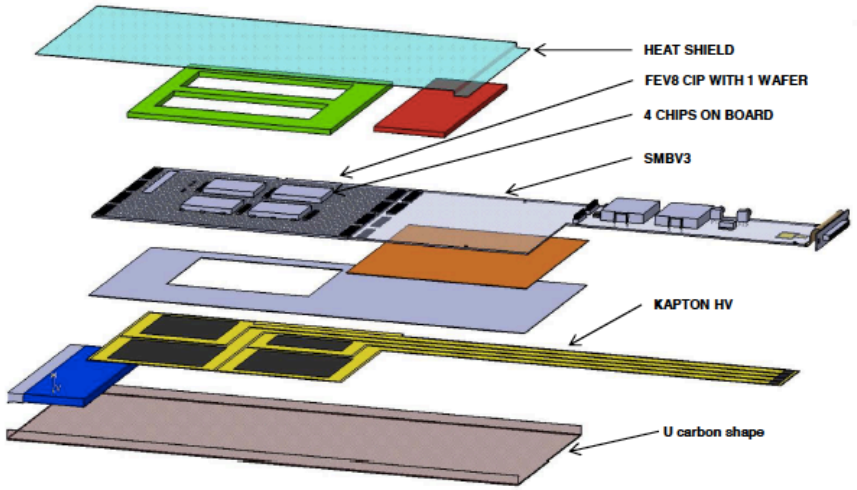
ECAL: Si-W (CALICE)

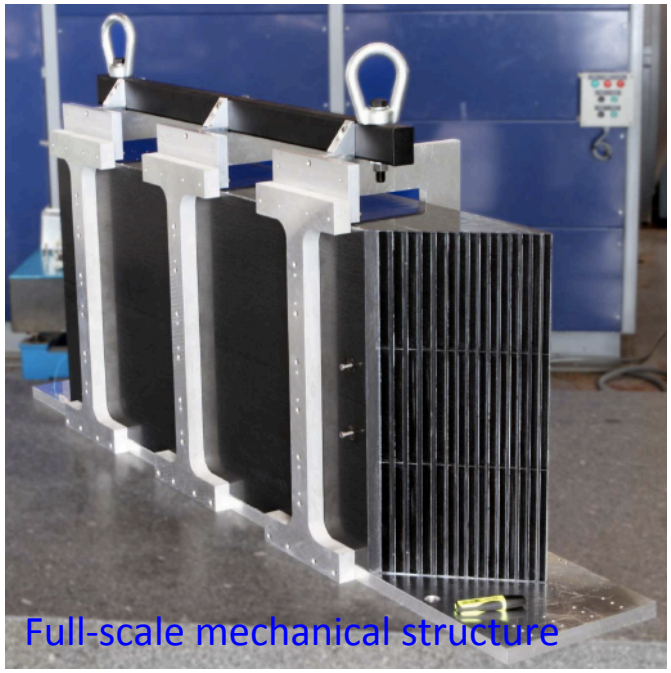
Technological Si-ECAL prototype

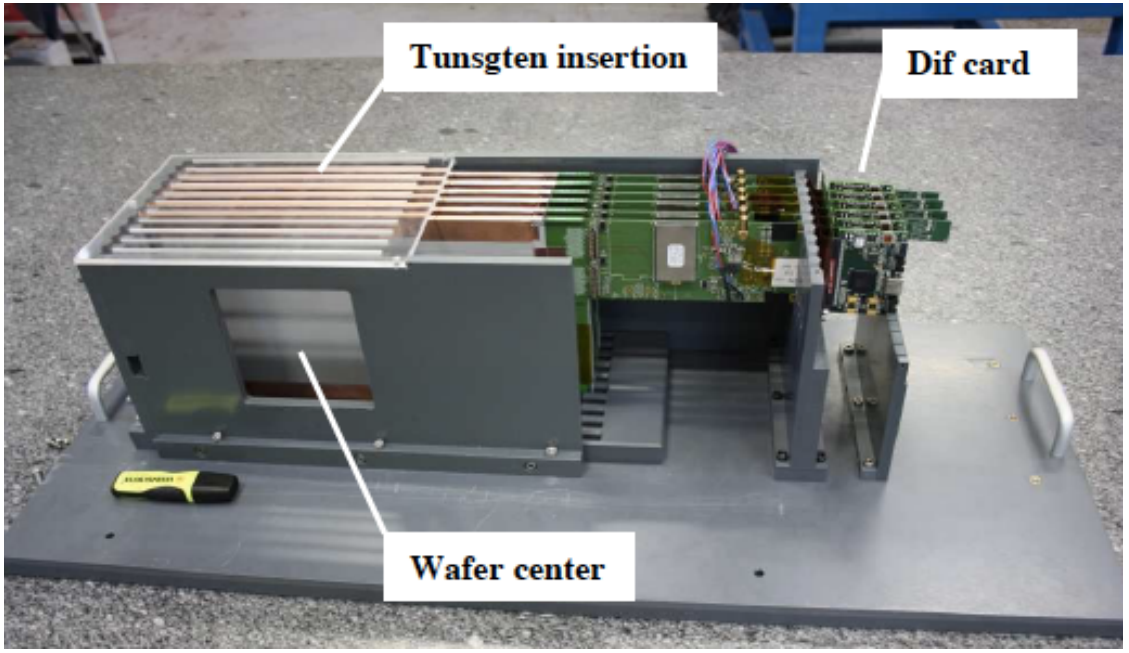
Real-scale detector integration model

Large Si sensors with small 5×5 mm^2 PADs
SKIROC ASIC "in" thin PCB

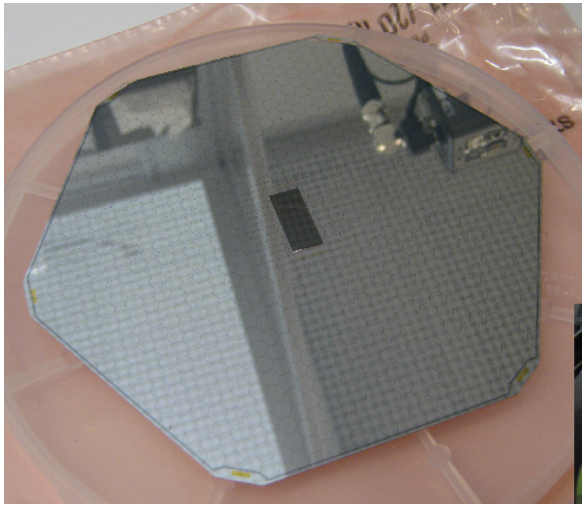
System with 1200 cells in DESY test beam in 2012

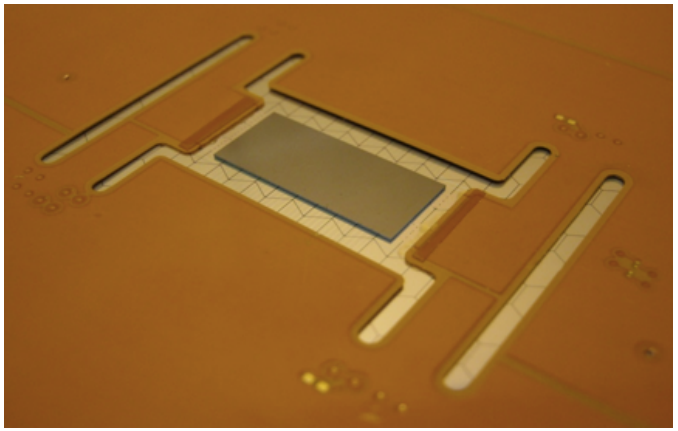


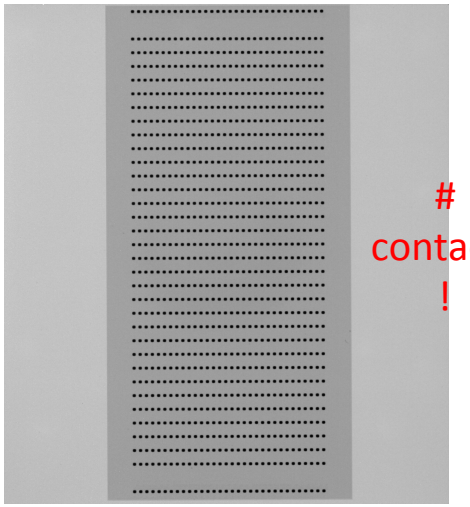

Full-scale mechanical structure



ECAL: Si-W (SiD)

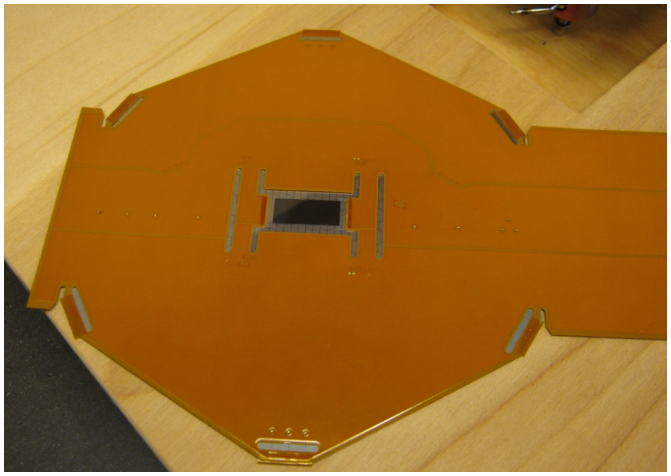


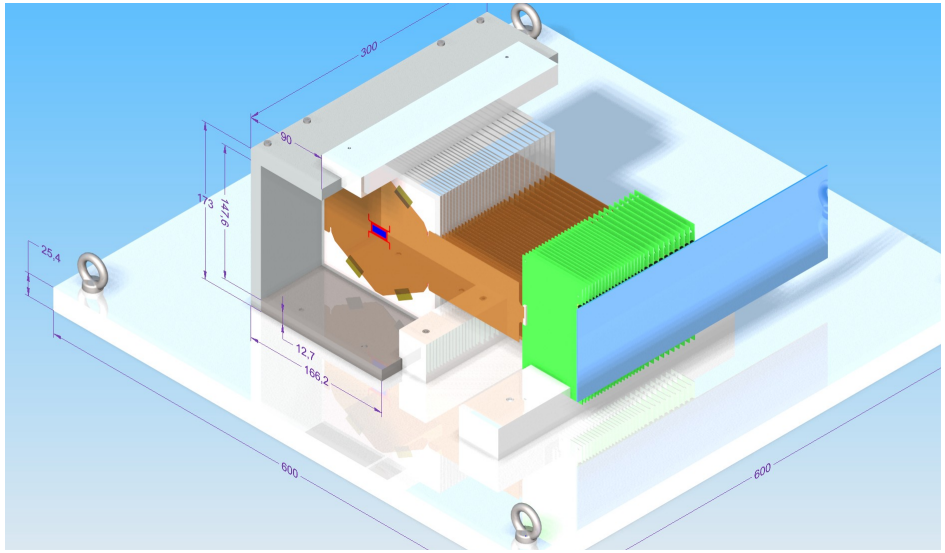




\# contacts !

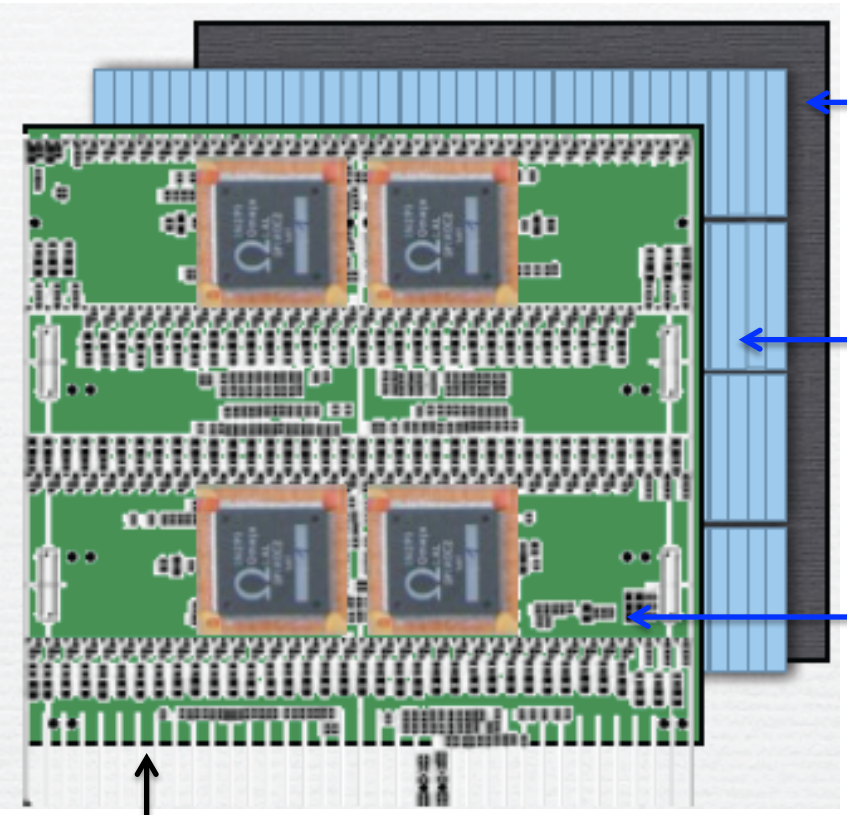
Successful **bonding** of 1024-channel KPIX chip and flex cable to SiD Silicon ECAL sensor





Test beam stack in preparation

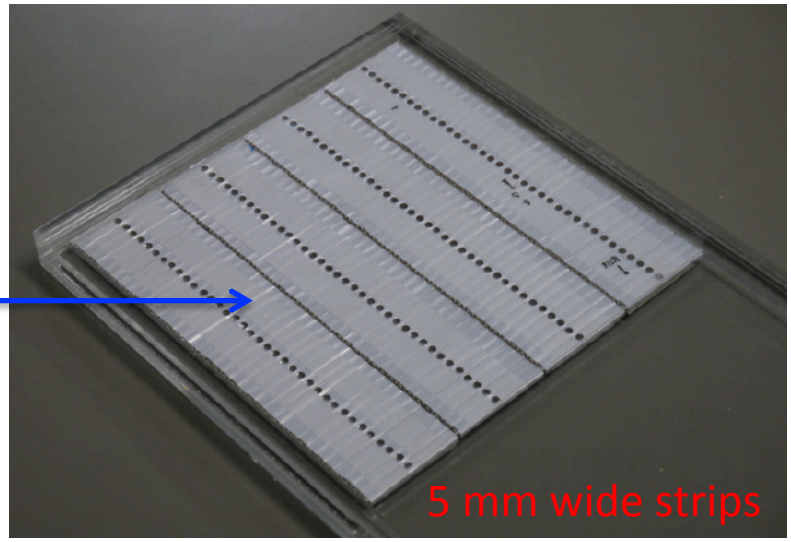
ECAL: Scint-ECAL (CALICE)



absorber

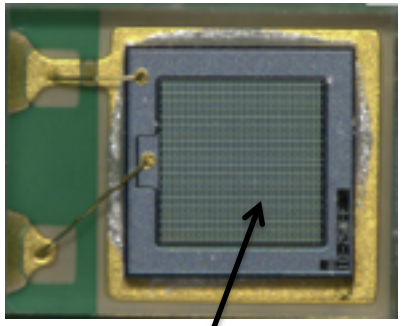
scintillator strips x,y

integrated electronics (SKIROC)



Strips of 45*5*2 mm^3, 144 channels/ plane

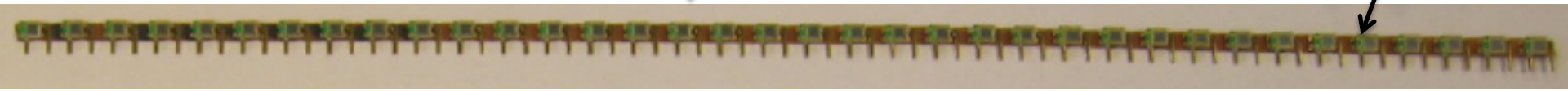
MPPC
1600 pixels
1×1 mm^2



Currently in DESY test beam, October 2012

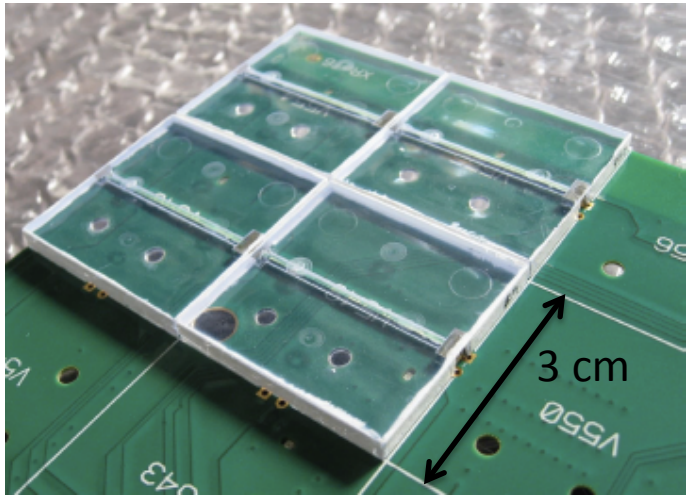
1 cm

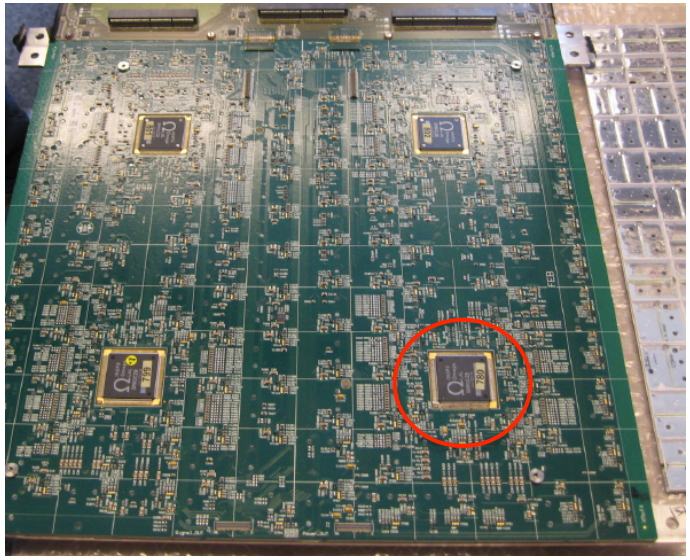
Row of MPPC (SiPM)

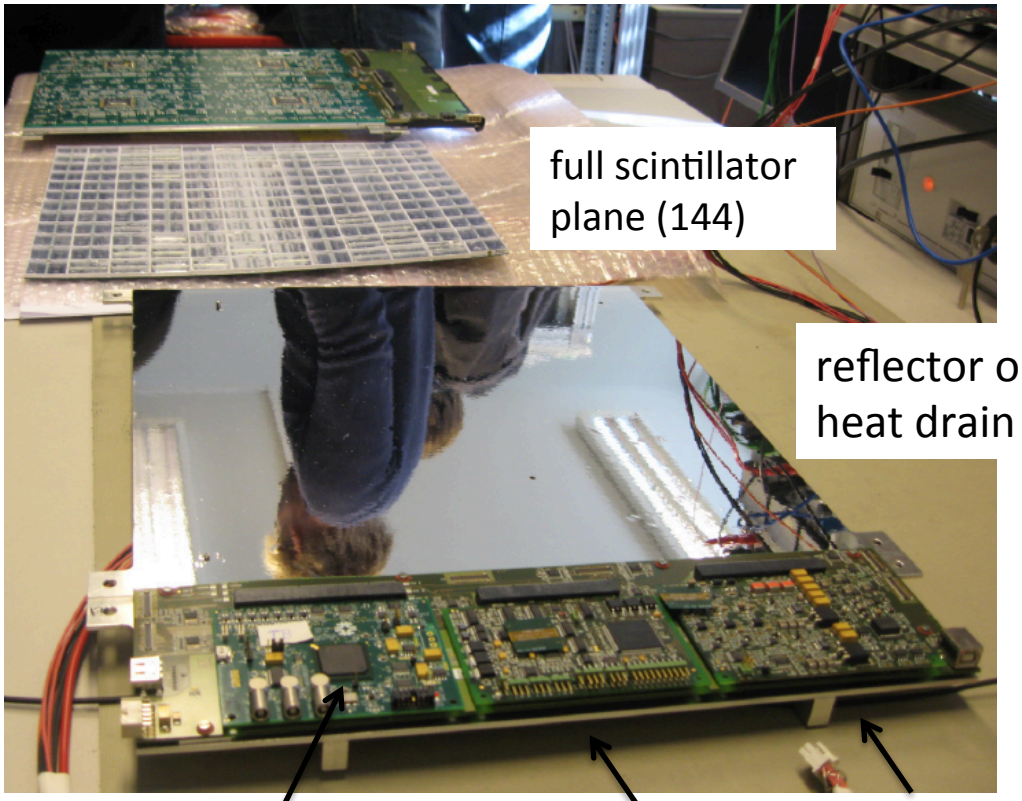


A-HCAL (CALICE)

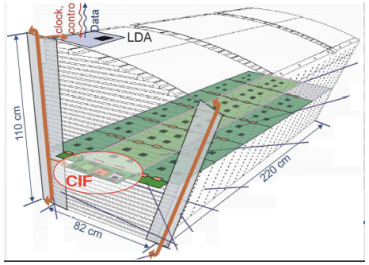
AHCAL 2nd generation fully integrated prototype planes, now in DESY test beam





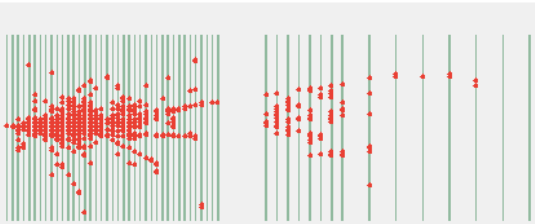


integrated electronics, based on SPIROC2b with self-triggering, timing, power pulsing

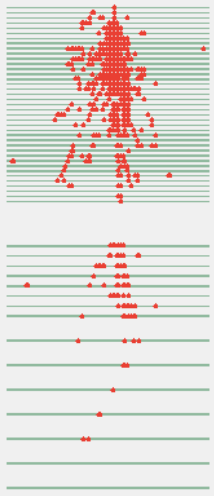


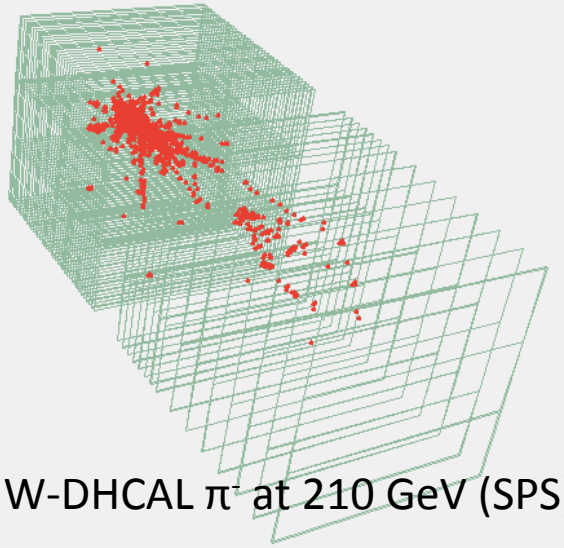
HCAL: DHCAL (CALICE)

Steel DHCAL
Tungsten DHCAL
500'000 readout channels



54 glass RPC chambers, 1m^2 each
PAD size 1×1 cm^2
Digital readout (1 threshold)
100 ns time-slicing
Fully integrated electronics
Main DHCAL stack (39) + tail catcher (15)
Total 500'000 readout channels





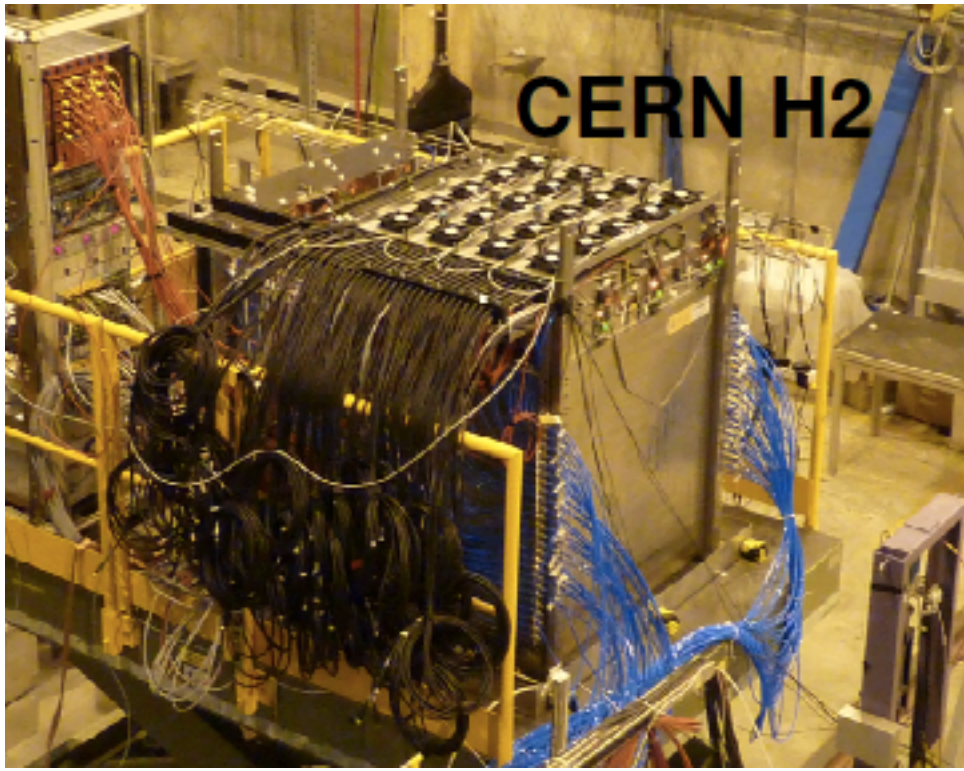
W-DHCAL π^- at 210 GeV (SPS)

Successfully tested:
2010+2011 **Fermilab**
Steel absorber
2012 **CERN** PS + SPS
Tungsten absorber

CERN test setup includes **fast readout RPC** after (**T3B**)

HCAL: SDHCAL (CALICE)

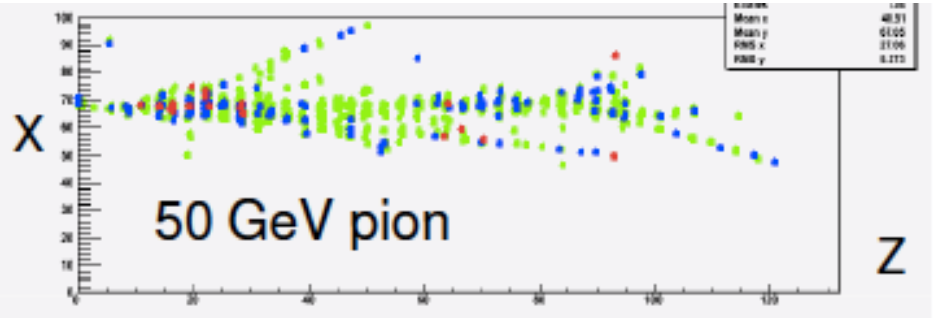
Steel SDHCAL
500'000 readout channels

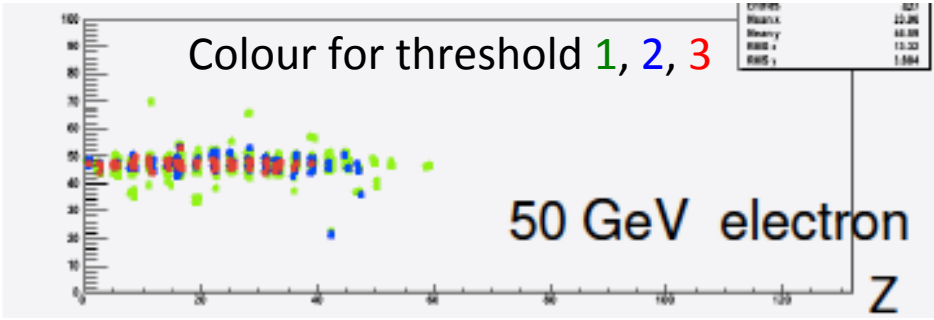


~50 glass RPC chambers, 1m^2 each
PAD size 1×1 cm^2
Semi-digital readout (3 thresholds)
200 ns time-slicing
Fully integrated electronics

With power-pulsing !
Separate power-pulsing tests in 3T magnet
=> Stable signal response

Full SDHCAL stack **successfully tested**:
2012 (2011) CERN - ongoing
Steel absorber



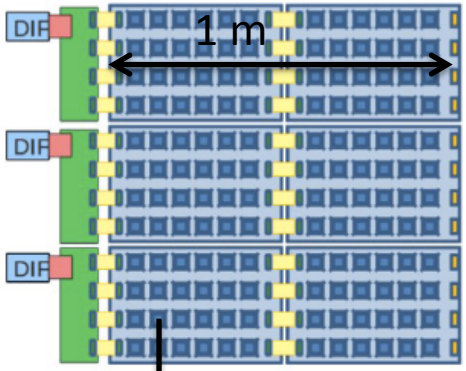


Calorimetry: Micromegas / GEM

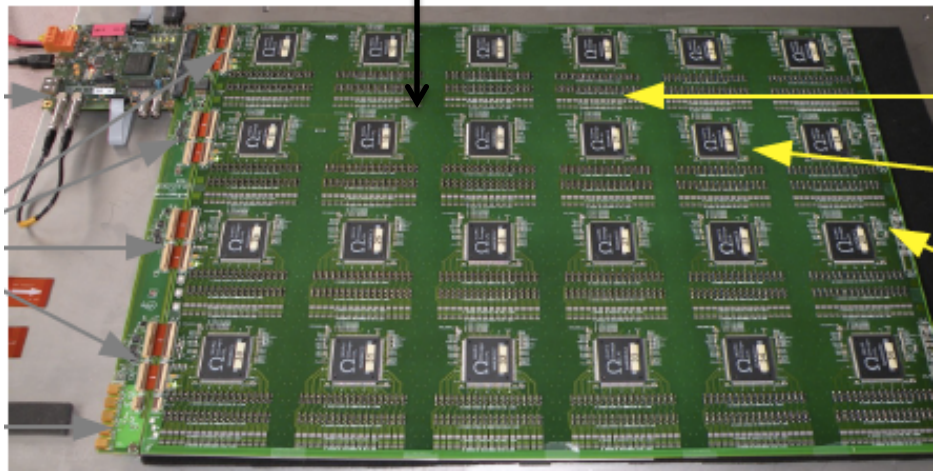
Micromegas

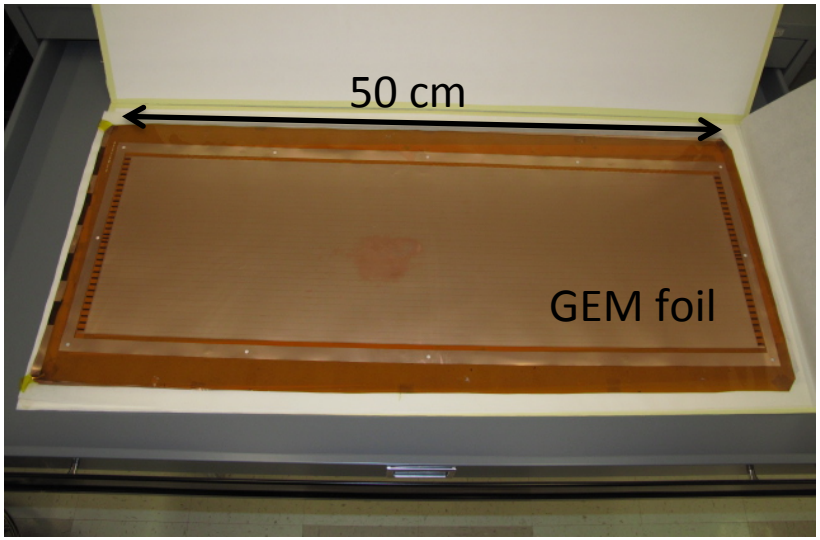
Two 1 m^2 chambers, multi-threshold readout

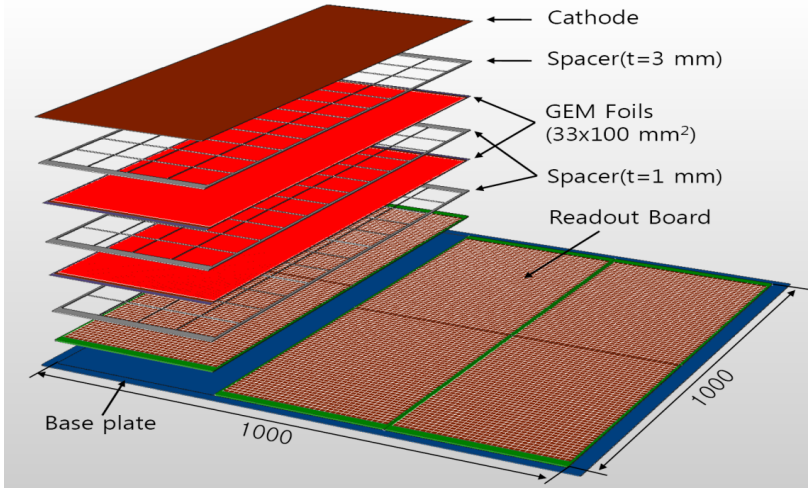
Successfully tested within SDHCAL stack, 2012



32x48 pads of 1 cm^2 on back side

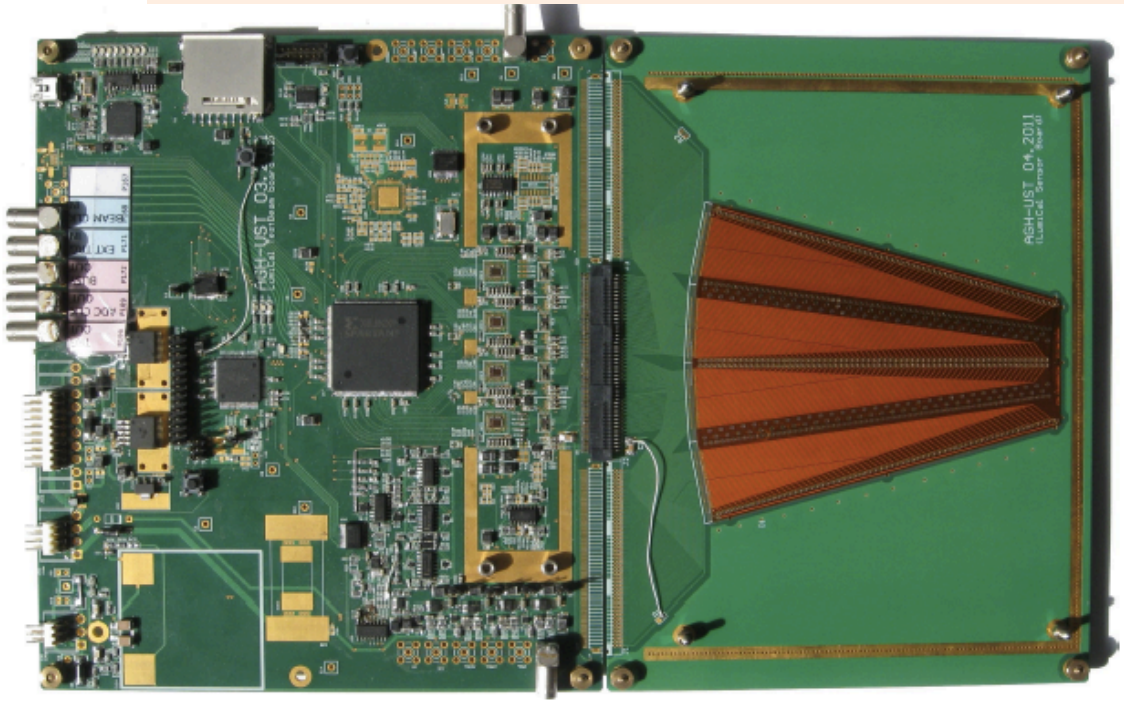






After successful tests with 30×30 cm **GEM chambers**, development towards of 1m^2 plane has started.

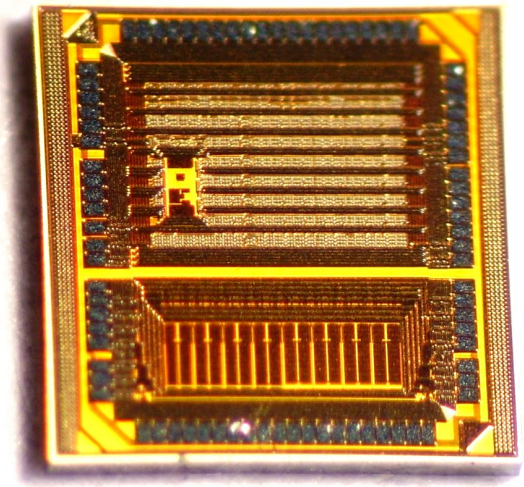
Forward calorimetry



Fully instrumented sensor planes

- Silicon (and GaAs) planes
- Dedicated FE and ADC ASICs (4-metal 350 nm CMOS techn.)
- Stable operation in beam
- S/N = 20 for MIP
- Good signal uniformity

Also: successful radiation tests of large-scale GaAs sensors

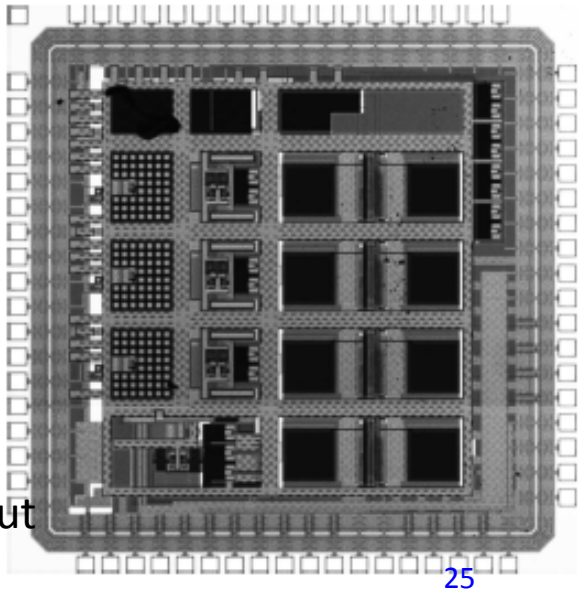


New ADC ASIC prototype 130 nm

- 8-channel, 10 bit SAR
- Fully differential
- 40 MHz

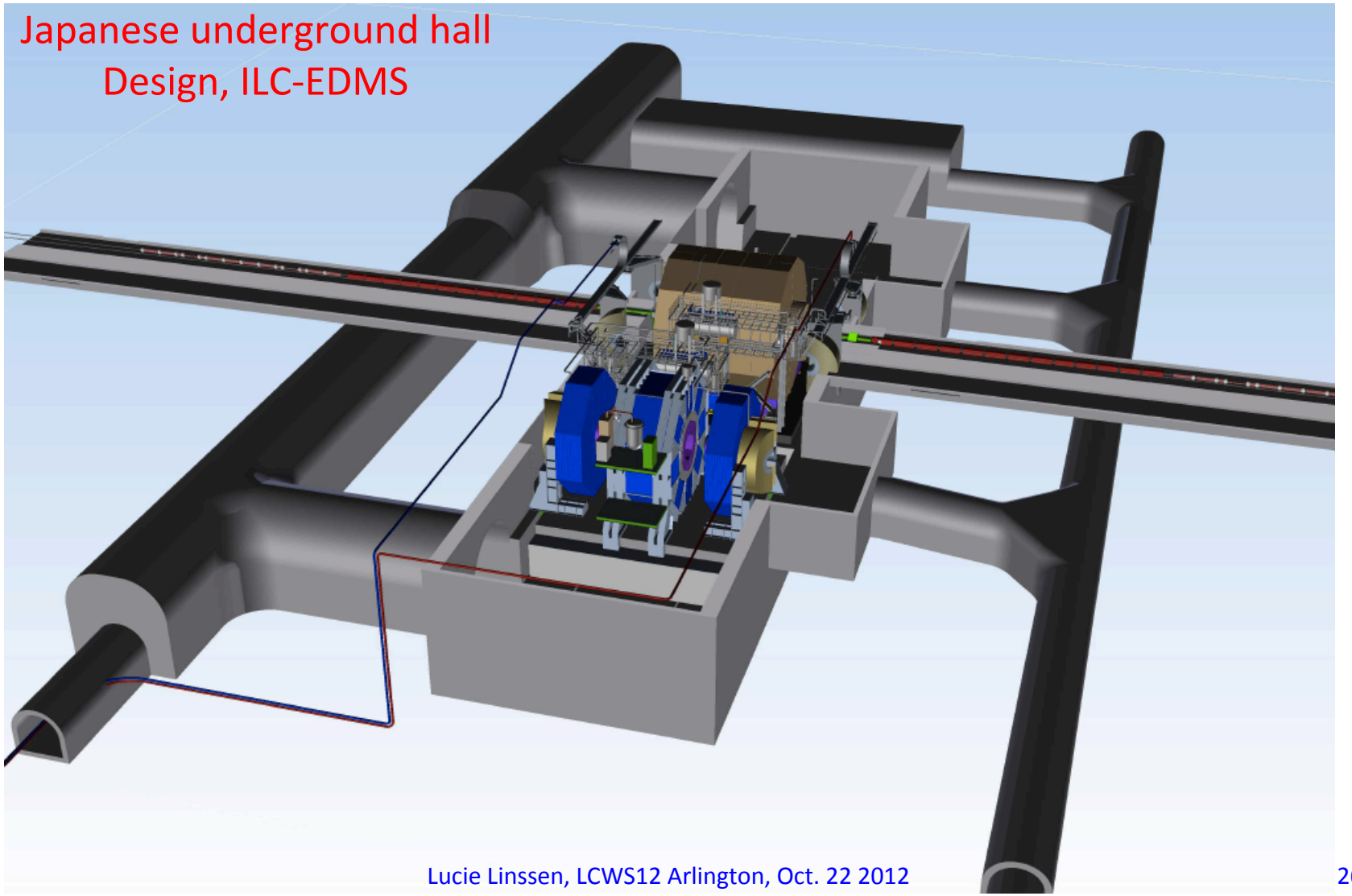
BEAN chip

- 180 nm CMOS
- FE+ADC
- beam diagnostics output

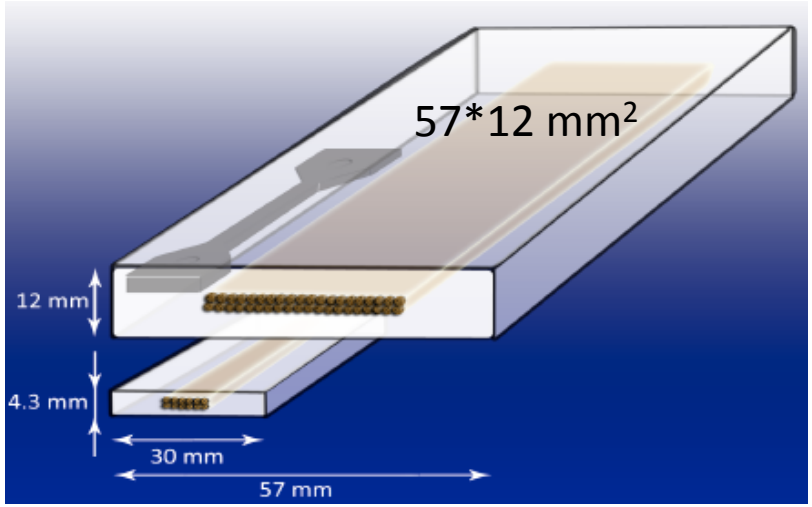


Engineering

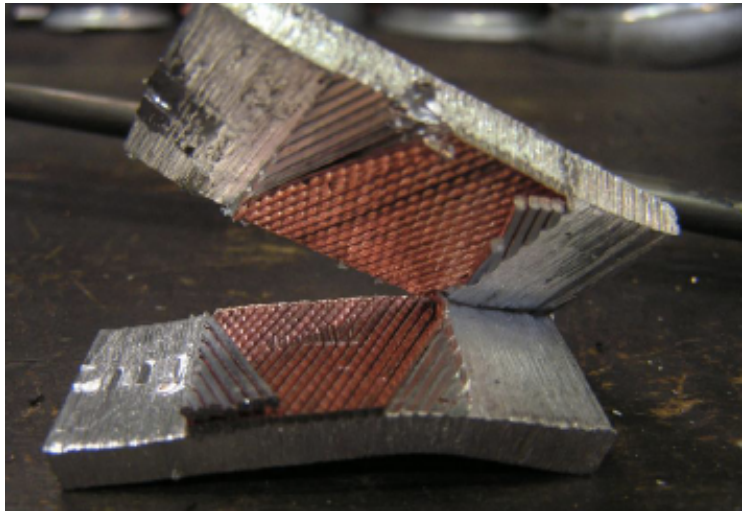
Progress in engineering work, applied from the very large to the very small
Picture illustrates**: interplay and data exchange between ILD / SiD / accelerator**



Solenoid coil

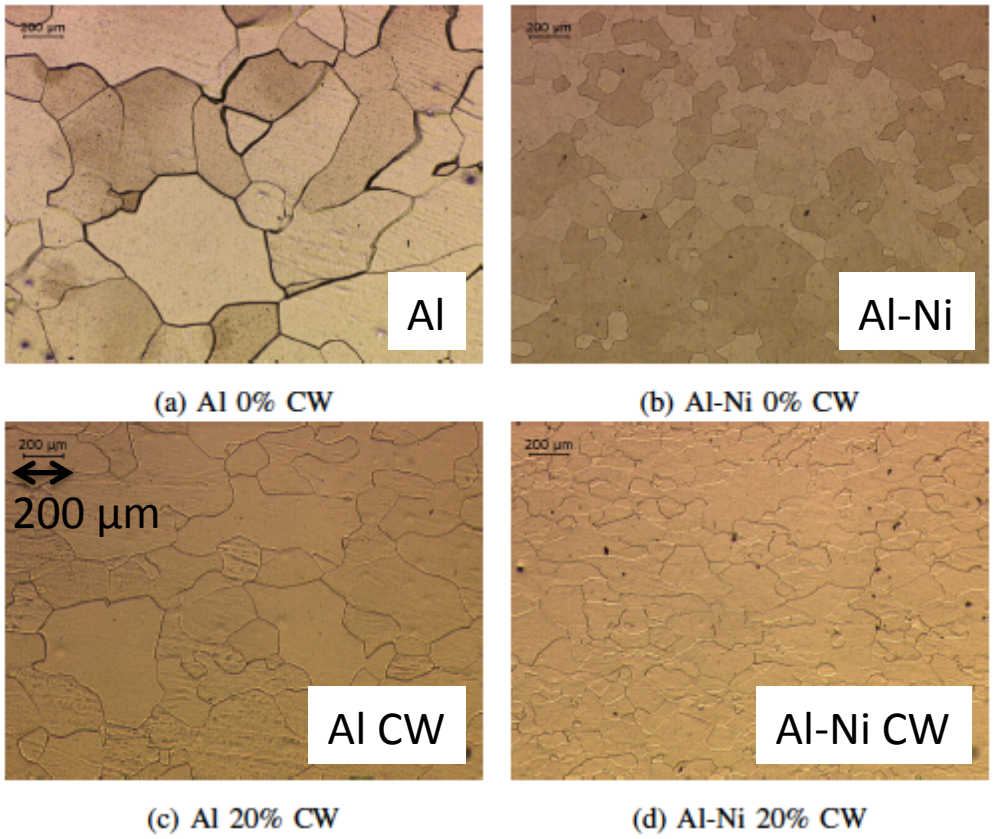


Conductor size, compared to ATLAS solenoid conductor



Shear test

Extrusion of Al-Ni reinforced conductor



Change in material properties of Al and Al-Ni before and after cold-working

Material property trends behave as expected

summary and outlook

Summary

Despite funding difficulties, there is a broad ongoing detector R&D program in

- Pixel detector
- TPC tracker
- Forward-region tracking
- PFA-based calorimetry + forward calorimetry
- While main silicon tracker R&D (equally challenging !) lags a bit behind

R&D is successfully moving to fully integrated technologies

- This holds in particular for calorimetry

My personal comment:

In the coming years, strengthening is required in domains of:

- **Low-mass Vertex-detector + Tracking integration issues**
- **Power pulsing !**

With many **thanks to**: Karsten Buesser, Dominik Dannheim, Cristian Fuentes, Wolfgang Lohmann, Jochen Kaminski, Stefanie Langeslag, Felix Sefkow, Yasuhiro Sugimoto, Tohru Takeshita, Ivan Vila ….

….and for DBD's and lots of material I simply found on various LC sites ….

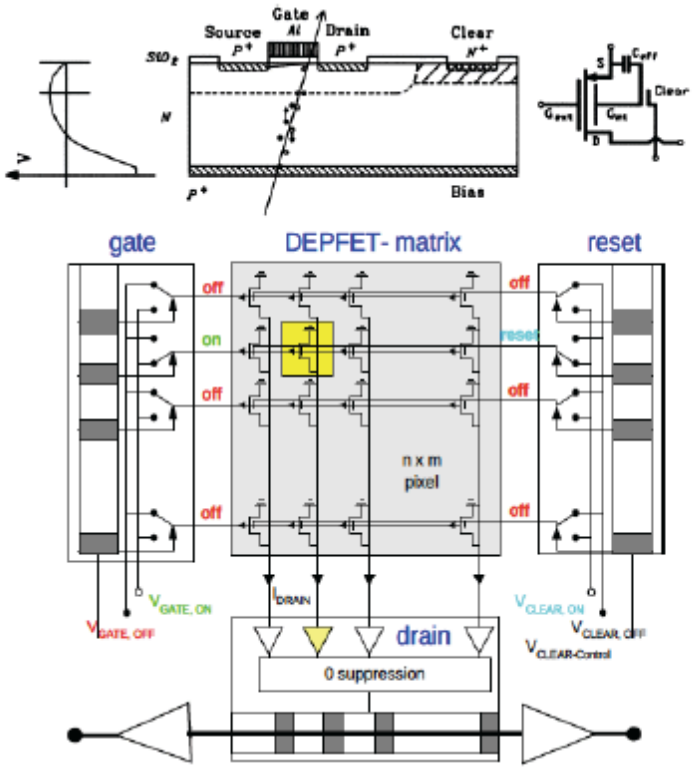
SPARE SLIDES

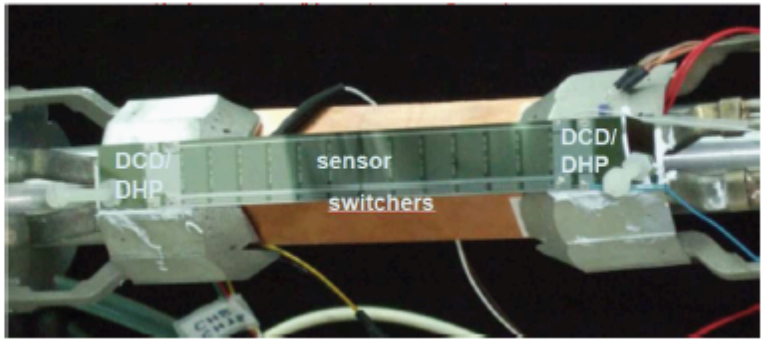
Vertex detector: DEPFET (ILC)

- The Depleted Field-Effect transistor relies on a depleted layer located under a FET.
- A Potential minimum is created in the channel of the transistor
- Accumulation of charge from ionizing particles modifies charge distribution in the channel and increases transistor current

- Monolithic sensor allows for thin assembly (50 µm , ex: PXD6)
- Allows for small pixel size (~25x25 µm)

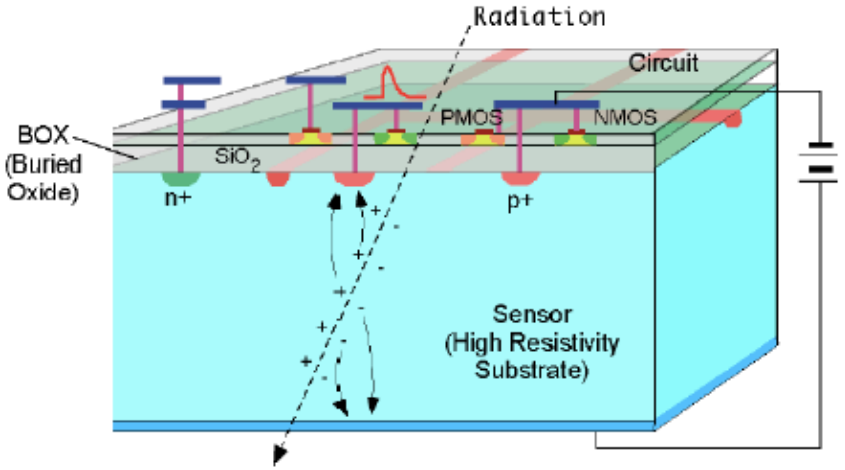
- Integrating sensor (Frame ~25-100µs)
  → coarse time stamping





Vertex detector: SOI pixel sensor

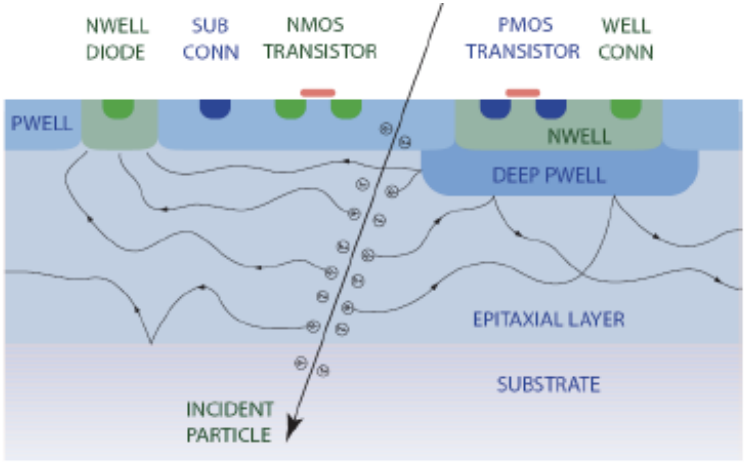
- CMOS sensor on SOI wafers
  - Fully depleted High-Resistivity sensor
  - Electronics on low resistivity wafer separated by BOX from sensing layer
- Allow for standard CMOS electronics
  - Fast time stamping possible
  - Complex pixel « intelligence »
  - Insulation of each device from bulk allows for low leakage-current operation



Digital ECAL: SPiDeR-INMAPS

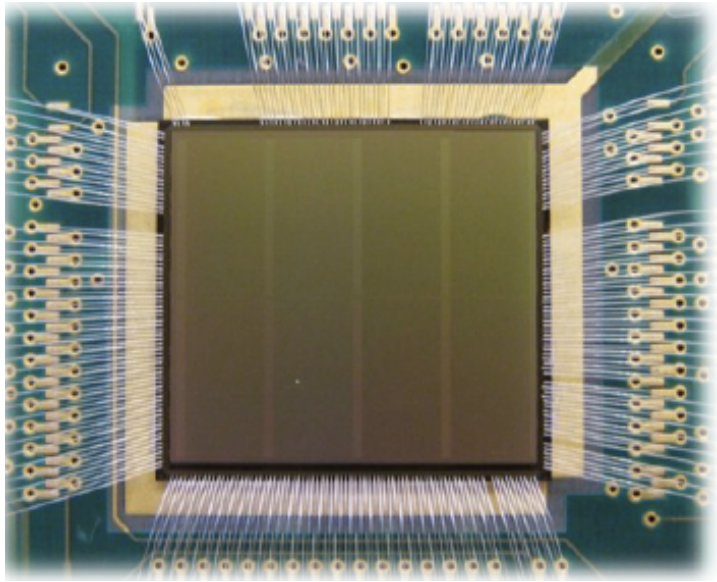
Digital ECAL concept for rates up to 100 particles/mm^2 => ~50 µm pixel size

- 168×168 pixel grid
- 50×50 µm^2 pixel size
- Digital readout
- Low noise
- INMAPS process
  - Deep P-WELL implant for charge collection
- Charge collected by diffusion to signal diodes



Successful BEAM tests at CERN and DESY

- With MIPs and particle showers
- Confirms increased MIP efficiency with INMAPS technology
- Shower multiplicity increases with incident energy => indicating validity of DECAL concept



TPAC sensor