Status of the CALICE Scintillator HCAL Engineering Prototype

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LCWS 2012,
October 24th 2012

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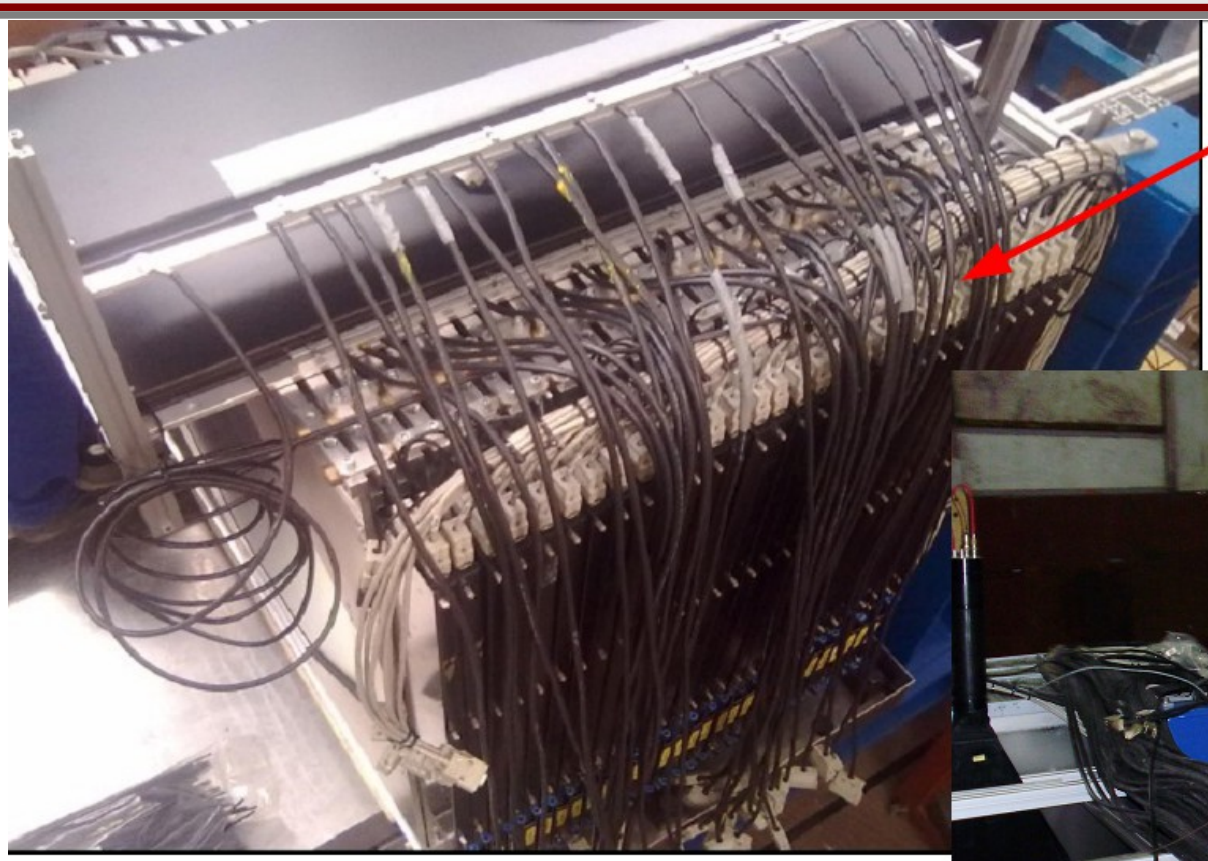
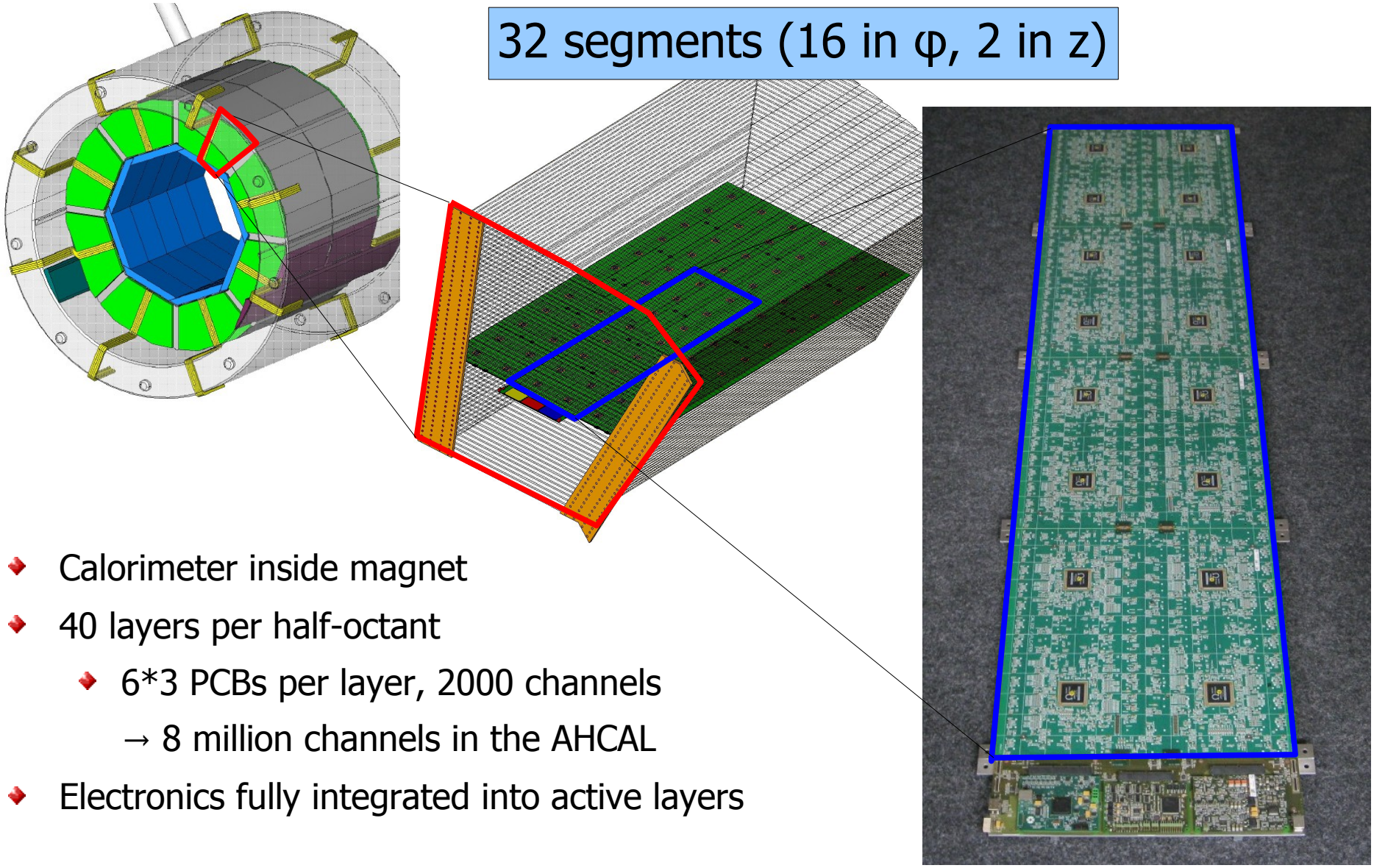
AHCAL Physics Prototype



Not scalable to full detector
→ Build realistic prototype

The AHCAL Engineering Prototype

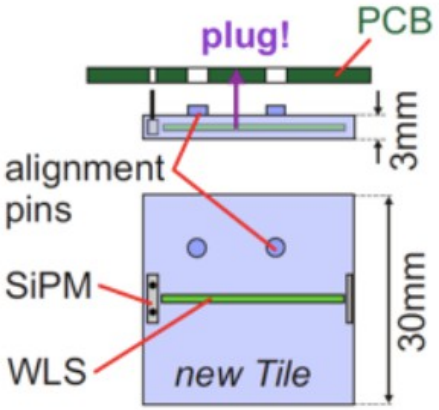


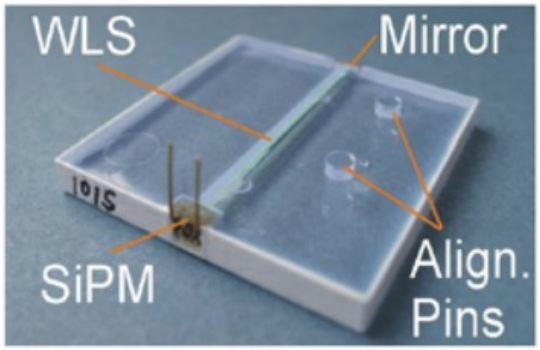
- Calorimeter inside magnet
- 40 layers per half-octant
  - 6*3 PCBs per layer, 2000 channels

    → 8 million channels in the AHCAL
- Electronics fully integrated into active layers

Signal Sampling

- Signal from scintillating tiles
  - 30x30x3mm^3
  - Fiber collects and shifts light
  - Alignment pins plug into PCB
- Sampled by individual SiPM per channel
  - 796 Pixels
  - Gain 500k-3000k
- Assembled tiles with SiPMs from ITEP
  - Bias adjusted for 15 Pixels/MIP
  - Dark rate at 0.5MIP ~20Hz
- Different tile options under consideration

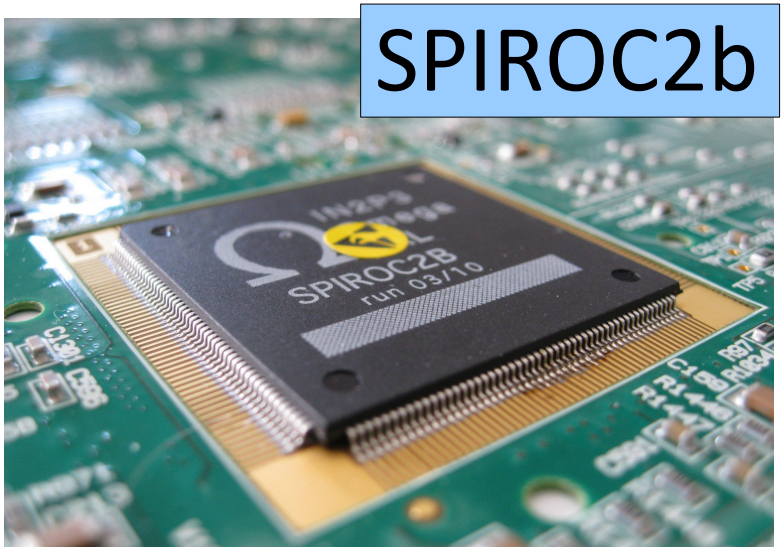




Readout Chip

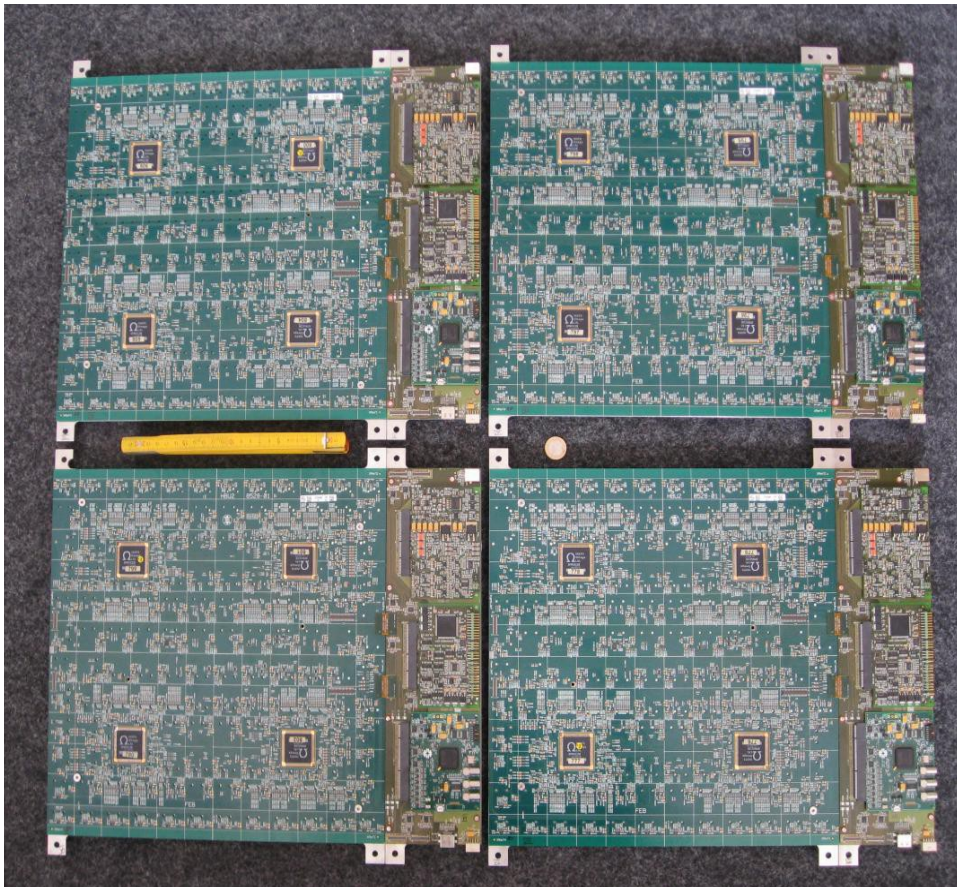
- SPIROC ASIC family designed by LAL, Orsay
- Provides readout for 36 SiPMs
  - Individual bias voltage per channel
  - 12bit dual gain ADC
  - Auto trigger
    - External validation mode
  - 12bit TDC (<1ns resolution)
  - Low power dissipation (25uW/channel)

    → Power pulsing (<1% duty cycle)
- Currently using SPIROC2b
  - Large quantities
- SPIROC2c available
  - Bug fix release
  - Already assembled



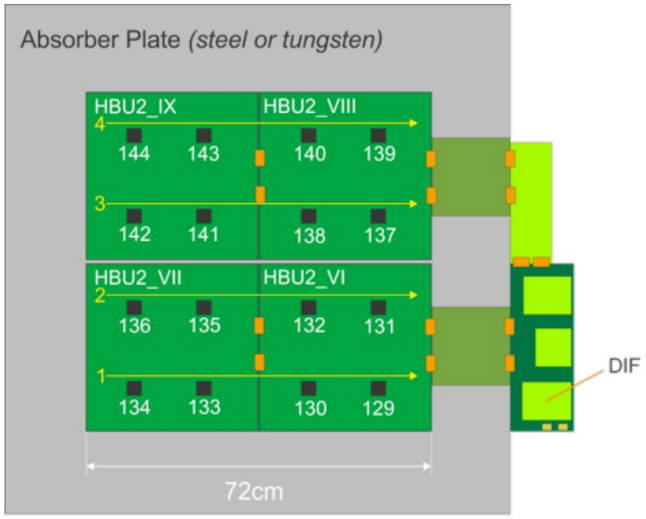
The HCAL Base Unit (HBU)

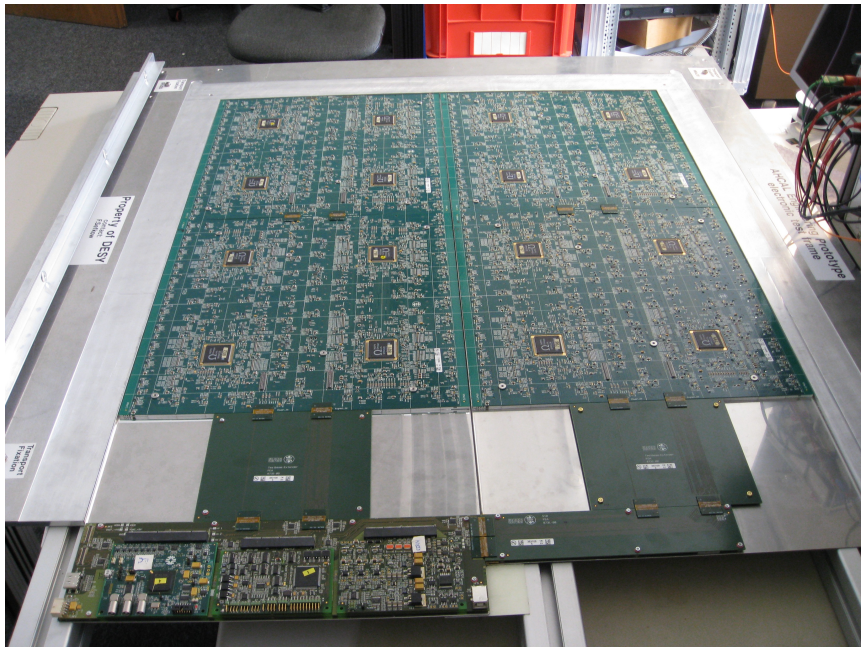
- 6x3 PCBs per layer
  - ~50000 boards for full HCAL
- 4 ASICs, 144 channels per PCB
- Integrated SiPM calibration system
  - Individual LED per channel
- 8 HBU2 boards available
  - 4 fully equipped and calibrated in DESY electron beam
  - 1 half equipped
  - 1 for SPIROC2c testing
- USB LabView DAQ for testing



Hadron Testbeam Setup

- 2x2 PCBs (72x72cm^2) in hadron testbeam next week
  - Last layer behind W-DHCAL (3.8λ_i)
  - Mechanical setup finished
- Measure radial hadron shower time development (similar to T3B)
  - Channelwise hit timing (SPIROC2b TDC)
- Larger scale system test
  - 576 channels
  - Readout of two slabs
  - Commissioning





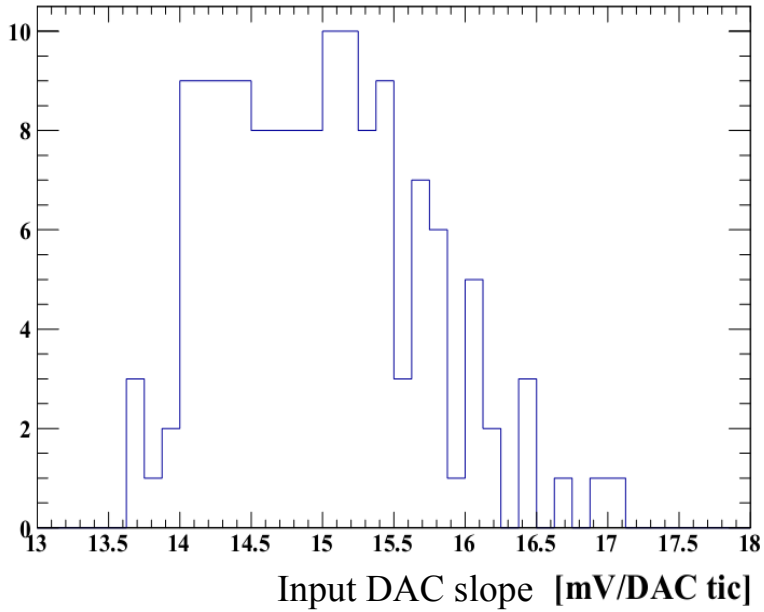
Detector Commissioning

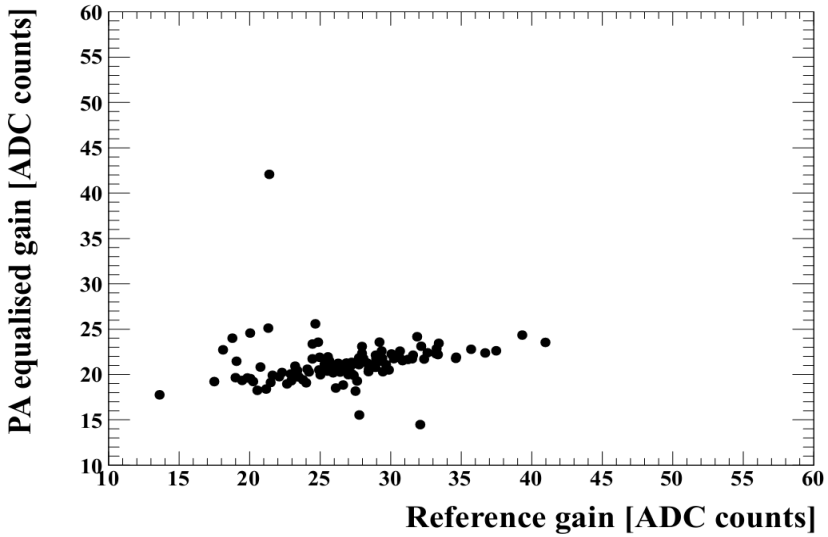
Tasks in commissioning:

- Create tilemaps
  - Group tiles by bias voltage
- Setup bias voltages for each channel individually
  - One DAC per channel
  - Low power design, need individual DAC calibration
- Configure preamplifiers for homogenous MIP response in ADC counts
  - Measure channel-individual preamplifier curve
- Setup Autotrigger thresholds
  - 10bit global threshold
  - 4bit channelwise fine tuning
  - Greatly depends on SiPM noise rate, expected beam rate etc.

Commissioning Results

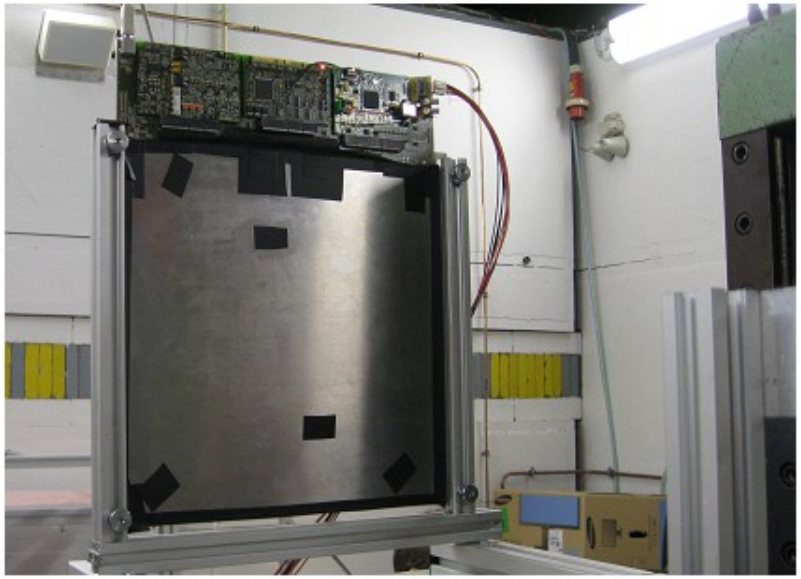
- Individual bias DAC calibration
  - DAC slope differs between channels
  - 20mV uncertainty after calibration
  - Would be 120mV without calibration
- Setup preamplifiers to compensate SiPM gain spread
  - 5-10% spread after preamplifier setup
- Set global trigger threshold
  - Measured dark rate vs. threshold position

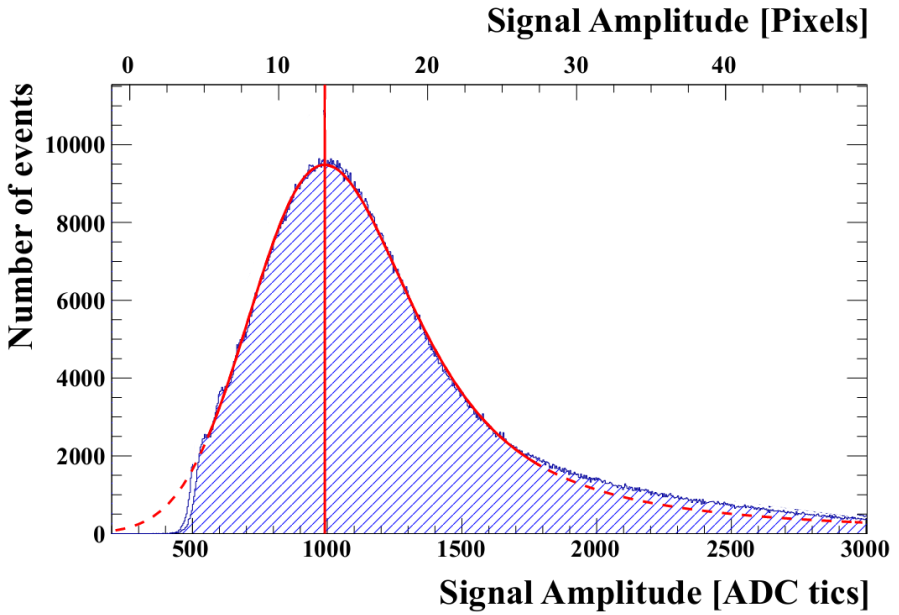




MIP Calibration

- All 4 boards for CERN testbeam calibrated in DESY electron test beam
  - 2-4GeV positron beam
    - ~3% difference between true MIPs and 3GeV positron
- Fully self-triggered operation:
  - Dark rate !< event rate
- Externally validated trigger operation
  - Trigger rate independent of noise rate
  - Suppresses most noise
- Fit with Landau-Gaussian convolution
  - MPV → MIP position
- See talk by Katja Krueger



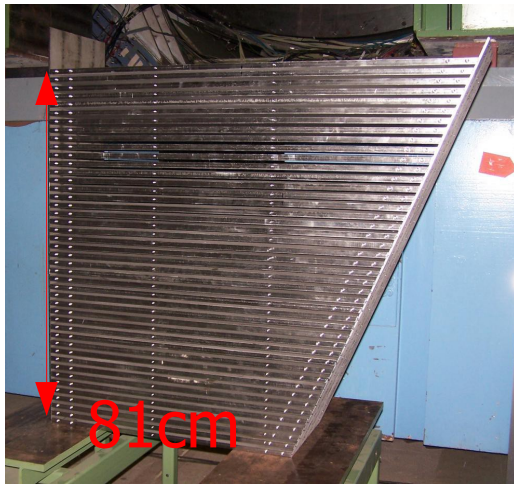


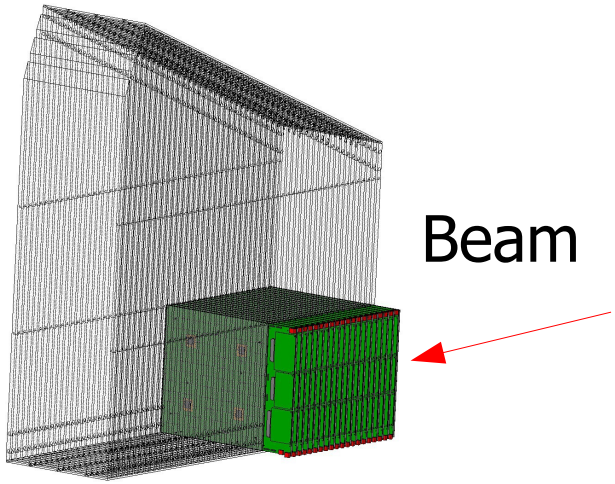
Future perspectives

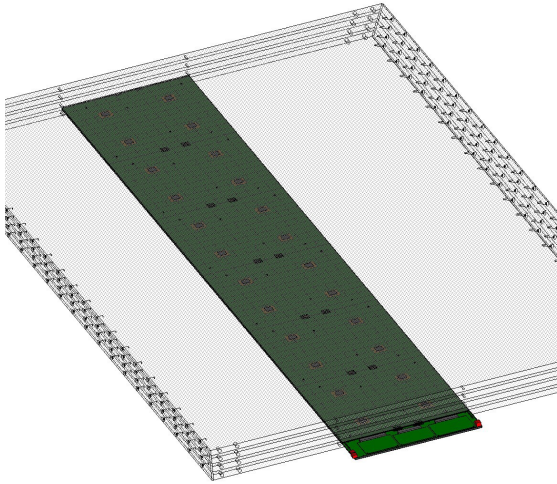
- ILD prototype absorber structure available at DESY
  - Slab power dissipation and heating test
  - Power pulsing
- Next year: ~10 single PCB layers with steel absorber (MiniCal)

→ EM showers in electron testbeam

- Further DAQ development essential

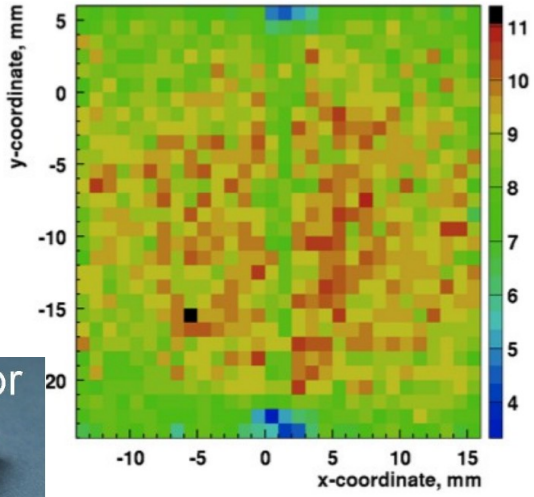


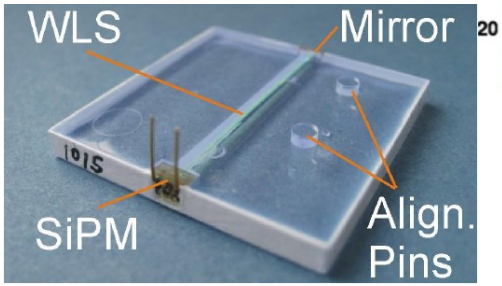


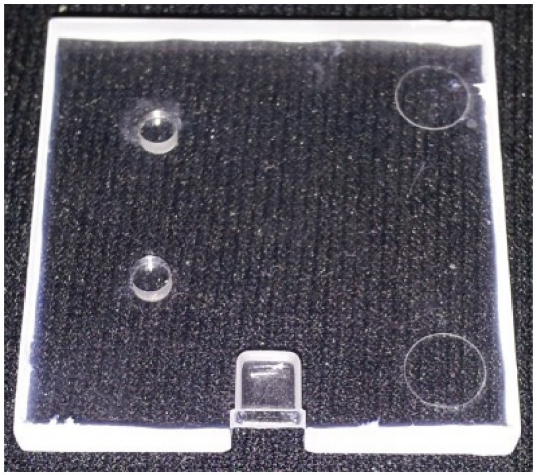


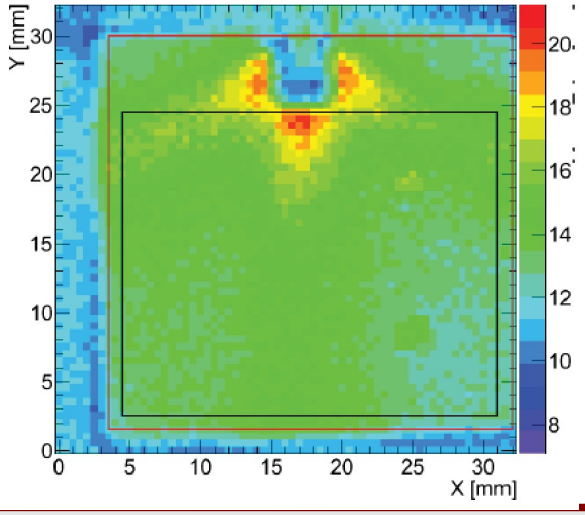
Scintillator Tile Options

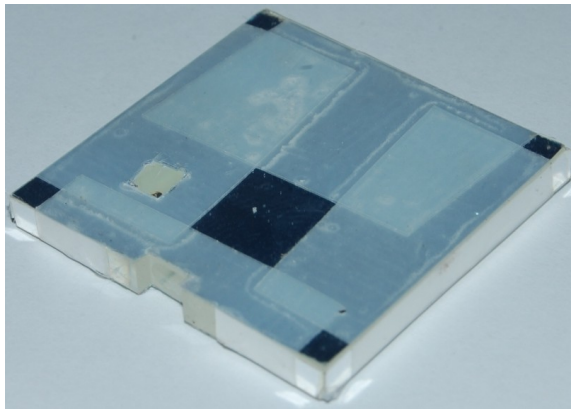
- MiniCal as SiPM/tile testbench
- Different tiles per layer
  - Fiber-less tile from MPI Munich shows good homogeneity, easier coupling
  - Hamburg University: individually wrapped tiles
- Different SiPM manufacturers/types







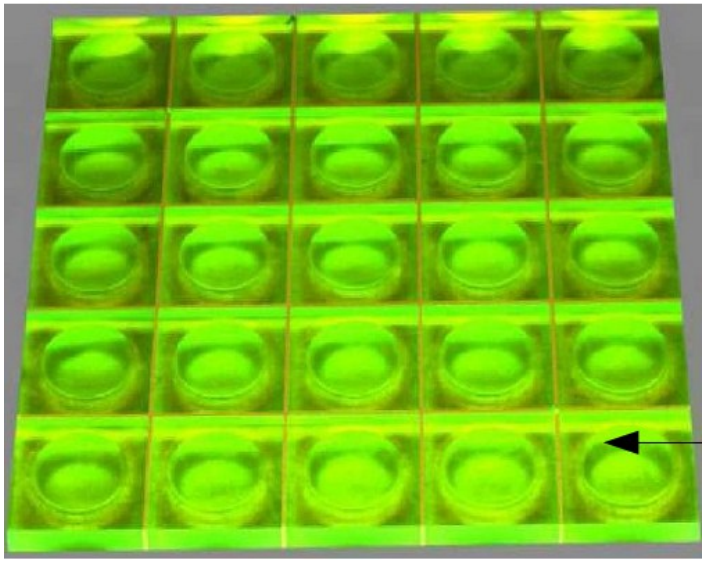


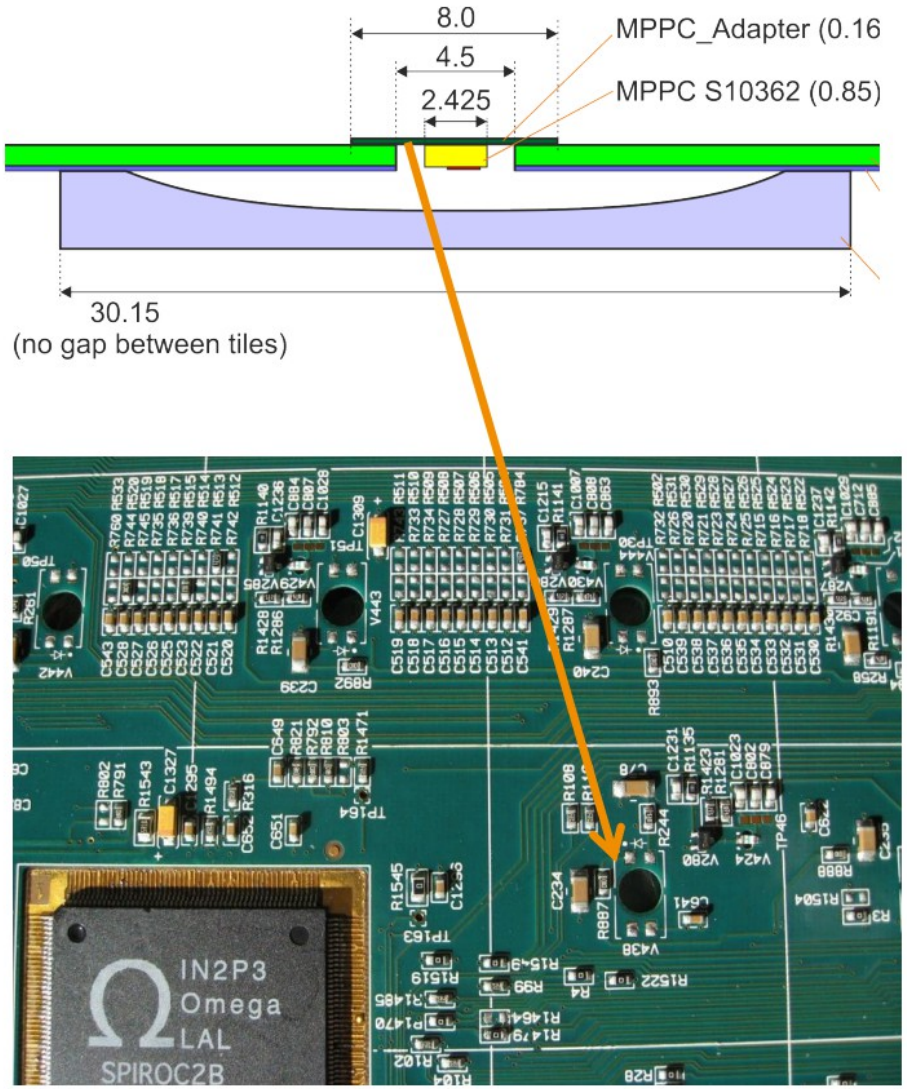


Surface Mounted SiPMs

- Northern Illinois University:
  Mount SiPMs on PCB, not in the tile
  - Eases assembly process

    → „Megatile“
- Tiles are dented to improve uniformity
- AHCAL PCB for surface mounted SiPMs produced and ready





Summary and Outlook

Summary

- AHCAL engineering prototype in development
- Prototype hadron testbeam at CERN, starting next week
- 4 new HBUs commissioned for prototype layer
- Successful DESY beam tests

Outlook

- Small calorimeter stack next year
- Using existing absorbers prototypes
- Test bench for different tiles and SiPMs
- Big ($1m^3$) technological prototype for hadron shower testbeams