

Status of FONT5 upstream feedback

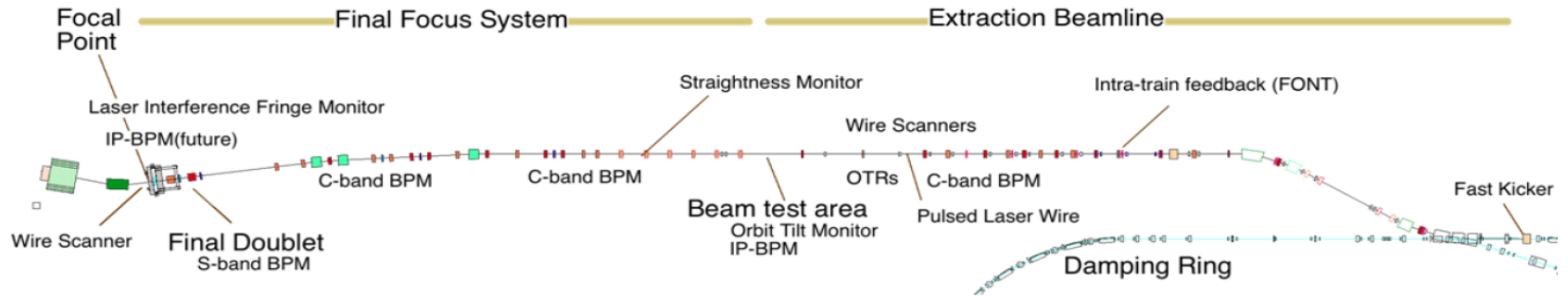
Glenn Christian

Robert Apsimon, Philip Burrows, Doug Bett, Neven
Blaskovic, Michael Davis, Young-Im Kim, Colin Perry
John Adams Institute, Oxford University

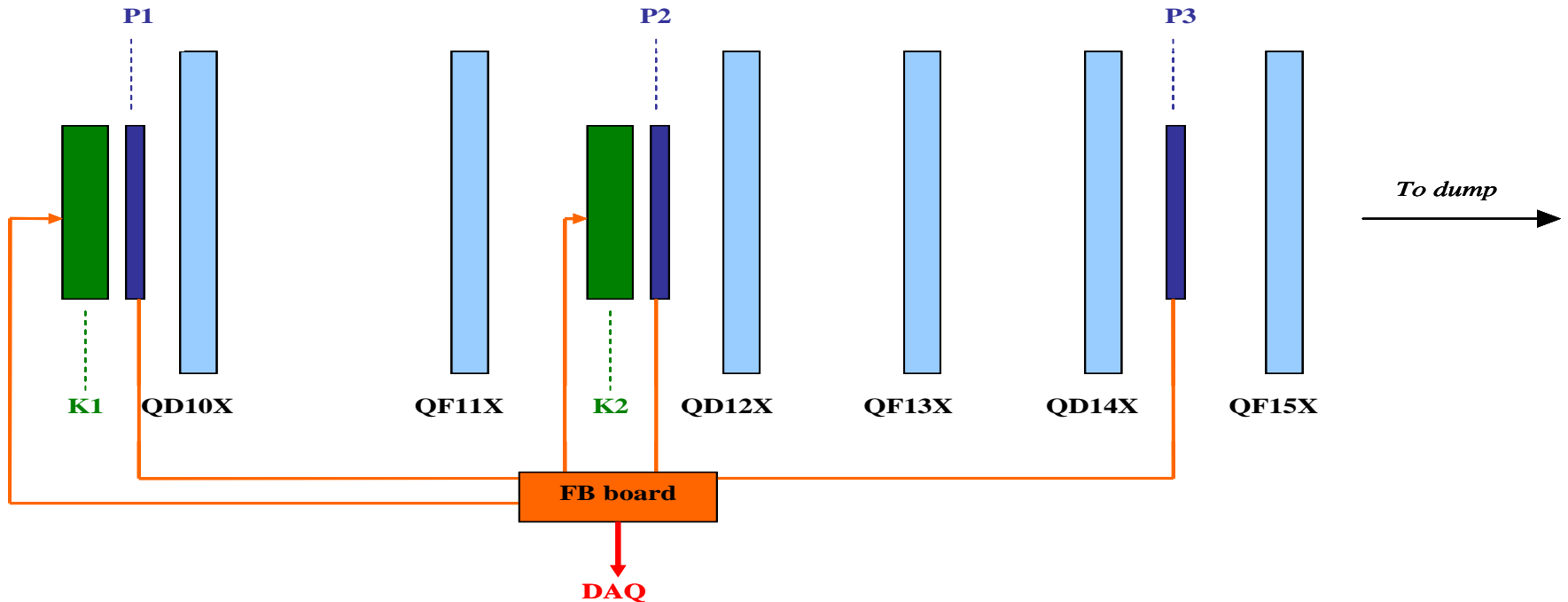
Javier Resta Lopez
IFIC, Valencia

26 June 2012
ATF2 Project Meeting

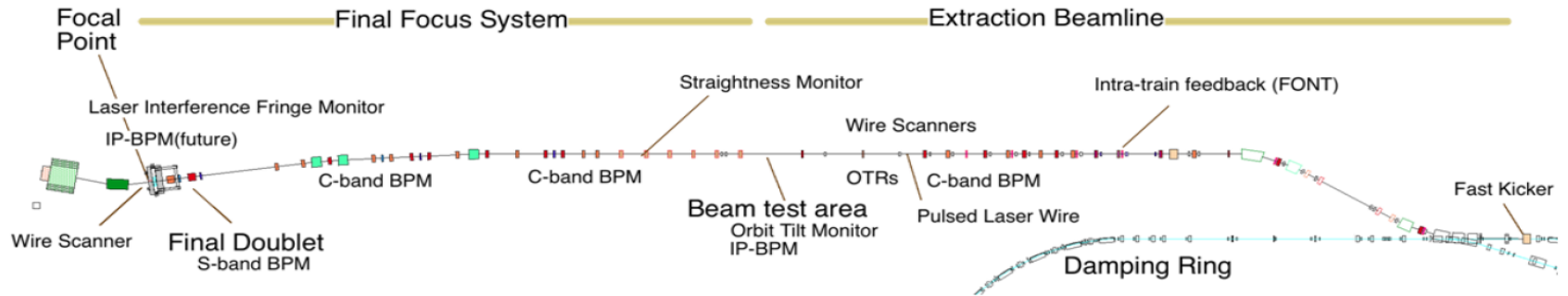
FONT5 upstream feedback system @ ATF2



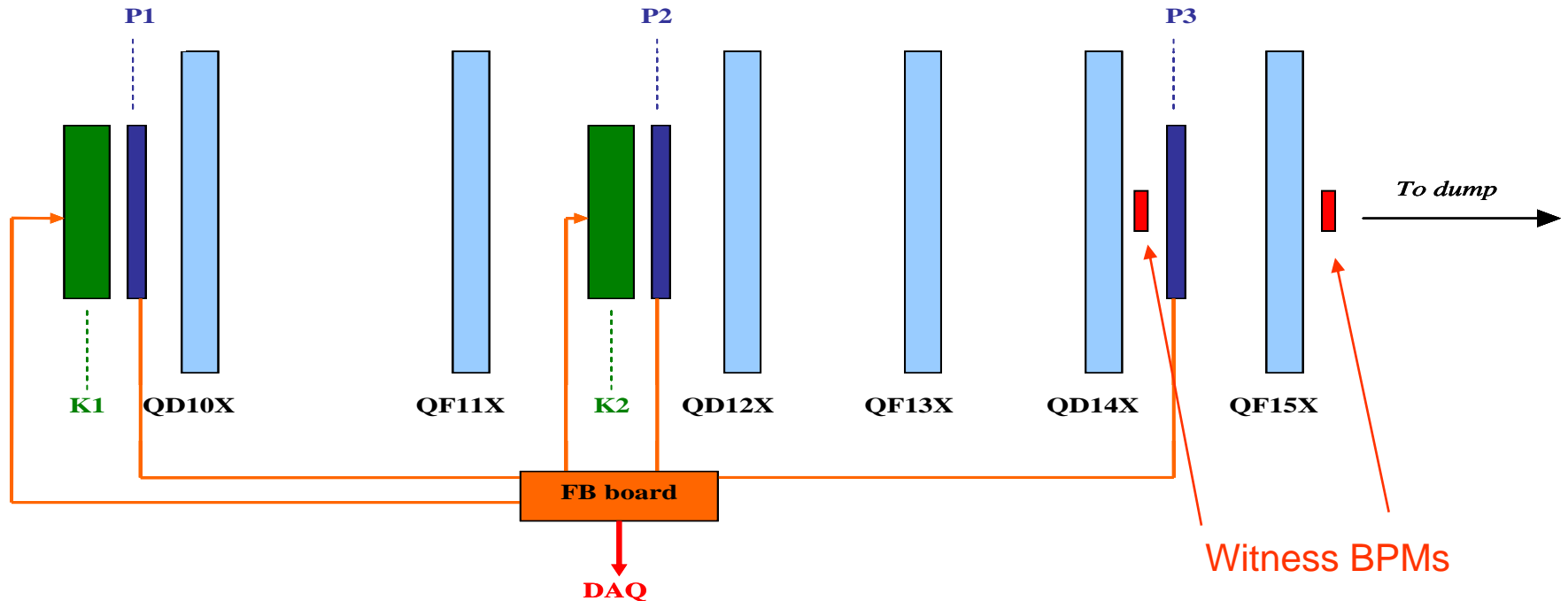
- Two phase FB (position and angle) system to stabilise beam to the 1 micron level at entrance to FF
- Bunch-by-bunch system (measure first bunch, correct subsequent bunches in train)
- 3 stripline BPMs (on movers), 2 stripline kickers



FONT5 upstream feedback system @ ATF2



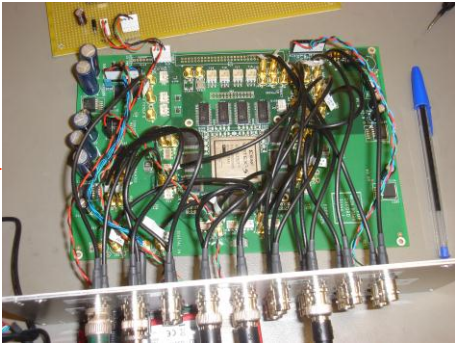
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FONT5 Hardware



Analogue Front-end
BPM processor



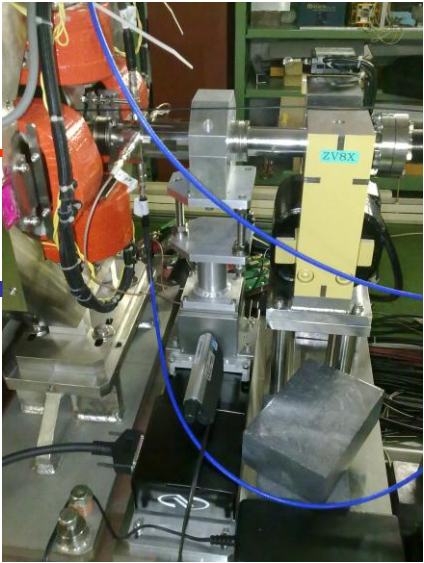
FPGA-based digital
processor



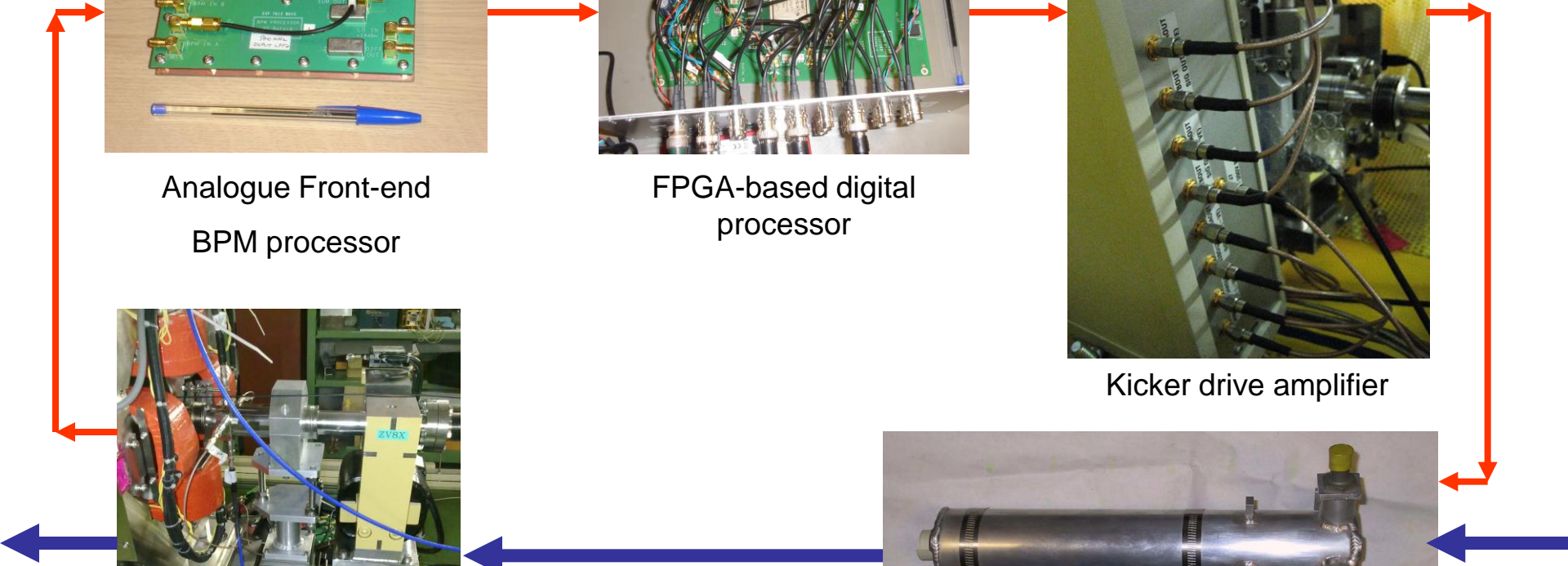
Kicker drive amplifier



Strip-line kicker



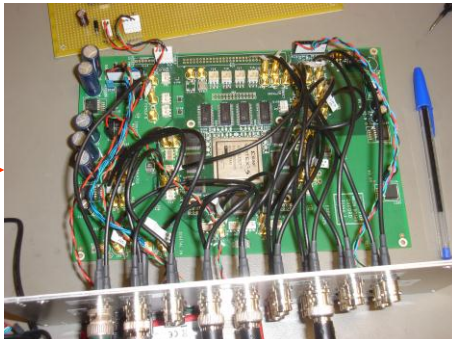
Strip-line BPM with
mover system



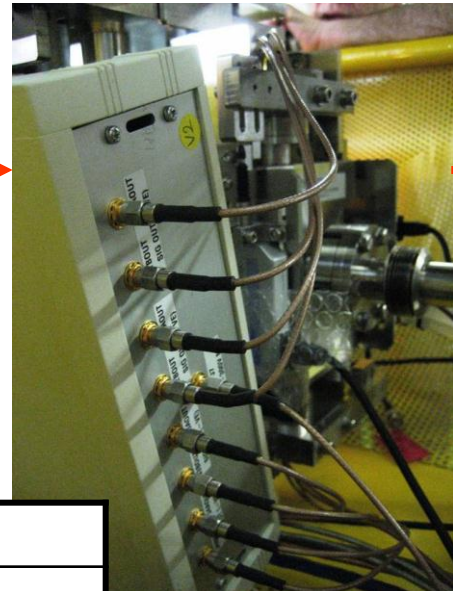
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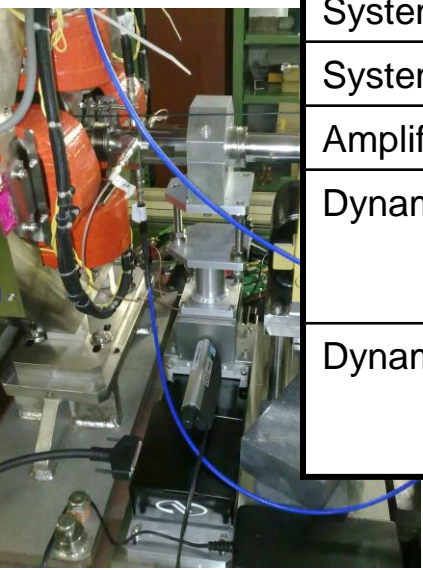
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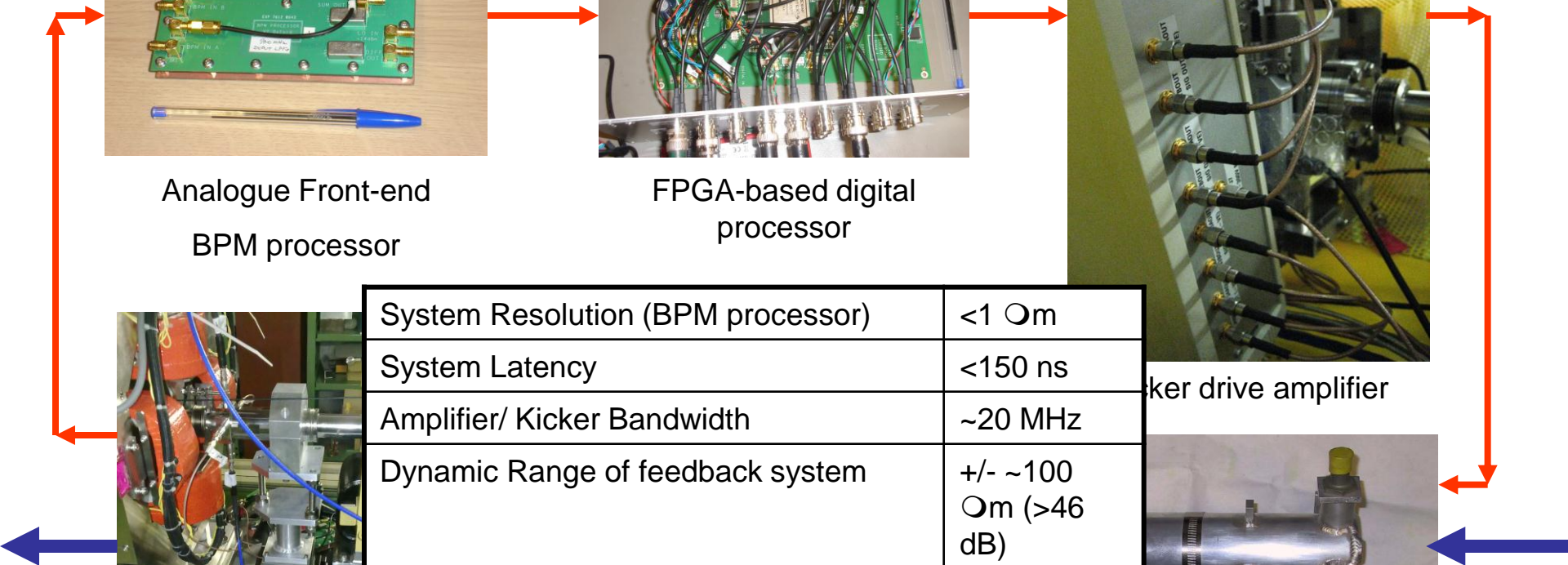
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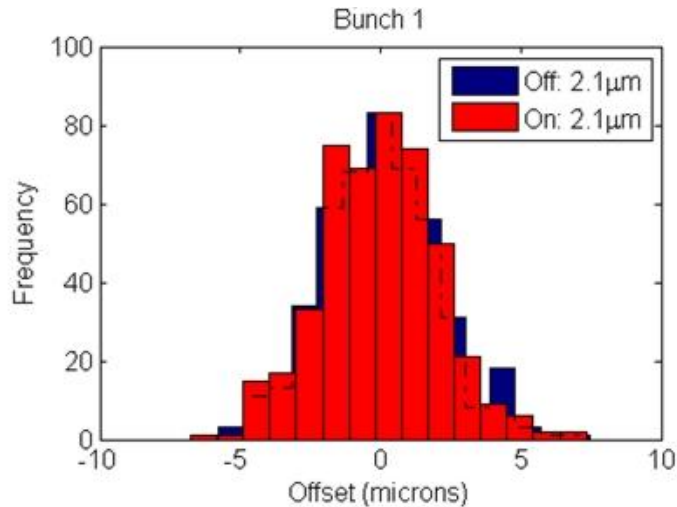
Strip-line kicker

System Resolution (BPM processor)	<1 \O m
System Latency	<150 ns
Amplifier/ Kicker Bandwidth	\sim 20 MHz
Dynamic Range of feedback system	+/- \sim 100 \O m (>46 dB)
Dynamic range of the BPM system	+/- \sim 500 \O m (>60 dB)

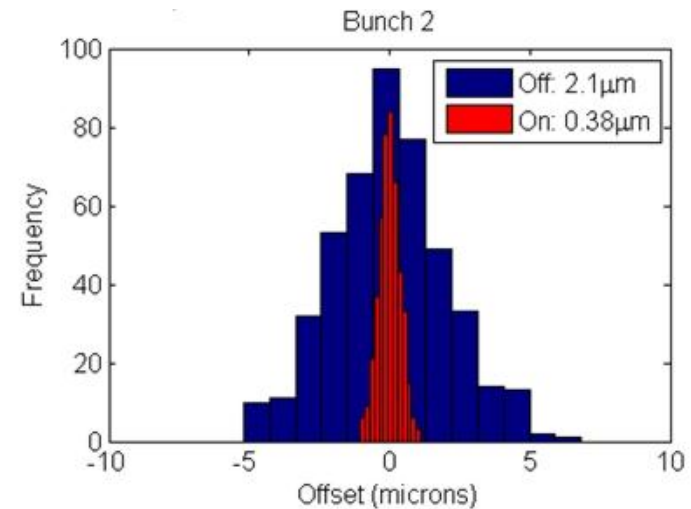
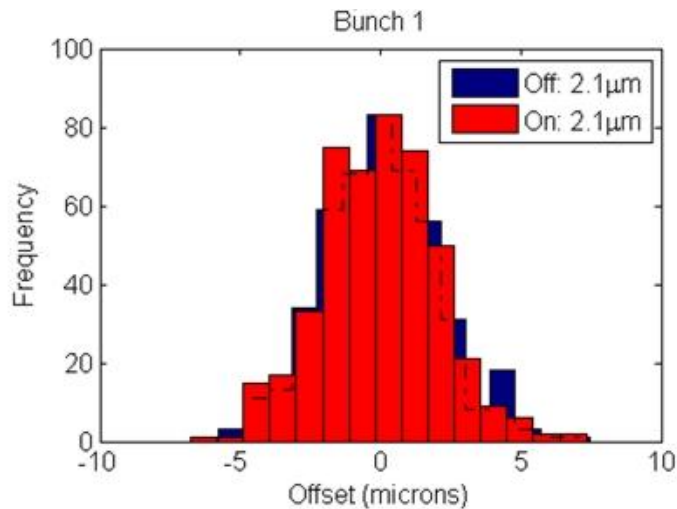
System parameters



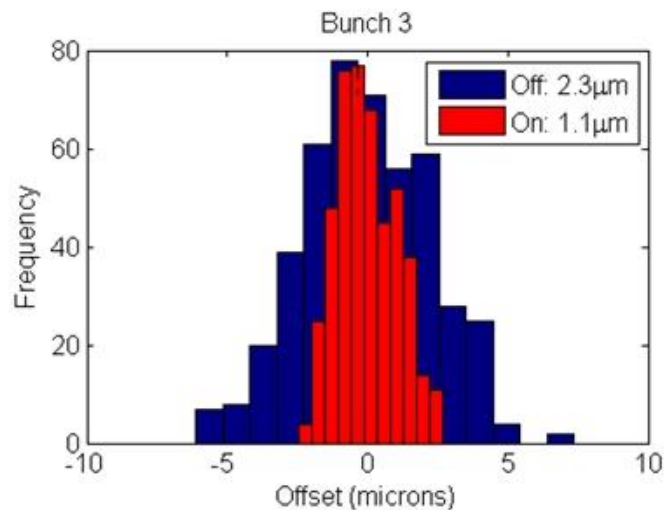
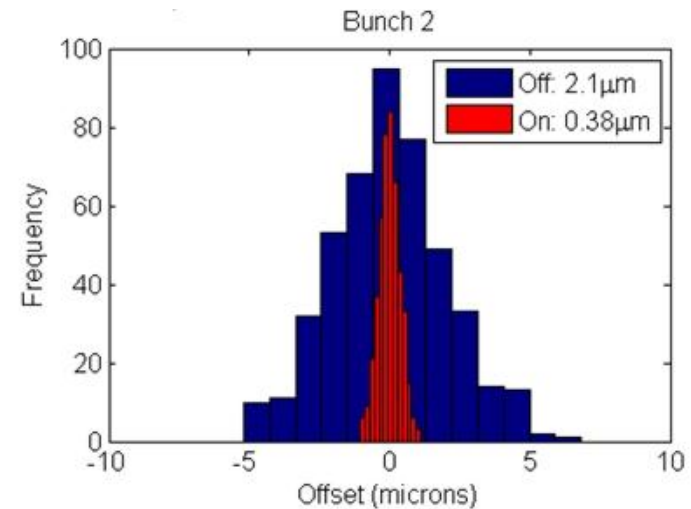
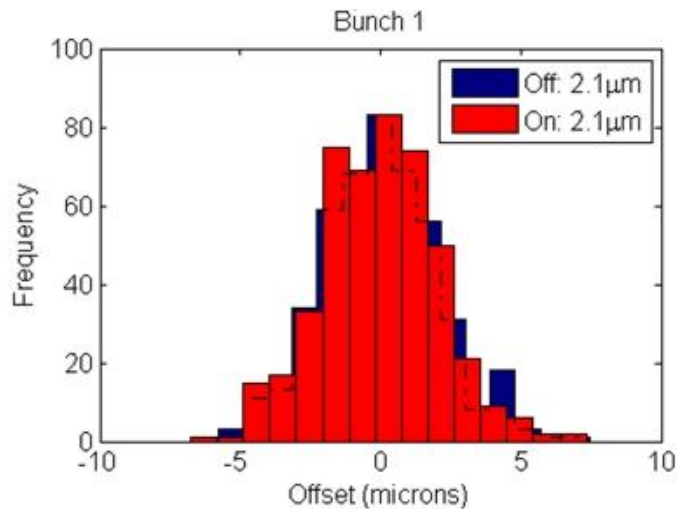
Feedback Performance (2) – Jitter Reduction @ P2 (16 April 2010)



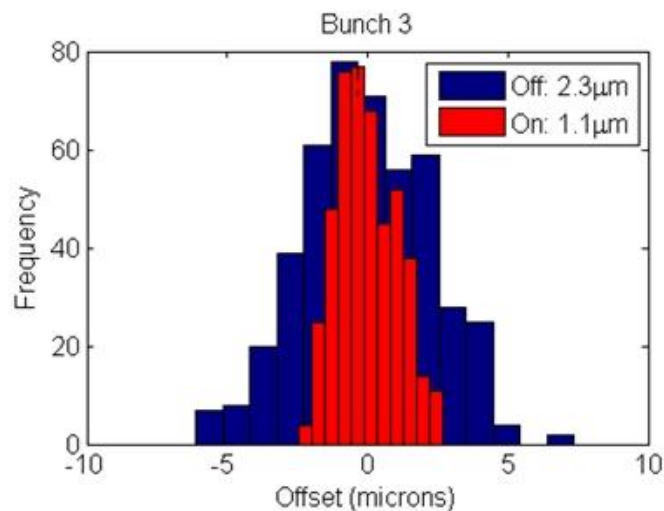
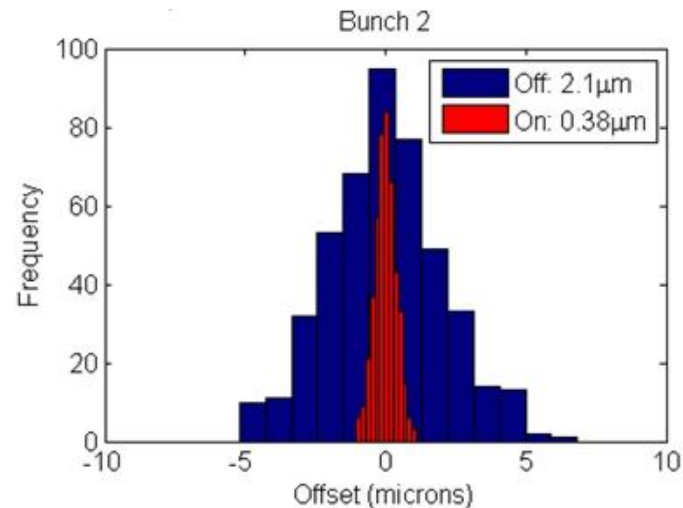
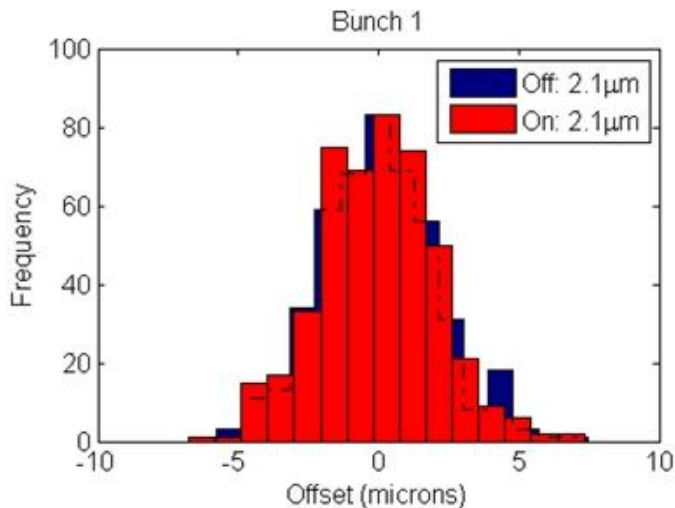
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Measured bunch-to-bunch correlations:

Bunch 1 – Bunch 2 : 98 %

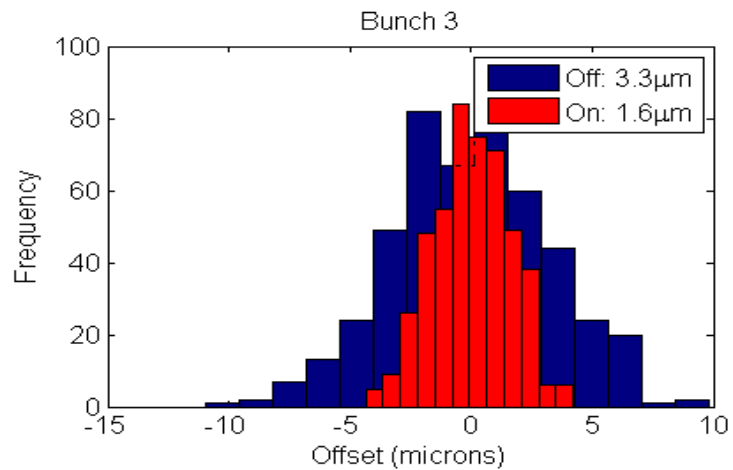
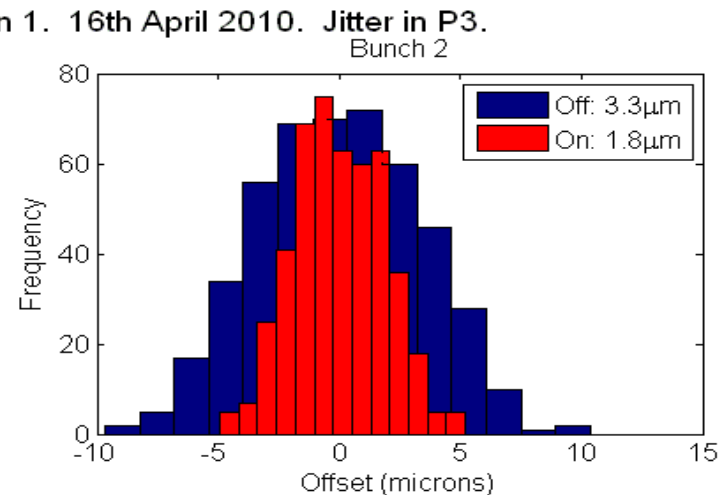
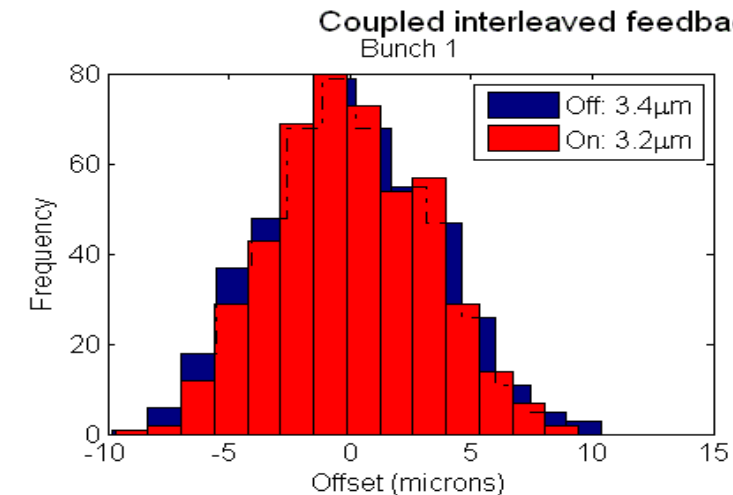
Bunch 2 – Bunch 3 : 89 %

(Bunch 1 – Bunch 3 : 85 %)



Bunch 2 result implies resolution of ~ 300 nm!

Feedback Performance (3) – Jitter Reduction @ P3 (16 April 2010)



Measured bunch-to-bunch correlations:

Bunch1- Bunch2 = 84%

Bunch2 - Bunch3 = 87%

(Bunch1- Bunch3 = 94%)

Summary of FONT data-taking visits 2012

- March 2012 – 1 week [Bett, Davis, Blaskovic]
 - 1 week, 2 shifts.
 - Further investigations of phase jitter effects.
- April 2012 – 1 week [Bett, Davis, Blaskovic]
 - 2 shifts
 - First tests of new FB firmware (with online phase compensation) – see later!
- May 2012 – 2 weeks [Davis, Blaskovic]
 - 2 shifts per week
 - Troubleshooting problems with new firmware & first look at IP cavity signals
- June 2012 – 2 weeks [Kim, Bett, Blaskovic, Perry (wk2), Christian (wk2)]
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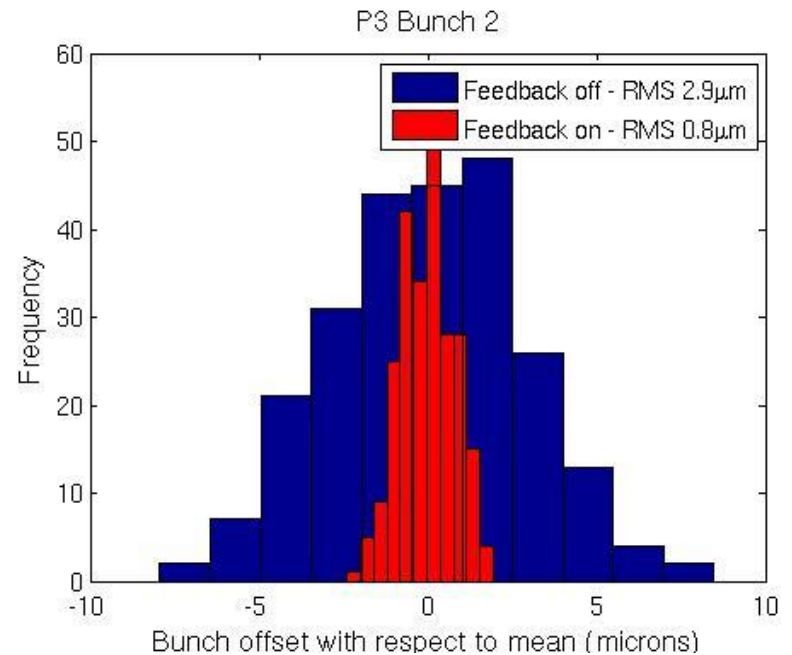
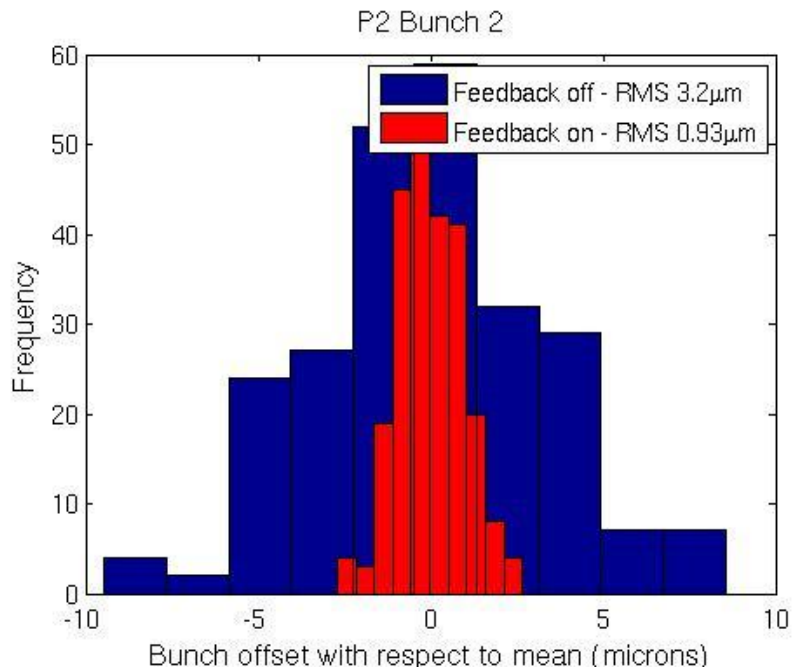
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 - First week mainly monitoring IP cavity BPM signals, second week tests of new IPFB kicker installed at IP.
- More details can now be found on ATF Twiki/eelog system.
- Attention slowly shifting from upstream dual-phase FB system to IP feedback
 - See talk on IP feedback (P. Burrows) Thursday 14:40 JST!

Upstream FB status

- Since ~2010, aim with upstream system has been to demonstrate similar level of performance in K2 loop as seen with K1, and observe correction downstream.
 - Programme of modification to processors in 2011 (Better matching of cable lengths into hybrid, suppression of pickup on ADC sampling clocks, BP-filtering FPGA clock)

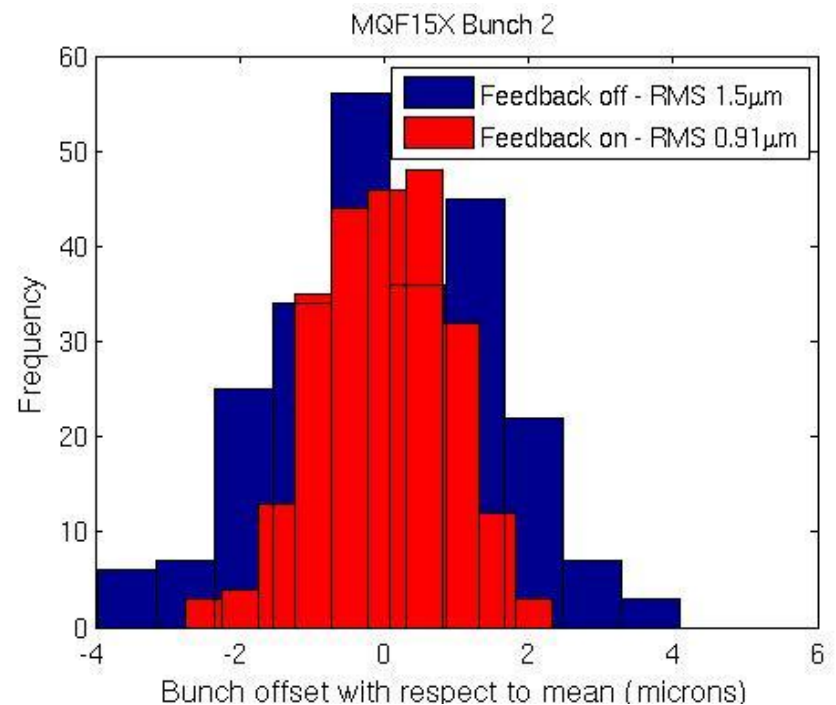
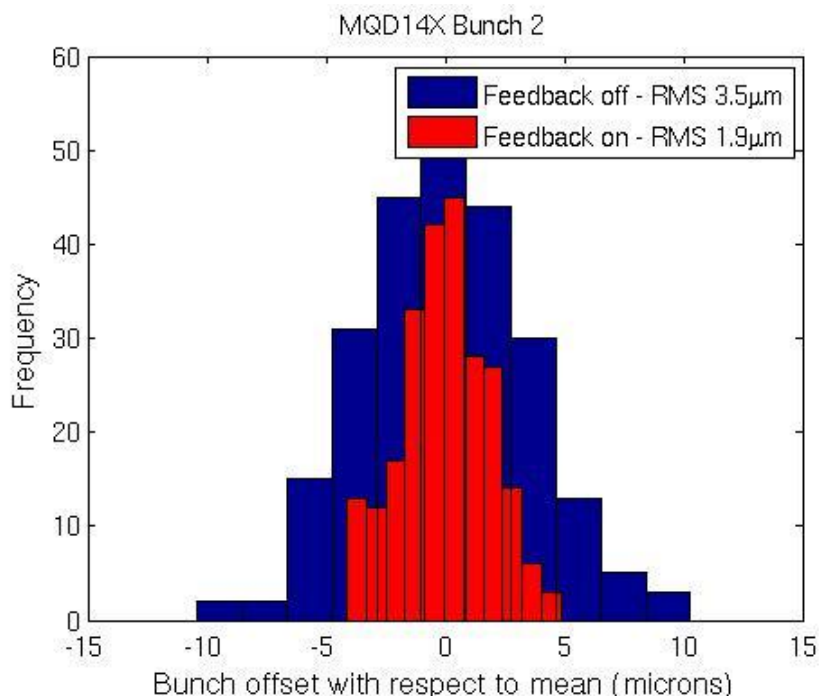
December 2011 FB results

Feedback BPMS



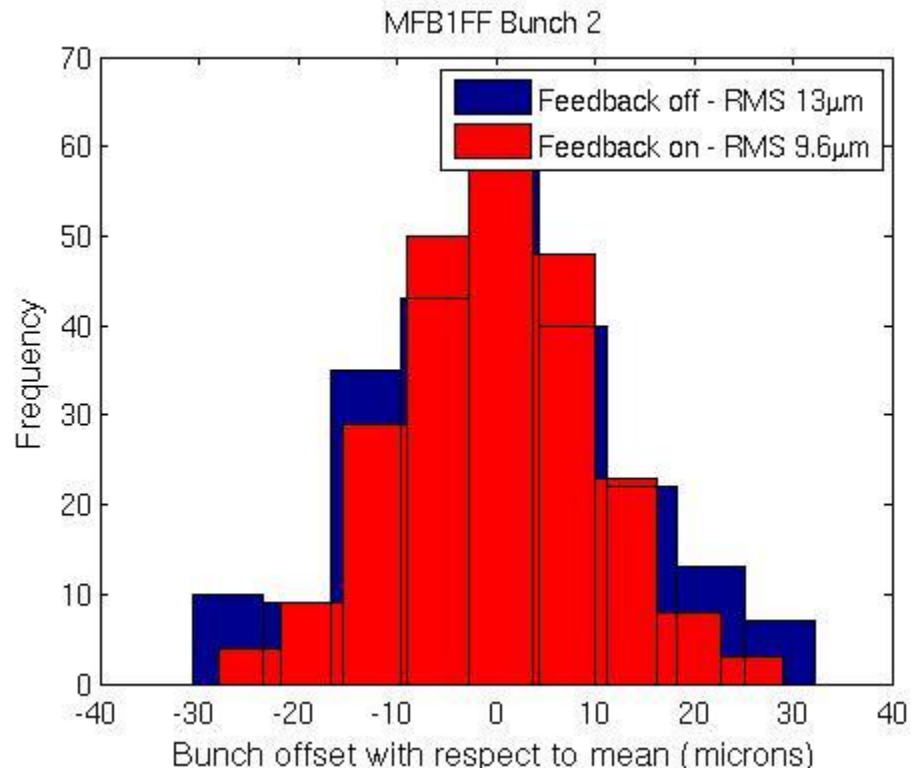
December 2011 FB results

Witness BPMS (1)



December 2011 FB results

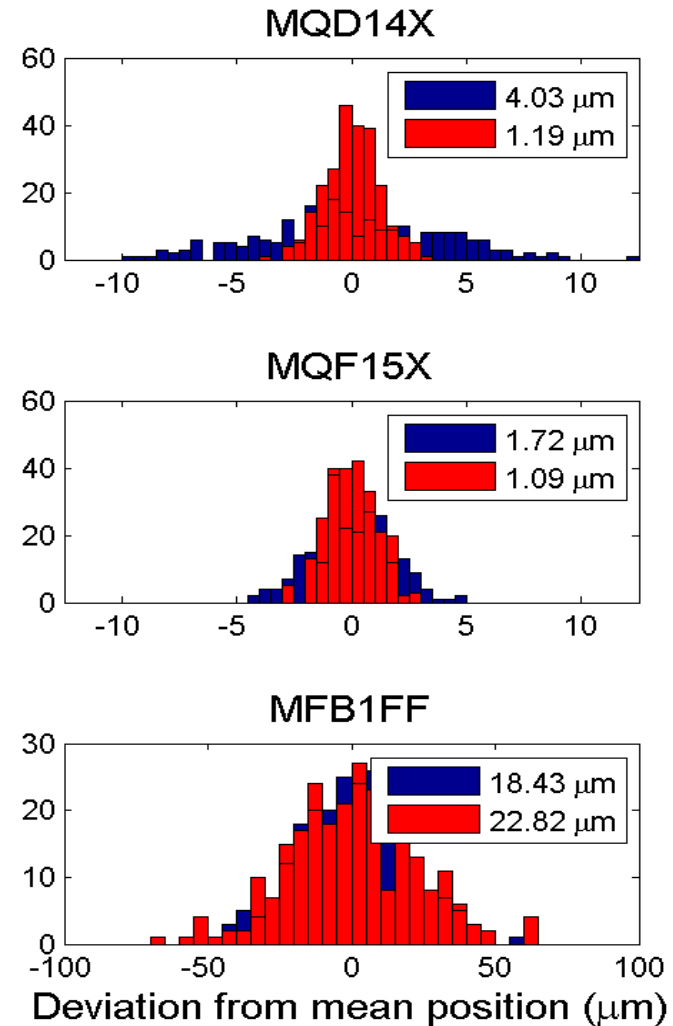
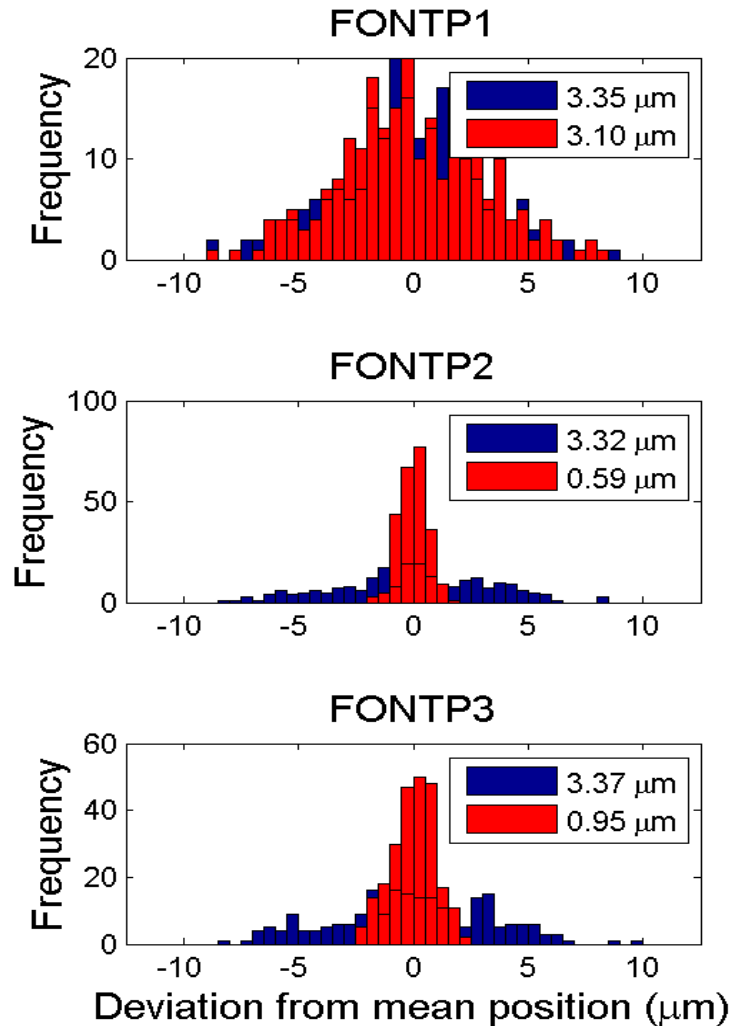
Witness BPMS (2)



Feedback examples (14 Dec 2011)

Second Bunch

Run6_141211



Upstream FB status

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 - Programme of modification to processors in 2011 (Better matching of cable lengths into hybrid, suppression of pickup on ADC sampling clocks, BP-filtering FPGA clock)
- Focused on studying performance limitations of the system: processor noise, systematic effects of LO phase jitter wrt bunch, and understanding discrepancy between observed FB performance and expected limit:
 - Observed correction level at FB BPMs < 0.4 microns
 - Measured (apparent) resolution of BPMs: 1 – 3 microns!!

BPM resolution tests (parasitic)

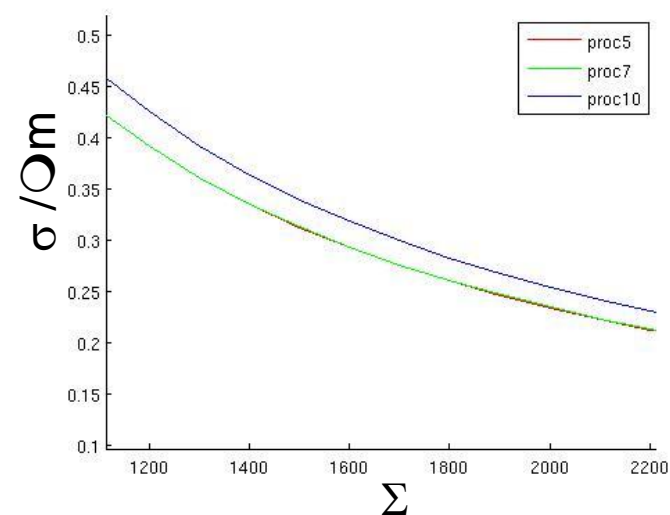
October 2011 – 3 processors on P2 (Charge ~1000-1500 cnts,
Jitter 3-4 microns)

Proc1	0.55	0.56	0.53	0.50	0.45	0.50
Proc2	0.56	0.54	0.40	0.35	0.44	0.43
Proc3	0.60	0.51	0.35	0.33	0.35	0.36

December 2011 – 2 processors on P1,P2,P3

Board #	Method	P1 soln	P2 soln	P3 soln
	1 3-BPM fit	3.01	0.61	0.61
	2 3-BPM fit	1.49	0.79	0.80
BOTH	2-on-1 pairwise	0.39	0.67	0.40
	1 3-BPM fit	3.38	0.70	0.70
	2 3-BPM fit	2.25	0.77	0.78
BOTH	2-on-1 pairwise	0.39	0.53	0.36

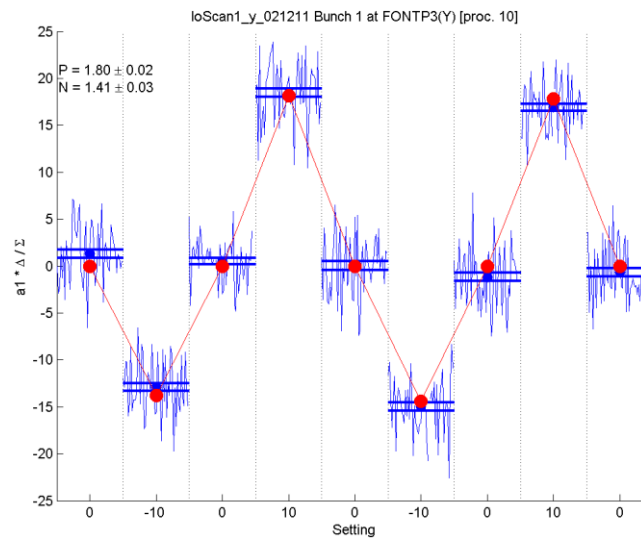
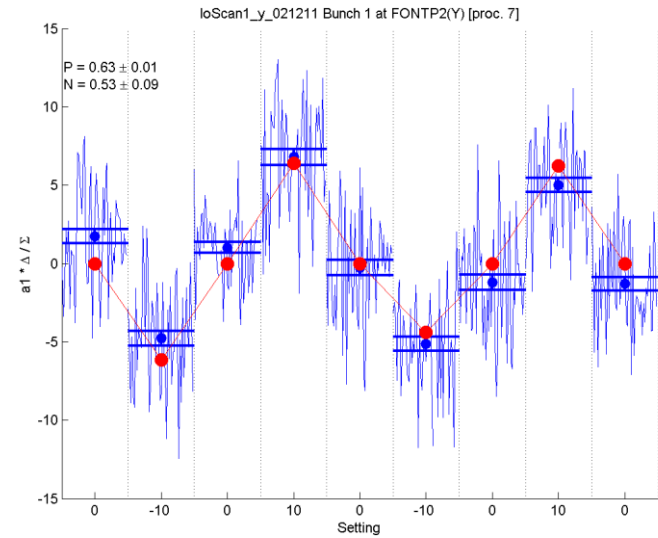
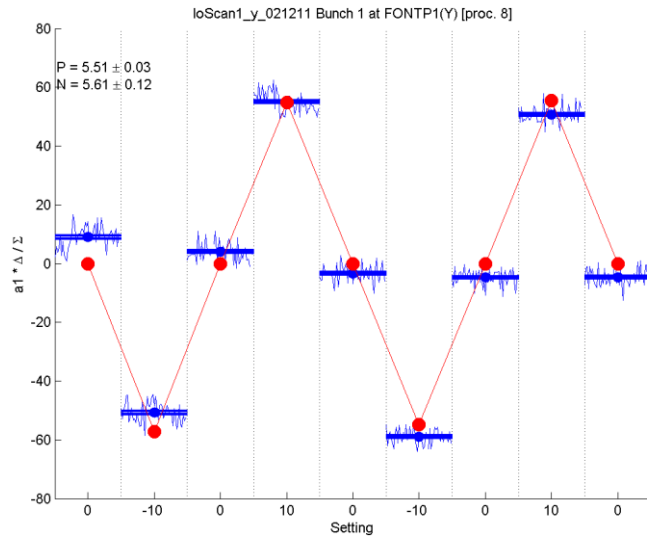
Minimum resolution based
on noise alone



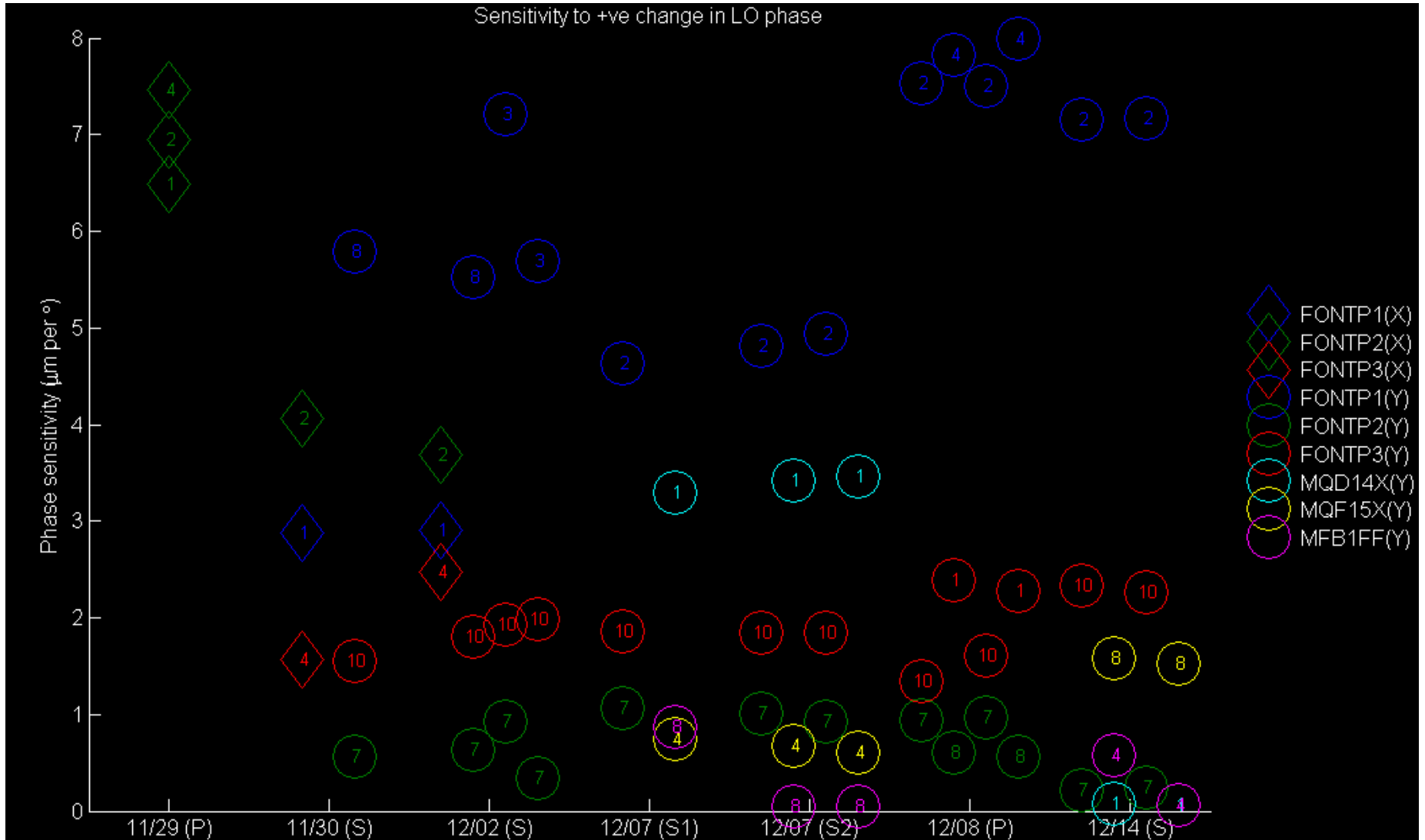
Upstream FB status

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- Focused on studying performance limitations of the system: processor noise, systematic effects of LO phase jitter wrt bunch, and understanding discrepancy between observed FB performance and expected limit:
 - Observed correction level at FB BPMs < 0.4 microns
 - Measured (apparent) resolution of BPMs: 1 – 3 microns!!
- Previously knew about differing sensitivity of FONT BPMs to phase jitter between bunch and LO (especially at P1), and strongly suspected this was limiting contribution to apparent resolution, but only earlier this year realised strong correlation between measured position jitter and LO phase jitter
 - Driven programme for early this year – trying to compensate for LO phase jitter in the feedback loop.

LO phase scans example (02/12/11)



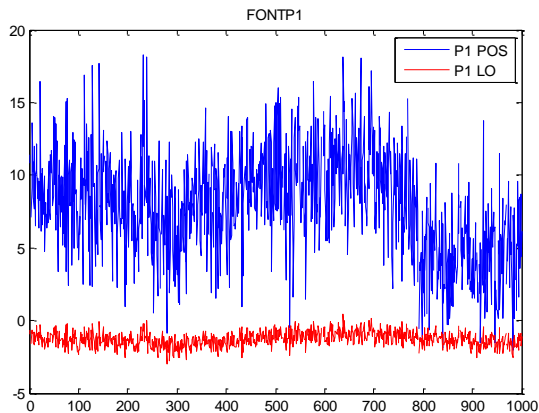
LO phase scans (Nov-Dec summary)



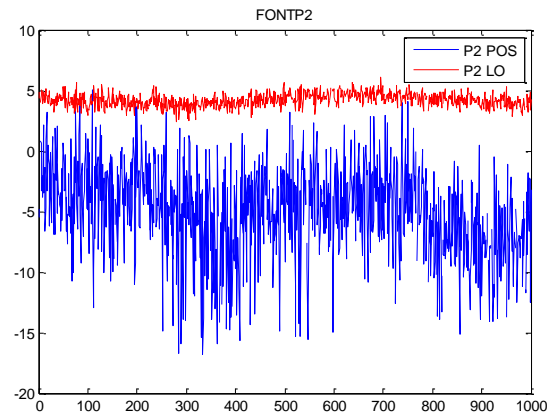
BPM/LO correlations

(1000 pulse parasitic dataset 13/12/11)

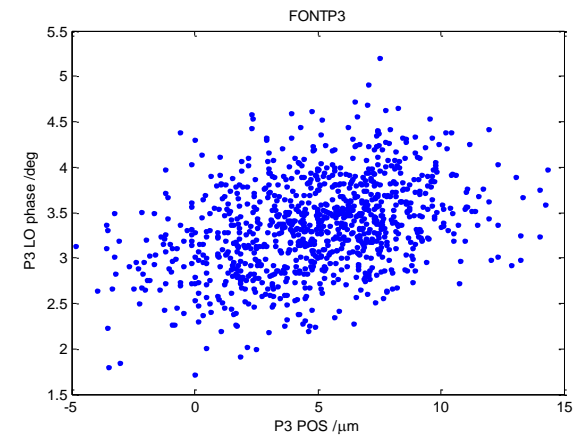
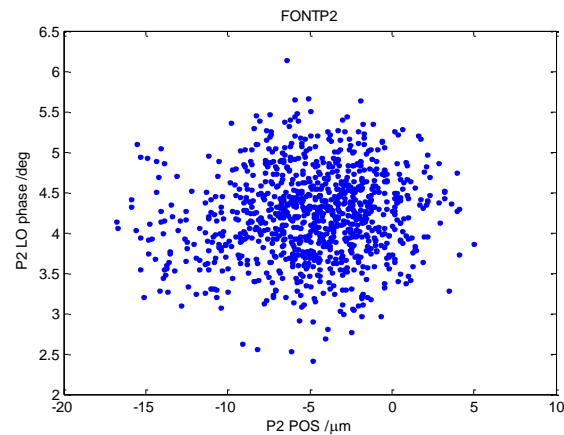
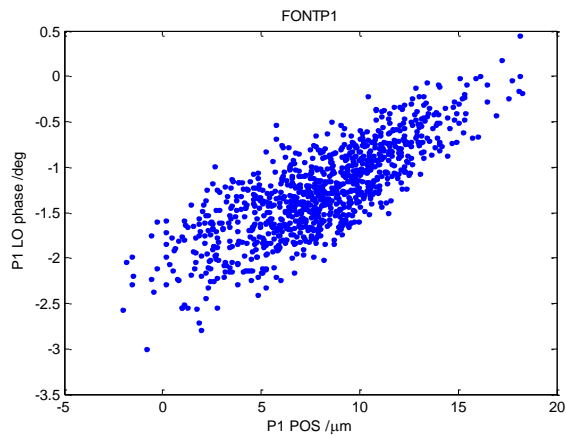
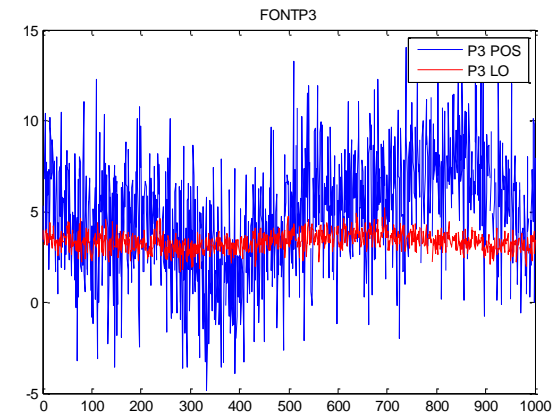
P1: $\rho=0.86$



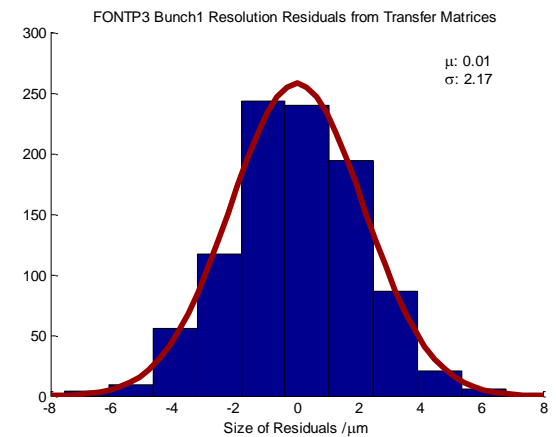
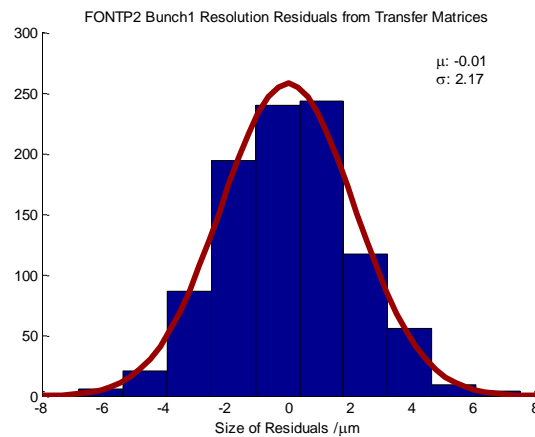
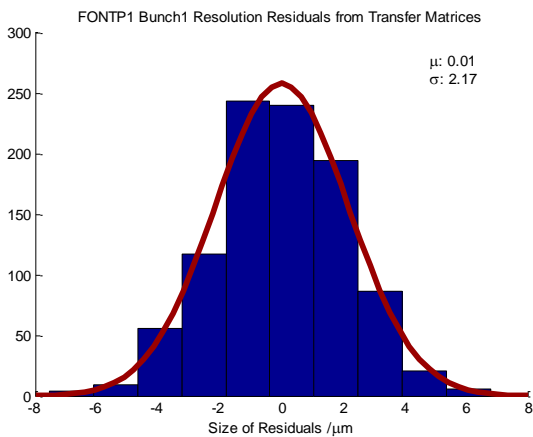
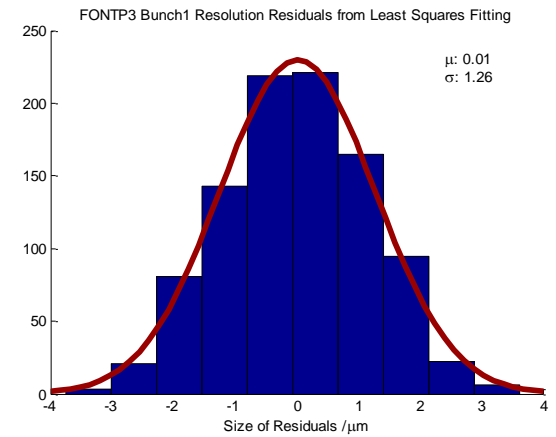
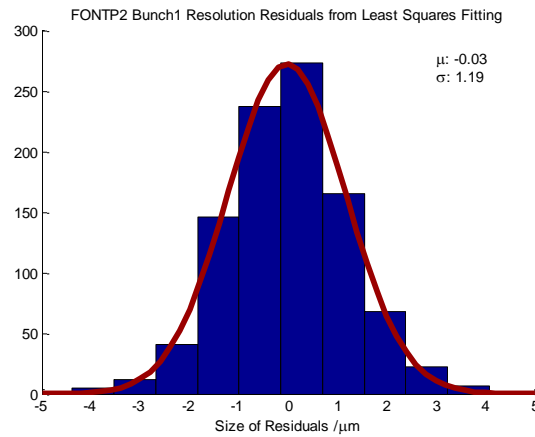
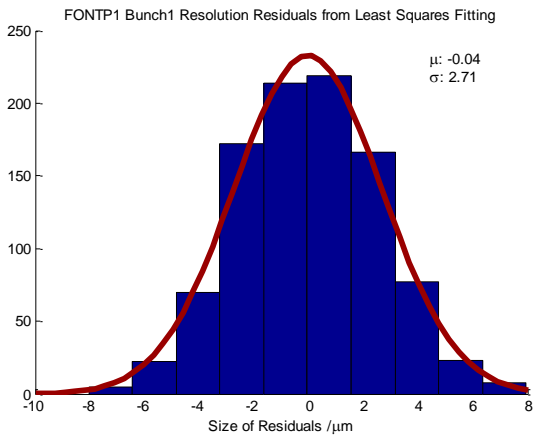
P2: $\rho=0.01$



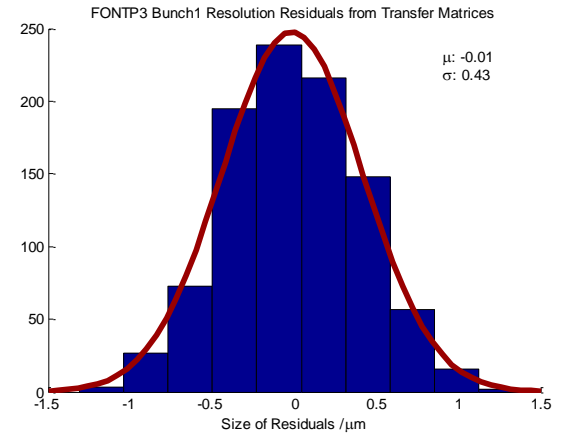
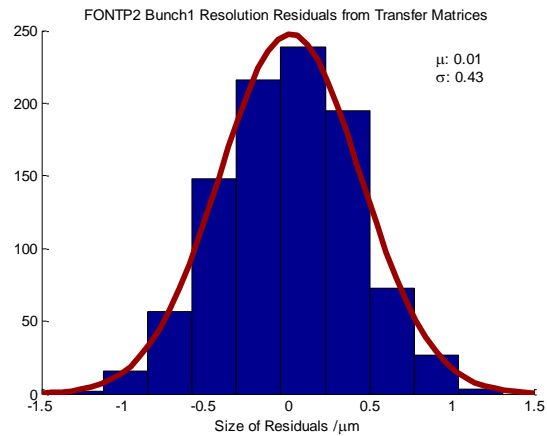
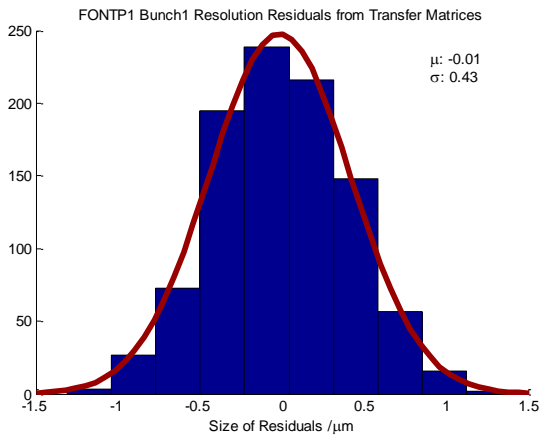
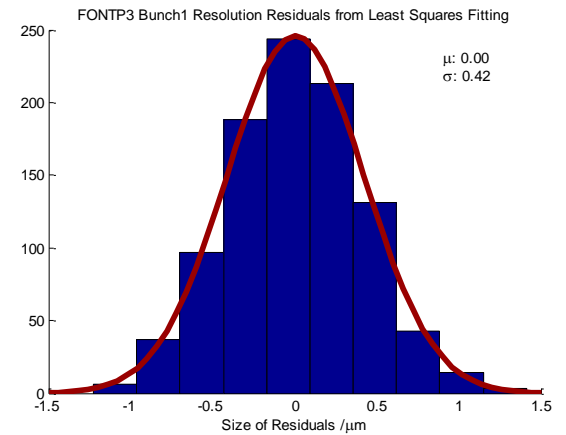
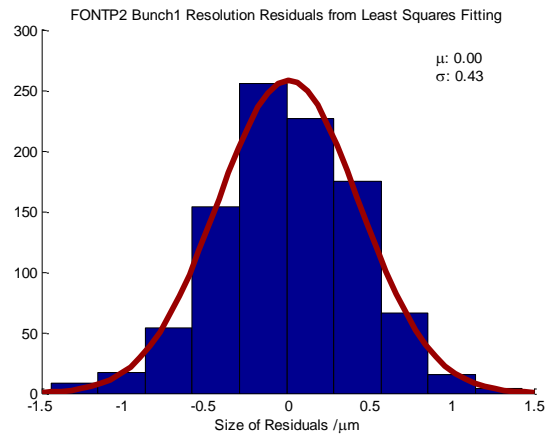
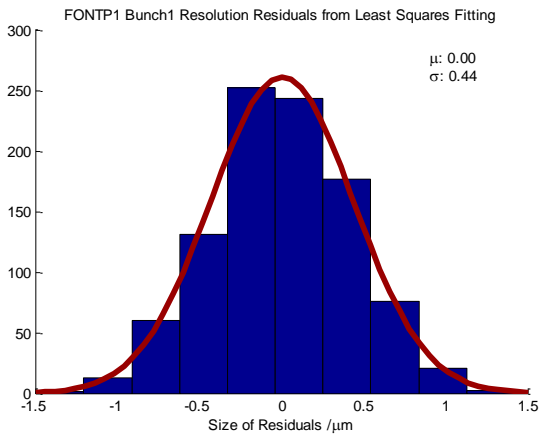
P3: $\rho=0.31$



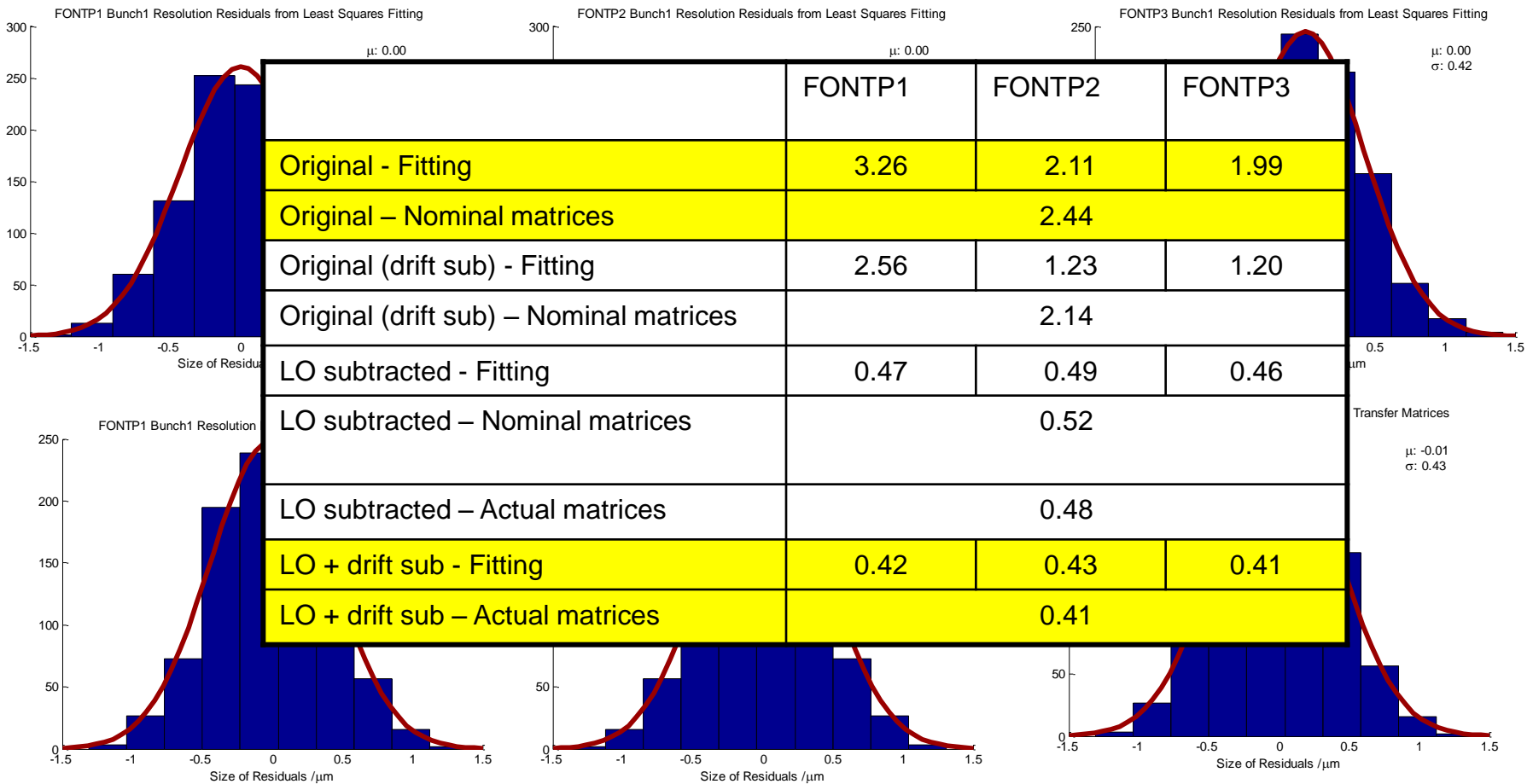
Original residuals – drift subtracted (1000 pulse parasitic dataset 13/12/11)



Resolution residuals – LO phase jitter subtracted + drift removal



Resolution residuals – LO phase jitter subtracted + drift removal

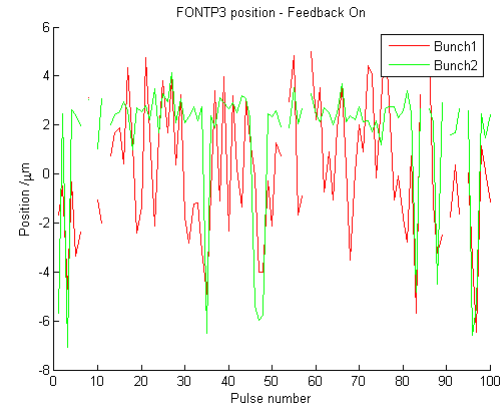
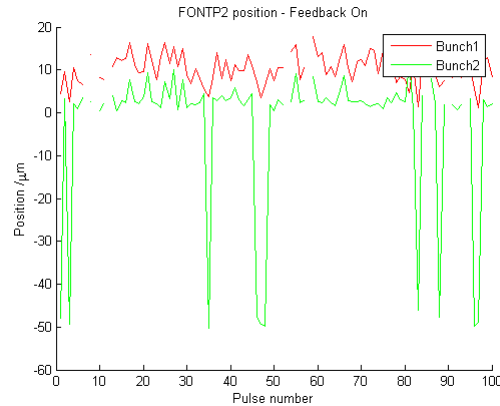
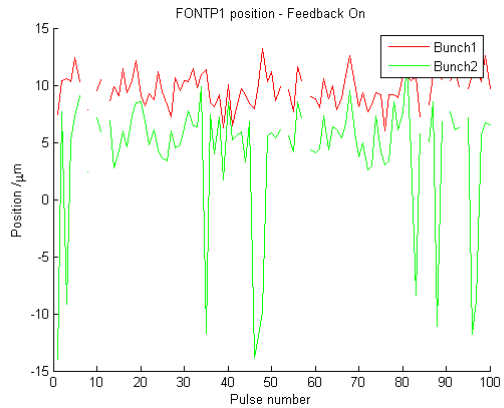


Mitigating against bunch phase jitter wrt LO

- Understand why see good correction at FB control BPMS but not witness BPMs
 - FB system will couple relative phase jitter back into the beam (e.g. synchrotron motion turns into vertical beam jitter)
- Mitigation options
 1. Remove effects (eg synchrotron motion) in DR
 - Feed-back/forward on beam in DR **Hard**
 2. Immunise against effects in DR
 - Feed-forward on the LO to track the bunch phase **Easier**
 3. Subtract the phase jitter from position data OFFLINE, and correct the feedback signal ONLINE
 - **Easiest, OFFLINE already done, ONLINE requires firmware mods**
 - **Proposed solution in first instance**

$$y = G \left(\frac{\Delta - k_{\phi} \Sigma_Q}{\Sigma_I} \right)$$

Phase jitter compensation firmware



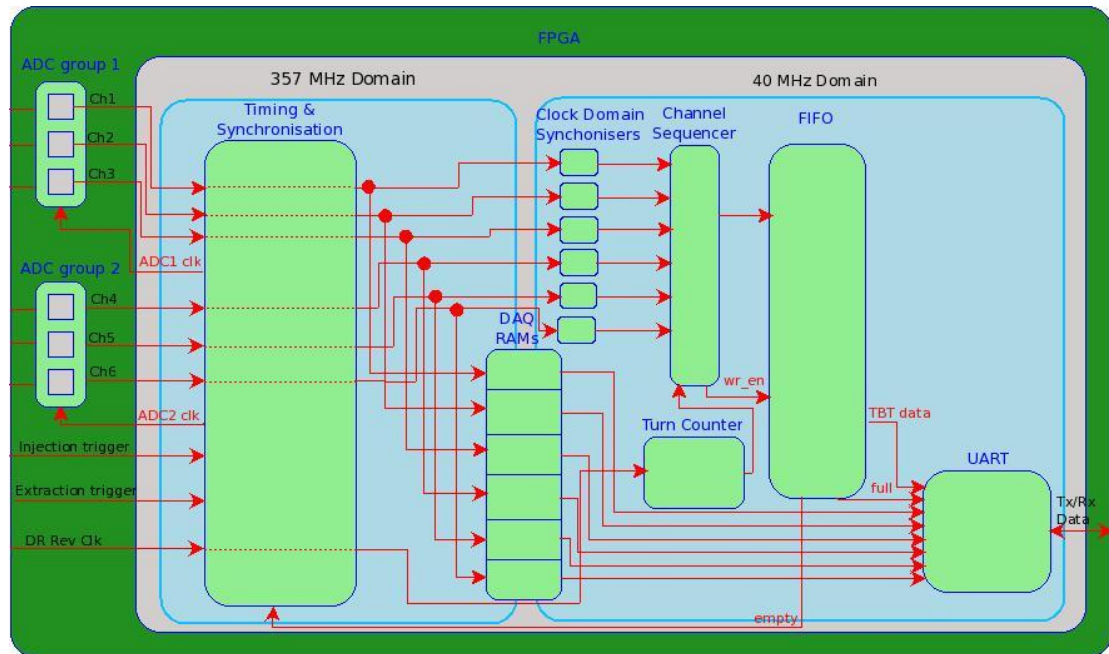
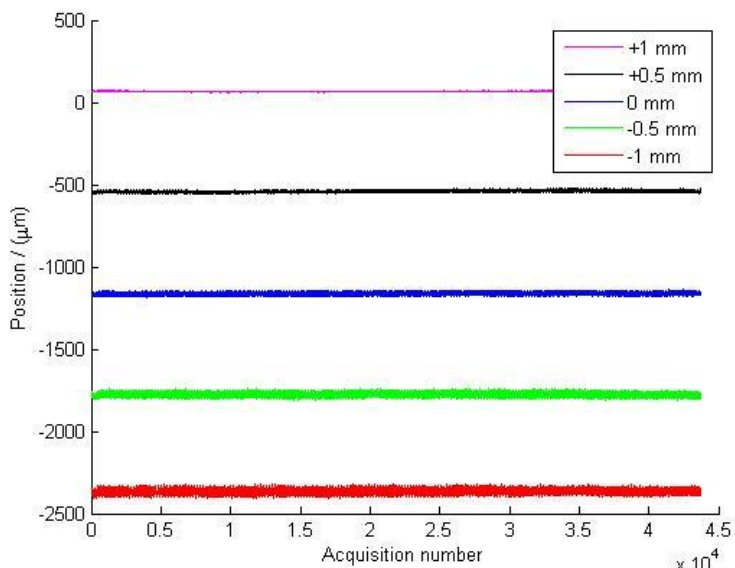
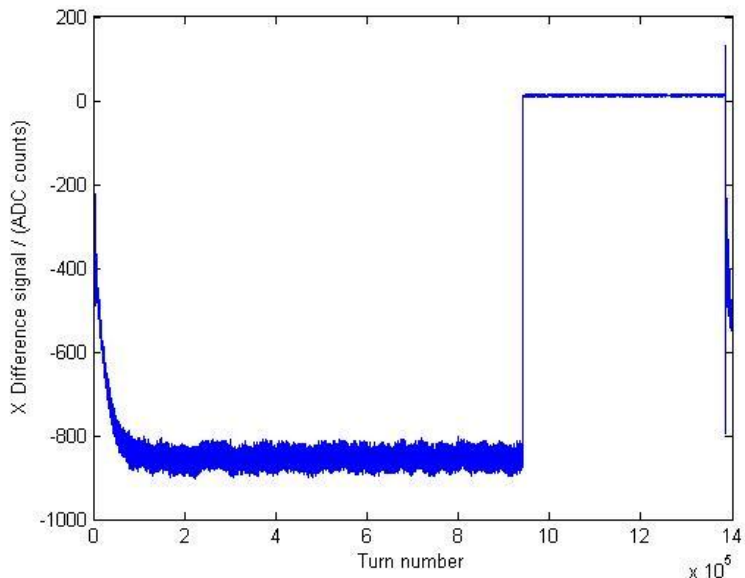
- Problem with new firmware discovered in the K1 FB loop (K2 appears to be fine!) – compounded with several other issues: amplifier failure, cable failure, DAQ problems ...
- Glitches appear to be firmware related (standard ‘non-phase compensating’ FW works fine)
- Problem needs careful debugging in lab with controlled inputs to the board.

Summary

- Feedback performance determined by three quantities: bunch-to-bunch correlation (beam), resolution (processor), and gain (system)
- Over the past year or so spent a lot of time and effort in understanding and mitigating effects limiting resolution
 - Minimising processor sensitivity to LO phase jitter – optimising the path lengths to hybrid
 - Reducing ADC noise pickup – timing jitter on ADC clocks
 - Removing BPM sensitivity to phase jitter
 - Now see very good resolution ~400 nm, in all BPMs, and perfect agreement between machine model and fitting beam trajectory
- Feedback – goal has been to reproduce excellent correction previously seen in P2 at P3 also, and maintain this correct downstream
 - Very good results obtained for P2,P3 (down to ~500-600 nm) correction factor 3-5 , but in general not preserved at witness BPMs
 - Should be able to see better downstream corrections from the removing the phase sensitivity of the BPMs in the feedback correction.
 - Firmware with phase jitter compensation in the FB been tested, but showed glitching in one FB loop – needs thorough testing in lab.

Spare

ATF Damping Ring Multi-bunch Diagnostics

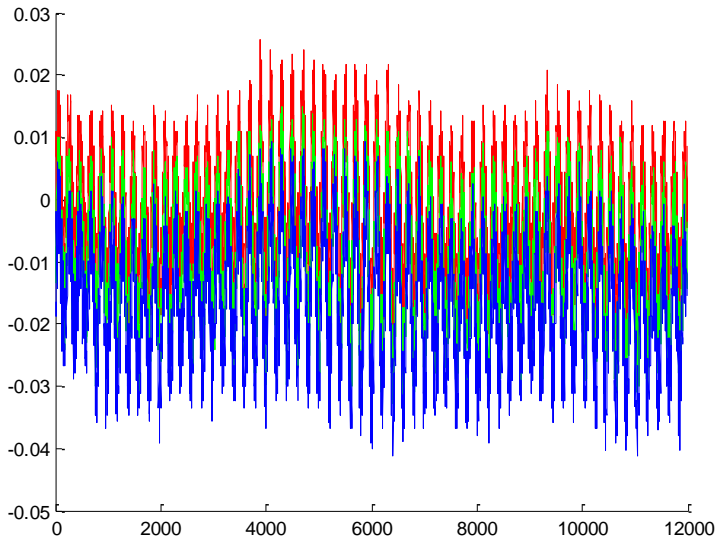


Modified feedback hardware for multi-bunch turn-by-turn DAQ from ATF damping ring

- Up to 3 bunches, 3 channels, from up to 2 BPMs
- Records 131,071 samples per pulse (up to 15% of damping period for single bunch, single channel)
- Can record n-turns-in-m to vary time window and resolution

Bunch phase oscillations at extraction wrt LO

SumQ/SumI – ‘raw’ data



3 distinct frequencies:

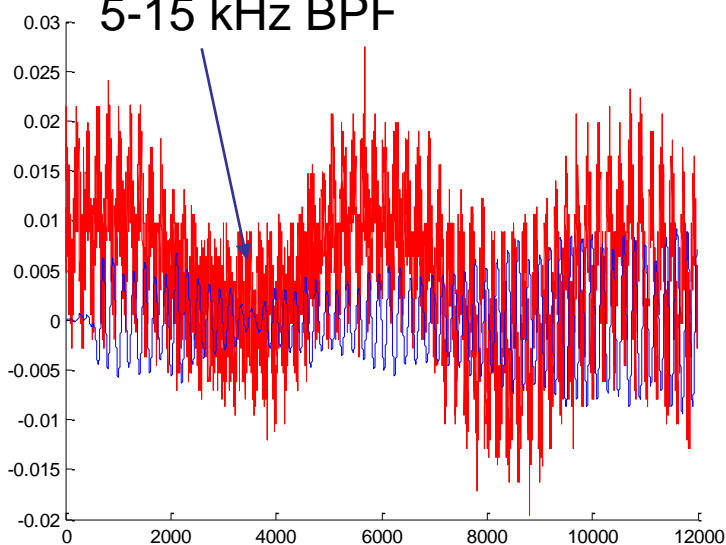
10.8 kHz – synchrotron

434 Hz slow oscillation (unknown)?

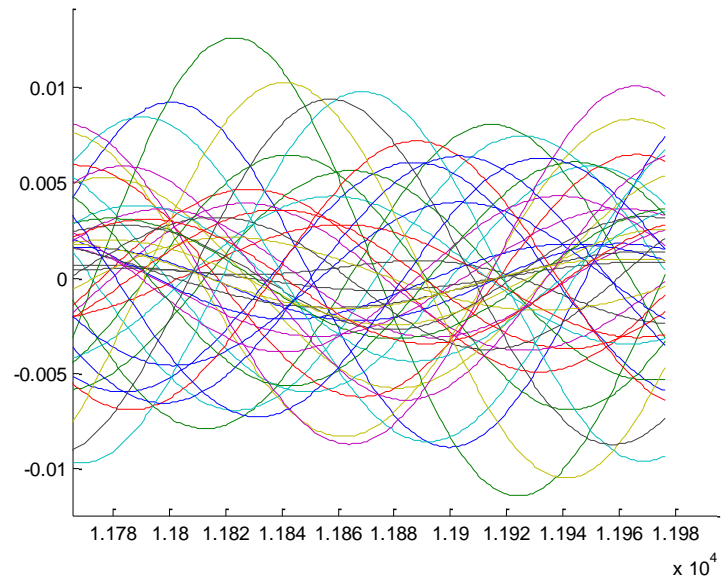
735 kHz fast oscillation – aliased?

Last 200 turns before extraction

5-15 kHz BPF



All pulses : Bunch 3



BPM processor resolution and FB performance limitations

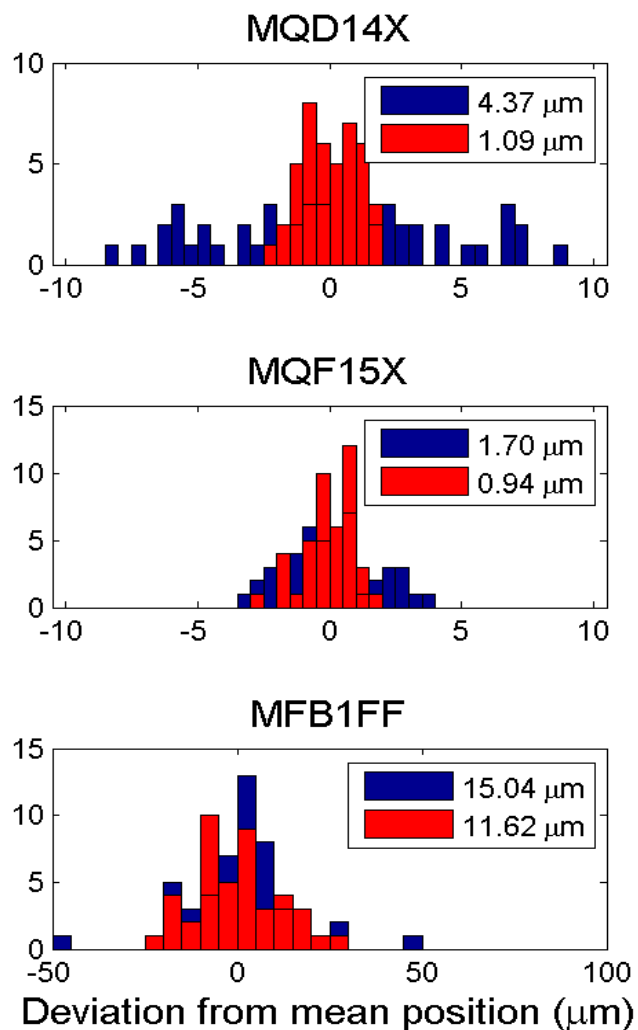
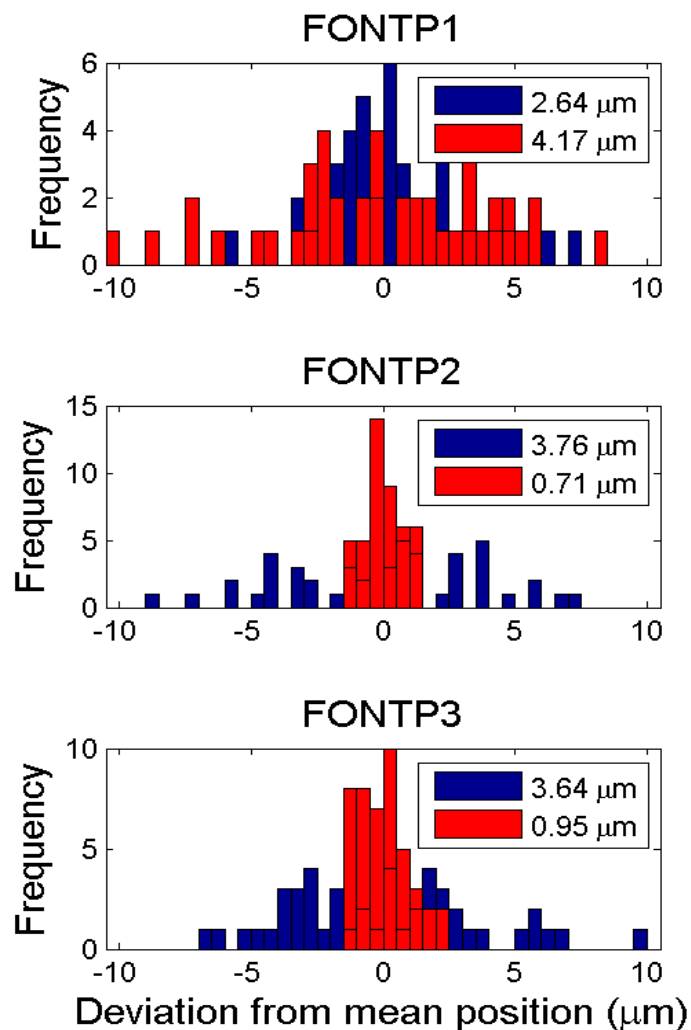
- Standard 3-BPM resolution method gives 'average' resolutions of 1 – 2 micron across 3-BPM system, however FB system performance in P2-K1 loop show ~300 nm.
 - Believe we were lucky with processor at P2, and that all processors have different resolutions due to different sensitivity to LO jitter
 - Largest effect due to path length imbalance to hybrid (unique for each processor) – larger residual from subtraction, more susceptible to LO jitter
 - All processors optimised, to be tested in Autumn
- Even if resolution 'perfect', system performance still determined by beam jitter conditions
 - Measured bunch-to-bunch correlations of >94% needed to make useful correction on ~3 micron beam jitter (50 % needed to break even)
 - Bunch 3 assumed to be on edge of ~310 ns EXT kicker pulse

Processor Improvements (2011)

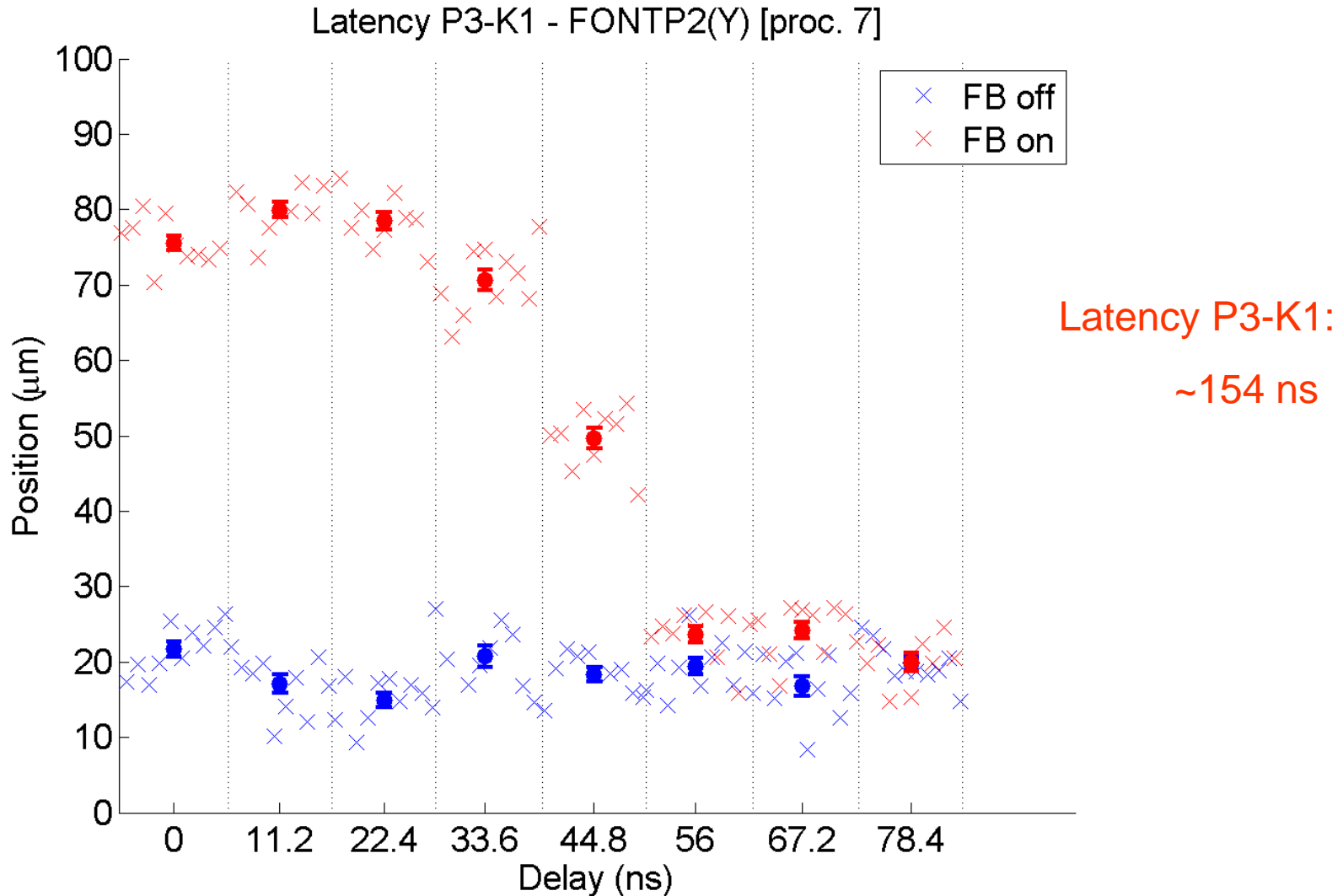
- Hypothesis that discrepancy between FB results and resolution due to sensitivity of measured position to LO phase jitter
 - All processors/BPMs exhibit different sensitivity to LO jitter wrt beam. (P2 just happens to be least sensitive.)
 - Effects cancel for measurements using just one BPM, for example FB, whereas measurements involving correlating positions across several BPM, appear to have poor resolution.
 - Largest effect due to path length imbalance to hybrid (unique for each processor) – larger residual from subtraction, more susceptible to LO jitter
- All processors optimised (summer 2011)
 - Input cables optimised for matched path length at hybrid
 - Sum loopback cables re-made to phase sum and difference channels
- Also, discovered and fixed problem with sampling jitter caused by noise pickup on ADC clocks from FPGA (affected correlated measurements across more than one BPM, hence contributed to effective resolution)

Feedback examples (14 Dec 2011)

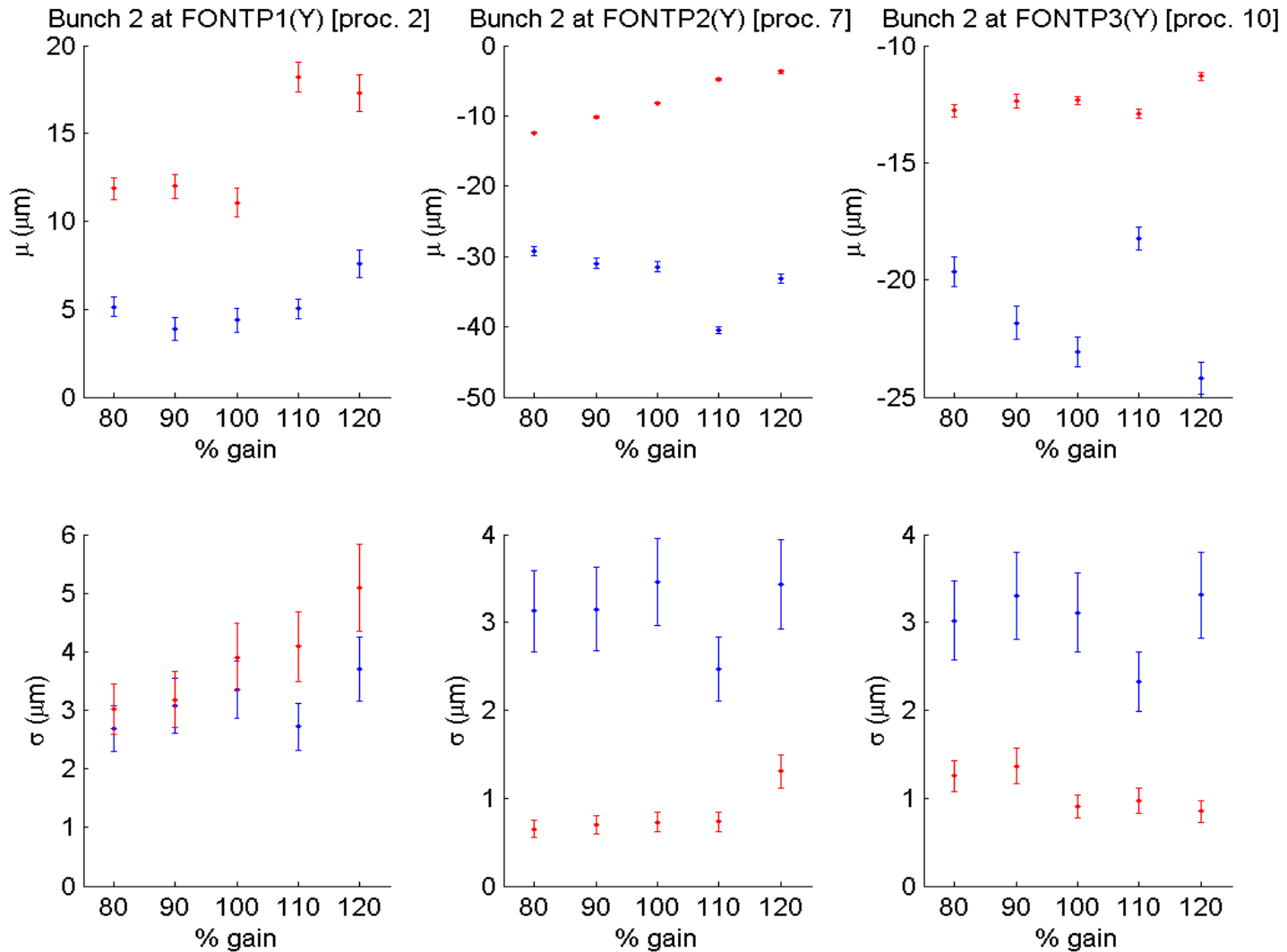
Run5_141211



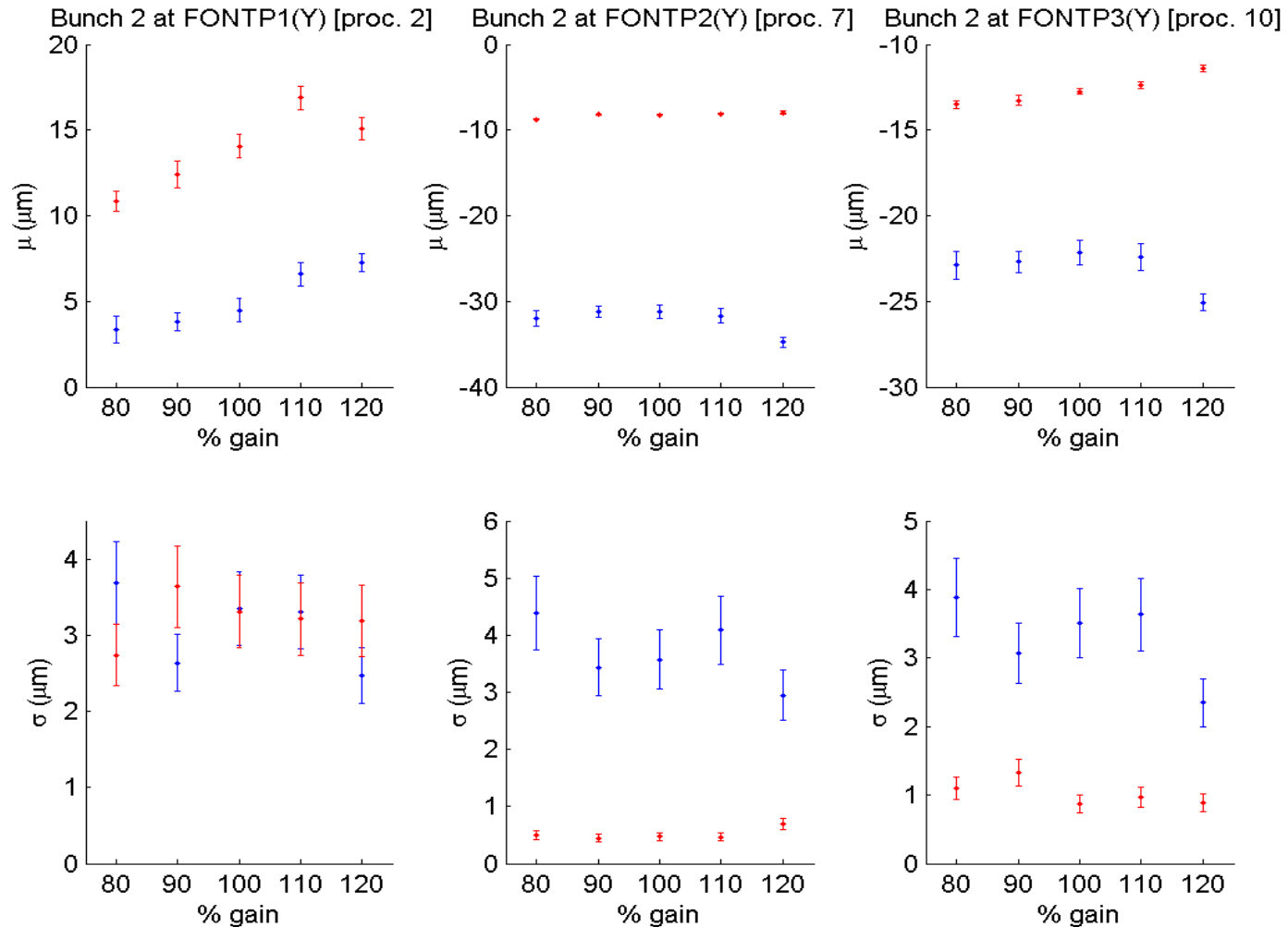
Latency (Dec 2011) – not-optimised



Kicker K1 gain scan (14/12/11)



Kicker K2 gain scan (14/12/11)



Original residuals

(1000 pulse parasitic dataset 13/12/11)

