R&D on sensors and readout for the CLIC vertex detector

European Linear Collider Workshop ECFA 2013

27-31 May 2013, DESY, Hamburg

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on behalf of the CLIC Detector and Physics Study

Outline

- CLIC Vertex detector layout and requirements
- Timepix: simulation, digitisation, measurements
- CLICpix readout ASIC development
- Medipix3 TSV project
- Sensor production and measurements
- Summary

CLIC Machine environment

Beam pattern

20 ms

312 BX

156 ns

- 156 ns bunch trains, 20 ms gaps
  → trigger-less readout, power-pulsing
- Large background in vertex and forward regions:
  - 2-3% maximum pixel occupancy / train (incl. clustering + safety factors)

  -> Time stamping with ~10 ns accuracy, to reject background

- Moderate radiation exposure:
  - NIEL: < 10^{11} $n_{eq}/cm^2/y$
  - TID: < 200 Gy / year

  (~10^4 below LHC!)

1 metre

FTD

VXEC

VXB

SIT 2

SIT 1

Beryllium beam pipe

Steel beam pipe

Vertex detector requirements

→ Good single point resolution: $\sigma_{SP} \sim 3$ µm
  → Small pixels ~ 25x25 µm^2

→ Low material budget: X ≲ 0.2% X_0 / layer
  → Corresponds to ~200 µm Si
  → Air-flow cooling + Low-power ASICs (~50 mW/cm^2)

- No technology option available fulfilling simultaneously all requirements:

  [See talk by P. Roloff]
  → Simulation studies: impact of layout on performance
  → R&D on sensors & readout
  → Integration/assembly + cooling + power-pulsing studies
  [See talk by F. Duarte Ramos] [See talk by C. Fuentes]

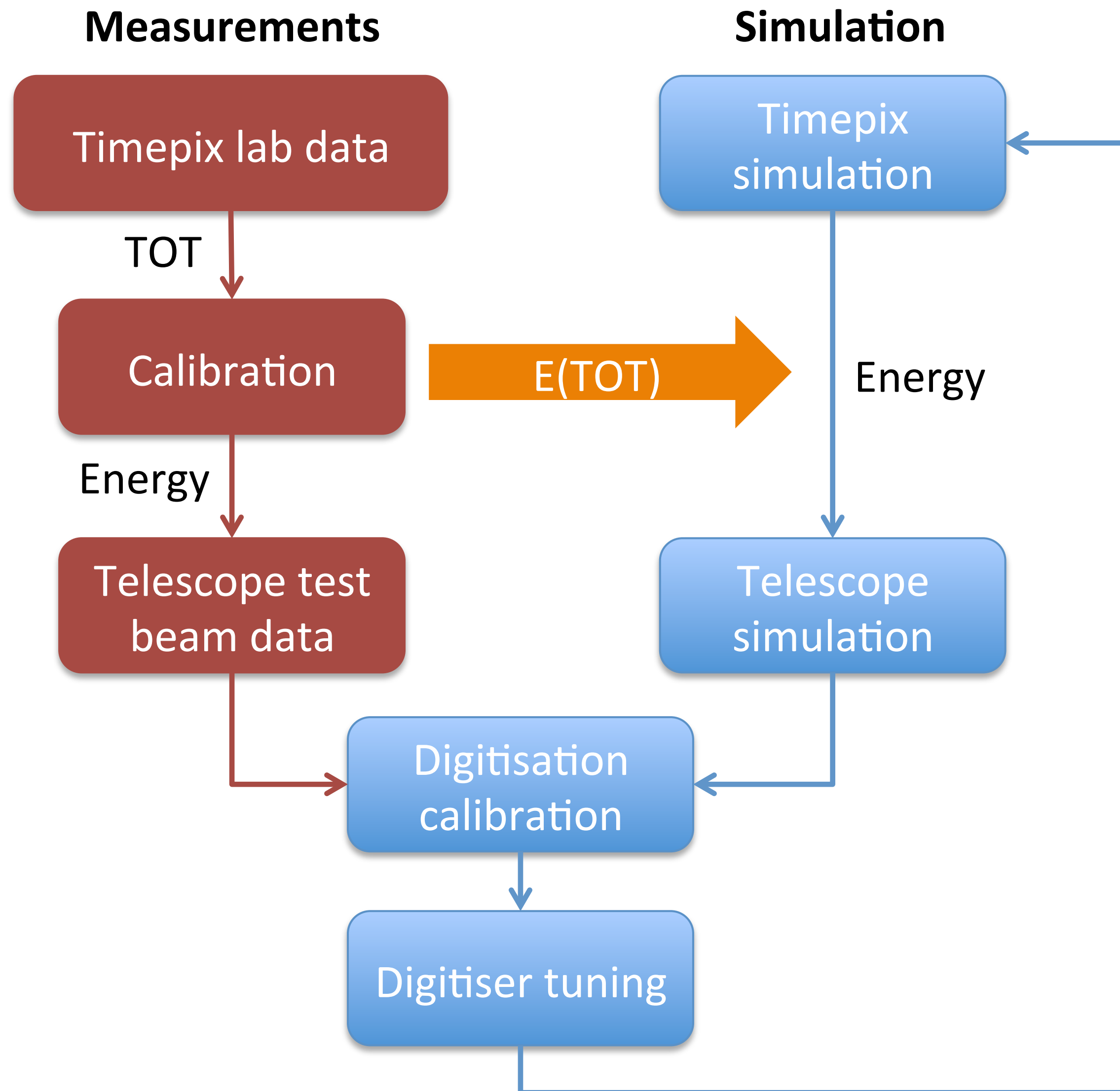
Medipix/Timepix hybrid ASICs family

Chip	Year	Process	Pitch [μm²]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm	55x55	∫TOT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm	55x55	γ counting	Sequential (full frame)	Medical
Timepix3	2013	130 nm	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
Smallpix	2013	130 nm	~40x40	TOT + ToA, γ counting + ∫TOT	Sequential (data comp.)	HEP, Medical
CLICpix demonstrator	2013	65 nm	25x25	TOT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
CLICpix	tbd	65 nm	25x25	TOT + ToA	Sequential (data comp.)	CLIC vertex detector

TOT: Time-Over-Threshold → Energy
ToA: Time-of-Arrival → Time stamping

- Taking advantage of smaller feature sizes:
  - Improved noise performance
  - Increased functionality and/or
  - Reduced pixel size

Calibration and simulation tuning



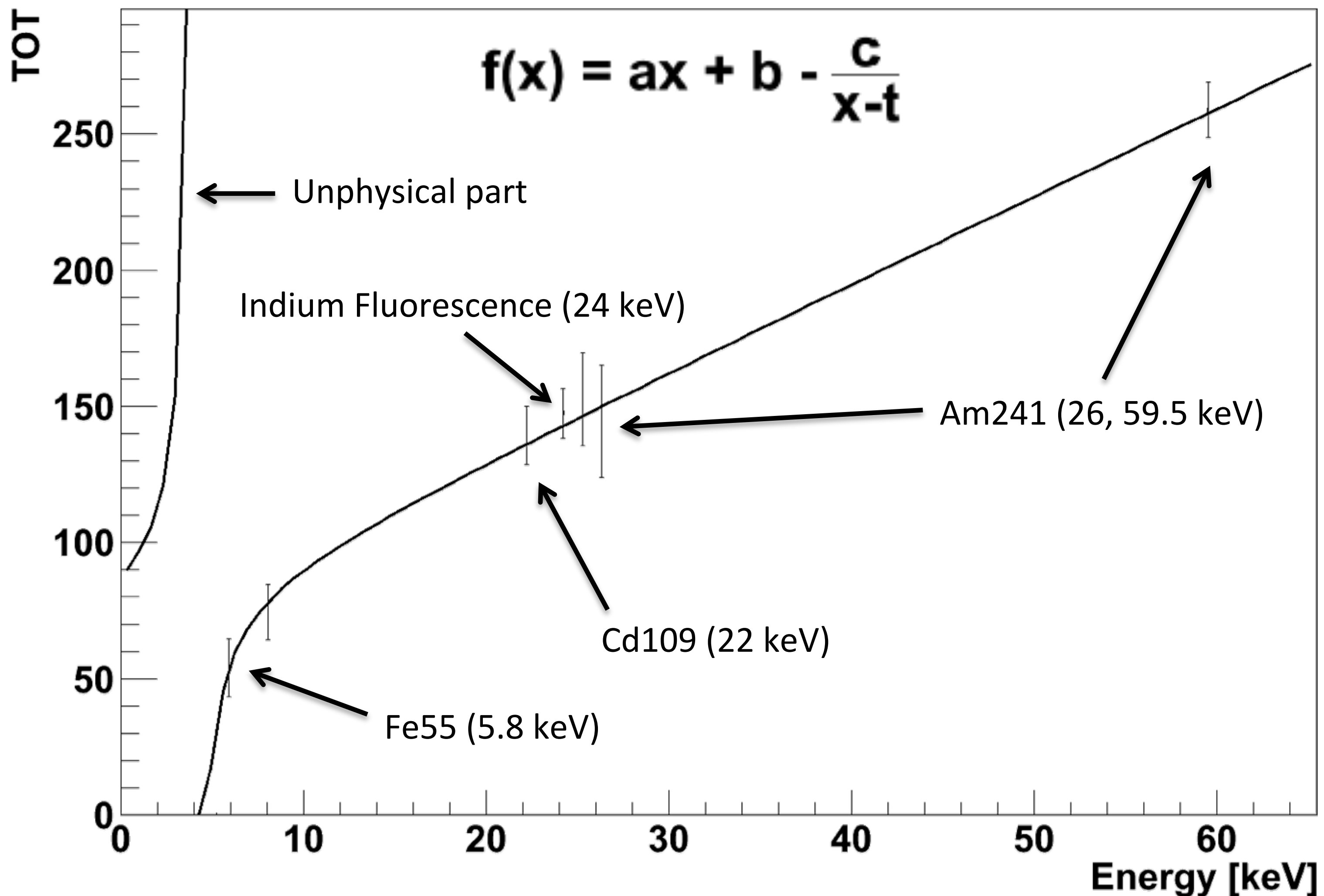
Timepix calibration and digitisation tuning

Calibration of Pixel detector plays an important role for:

- Tuning of digitization model
  - E vs. TOT relation is non-linear
  - Simulation output is in Energy (Geant4 deposits)
- Optimise tracking resolution
  - Energy weighting improves reconstruction of hit position in multi-pixel clusters
- Calibration method procedure:
  - Acquire TOT spectra for each pixel with reference energy deposits (e.g. radioactive sources, fluorescences)
  - Determine peak TOT for each energy and pixel
  - Fit the preamplifier characteristic response function to data (4 parameters)
  - Use fitted parameters to translate TOT to energy, pixel-by-pixel

Timepix calibration and digitisation tuning

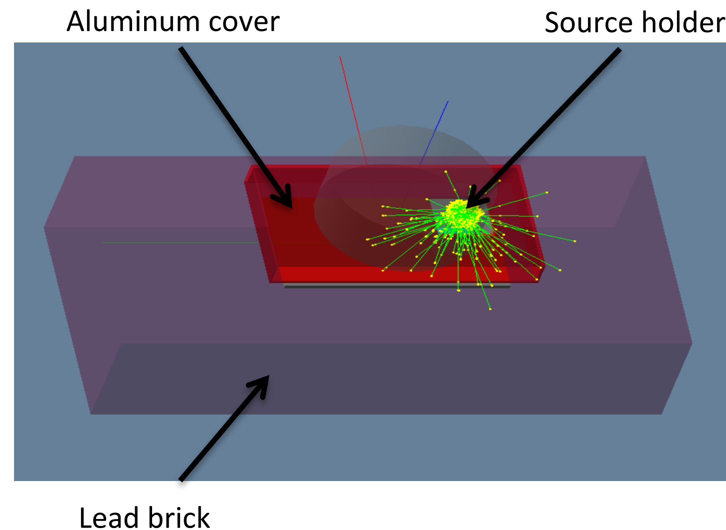
Experimental TOT(E) for one pixel, i.e. « Surrogate function »

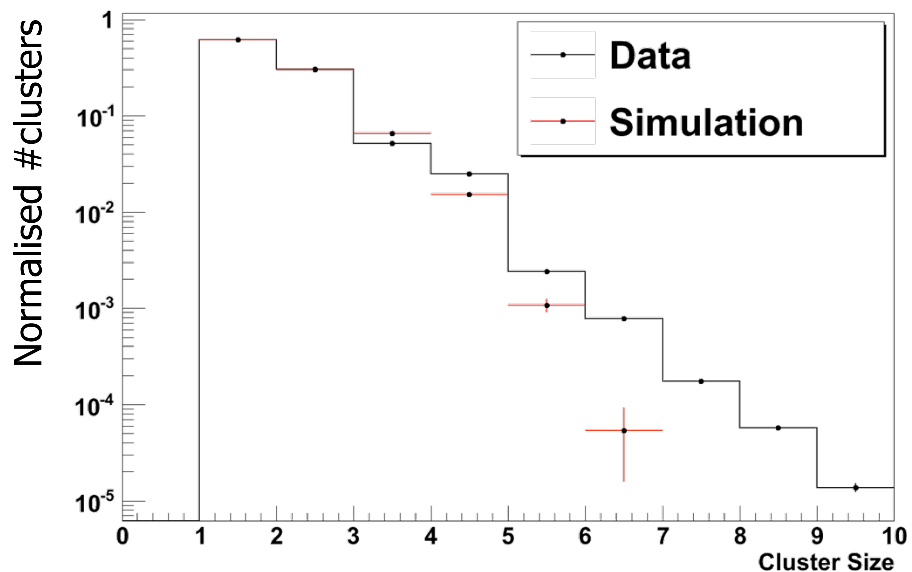


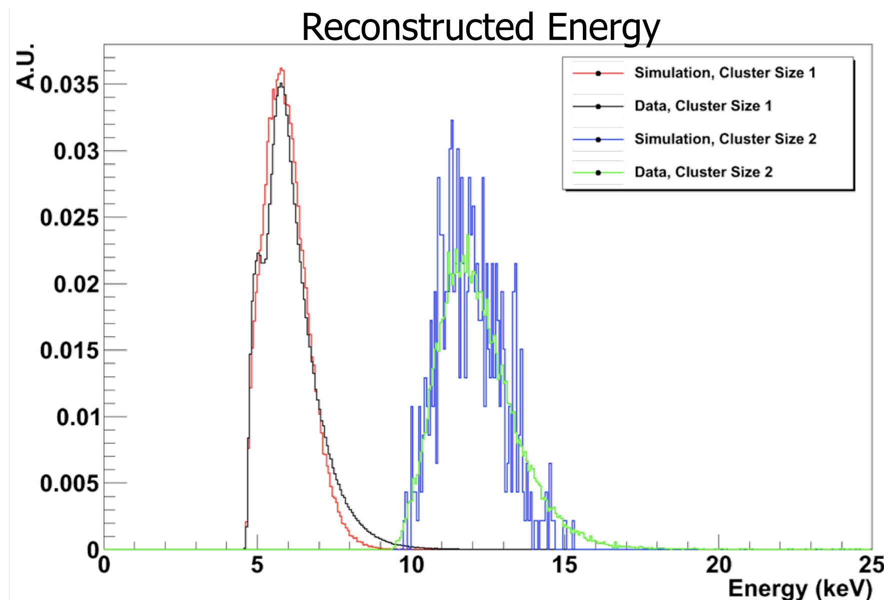
Timepix calibration and digitisation tuning

Experimental data were compared to Geant4 simulation of the setup

- To calibrate the simulation using the ballistic model we need to include Chip effect on the measurement (noise, crosstalk)
- Tuning digitisation to reproduce Cluster Size distribution and Energy Resolution of the Timepix sensor



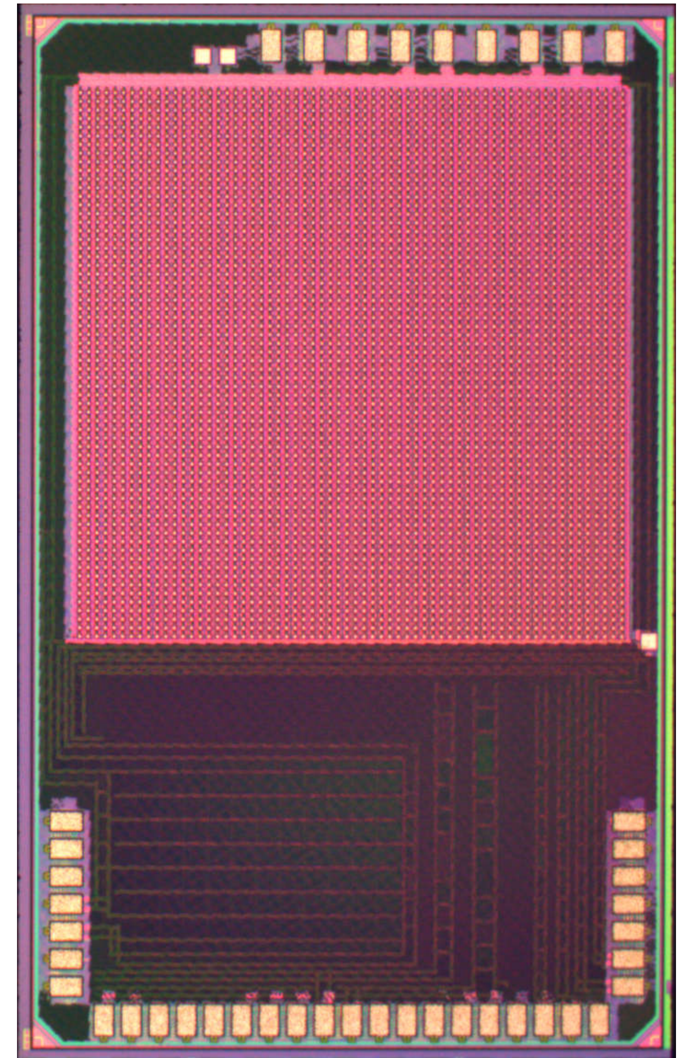




CLICpix demonstrator chip

- Demonstrator chip designed with fully functional 64x64 pixel matrix
  - 65 nm CMOS technology
  - Small pixel pitch (25 x 25 μm^2)
  - Simultaneous 4-bit TOA and TOT per pixel
  - Front-end time slicing < 10 ns
  - P_{analog} ~ 2 W/cm^2 (peak)
    - power-pulsing → P_{avg} < 50 mW/cm^2

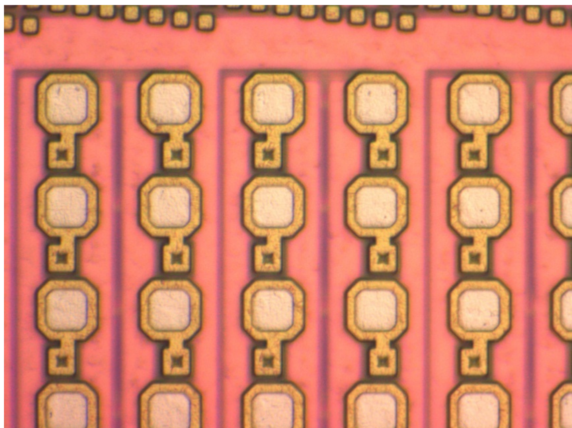
- Submission November 2012 in Multi-Project Wafer run
  - 100 chips delivered in February 2013



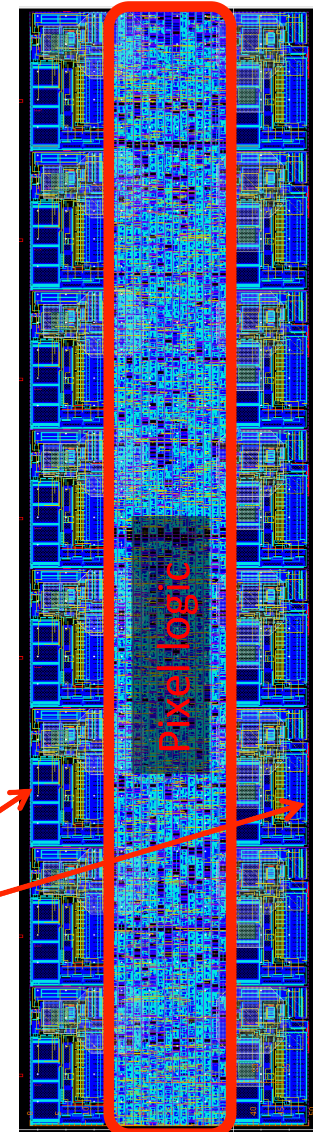
Chip photograph

CLICpix demonstrator pixels

- Pixel analog part contains
  - Single-ended preamplifier with ~30 ns rise time
  - Fast discriminator (<5 ns delay)
  - 4-bit threshold adjustment DAC
- Digital part is shared among 16 adjacent pixels
  - One 4-bit TOA and TOT counter per pixel
  - Clock distribution tree
  - Selectable Zero-Compression logic

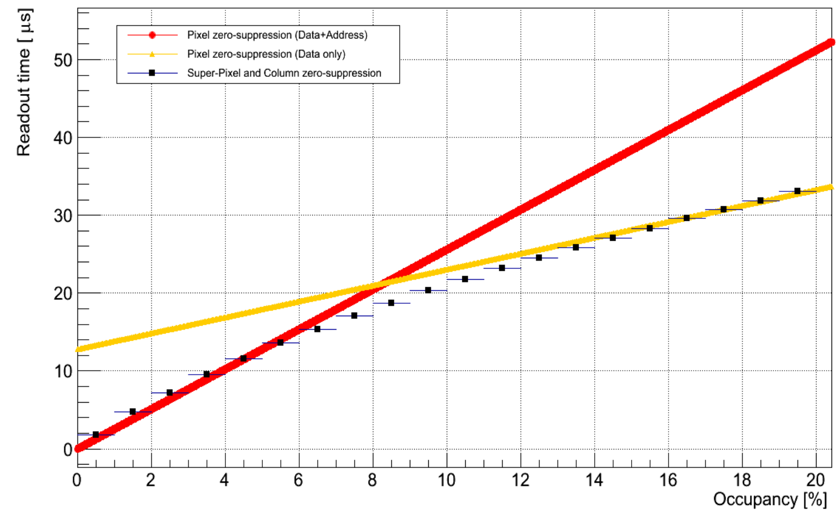


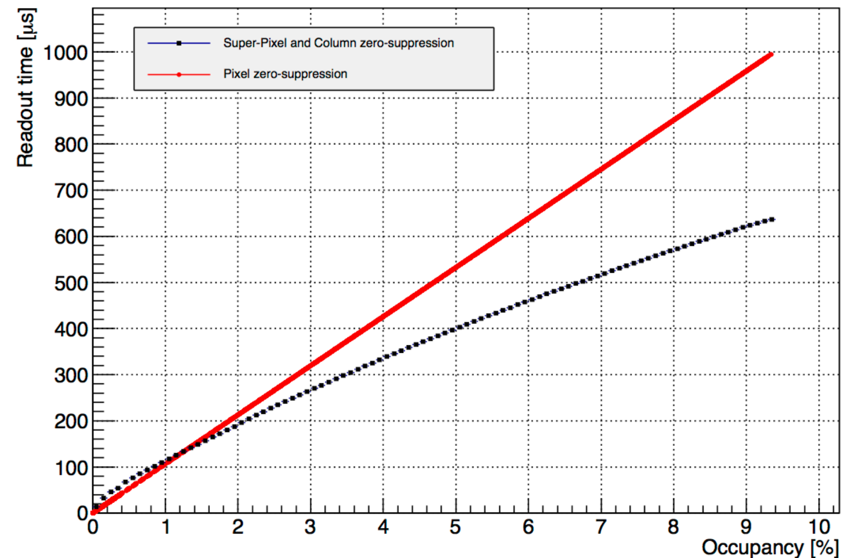
Analog pixels



CLICpix data compression

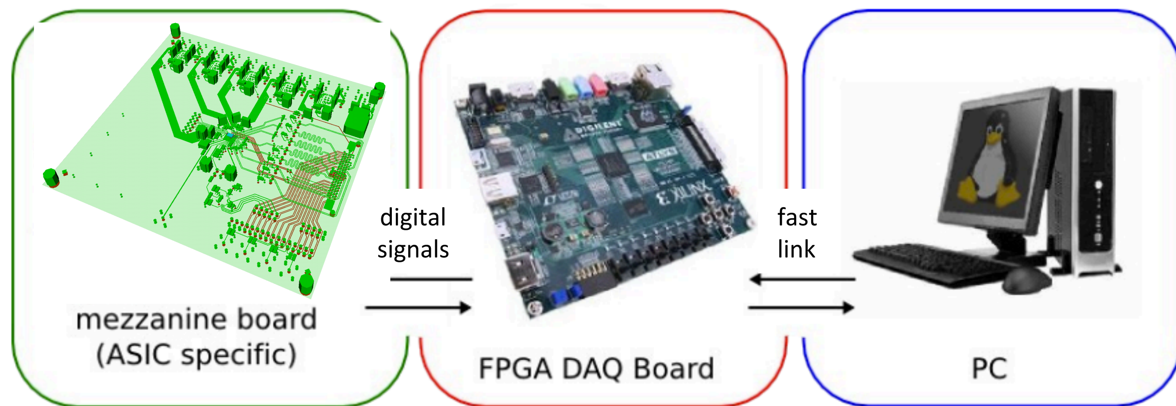
- 20ms hard limit on ladder readout time
  - the faster a chip is read out, the lower the power consumption will be
- Geant4 simulations under CLIC conditions to estimate CLICpix chip readout time versus occupancy for various compression schemes
- 8 bits of data per pixel (TOT+TOA)
- 640 Mbits/sec
  - 320 MHz clock using Double Data Rate
- Zero-suppression (red line)
- Zero-compression with pixel, superpixel, and column skipping (black dots)
- Data compression schemes are implemented on the chip and selectable to best suit each region of the vertex detector

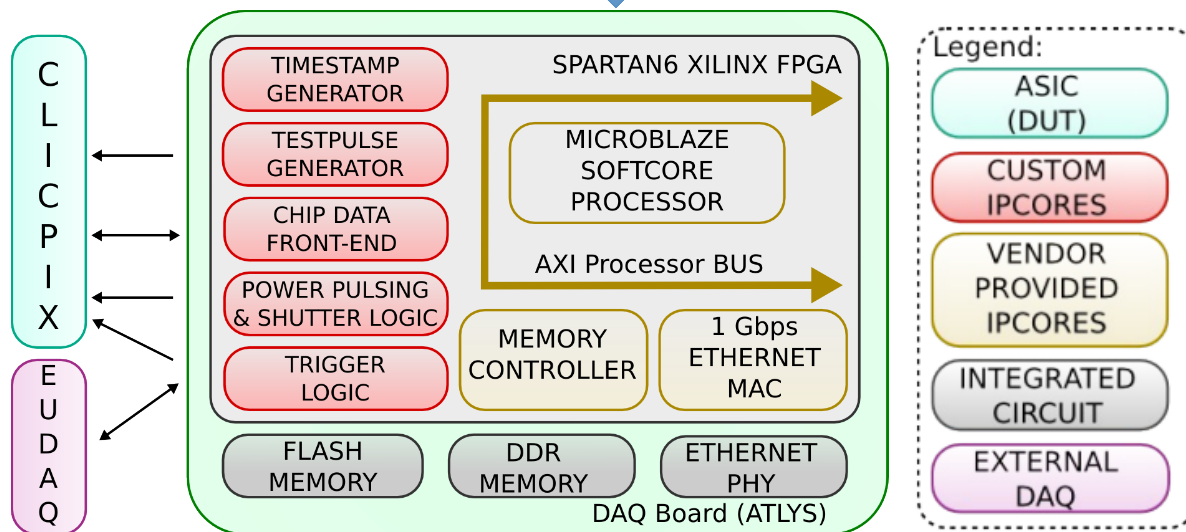




CLICpix Readout

<u>Architecture being developed at CERN</u>



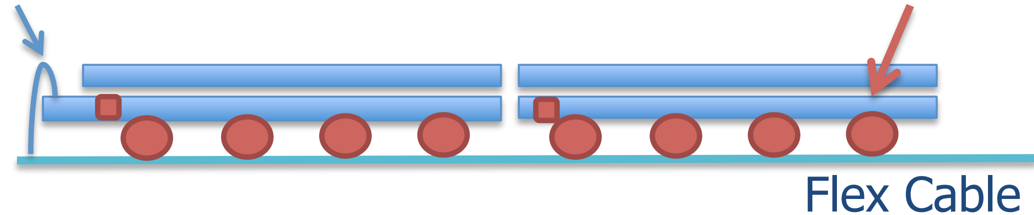


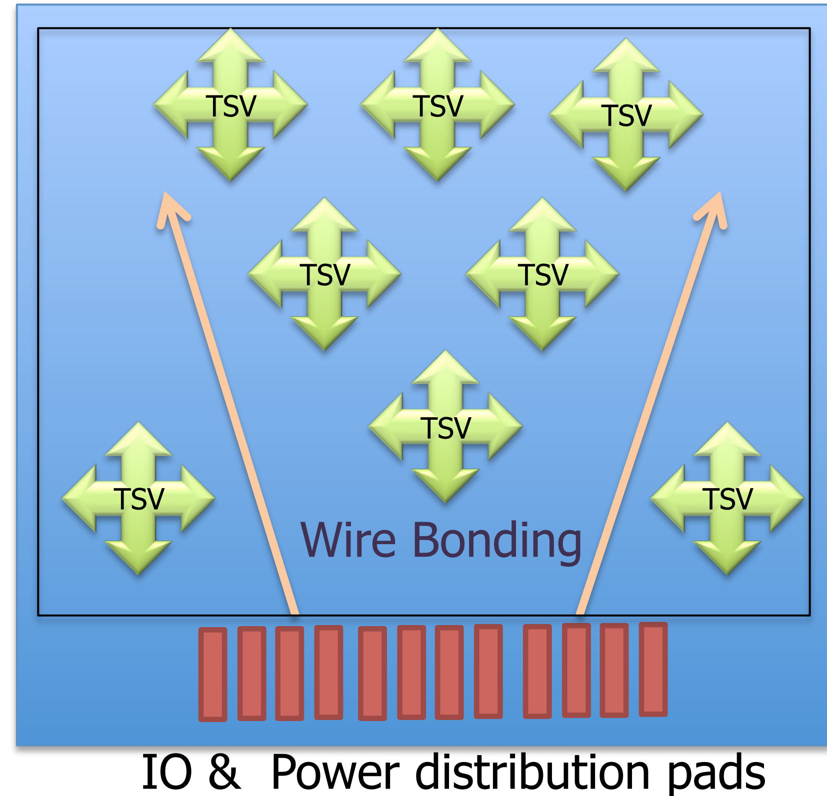
- Spartan 6 based DAQ system
- Modular architecture (HW/FW/SW)
- 1 Gbps Ethernet interface
- Compatible with EUTelescope infrastructure
- Support for all ASIC features such as power pulsing and fast readout

Status:
- ASIC PCB submitted to production
- FPGA firmware advanced

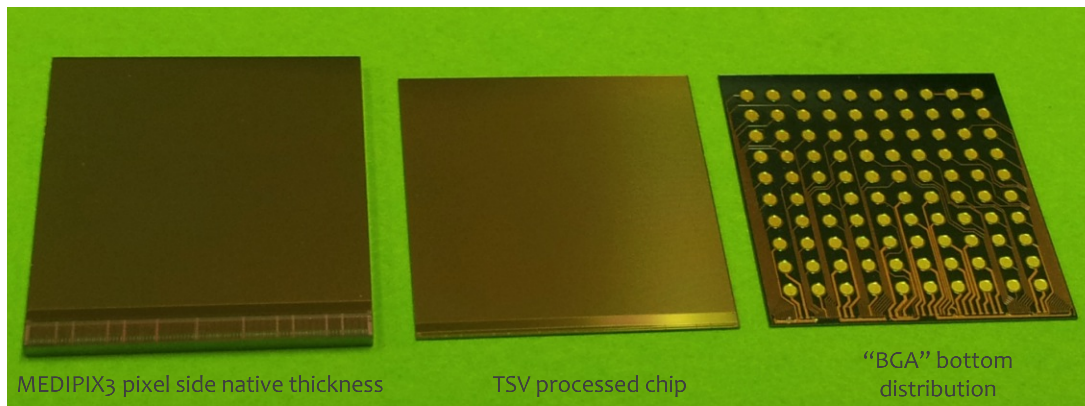
Medipix3 TSV project

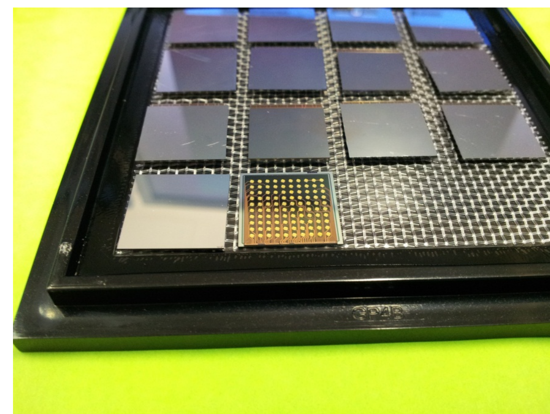
- Through Silicon Via (TSV) is a vertical electrical connection passing through a silicon wafer eliminating the need for wirebonds
- Ratio between active area and total area is increased by removing wirebonding pads
  - 4-side buttable
- No wire-bonding: High reliability
- Via-last TSV project with 10 Medipix3 wafers (130 nm) at CEA-LETI Grenoble



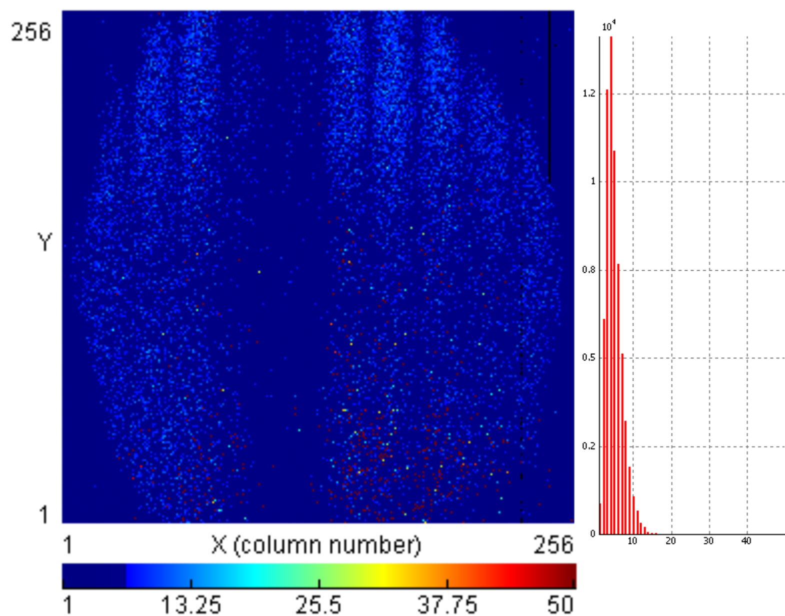


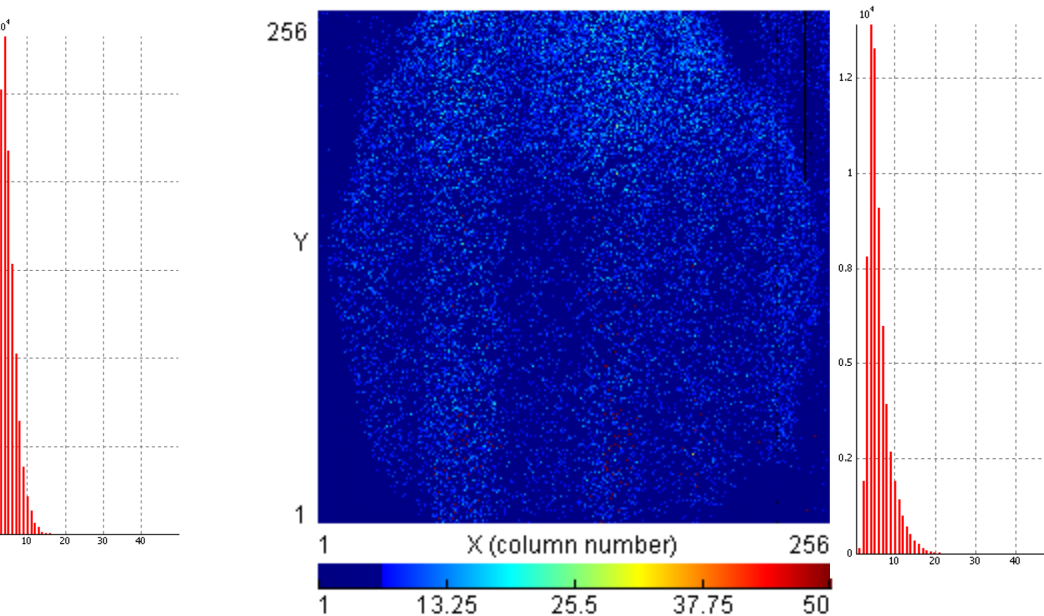
Medipix3 TSV project: results





Example noise floor measurement: no significant increase in noise after TSV processing





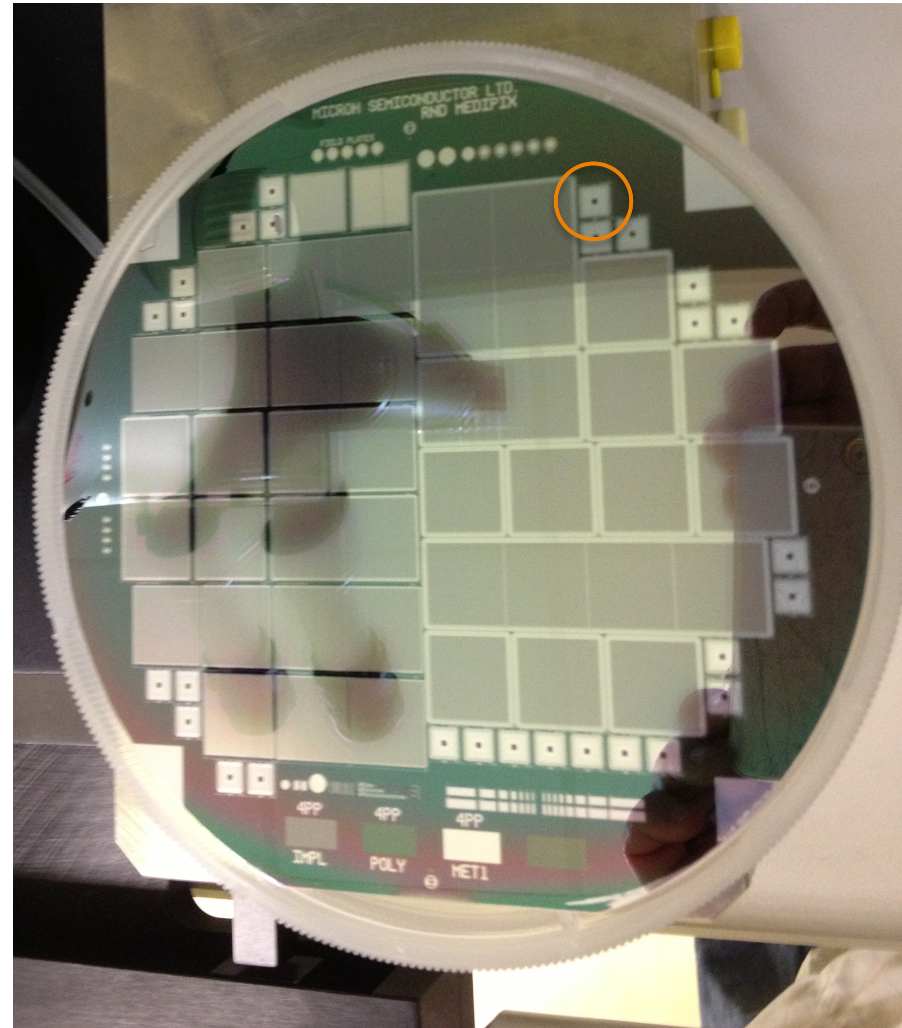
Before TSV

After TSV

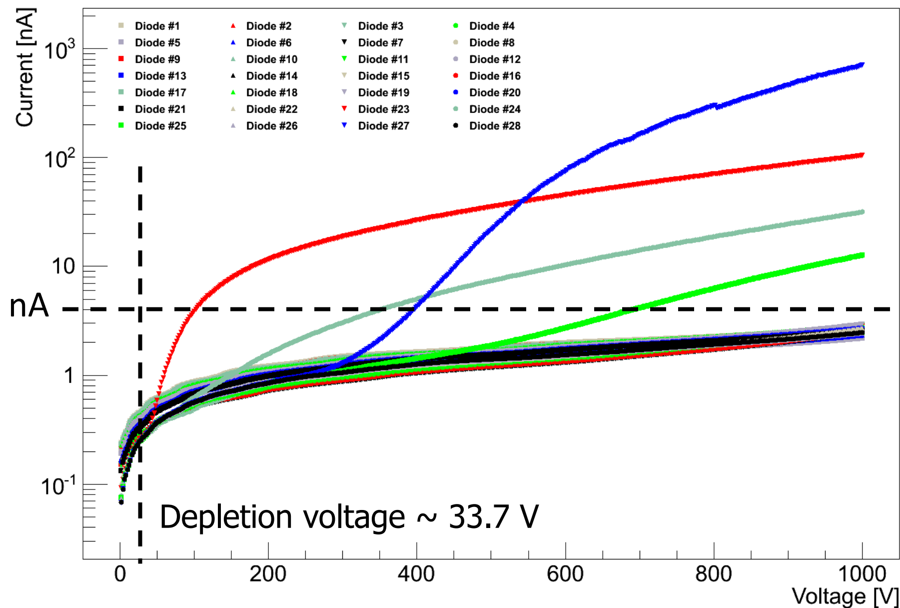
Sensor production

- Wafer production at Micron with sensor matching Timepix footprint (end of 2012)
  - Plan is to demonstrate the feasability of producing ultra-thin sensor and sensor assemblies
  - Sensor delivered in 100, 150, 200, and 300 um thickness
  - Sensor UBM deposited at IZM, waiting for dicing
  - Plan to flip-chip thin sensors to 100um thin ASIC wafer (Summer 2013)
- Wafer production at Micron with sensor matching CLICpix footprint (end of 2013)

200 μm thickness Micron wafer



Wafer 3022-1 200 μm - Diodes IV



Summary

- CLIC Vertex detector R&D on the way to meet physics and machine environment requirements
- Simulations and measurements on Timepix assemblies has allowed the development of robust calibrations techniques as well as a realistic digitiser that can be ported to larger frameworks
- CLICpix demonstrator ASIC has been produced, readout is being developed for testing
- Through Silicon Vias technology show promise in improving pixel detectors' active area and sensor assemblies robustness
- Sensor procurement ongoing towards thinner assemblies
- More details on the Vertex Detector Technology Indico page: https://indico.cern.ch/categoryDisplay.py?categId=2843

Thank you for your attention

Backup

Vertex detector requirements

- Integral part of tracking systems (in particular for low p_T)
- Efficient tagging of heavy quarks through precise determination of displaced vertices:

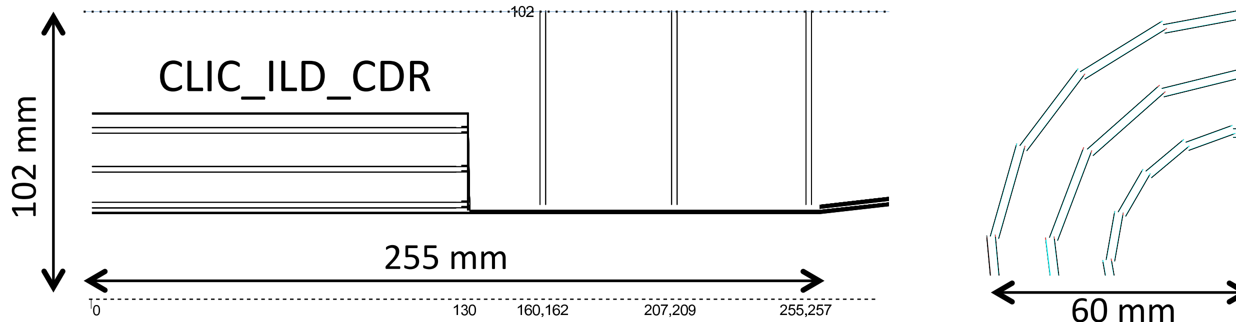
$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

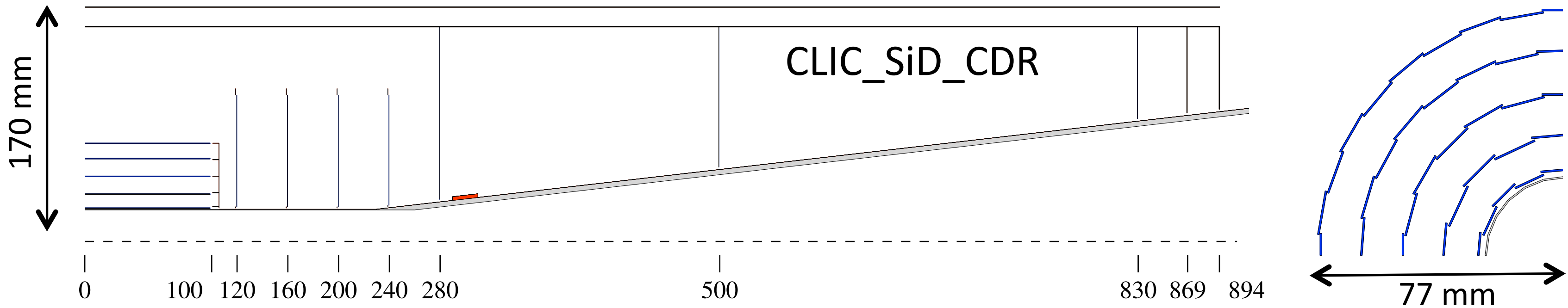
$$a \approx 5\mu m \quad b \approx 15\mu m$$

  → Good single point resolution: σ_{SP}~3 μm
    → Small pixels ~25x25 μm
  → Low material budget: X ≲ 0.2% X_0 / layer
    → Corresponds to ~200 μm Si, including supports, cables, cooling
    → Low-power ASICs (~50 mW/cm²) + air-flow cooling
- 156 ns bunch trains, 20 ms gaps → trigger-less readout, pulsed powering
- Time stamping with ~10 ns accuracy, to reject background
    → high-resistivity sensors, fast readout
- B = 4-5 T → Lorentz angle becomes important
- Full coverage down to low polar angles θ_{min}~7° → Barrel + EC geometry

- To date: no technology option available fulfilling all requirements
  → Simulation studies: impact of layout on performance
  → R&D on sensors & readout
  → Integration/Assembly + power-pulsing + cooling studies

CLIC Vertex detector concepts





	CLIC_ILD_CDR	CLIC_SiD_CDR	CMS
Material X/X0 (90°)	~0.9% (3x2 layer)	~1.1% (5 layer)	~10% (3 layer)
Pixel size	20 x 20 μm^2	20 x 20 μm^2	100 x 150 μm^2
# pixels	2.03 G	2.76 G	66 M
Time slicing resolution	~10 ns	~10 ns	<~25 ns
Avg. power/pixel	<~0.2 μW	<~0.2 μW	28 μW

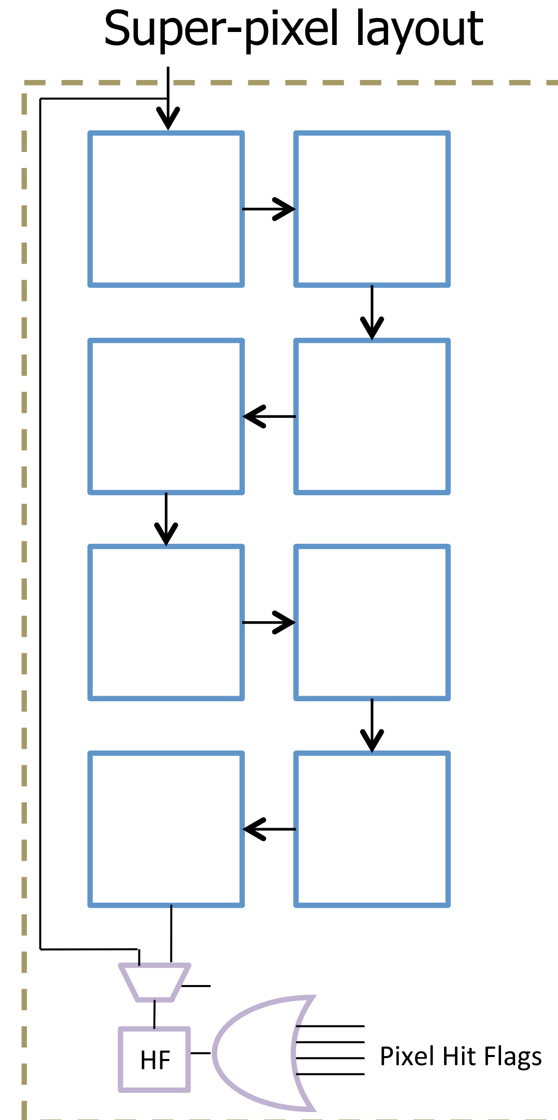
Vertex detector sensor technologies

Monolithic sensors	3D/Hybrid type CMOS sensors	Hybrid pixel sensors
DEPFET, FPCCD, MAPS • Low material budget (50 um thickness) acheivable with current technology • Fine granularity (down to 5um pixel acheivable) • Coarse timing only (integrating sensor) • Suitable for ILC vertex detector • Partially depleted sensors	**Chronopix, PLUME (MAPS), SOI pixel sensors** • Low material budget (50 um thickness) acheivable with current technology • Fine granularity (down to 5um pixel acheivable) • Coarse timing only (integrating sensor) • Suitable for ILC vertex detector • Partially depleted sensors	**Timepix3/SmallPix/CLICpix** • Low material budget to be demonstrated • Coarser pixel pitch (~25 um pixel size acheivable) • Fully depleted : Time slicing (~ 10 ns) for background reduction • Make use of widely available commercial technology (130nm, 65nm CMOS) • Fast sparsified read-out • Suitable for CLIC

CLICpix demonstrator digital summary

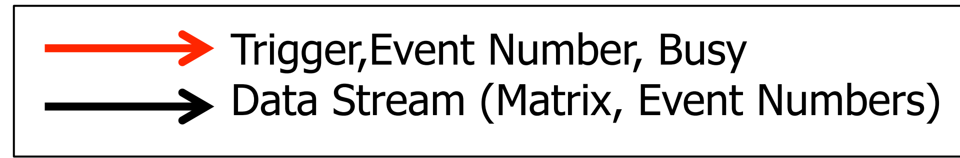
CLICpix Demonstrator - Digital part

Technology	65 nm (High-Vt Standard Cells)
Logic size	275 μm^2
Acquired Data	TOT and TOA
Counter Depth (LFSR)	4 bits TOT + 4 bits TOA (or counting, for calibration)
Target Clock Speed	100 MHz (acquisition) 320 MHz (readout)
Data type	Full Frame Zero compression (pixel, super-pixel and column skipping)
Acquisition Type	Non-continuous
Power Saving	Clock gating (digital part), Power gating (analog part)



Timepix Integration to EUDET/AIDA Telescope

Seemless integration of Timepix DUT into exisiting EUTelescope framework as one additional telescope plane



Developed at CERN

M-i-M TLU

TRIGGER LOGIC UNIT (TLU)

TLU Producer

EUDET Producer

Timepix Producer

Data Manager

Online Monitoring

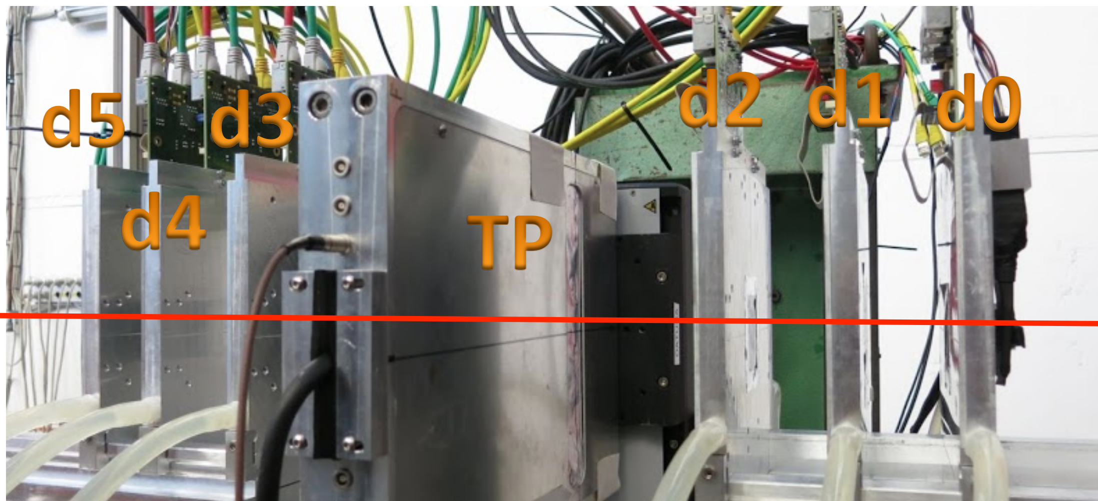
Reconstruction and analysis

EUDET (MIMOSA26)

TIMEPIX

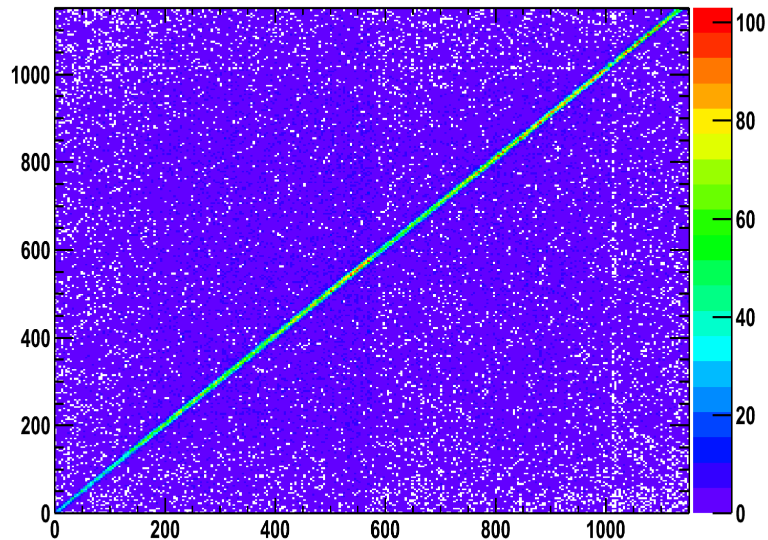
EUDET (MIMOSA26)

Cluster correlation and material budget



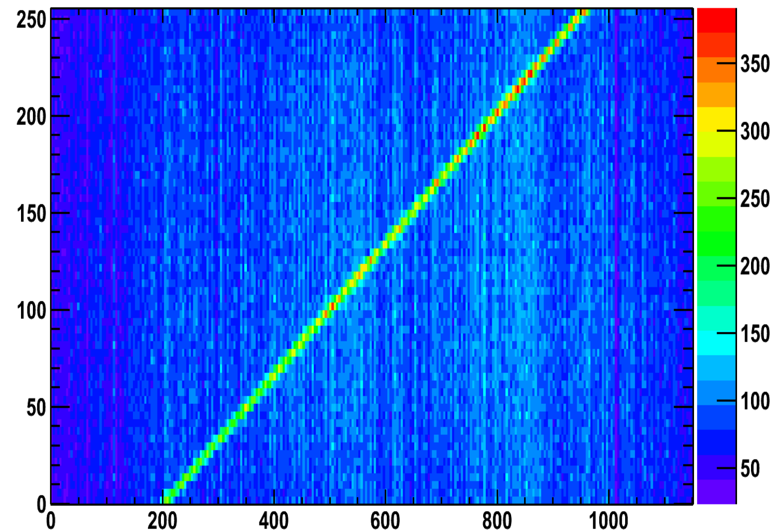
Beam (2-6 GeV)

Cluster Correlation d0-d2

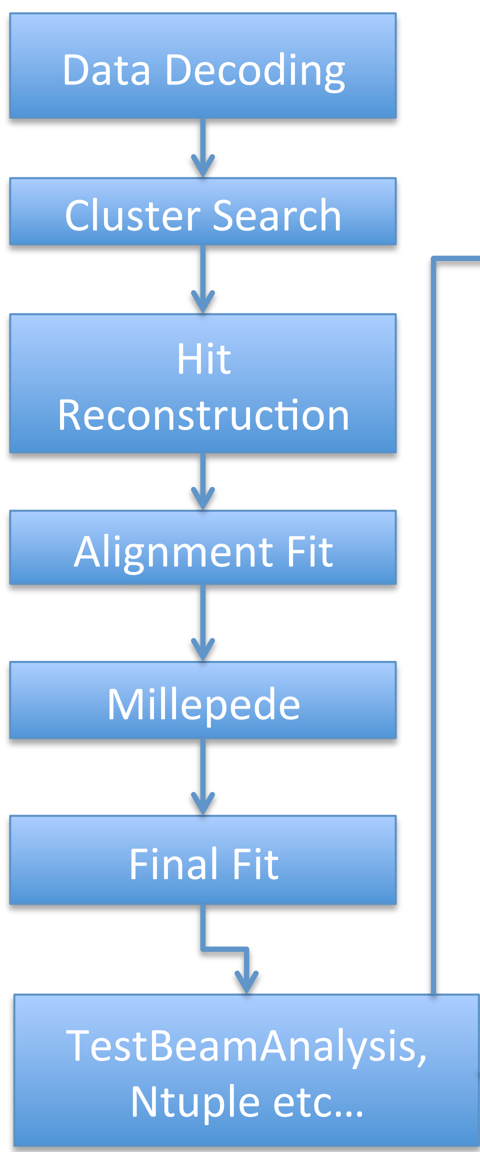


DUT material budget

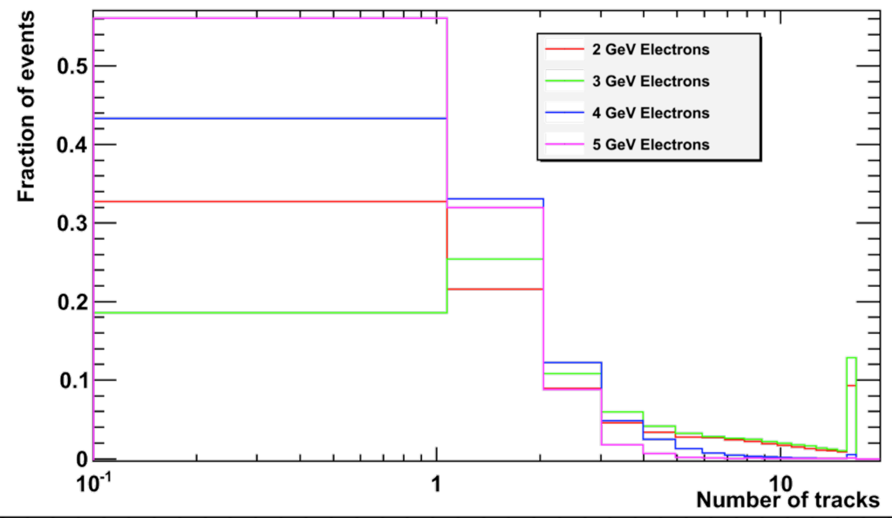
Cluster Correlation d2-TP



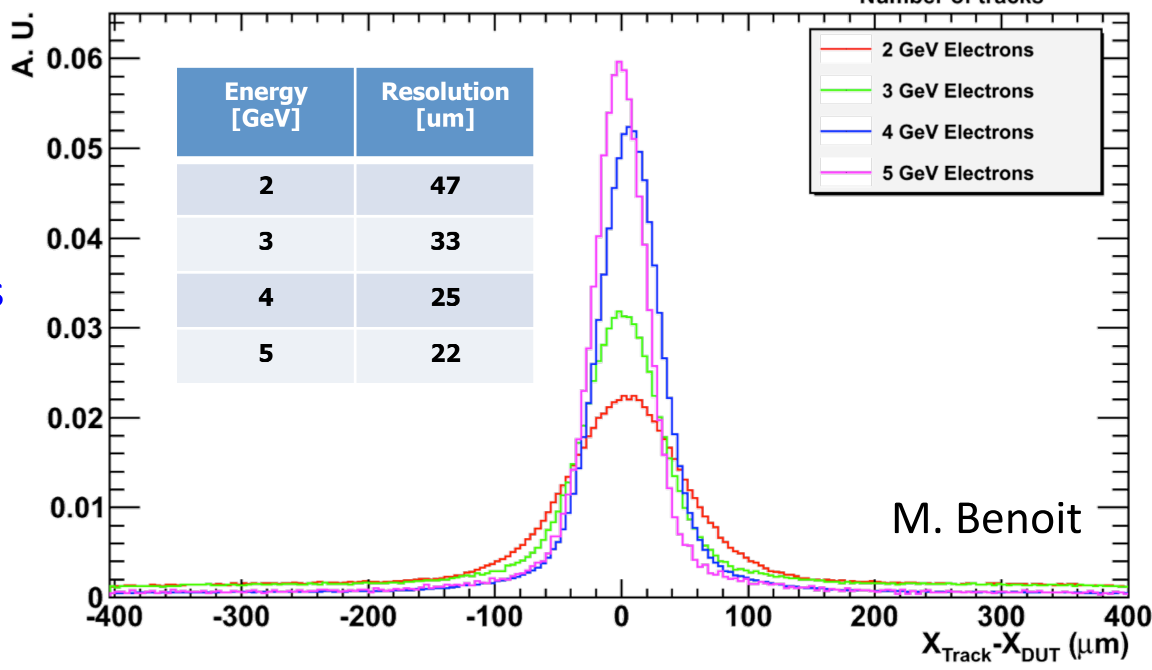
Feb. 2013 DESY Test beam results



Number of tracks



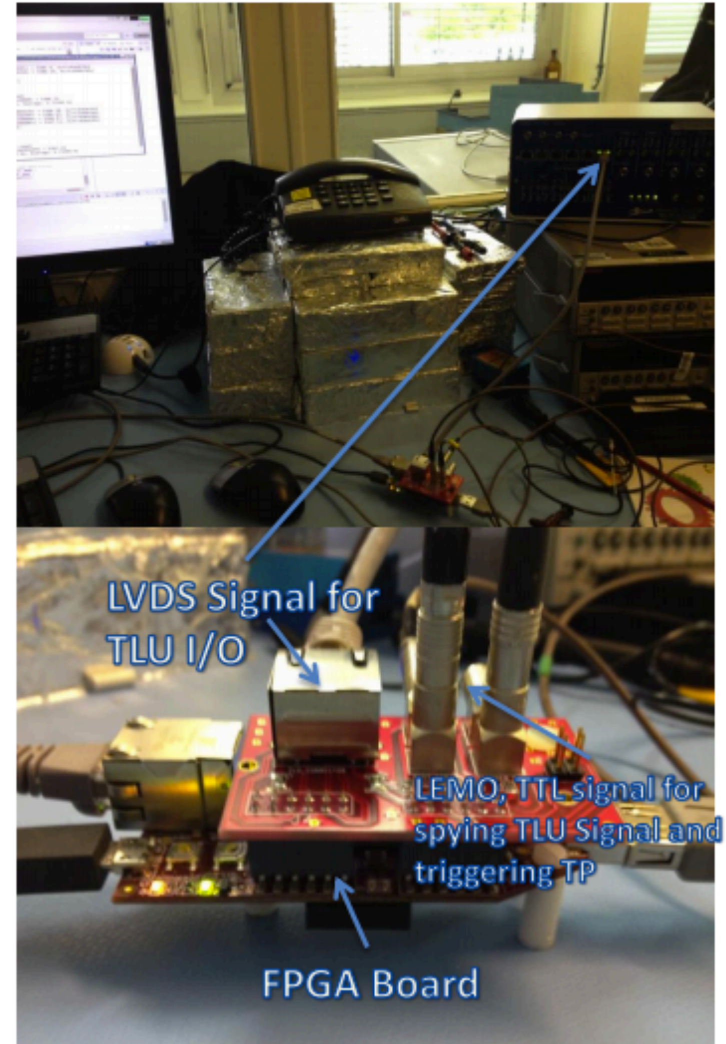
Residuals



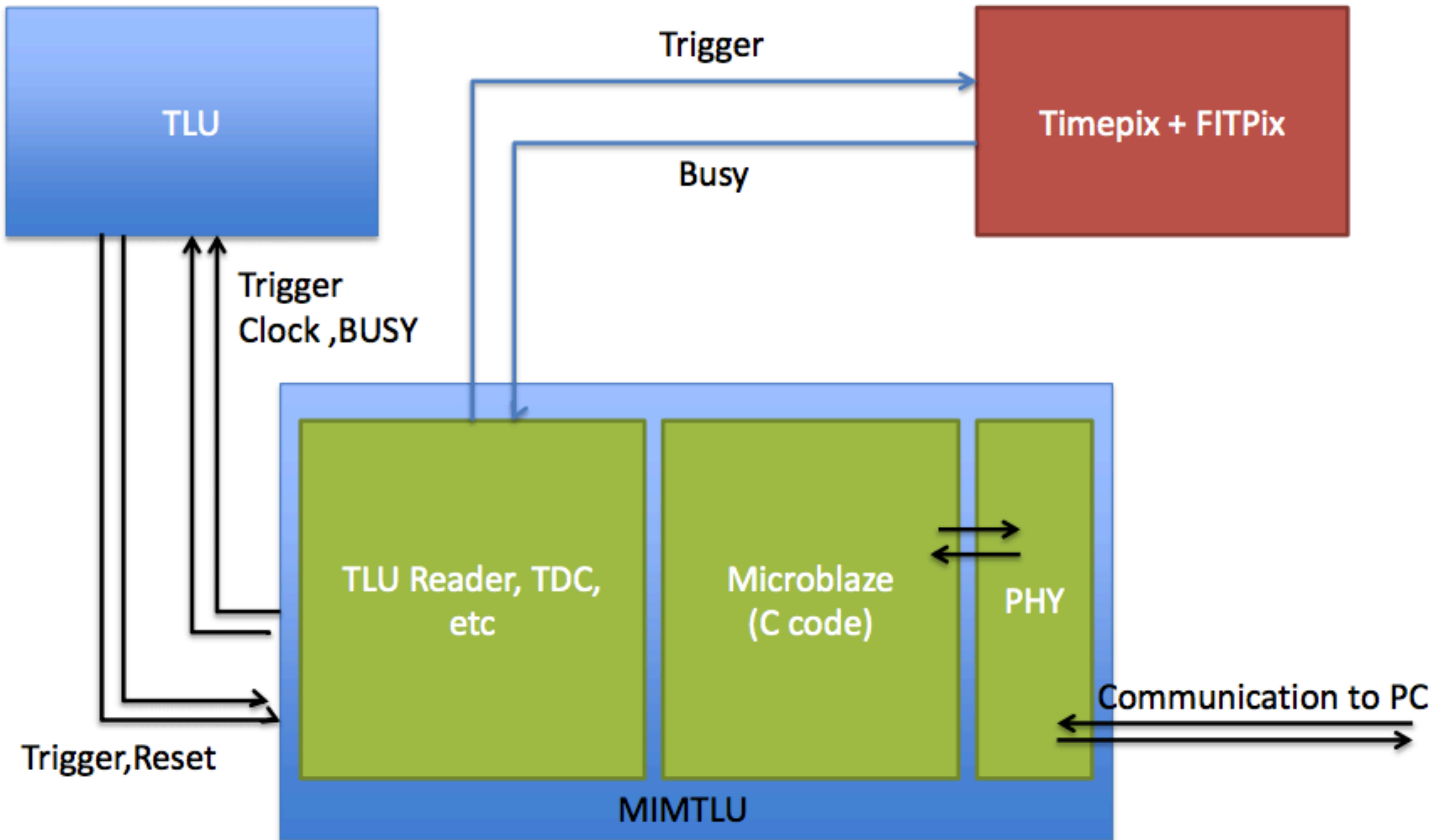
Energy [GeV]	Resolution [um]
2	47
3	33
4	25
5	22

Man-in-the-middle TLU

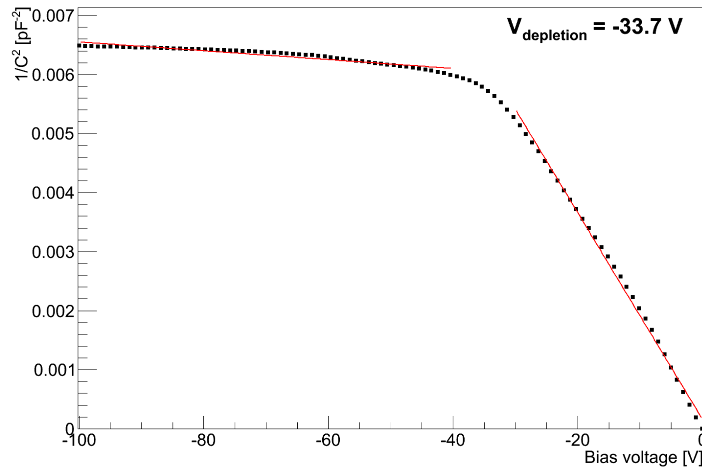
- Man-in-the-Middle TLU Reader is a interface to the trigger logic unit used by the EUDET Telescope
  - Handle the handshake on each trigger with the telescope system , transmit Event Number and synchronize with Timepix Producer via standard ethernet connection
  - Handle the FITPix readout trigering and BUSY
  - Provide full digital control of Timepix Trigerring
- Control through ethernet using a simple dependence free, open Library
- Compatible with mostly any PMOD equipped FPGA Developpement board
  - Reusable for CLICPix readout, Timepix3 readout
  - Low cost (~300 CHF)
- Possibility for other Use
  - TDC (see next slides)
  - Stand-Alone trigger interface to fitpix
  - Synchronisation studies (proposed by DESY)

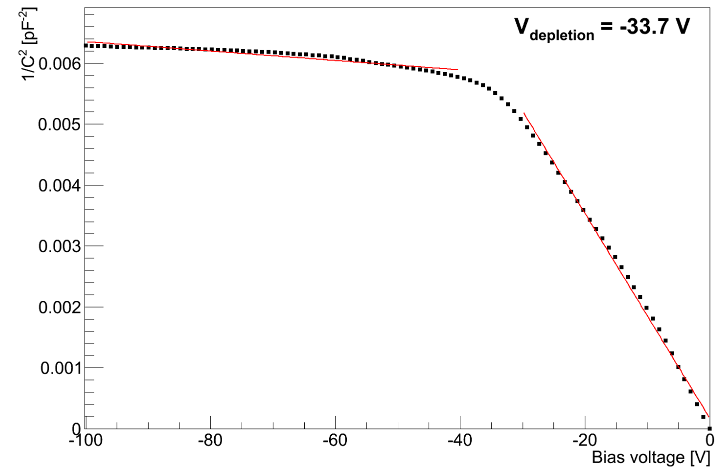


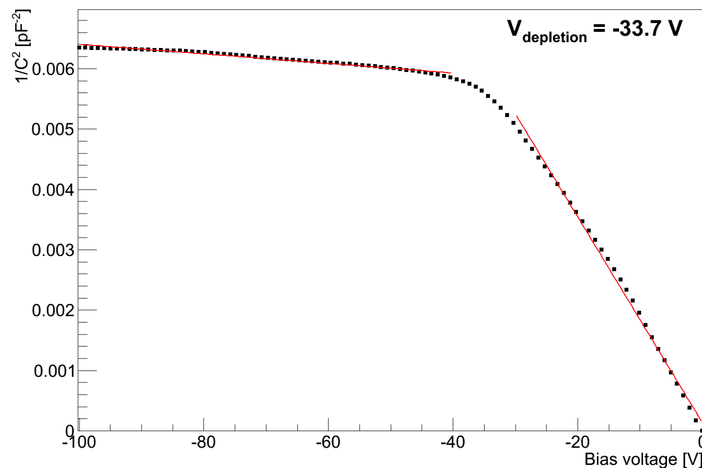
Man-in-the-middle TLU

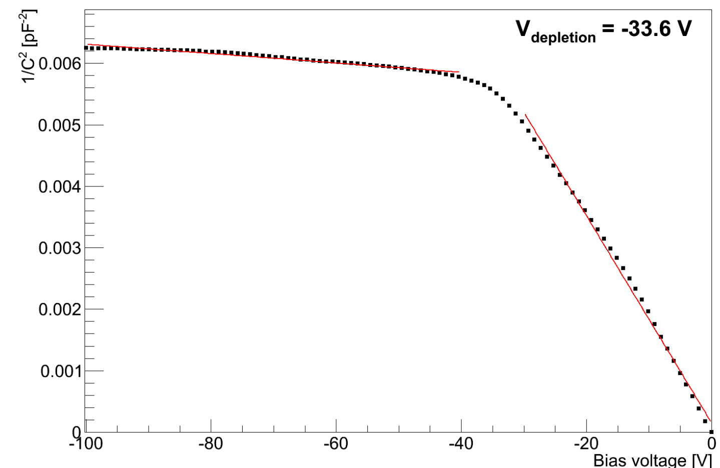


Micron Wafer C-V measurements









Single pixel I-V measurement