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DEPFET

Active Pixel Detector

DEPFET detectors for future e^+e^- colliders

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University of Bonn

On behalf of the DEPFET Collaboration

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Outline

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- SuperKEKB and ILC
  - Common requirements
- DEPFET system
  - Sensor development
  - ASICs
- Latest results
  - Lab and beam tests

The ILD vertex detector

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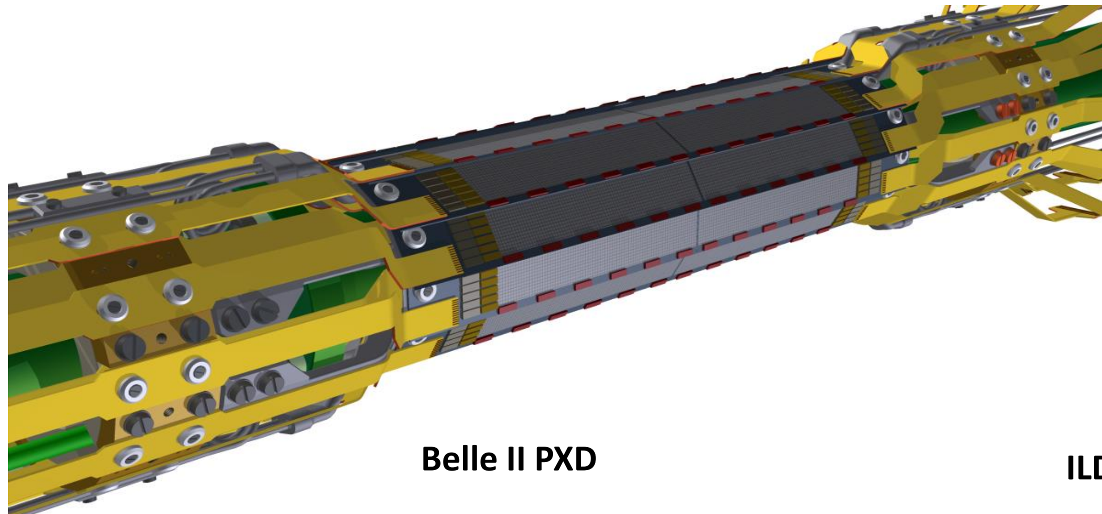
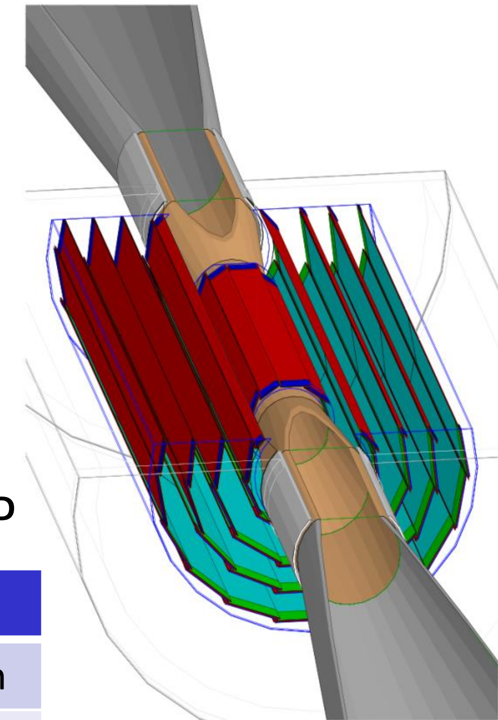
The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD



ILD 5-layer VXD

	ILD LOI 5-layer layout	Belle II	
Radii	15, 26, 38, 49, 60	14, 22	mm
Ladder length	123 (L1), 250 (L2-L5)	90 (L1), 122 (L2)	mm
Sensitive width	13 (L1), 22 (L2-L5)	12.5 (L1-L2)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	25x25 (L1-L5)	50x50 (L1), 50x75 (L2)	μm^2
Frame rate	20 (L1), 4 (L2-L5)	50	kHz

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

ILC detectors and Belle II

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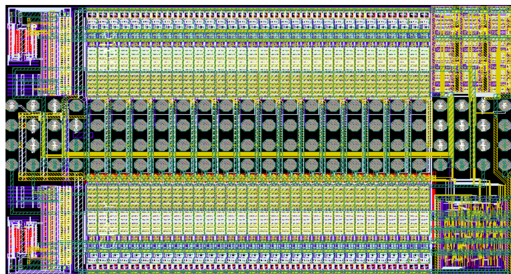
- Both detectors have very similar (challenging!) requirements:

	ILC	Belle II
Single point resolution	<5 μm	<10 μm
Radiation	~1 Mrad (10 years)	~20 Mrad (10 years)
Material budget	0.1 % X_0/layer	0.2 % X_0/layer
Frame time	25-100 μs	20 μs

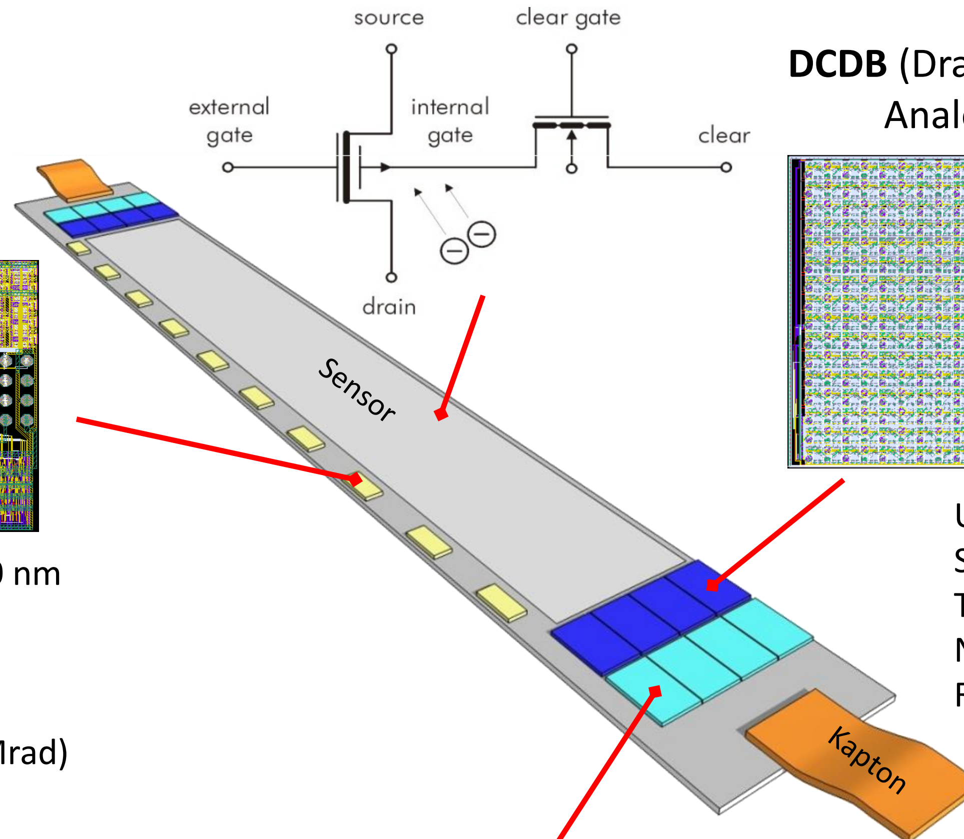
- High granularity for excellent spatial resolution
- Radiation tolerant to e^- (X rays) in the MeV (tens keV) range
- Low material budget:
  - Ultra transparent sensors with large SNR.
  - Low power dissipation
  - Minimal support, reduced services, and cooling material
- Fast readout

The DEPFET ladder

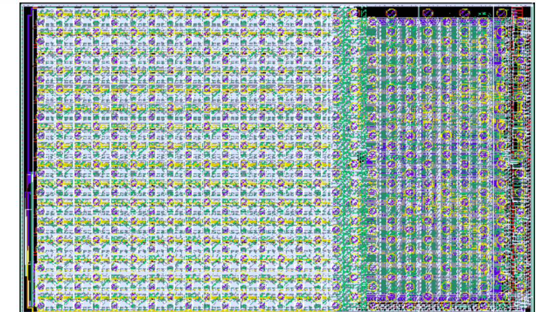
SwitcherB
Row control



AMS/IBM HVCMOS 180 nm
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

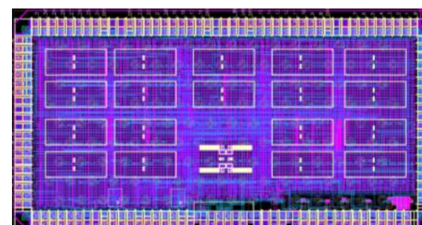


DCDB (Drain Current Digitizer)
Analog frontend



UMC 180 nm
Size 5.0 × 3.2 mm²
TIA and ADC
Noise 35 nA @ 100 ns/row
Rad. Hard proved (7 Mrad)

DHP (Data Handling Processor)
First data compression



IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm²
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

The DEPFET ladder

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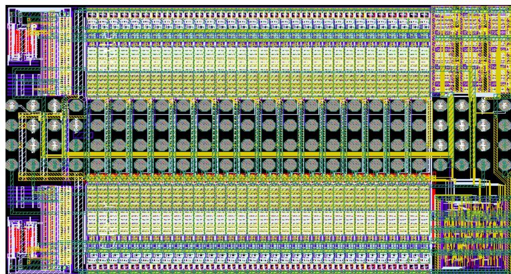
The full-size close to final versions of the ASICs are designed, produced and found to work

SwitcherB
Row control



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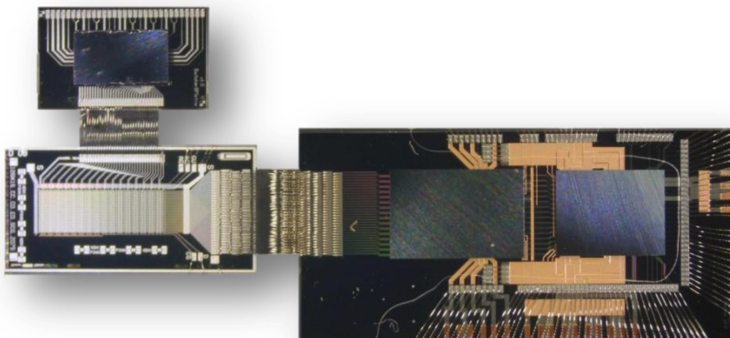

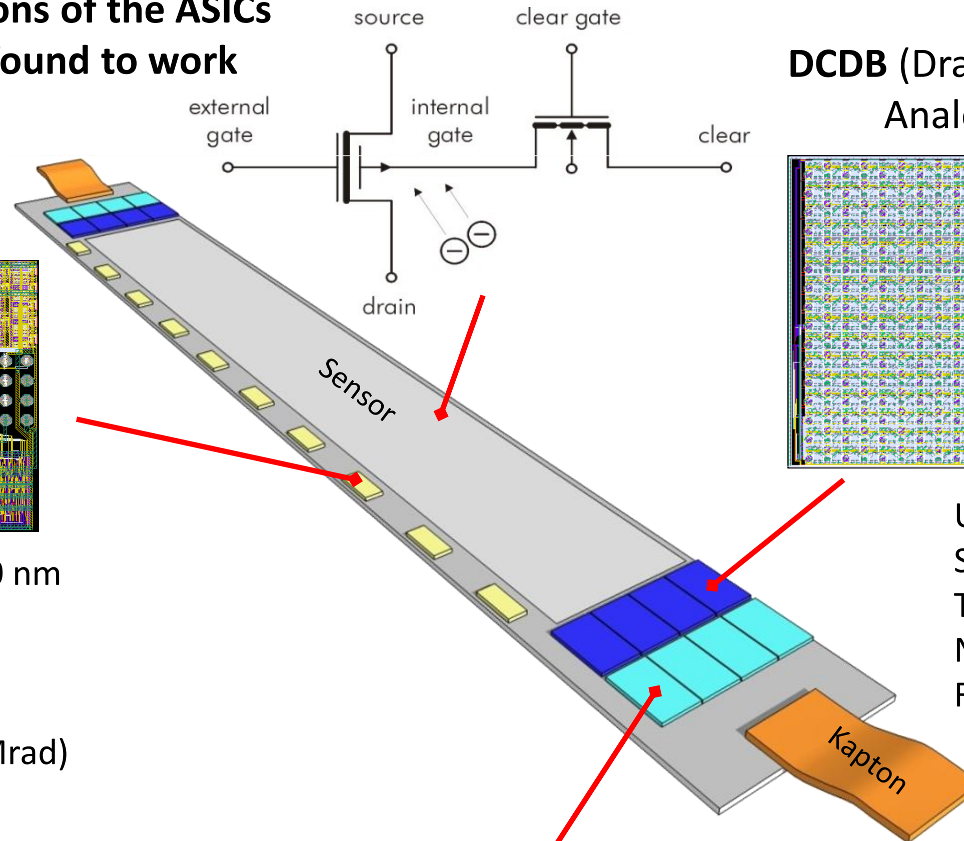

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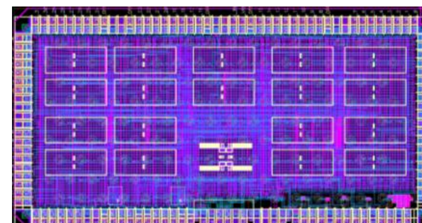

IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Off-module signal flow

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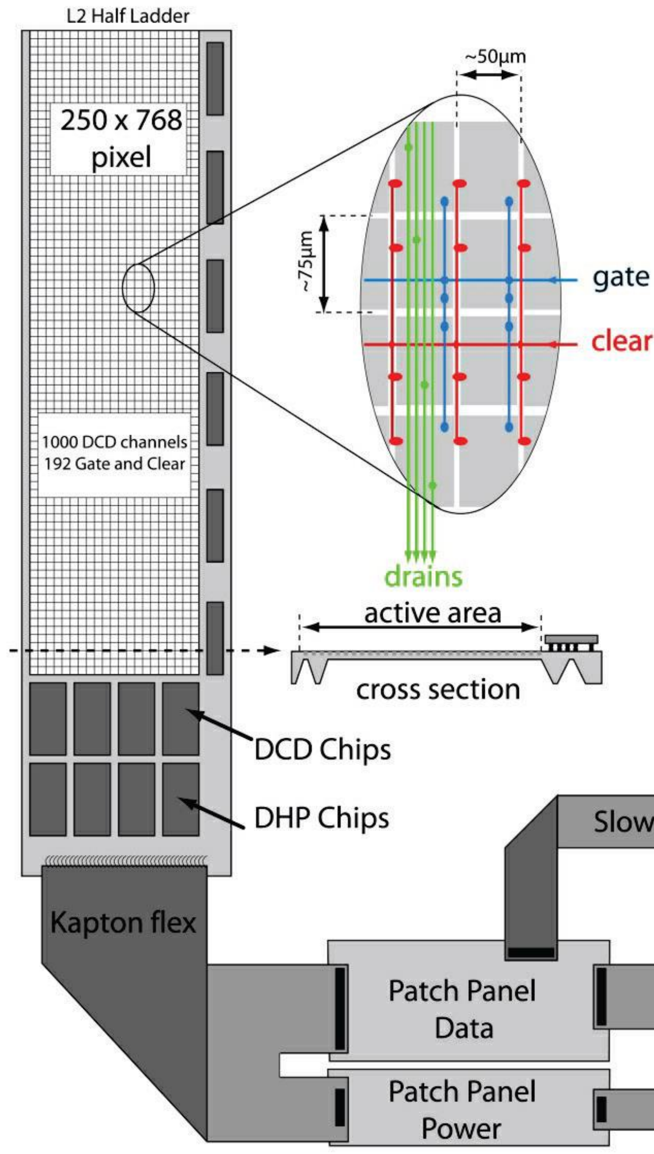
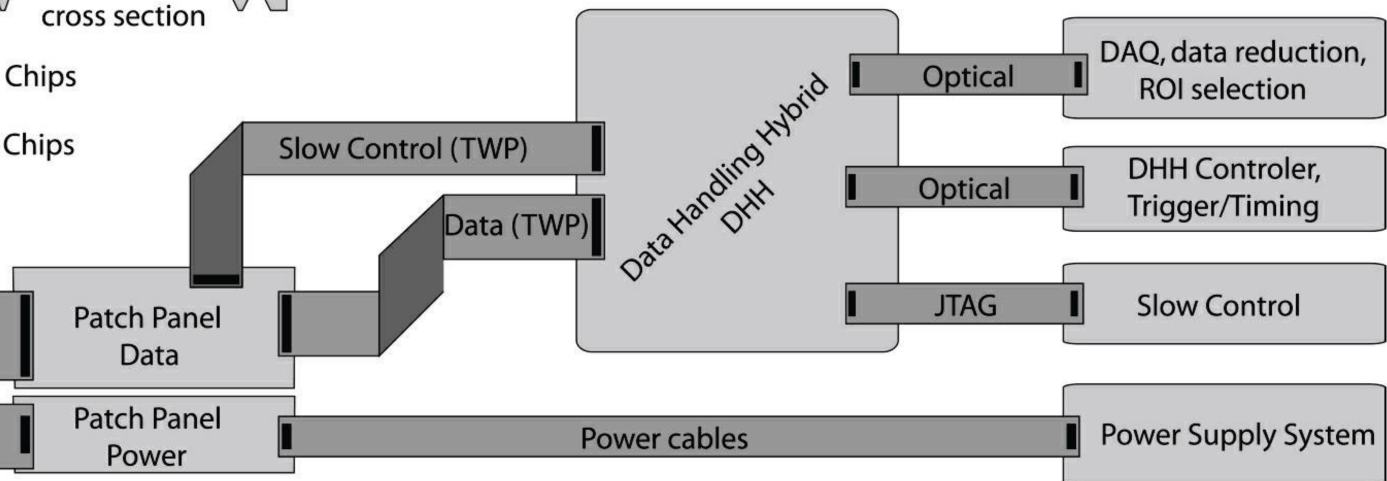


- **DHH** (Data Handling Hybrid)
  Electrical - optical interface
  Slow control master (JTAG)

- **ONSEN**
  Data buffer
  Reduction via ROI selection (DatCon, HLT)



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Thin DEPFET sensors

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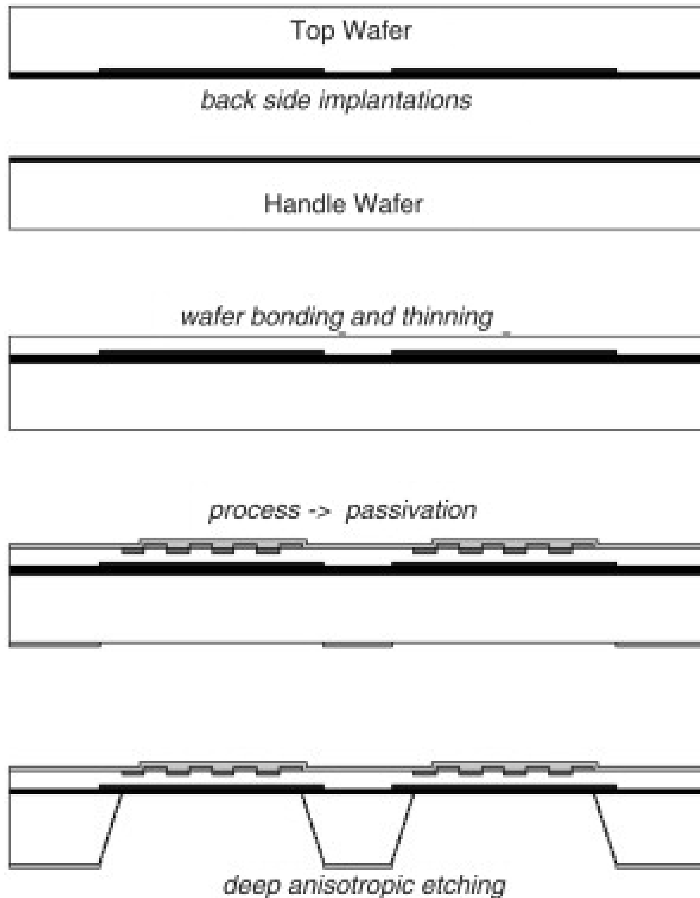
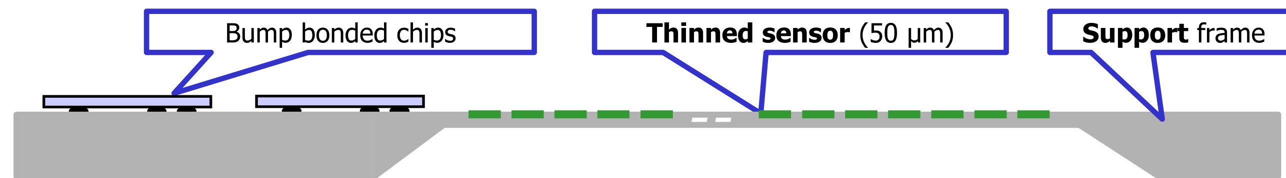
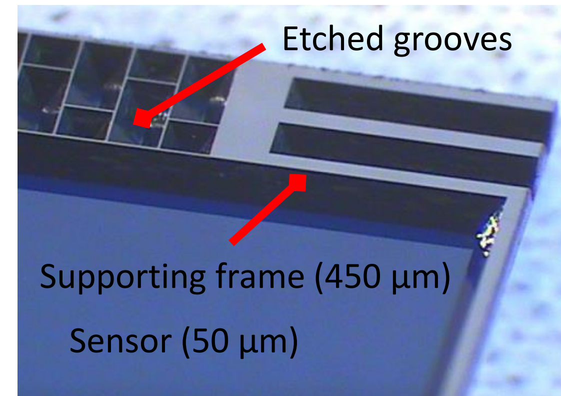
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor
→ One material: uniform and small thermal expansion







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PXD6 DEPFET latest prototype production

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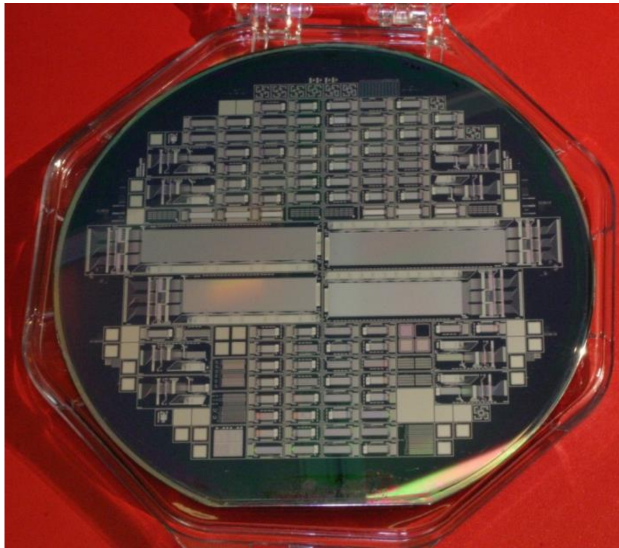
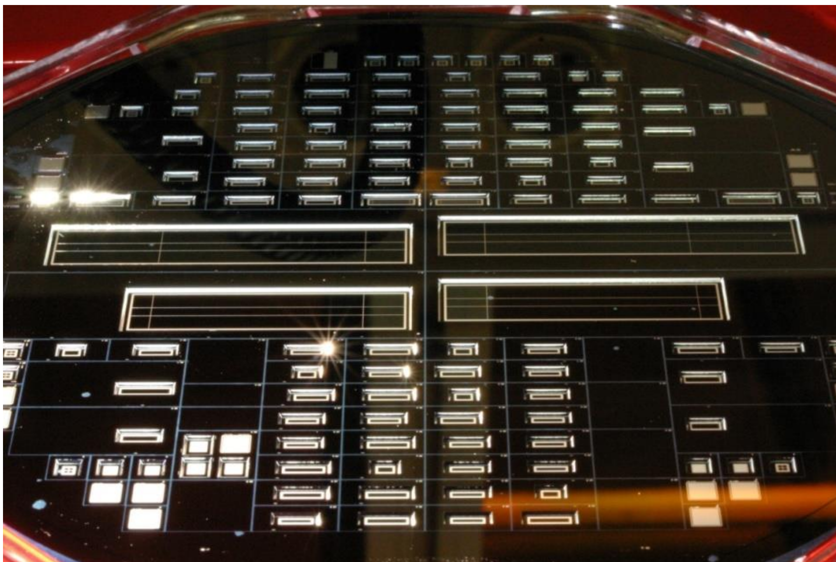
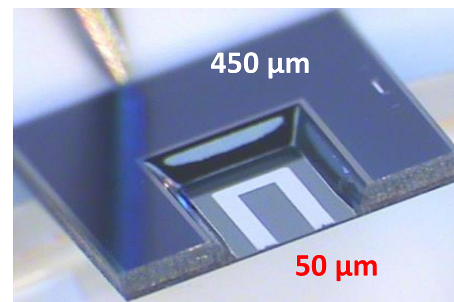


8 SOI wafers with 50 µm thin sensors (400 µm handle)

- Small test matrices to test different pixel sizes (50-200 µm)
- Design variations: short gate lengths, clear structures, drift
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level





90 steps fabrication process:

9 Implantations
19 Lithographies
2 Poly-layers
2 Alu-layers
1 Copper layer
Back side processing

First 50 µm thin DEPFET sensors produced!

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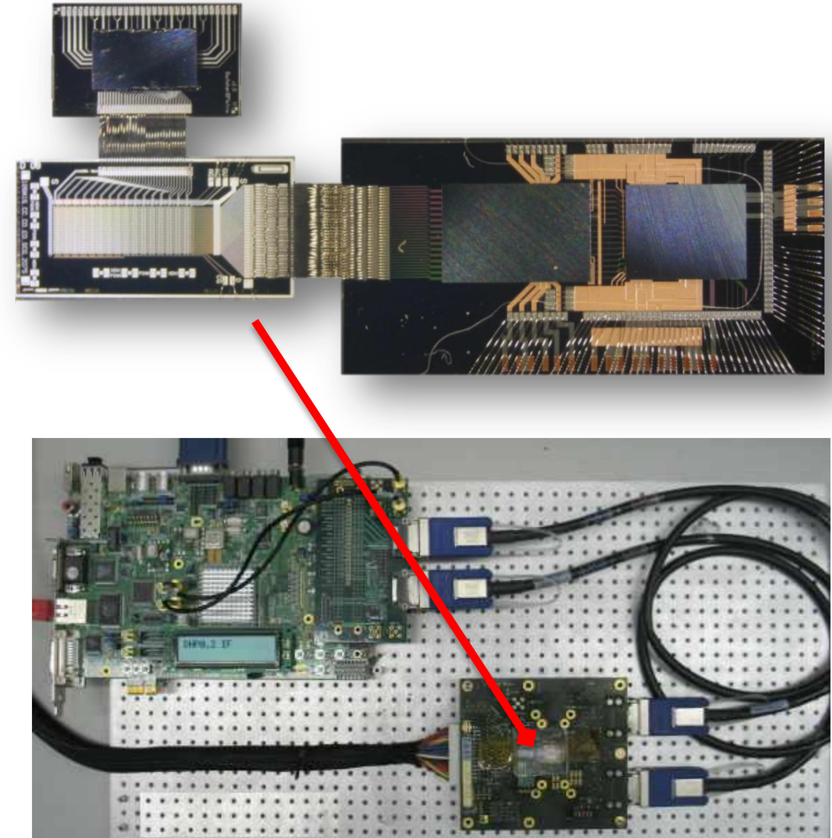
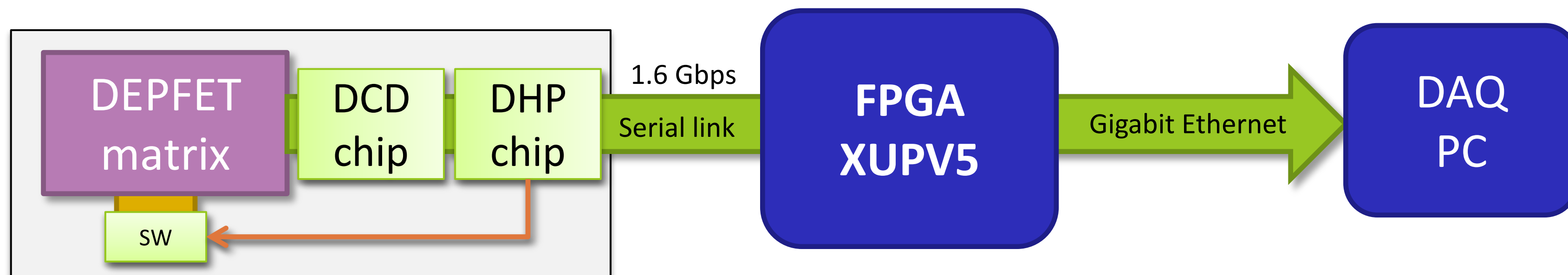
Hybrid 5.0 – Concept demonstrator

- Zero suppressed readout with the minimum necessary amount of components:
  - One Switcher-B
  - One DCDBv2
  - One DHP 0.2
  - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 μm^2 pitch
- Frame rate: 300 kHz (small matrix)





Laboratory tests: DHP

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- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

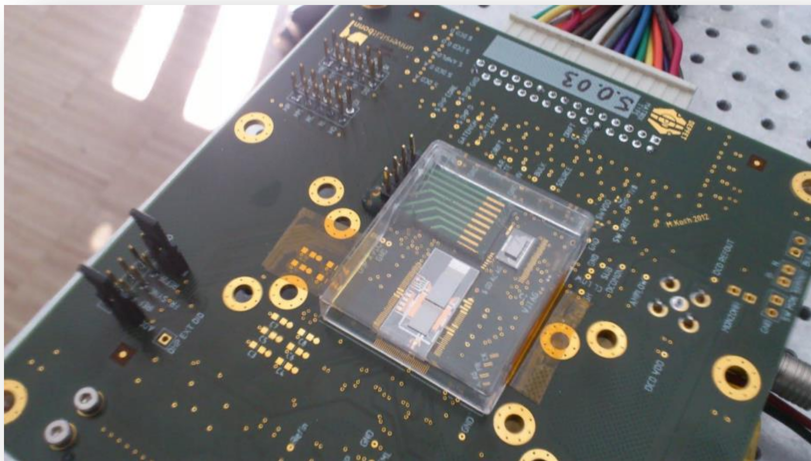
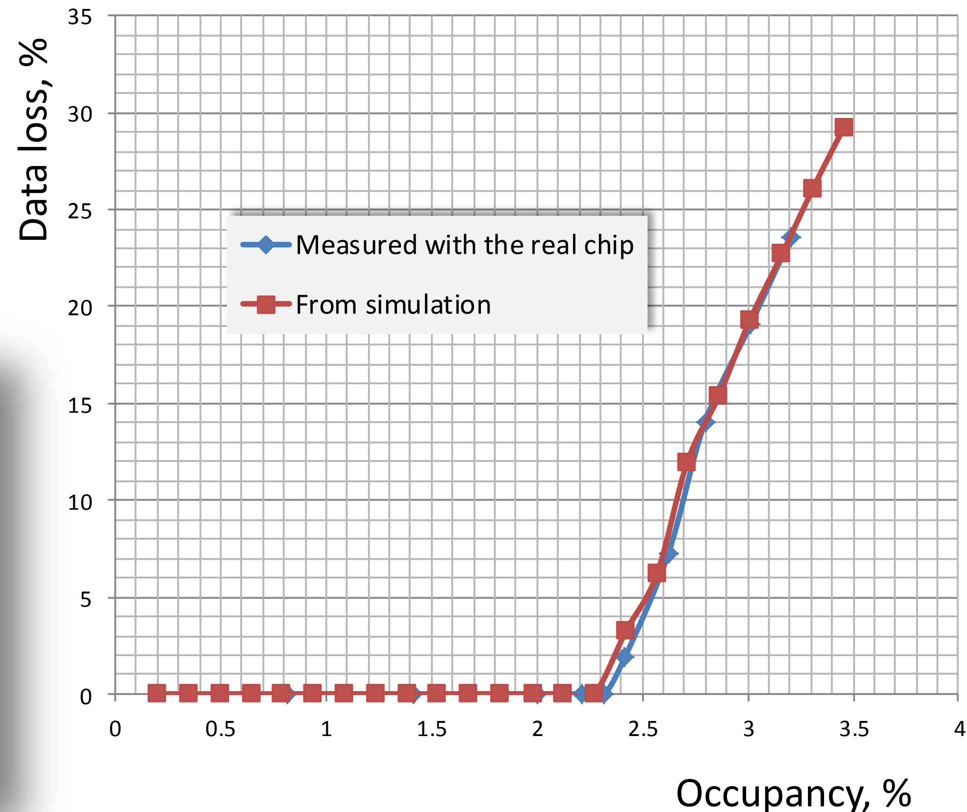


Photo of the hybrid 5 (without DEPFET matrix)



No data loss for the expected occupancy

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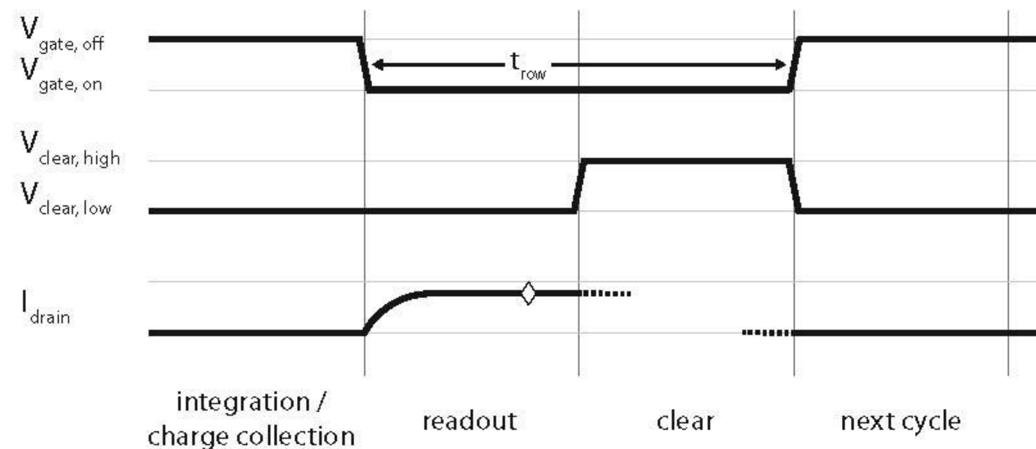
Laboratory tests: DHP

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link



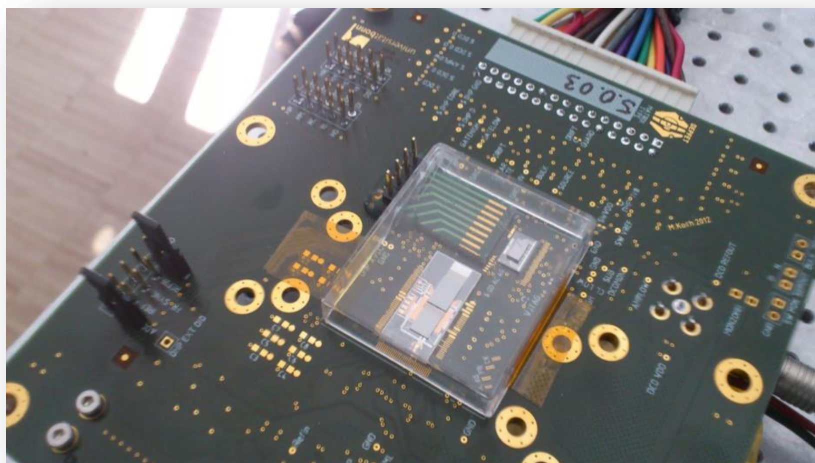
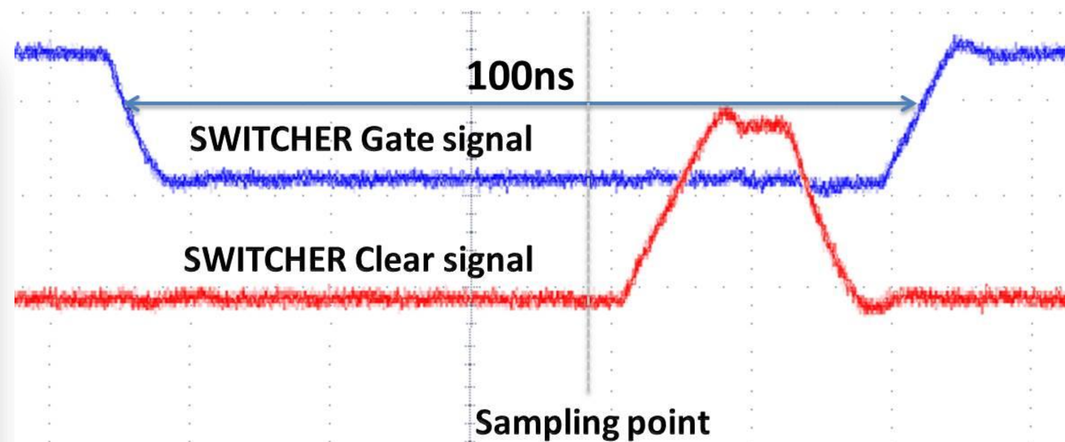


Photo of the hybrid 5 (without DEPFET matrix)

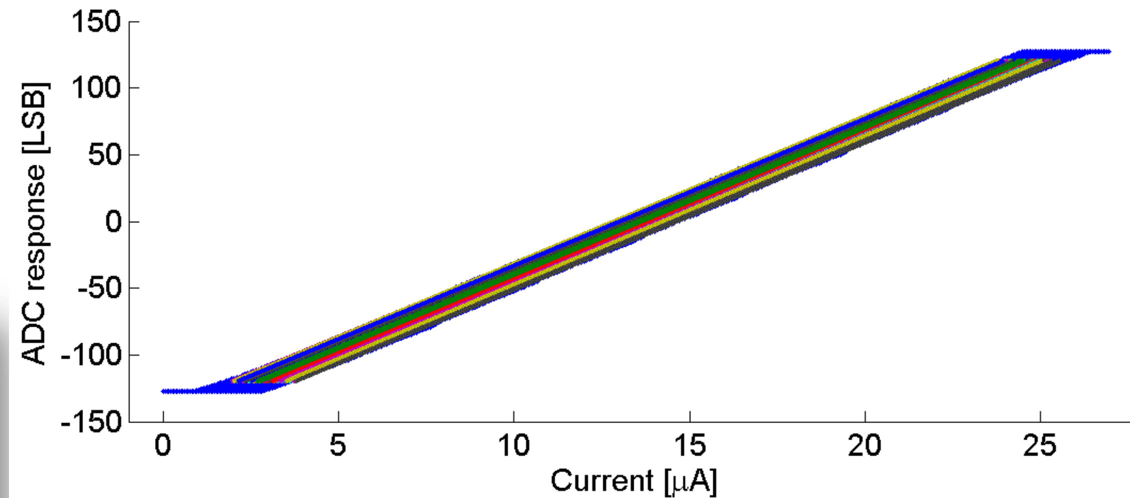


DHP can control the SwitcherB sequence

Laboratory tests: DHP

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

ADC vs Input current, all channels



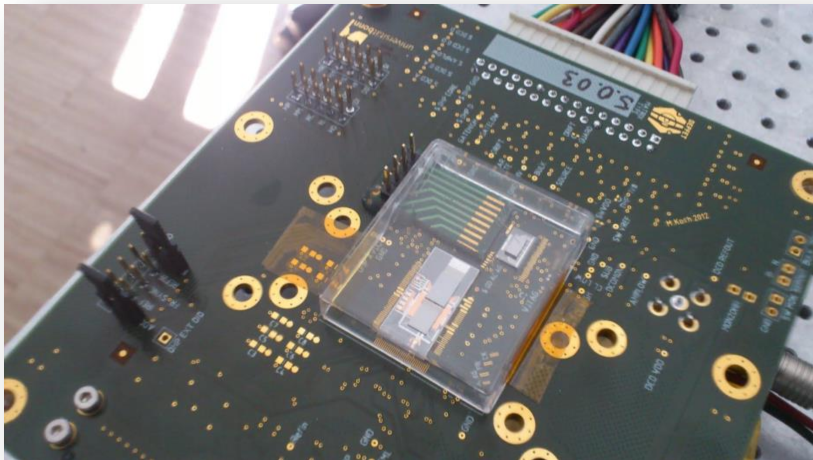


Photo of the hybrid 5 (without DEPFET matrix)

DCDB and DHP can communicate at full speed

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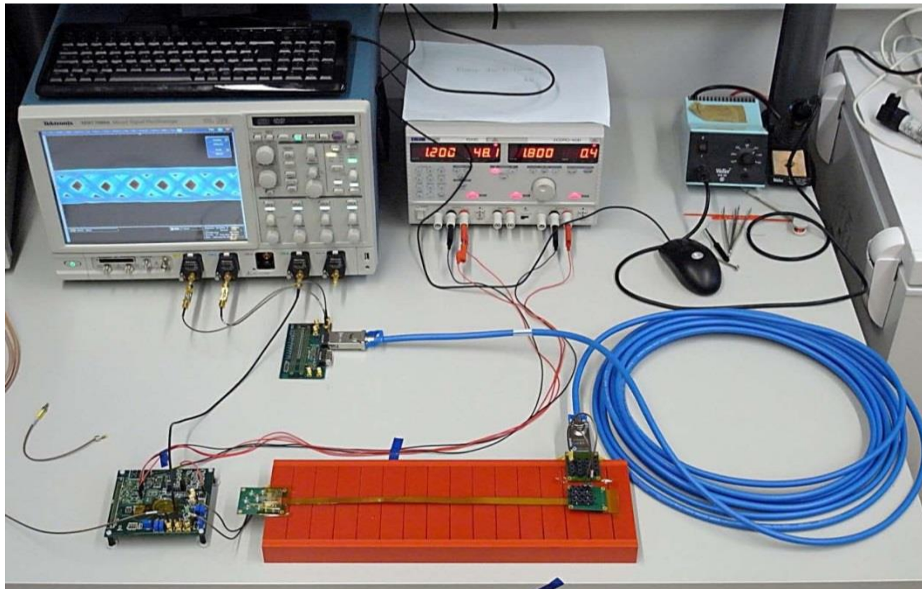
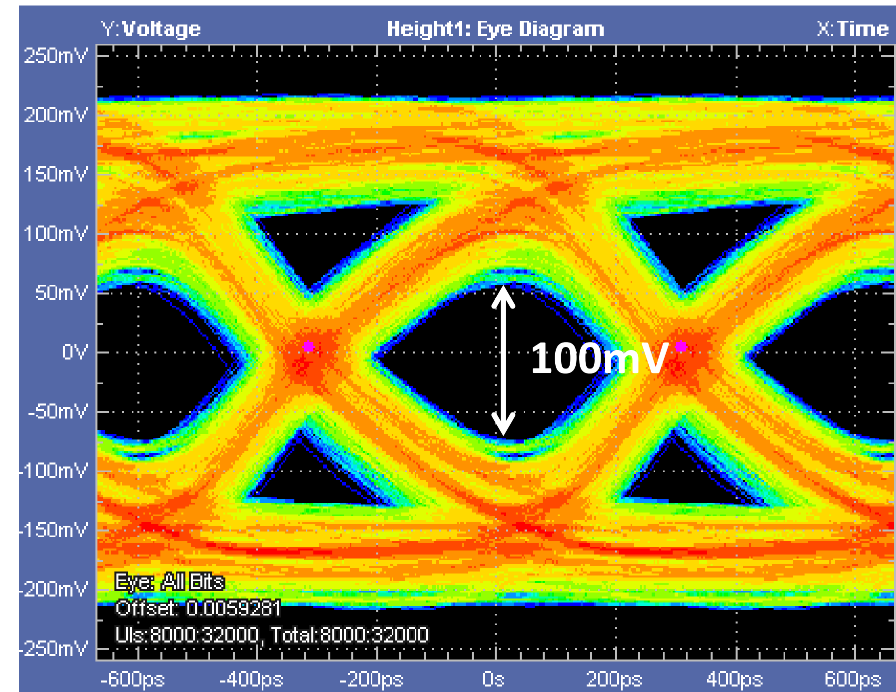
Laboratory tests: DHP

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link





Irradiated (100 Mrad) DHPT 0.1, can drive 15 m of Infiniband cable

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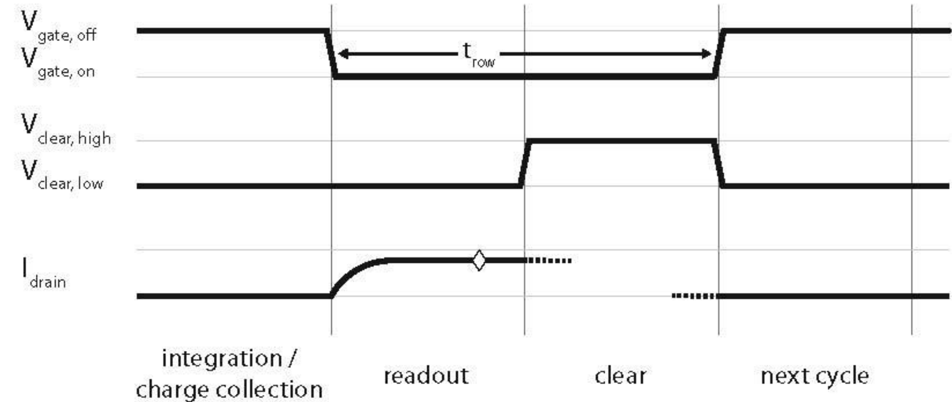
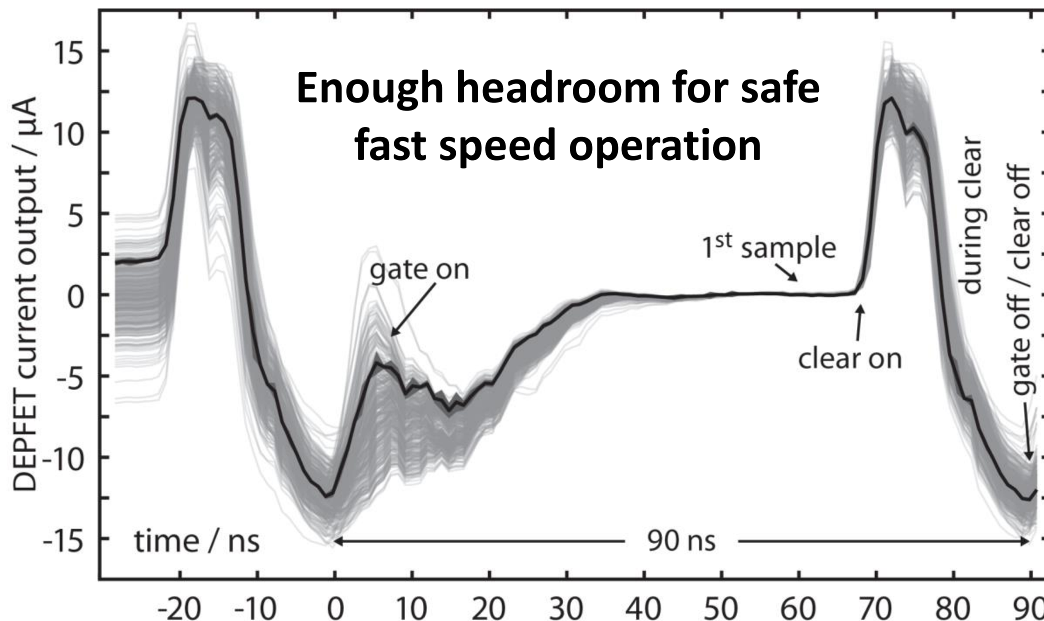
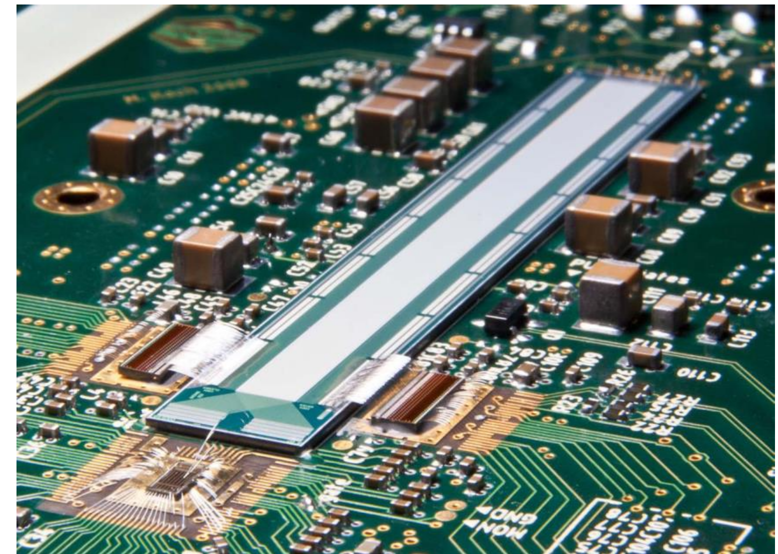
Laboratory tests: DCD

- DCD dynamic measurements
  Readout speed with single sampling
- Belle II PXD frame readout: 20 µs
  (50 KHz frame rate)
- Read-clear cycle: 100 ns
  (768 rows, 4 fold readout)







Long drain lines ~ 60 pF parasitic capacitance

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Laboratory tests: DEPFET sensor

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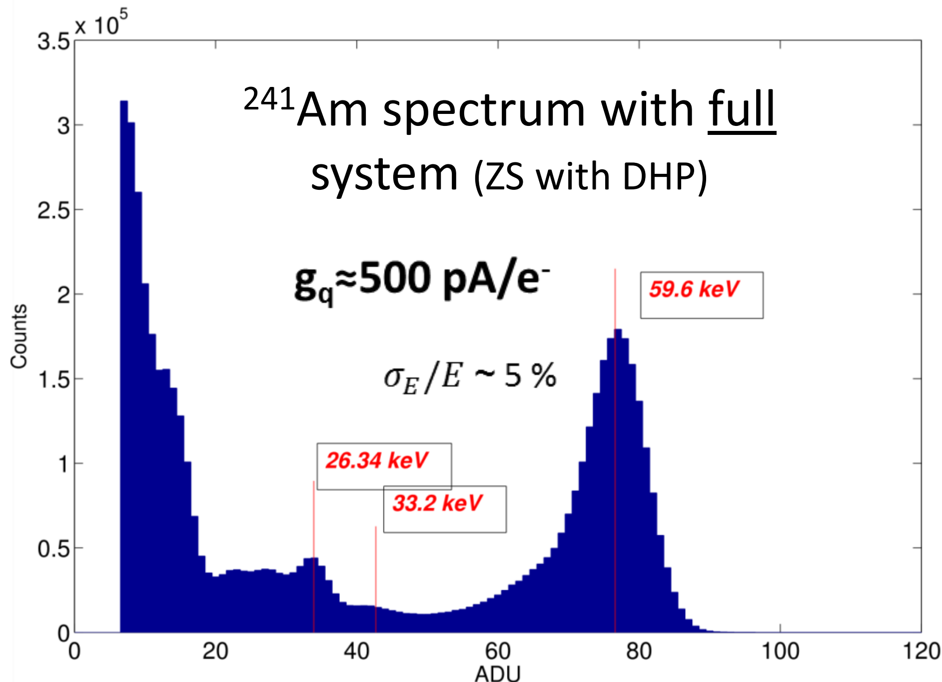
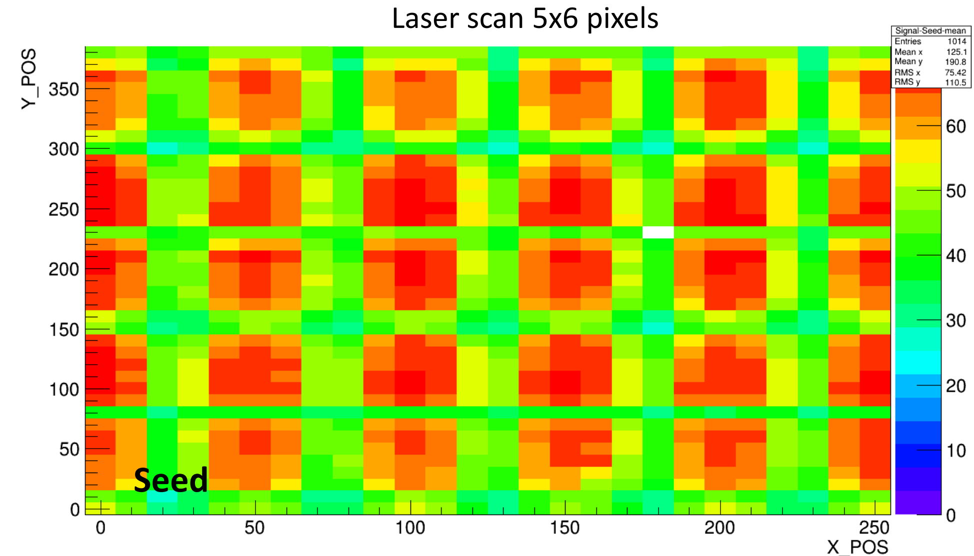
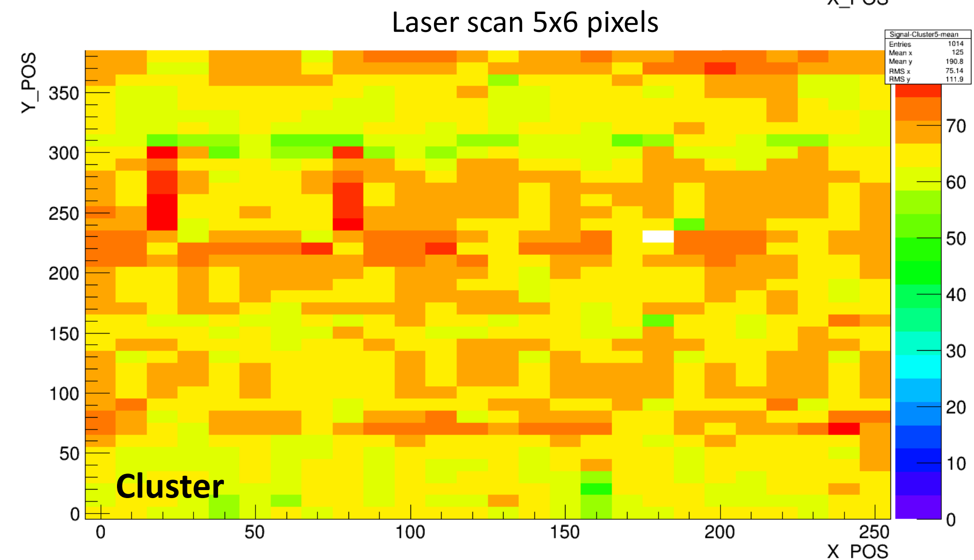
- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
  - Charge collection homogeneity
  - In pixel studies
- Radioactive source
  - System calibration







Homogeneous charge collection

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Beam tests

- DEPFET PXD6 extensively tested over the last campaigns
  - 120 GeV pions at CERN-SPS
  - 1-5 GeV electrons at DESY
- Sensor properties
  - Charge collection homogeneity, operating points, efficiency, angular scans
  - Various pixel sizes, gate lengths, clear structures, drift regions and pixel designs
- System related aspects
  - Power supply prototypes
  - DHH and ONSEN readout

Here, just an appetizer

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Beam tests

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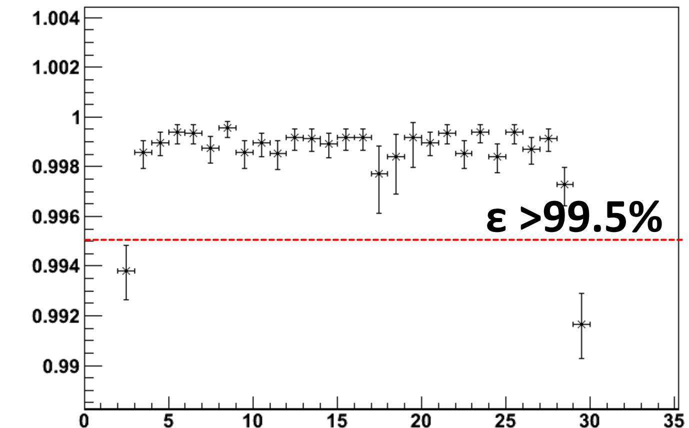
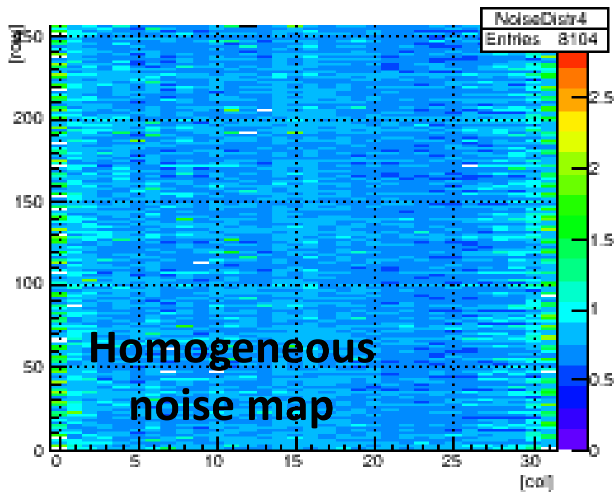
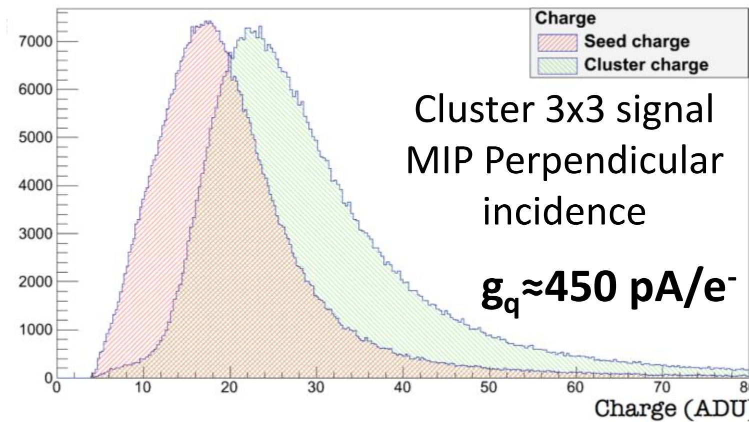
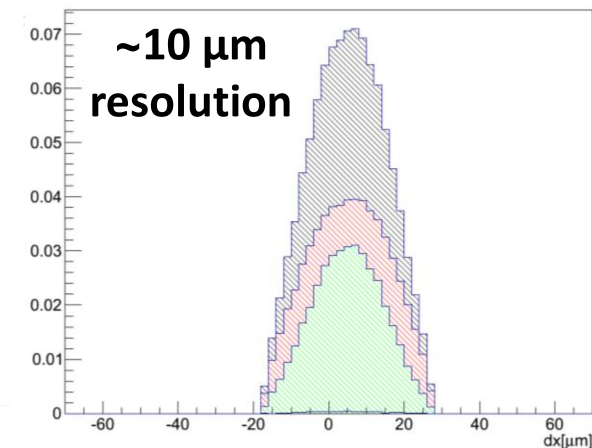
PXD6 Belle II design
Thin (**50** µm) sensor 32x64 pixels
Pitch 50x75 μm^2
SwitcherB and DCDB at full speed
Belle II prototype power supply
DCDB readout at 320 MHz
100 ns row time









Hybrid (Gate length)	Pitch [μm^2]	g_q [pA/e⁻]	Residuals [µm]
H.4.1.04 (6 µm)	50x50	275	~ 12 (Perpendicular incidence)
H.4.1.15 (5 µm)	50x75	600	~ 17 (Perpendicular incidence)

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Beam tests

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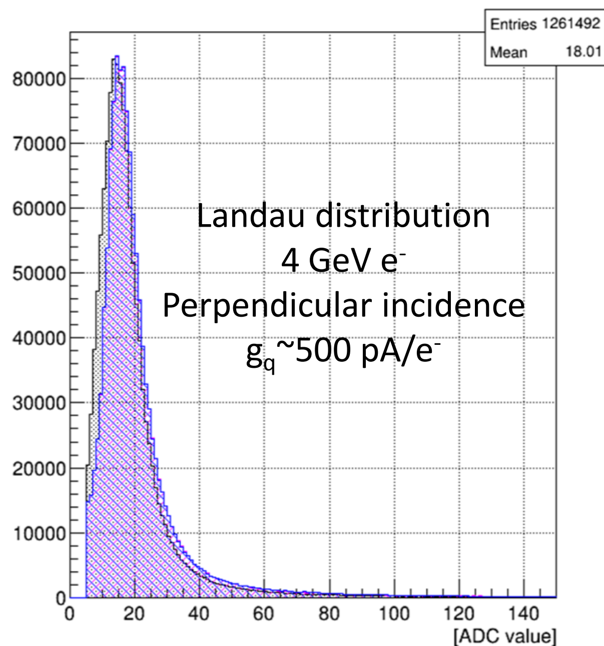
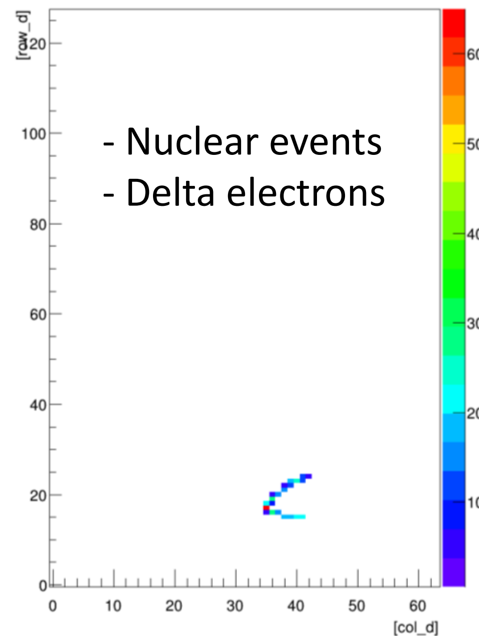
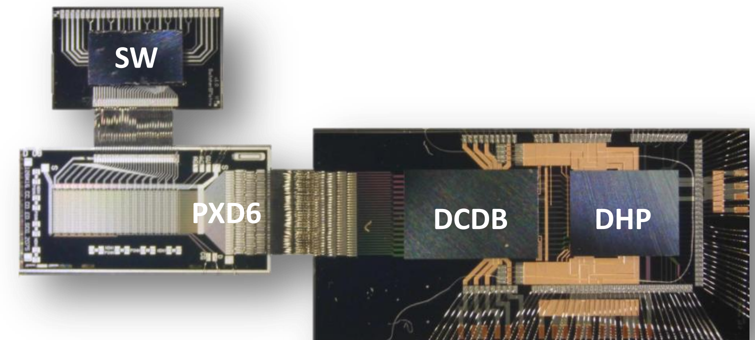
PXD6 Belle II design
Thin (**50** μm) sensor 32x64 pixels
Pitch 50x75 μm^2
SwitcherB, DCDB and DHP
Zero suppress readout
Final DAQ chain DHH+ONSEN







Data analysis is ongoing

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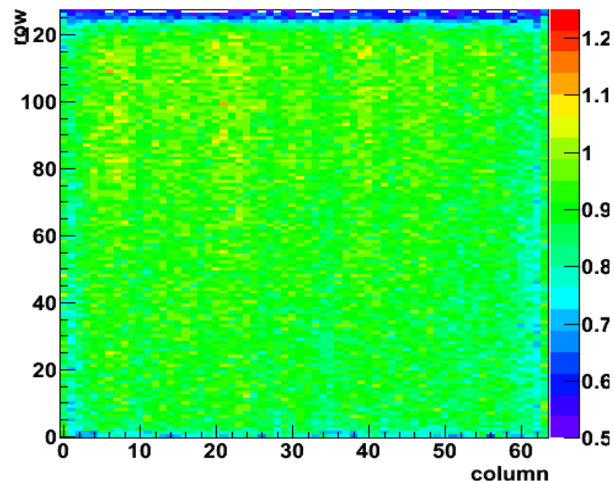
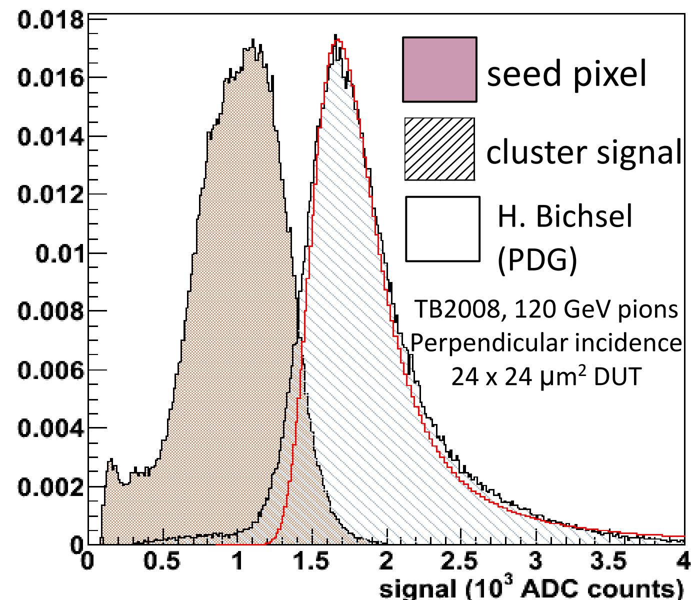
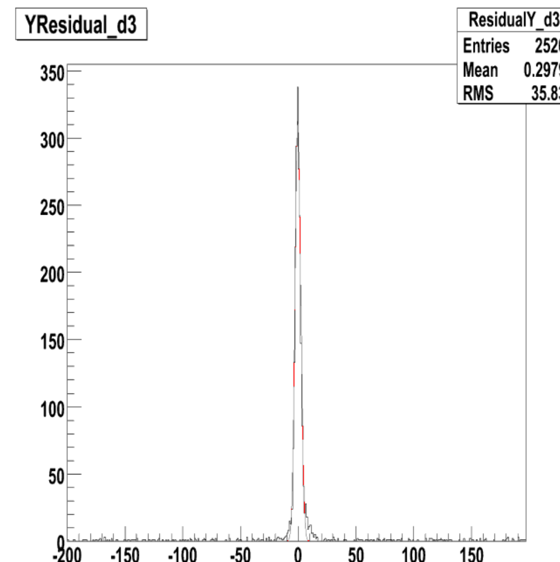
TB 2008 and 2009: PXD5 ILC sensors

Gain map: Deviation from average seed signal





- 64x128, 24x24x450 μm^3 CCG, 6 μm (TB2008)
  g_q=363pA/e^-
- 64x256, 20x20x**450** μm^3 CCG, 5 μm (TB2009)
  g_q~650 pA/e^-
- Resolution **σ~1 μm**, 20x20x**450** μm^3, analog readout with charge interpolation



ILC Design

→ Extensively tested

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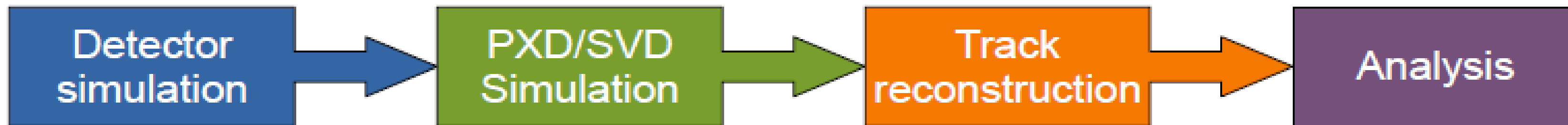
Expected resolution at ILC

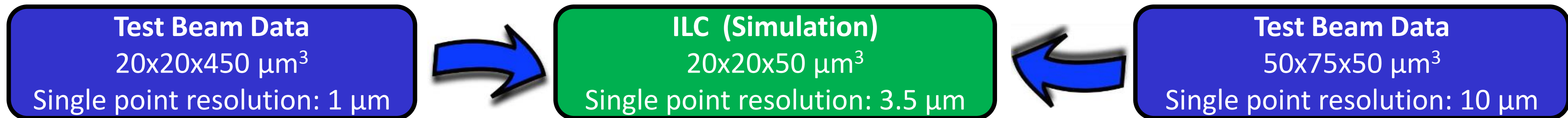


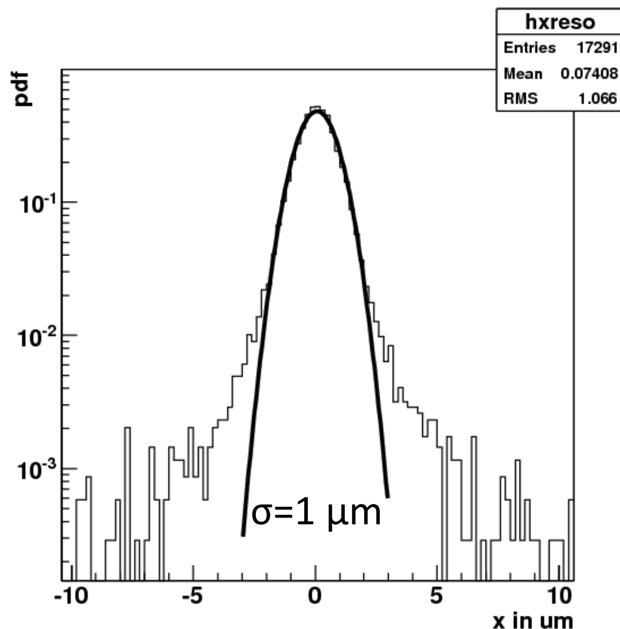
Particle gun (single event)
EvtGen (physics event)
Mokka geometry

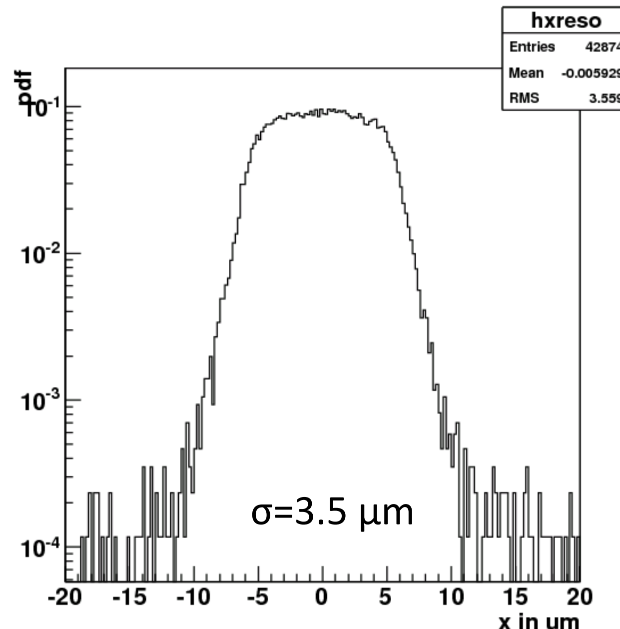
Ionization points
Signal points
Electronic noise
Digitization and clustering

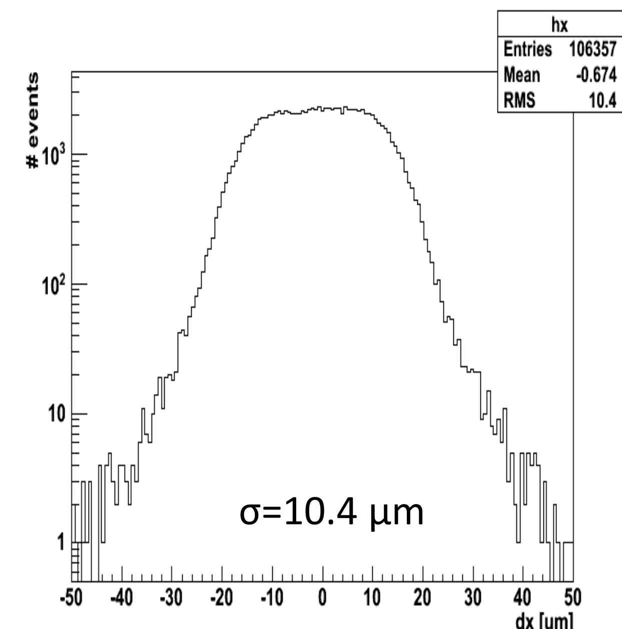
Marlin tracking
PXD+SVD+CDC

Physics channels









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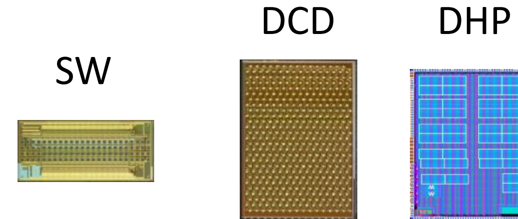
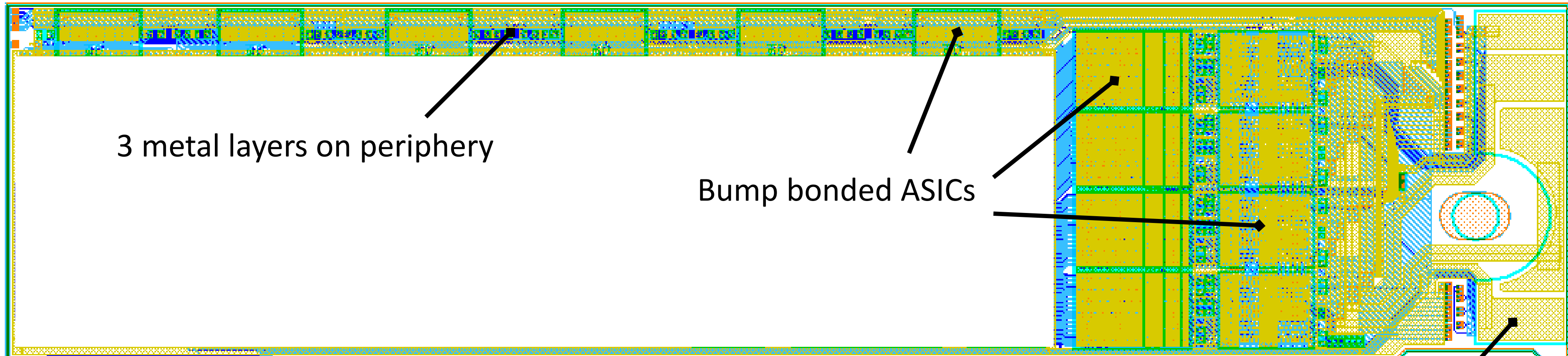
→ Simulation of ILC-type DEPFET sensors. B. Schwenker (Goettingen)

Electric MultiChip Module (E-MCM)

E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder





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Electric MultiChip Module (E-MCM)

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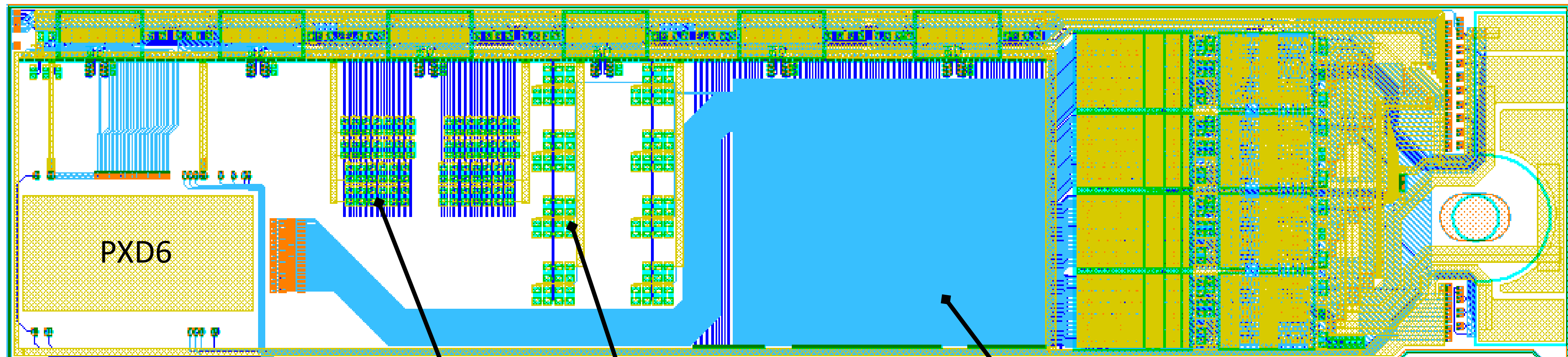
E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder



Metal system as close as possible to final → Electrical information

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Electric MultiChip Module (E-MCM)

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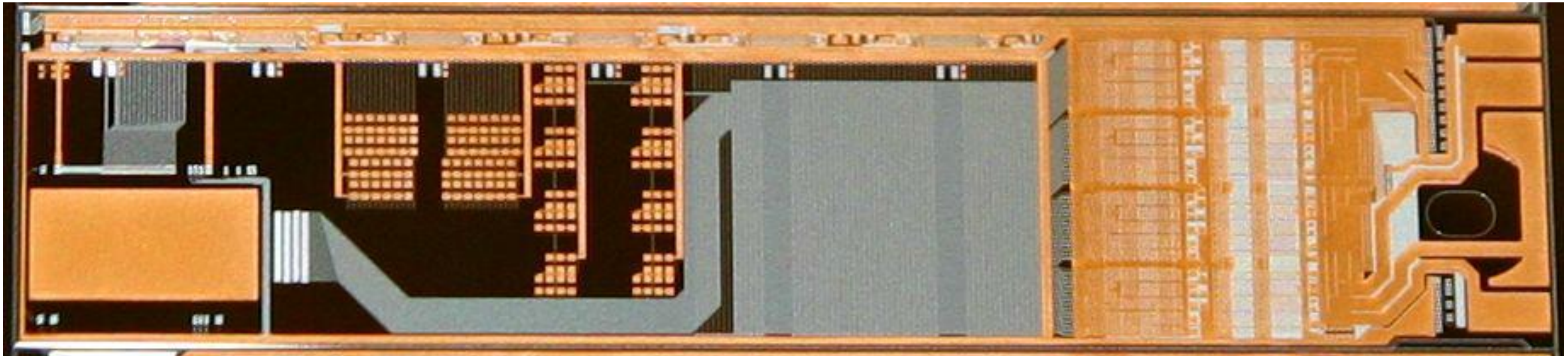
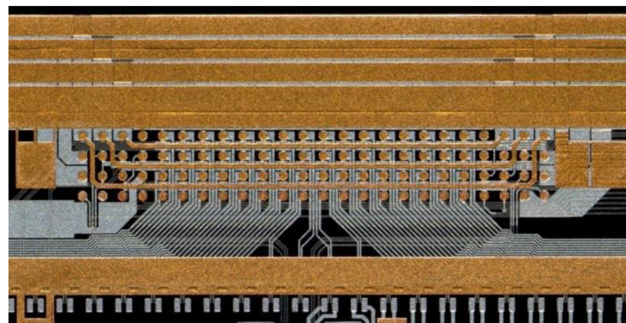
E-MCM in reality

→ **Modules produced, tested and ready for flip chip**





Detail of the Switcher landing area

↘ 4-fold readout possible

→ Two times faster frame readout keeping the row rate

Summary

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- The DEPFET Collaboration is developing ultra-transparent pixel sensors with integrated amplification
- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated
- The Belle II PXD boosted the development of DEPFET detectors
  → Direct benefit towards the ILC-VXD project (ILD-VXD layer concept '*engineered*')
- Building a real system: Every detail (although not covered here) is being considered
  → Interconnection technologies, rad. Hardness, cooling, mechanics, … (see backup)

→ For more detailed information: "DEPFET active pixel detectors for a future linear e+e- collider". M. Vos *et al*. arXiv:1212.2160

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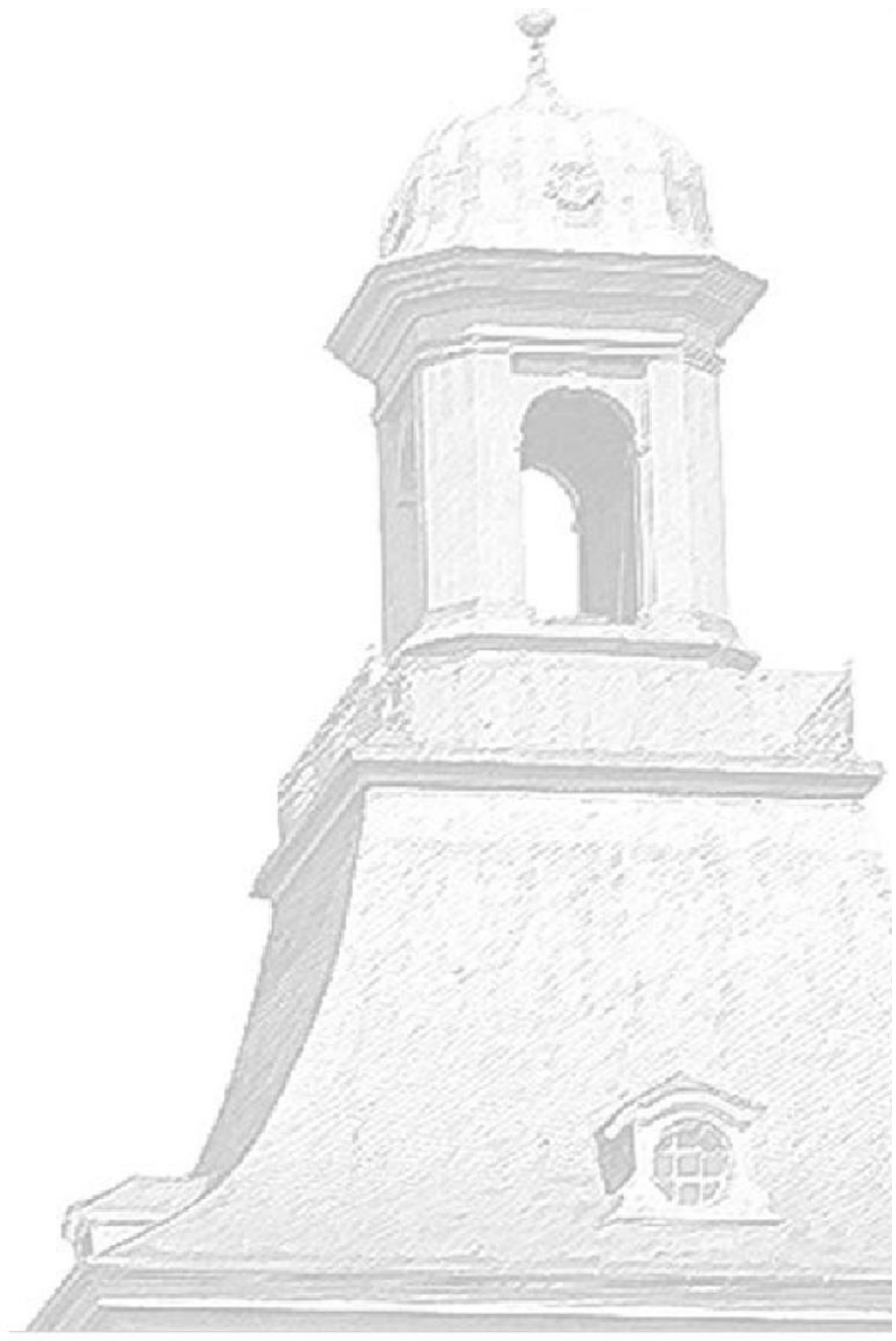
DEPFET

Active Pixel Detector

Thank you



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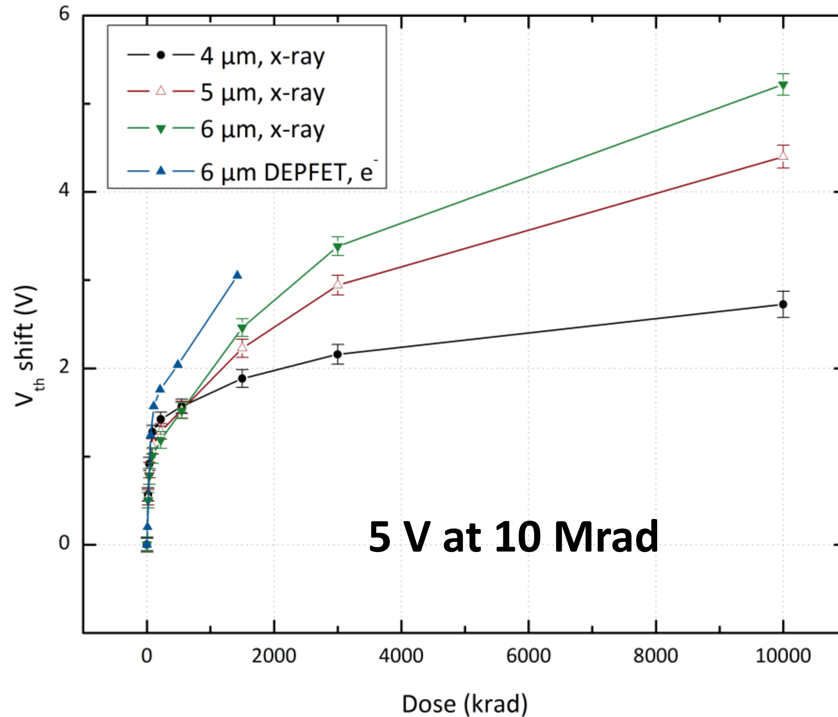
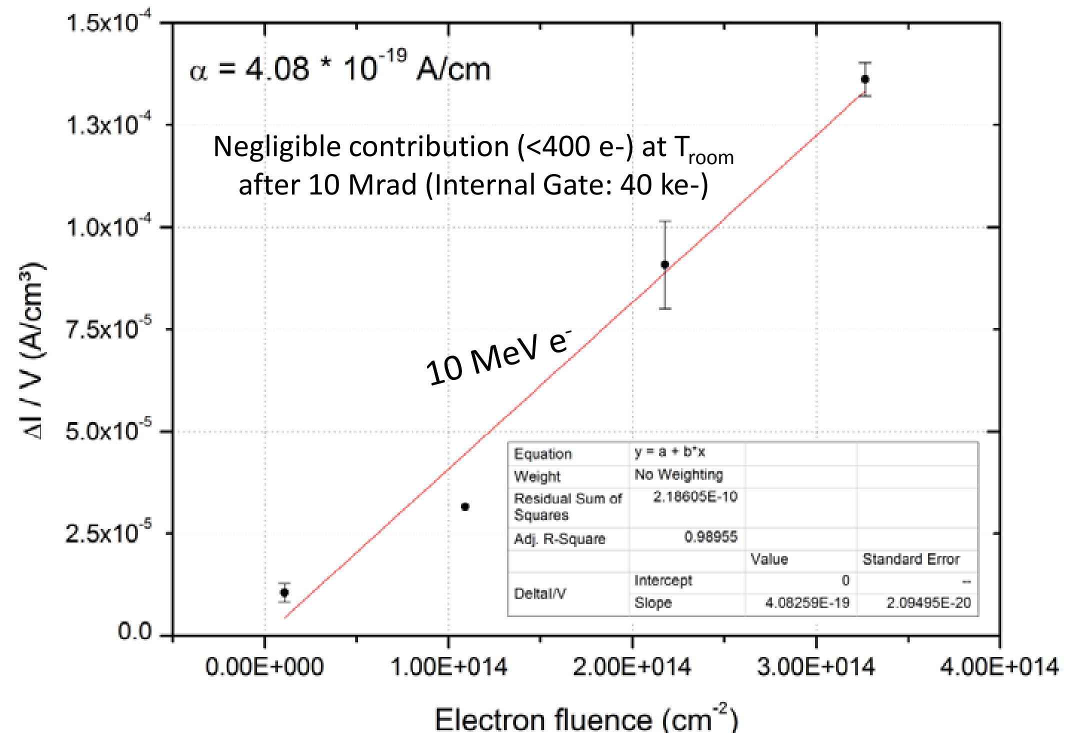
Radiation hardness

Oxide damage at Gates



Bulk damage



Damage constant: α_{el}=4.2·10^{-19} A/cm

Damage constant: α_{n}=4.0·10^{-17} A/cm

→ Hardness factor is lower than expected

$$\kappa_{meas} = \frac{\alpha(10MeVe^{-})}{\alpha(1MeVn)} = 0.014$$

$$\kappa_{theo} = \frac{NIEL(10MeVe^{-})}{NIEL(1MeVn)} = 0.06$$

✓ Relaxed bulk damage

✓ Threshold voltage shift can be handled by the system

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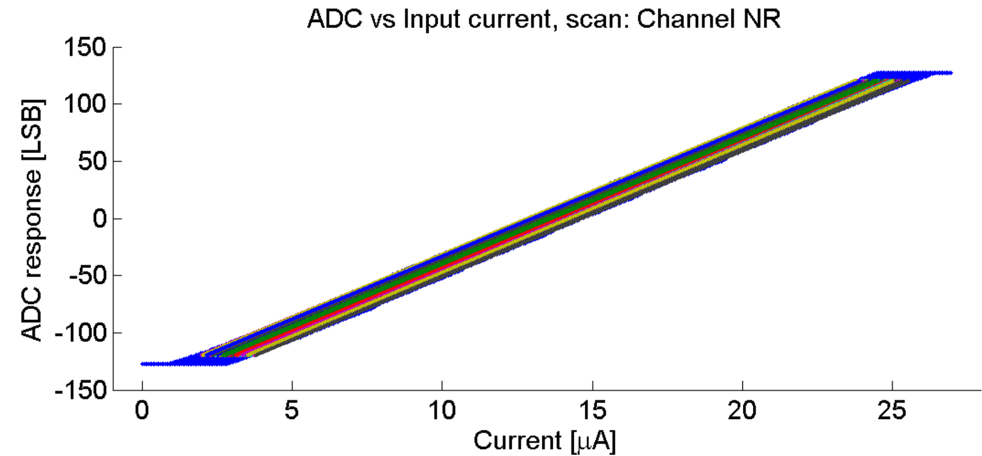
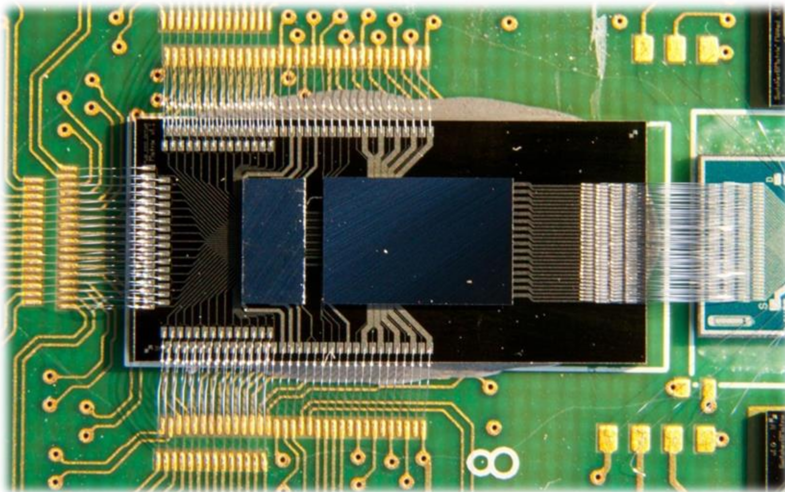
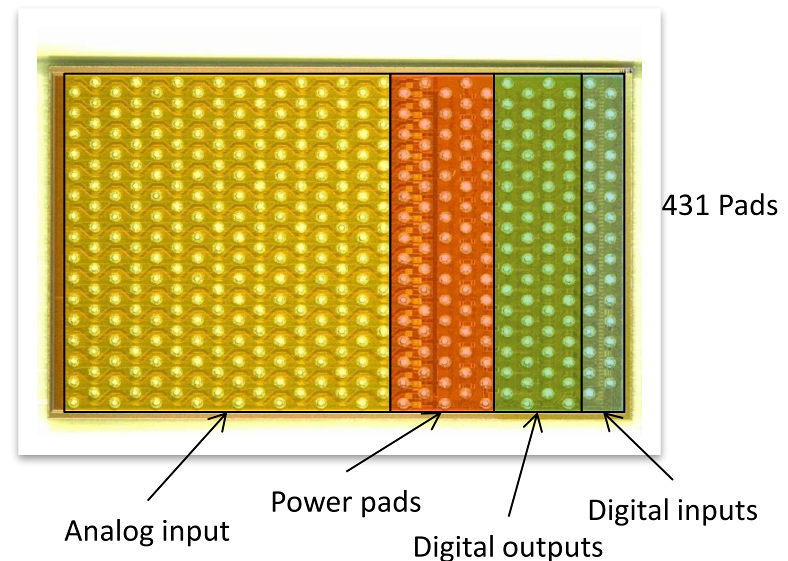
DCDB

Drain Current Digitizer for Belle II

- 512 ADCs
- Cyclic conversion
- 320 MHz clocked
- 100 ns conversion time
- Mean INL < 1.5LSB (Max <2.2 LSB)
- Gain variation < 5% (peak to peak)







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DCD Channel Layout

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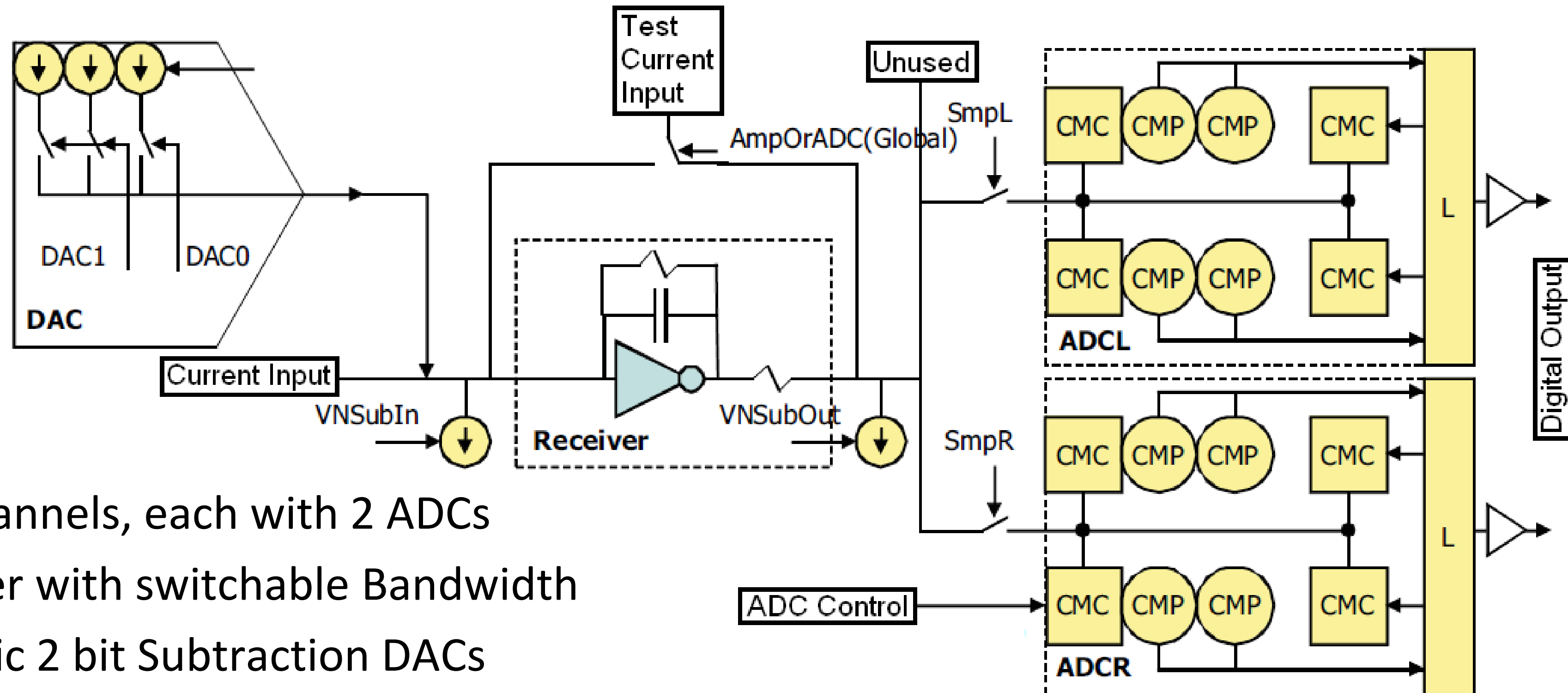


- 256 Channels, each with 2 ADCs
- Receiver with switchable Bandwidth
- Dynamic 2 bit Subtraction DACs
- ADC Operation
  1. Sample input current with two Current Memory Cells (CMC1 and CMC2)
  2. Compare Current from one CMC to low/high threshold
  3. If above/below low/high threshold, activate add/subtract current sources
  4. Copy current from CMC1, CMC2 and extra current sources to CMC3 and CMC4.
  5. Repeat from Step 2 (with CMC3 and CMC 4)

DHP 0.2

768x256
DEPFET Matrix

10Mhz read-out frequency

DCD chip
256 inputs, 8-bit ADC per input
4:1 output MUX

81.29Gbps
(320Mbps output data x 256 lines)

Deserializer

Switcher sequencer

Raw data memory

Pedestal memory

Pedestal subtraction

Common mode correction

FIFO 1

Analog blocks

Hit finder

FIFO 2

Link layer framing

8b/10b protocol

JTAG

DHP

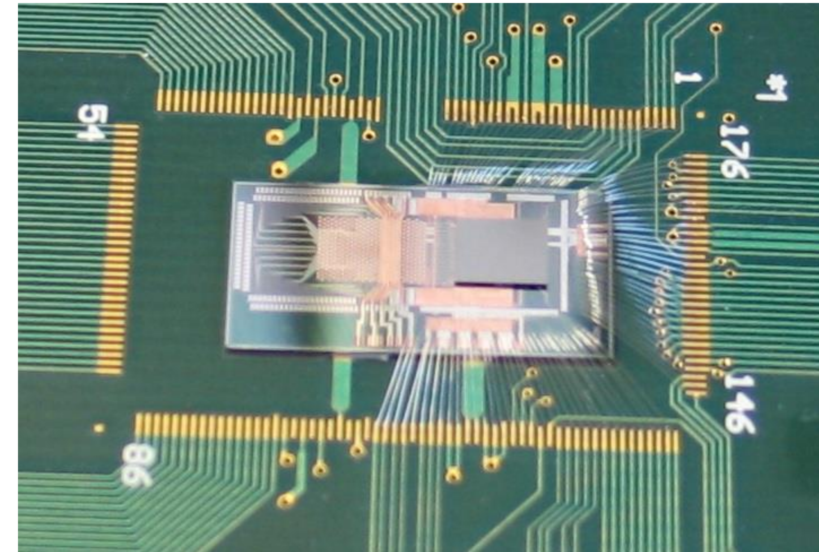
PLL

Gbit TX

Trigger

4x1.6Gbit output

One 1.6GB output link per chip



Data Handling Processor

- Digital common mode subtraction
- Digital pedestal compensation
- Zero suppression
- First full size chip
- Switcher control
- 1.6 Gb serial link
- 3 % occupancy with <1% data loss

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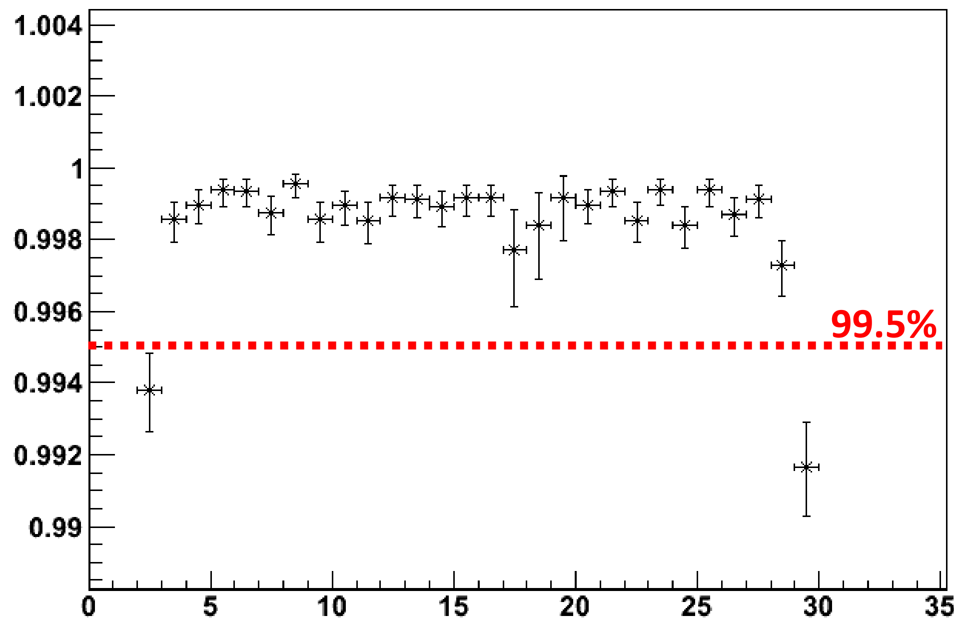
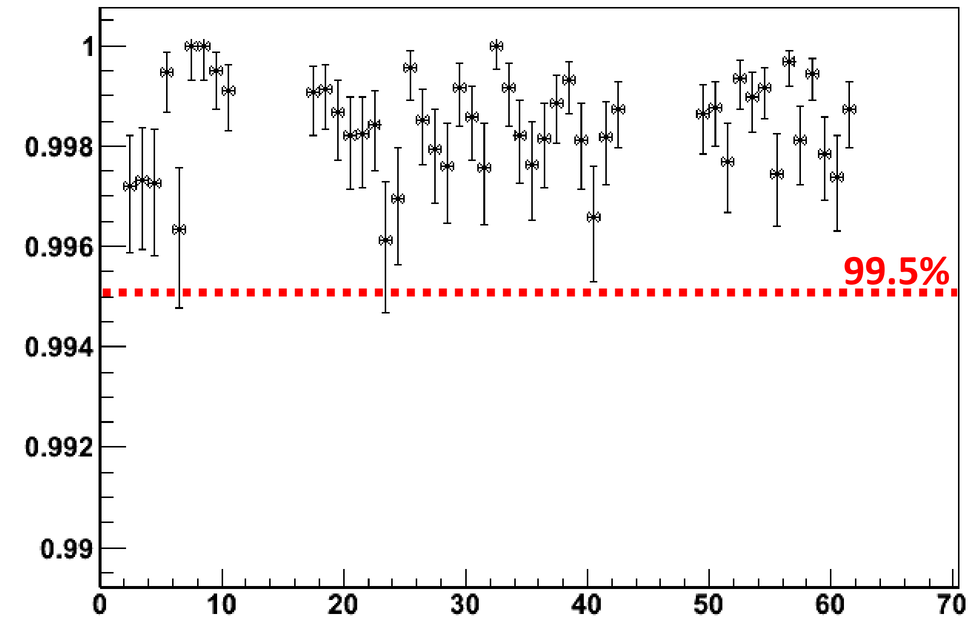
Detection efficiency





→ The efficiency is higher, both column and row wise, than 99.5%

Building the Belle II PXD

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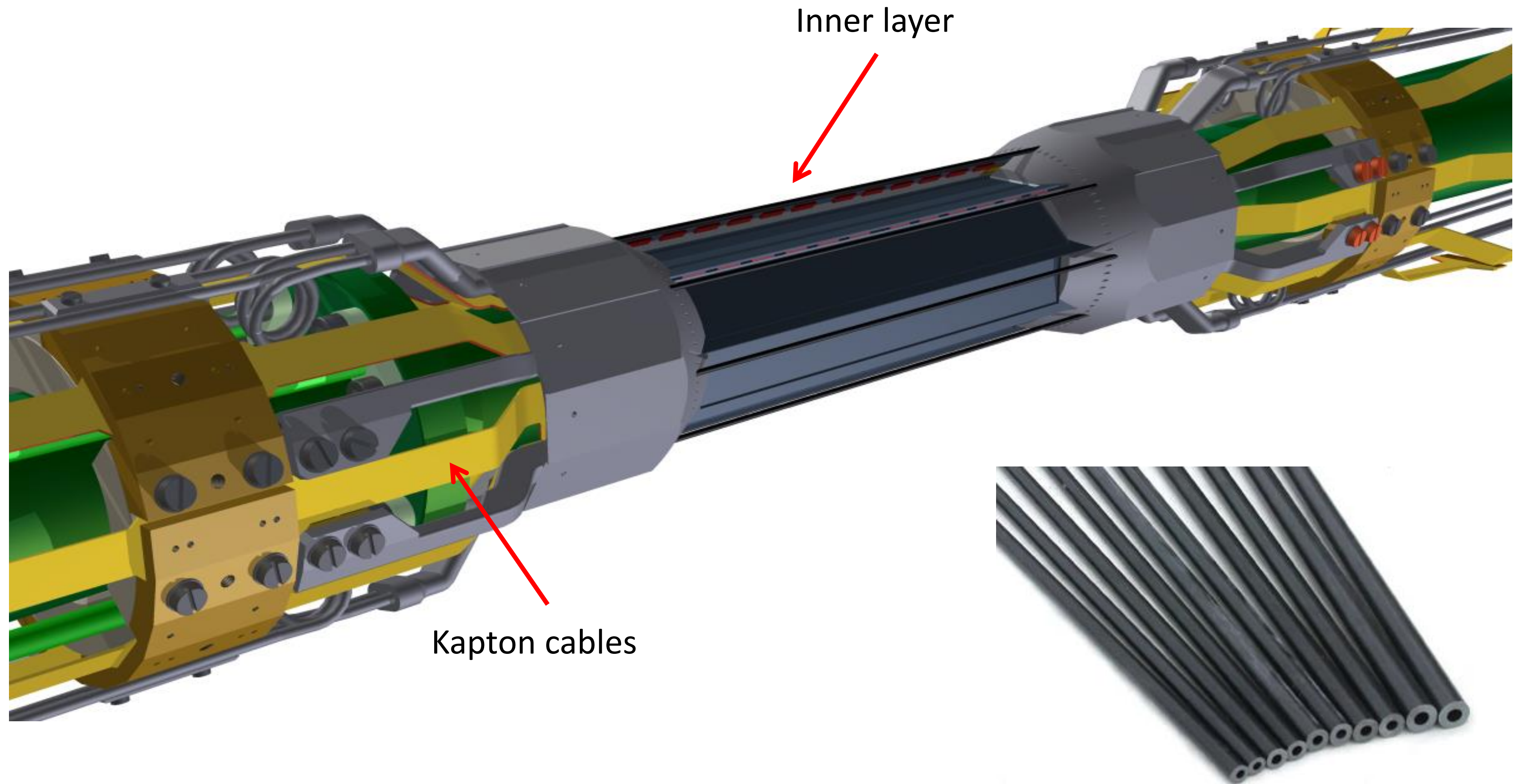

Inner layer close to the IP (14mm)

Additional carbon fibers capillaries to cool the Switchers, if needed (not tested yet)

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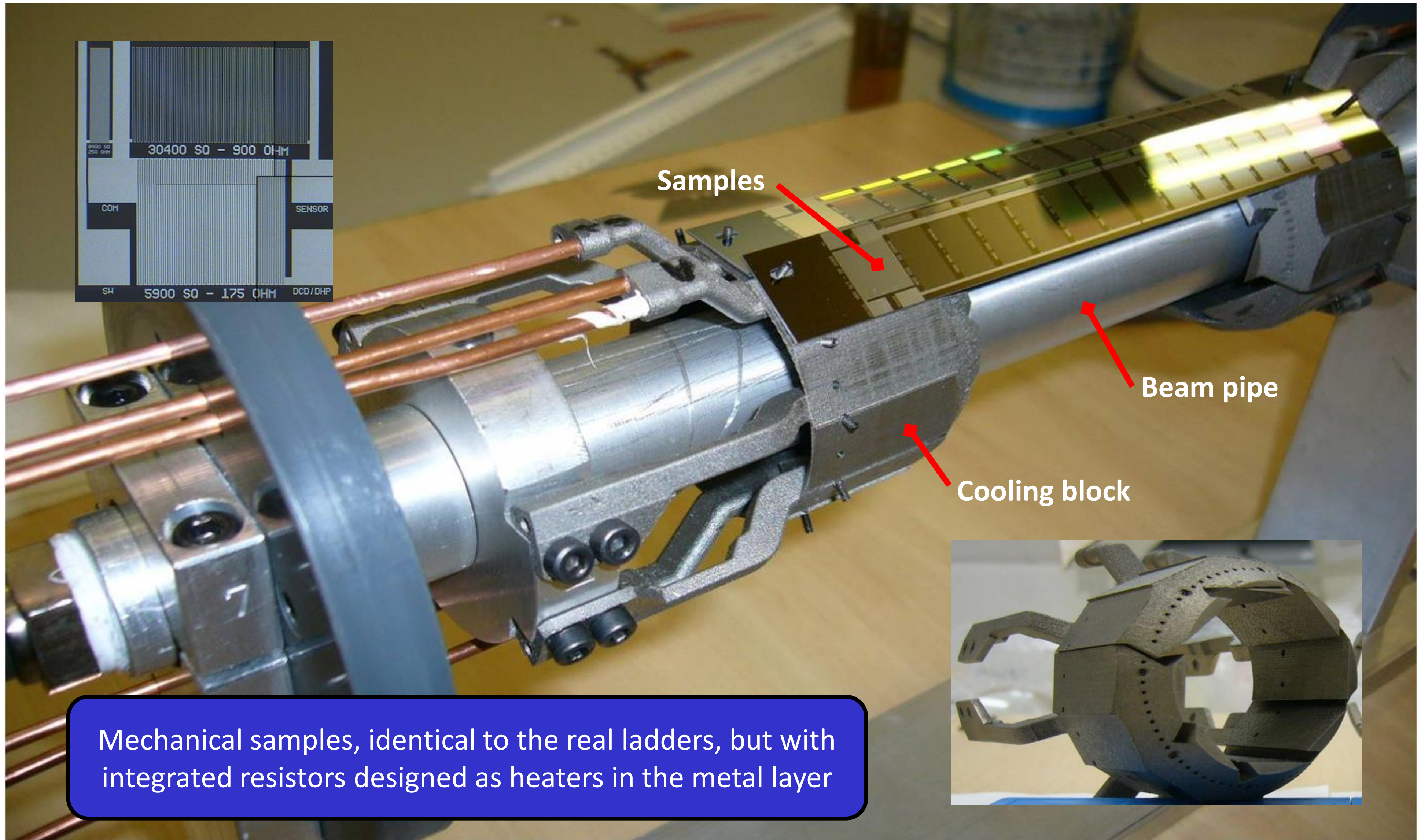
Measurements with mockup



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Thermo-mechanical measurements

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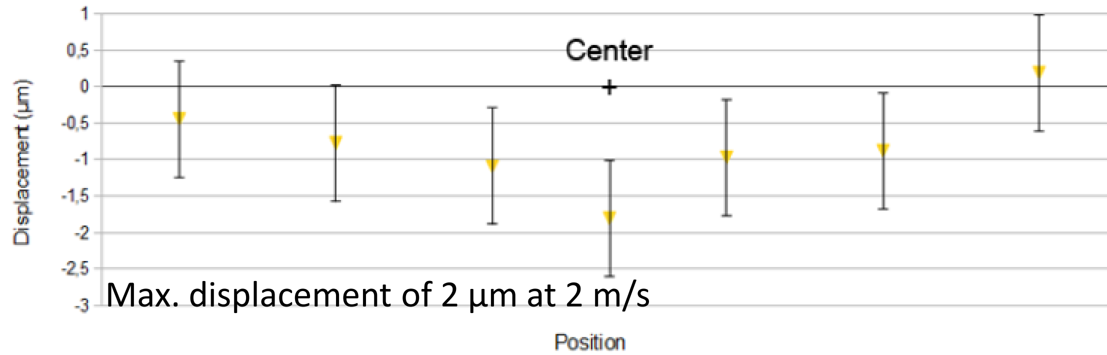
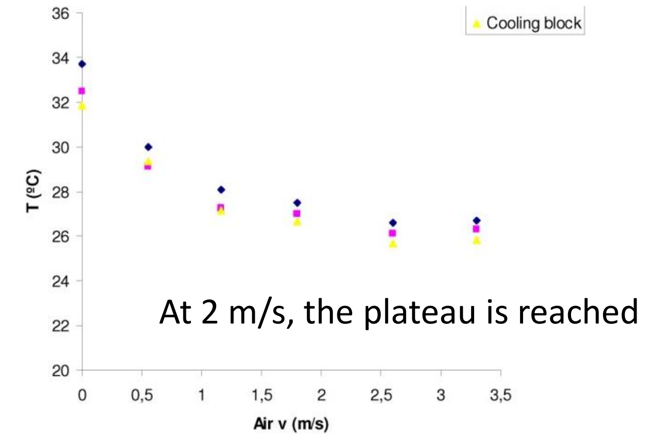
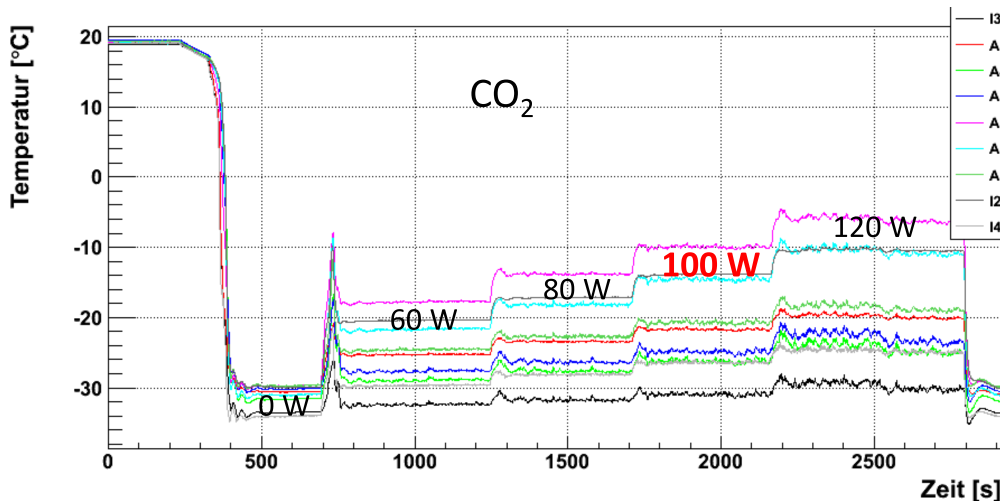
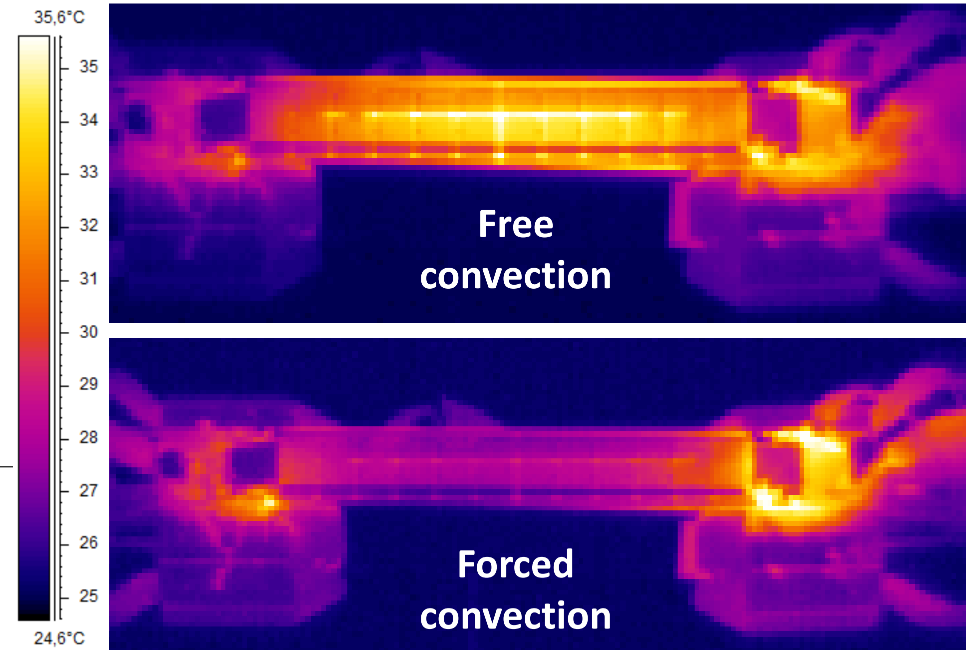




- Stainless steel
- Fast sintering
- Blue: CO_2 capillaries
- Yellow: Air channels





Cooling proof of principle

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ILC scenario: Power cycle and air only

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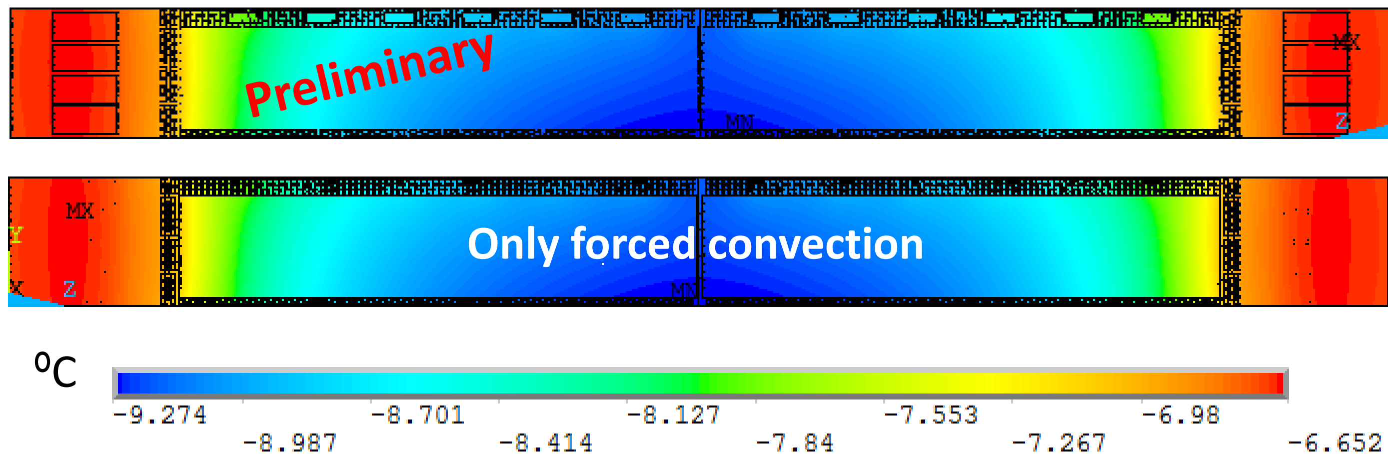
↘ Naïve approach using the XFEL hands-on:

- The power consumptions are weighted accordingly to the estimated duty cycle.

  → Completely shutting down the DEPFET and the analogue part of the electronics between trains → 1/25 power reduction if 1/100 duty cycle



- Tenv= -10 ⁰C
- Vair=2 m/s

The air speed and temperature are not optimized to minimize the temperature distribution

P_{FE}=(0.5/25.) W / per chip

P_{Sw}=(0.1/25.) W / per chip

P_{Sensor}=(1./25.) W in total

↘ Although <u>very</u> preliminary, the cooling seems feasible so far

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Material budget

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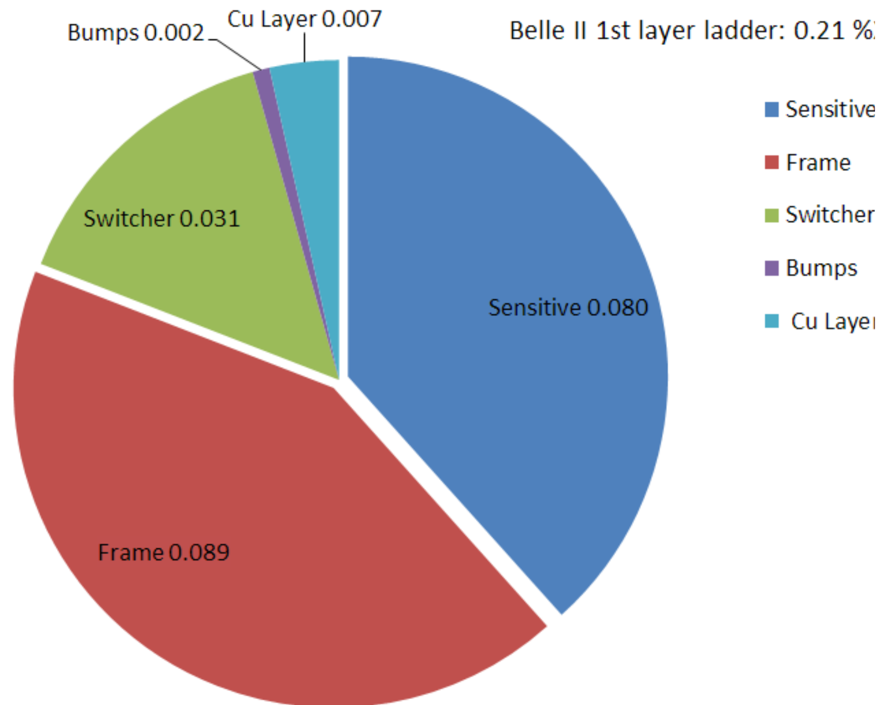

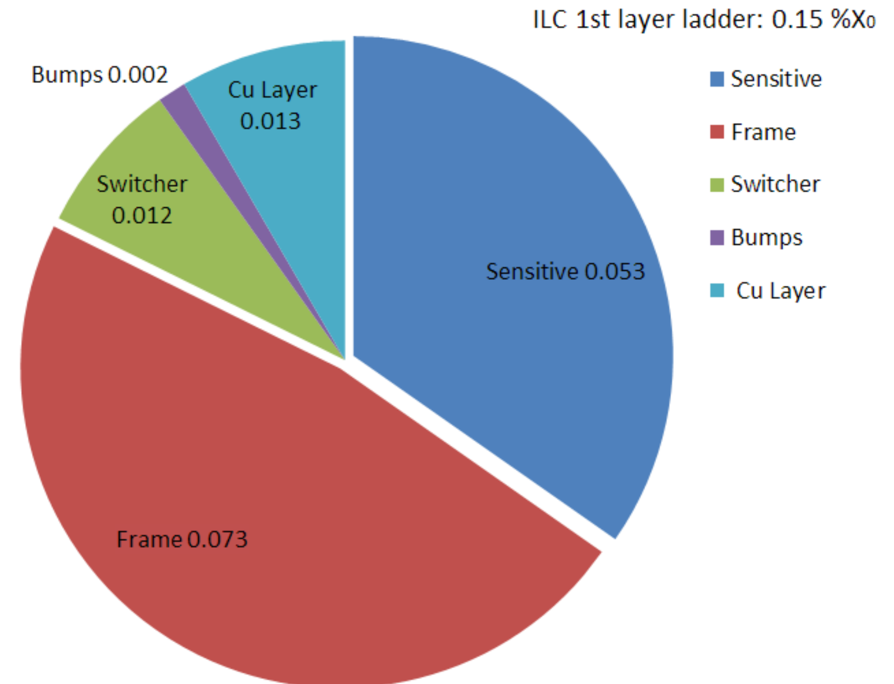

	Belle II	ILC
Frame thickness	525 µm	450µm
Sensitive layer	75 µm	50µm
Switcher thickness	500µm	100µm
Cu layer	only on periphery	50% cover over all
Total	0.21 %X0	0.15 %X0

ILD 3 double layer VXD option

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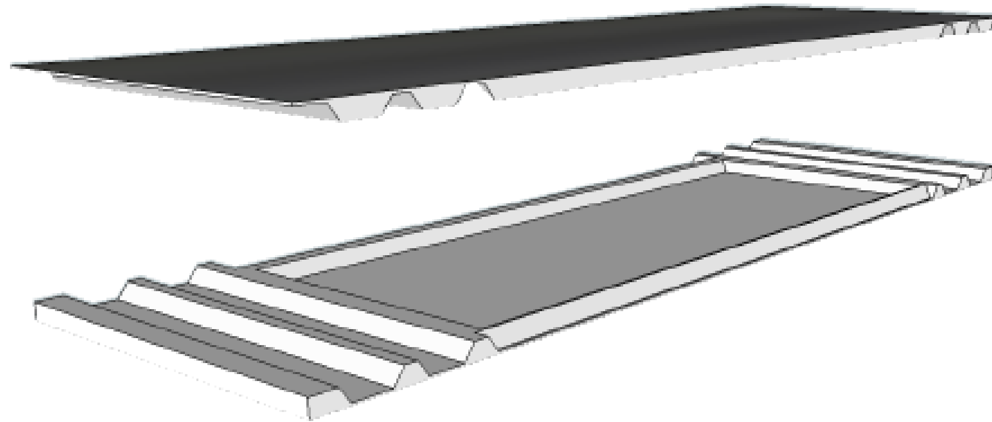
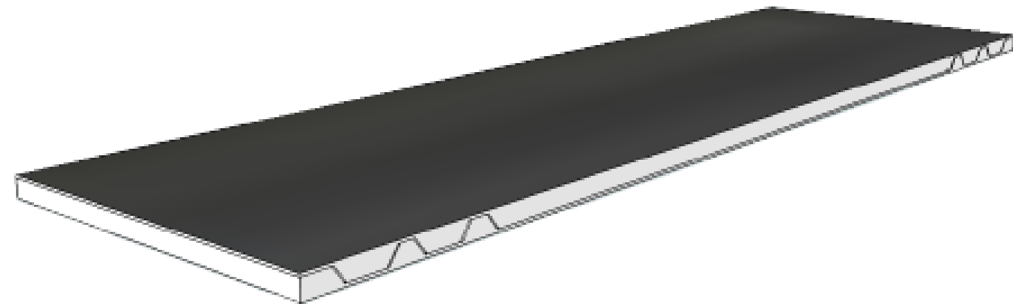


- Complementary etch grooves in support frames
- Same process step as thinning and micro-joint (Belle II)
- Adhesive joint between layers



- DEPFET technology is NOT linked only to the 5 layer VXD option
- Single ladder engineered to a large extent
- Double layer still needs R&D