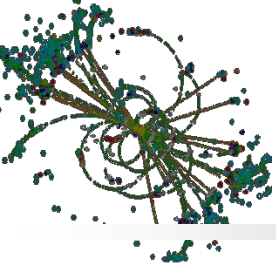

Vertex Detector R&D

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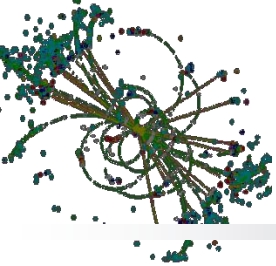
EE work is contracted to Sarnoff Corporation

Outline of the talk

- Why Chronopixel as Vertex Detector sensor ?
- Project milestones.
- Prototype 1 design and problems
- What is new in prototype 2
- Results of the second prototype tests.
  - Comparators offset calibration
  - Noise and cross-talks
  - Sensor capacitance
  - Power dissipation
- Suggestions for prototype 3
- Conclusions and plans



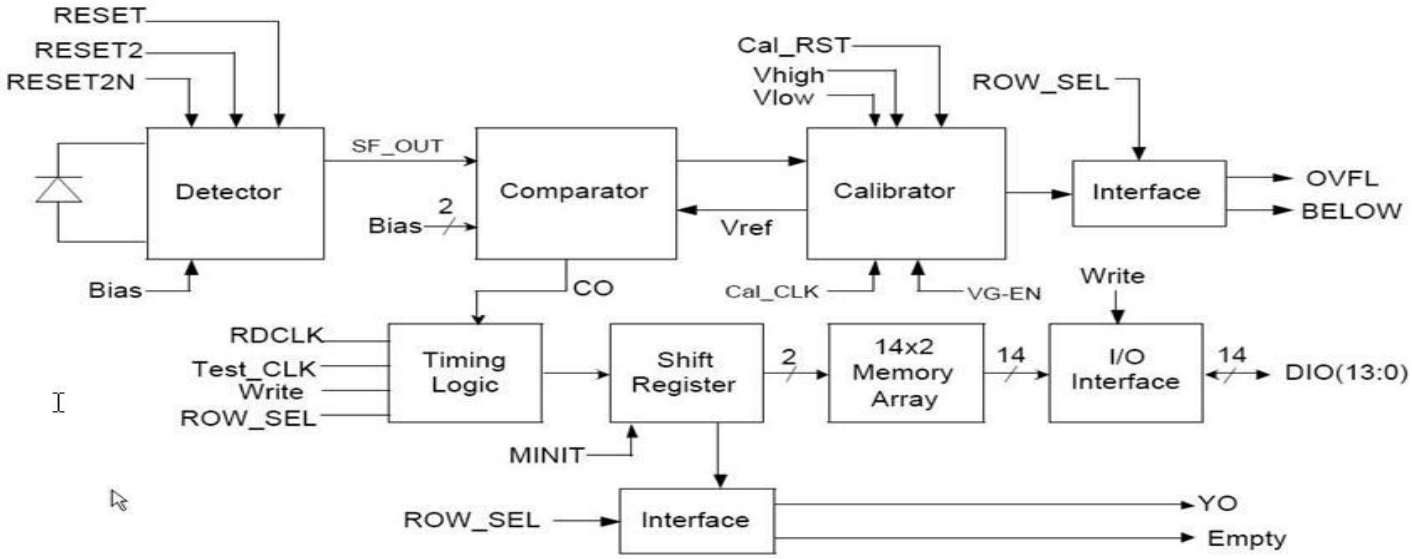
Why chronopixel?

- **Need for pixel detector with good time resolution:**
  - **Background hits density in ILC environment is of the order of 0.03 hits/mm^2 per bunch.**
  - **Bunch train at ILC, which lasts only 1 ms, has about 3000 bunches ⇒ 100 hits/mm^2 – too high for comfortable track reconstruction.**
  - **So we need to slice this array of hits into at least 100 time slices, and reconstruct tracks from hits belonging to the same slice. To do this, we need to know time of each hit with at least 10 μs accuracy.**
- **CCDs, often used as pixel detectors, by the nature of their readout, are very slow. Row by row readout takes tens if not hundreds of ms to read image. So we would integrate the entire bunch train in one readout frame.**
- **There is a number of pixel sensor R&D addressing this problem – CPCCD, different types of monolithic designs (readout electronics on the same chip as sensor), 3D technology. Neither of them (except, may be 3D) allows assigning time stamp to each hit.**
- **Chronopixel project was conceived to provide such ability.**
- **Chronopixel is a monolithic CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.**

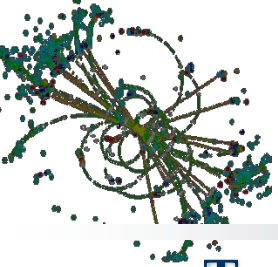
Timeline

- **2004 – talks with Sarnoff Corporation started.**
  - Oregon University, Yale University and Sarnoff Corporation collaboration formed.
- **January, 2007**
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
- **May 2008**
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
- **October 2008**
  - Design of test boards started at SLAC
- **September 2009**
  - Chronopixel chip tests started
- **March 2010**
  - Tests completed, report written
- **May 2010**
  - Second prototype design started
- **September 2010**
  - contract with Sarnoff for developing of second prototype signed.
- **October 2010**
  - Sarnoff works stalled
- **September 2011**
  - Sarnoff resumed work.
- **February 2012**
  - Submitted to MOSIS for production at TSMC. (47x47 array of 25 μm pixel, 90 nm process)
  - Modification of the test stand started as all signal specifications were defined.
- **June 6, 2012**
  - 11 packaged chips delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
  - Tests at SLAC started
- **March 2013**
  - Test results are discussed with Sarnoff and prototype 3 design features defined
- **May 2013**
  - Contract with Sarnoff (SRI International) in the signing. Packaged chip delivery – January 2014.

First prototype design



- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with Sarnoff company.
- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.
- If another particle hits the same pixel during the same bunch train, second memory cell is used for this event time stamp.
- During readout, which happens between bunch trains, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.
- Comparator offsets of individual pixels are determined in the calibration cycle, stored in digital form, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.
- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.



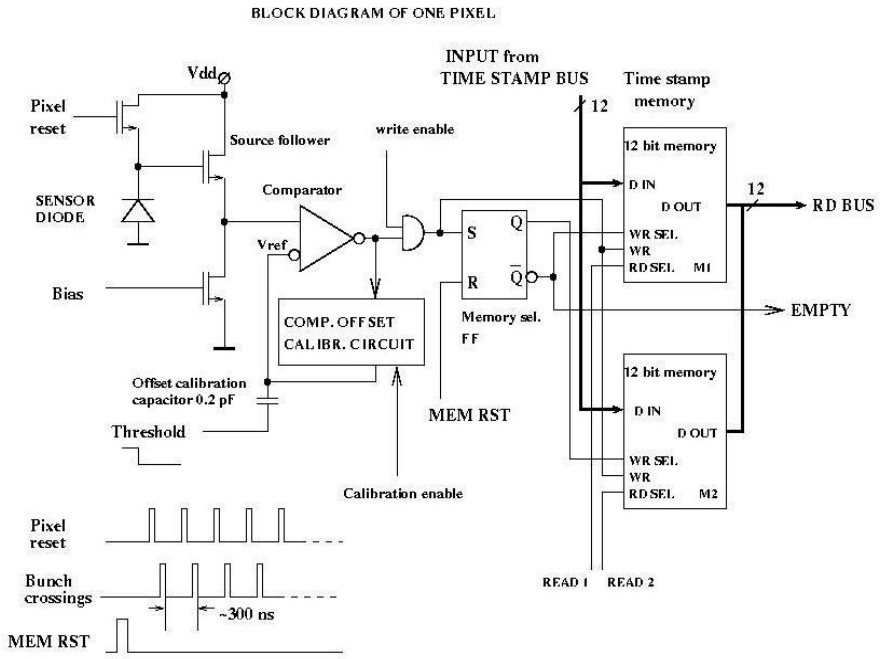
Conclusions from prototype 1 tests

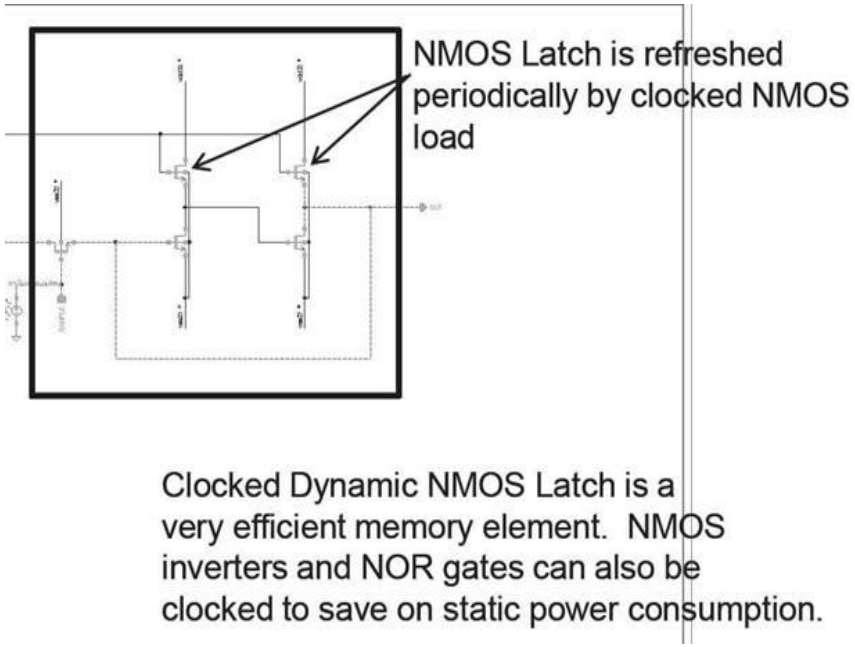
- Tests of the first chronopixel prototypes are now completed.
- Tests show that general concept is working.
- Mistake was made in the power distribution net on the chip, which led to only small portion of it is operational.
- Calibration circuit works as expected in test pixels, but for unknown reason does not work in pixels array.
- Noise figure with "soft reset" is within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e). Reduction of sensor capacitance (increasing sensitivity) may help in bringing it within specs.
- Sensors leakage currents ($1.8 \cdot 10^{-8} A/cm^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.
- No problems with pulsing analog power.

Prototype 2 features

- Design of the next prototype was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all electronics inside pixels only from NMOS transistors. It can allow us to have 100% charge collection without use of deep P-well technology, which is expensive and rare. To reduce all NMOS logics power consumption, dynamic memory cells design was proposed by SARNOFF.
- New comparator offset compensation ("calibration") scheme was suggested, which does not have limitation in the range of the offset voltages it can compensate.
- We agreed not to implement sparse readout in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.
- In September of 2011 Sarnoff suggested to build next prototype on 90 nm technology, which will allow to reduce pixel size to 25μ x 25μ
- We agreed to have small fraction of the electronics inside pixel to have PMOS transistors. Though it will reduce charge collection efficiency, but will simplify comparator design. It is very difficult to build good comparator with low power consumption on NMOS only transistors.

Prototype 2 design

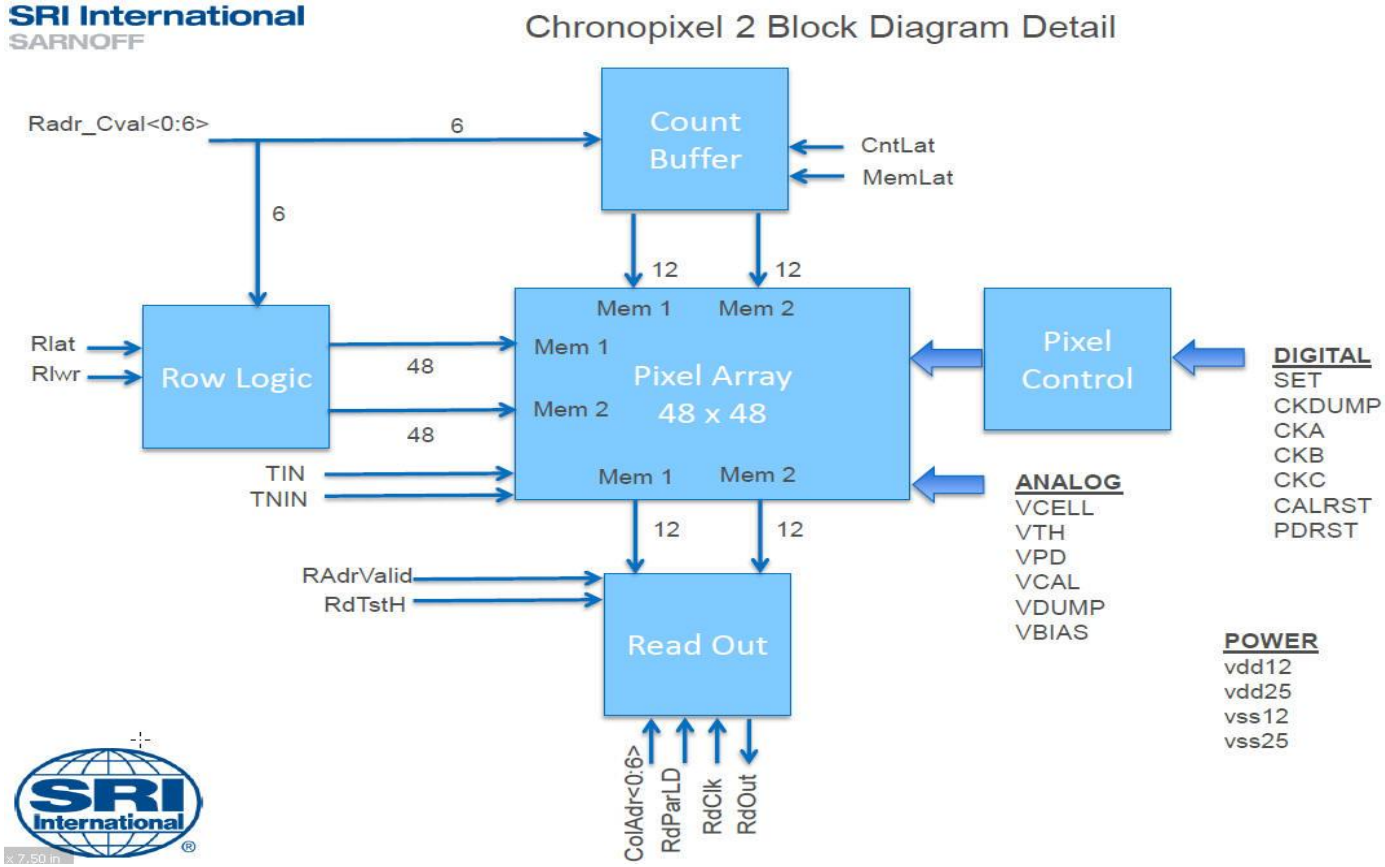




Comparator offset calibration circuit charges calibration capacitor to the value needed to compensate for the spread of transistor parameters in individual pixels. We needed to prove, that the voltage on this capacitor will stay unchanged for the duration of bunch train (1 ms).

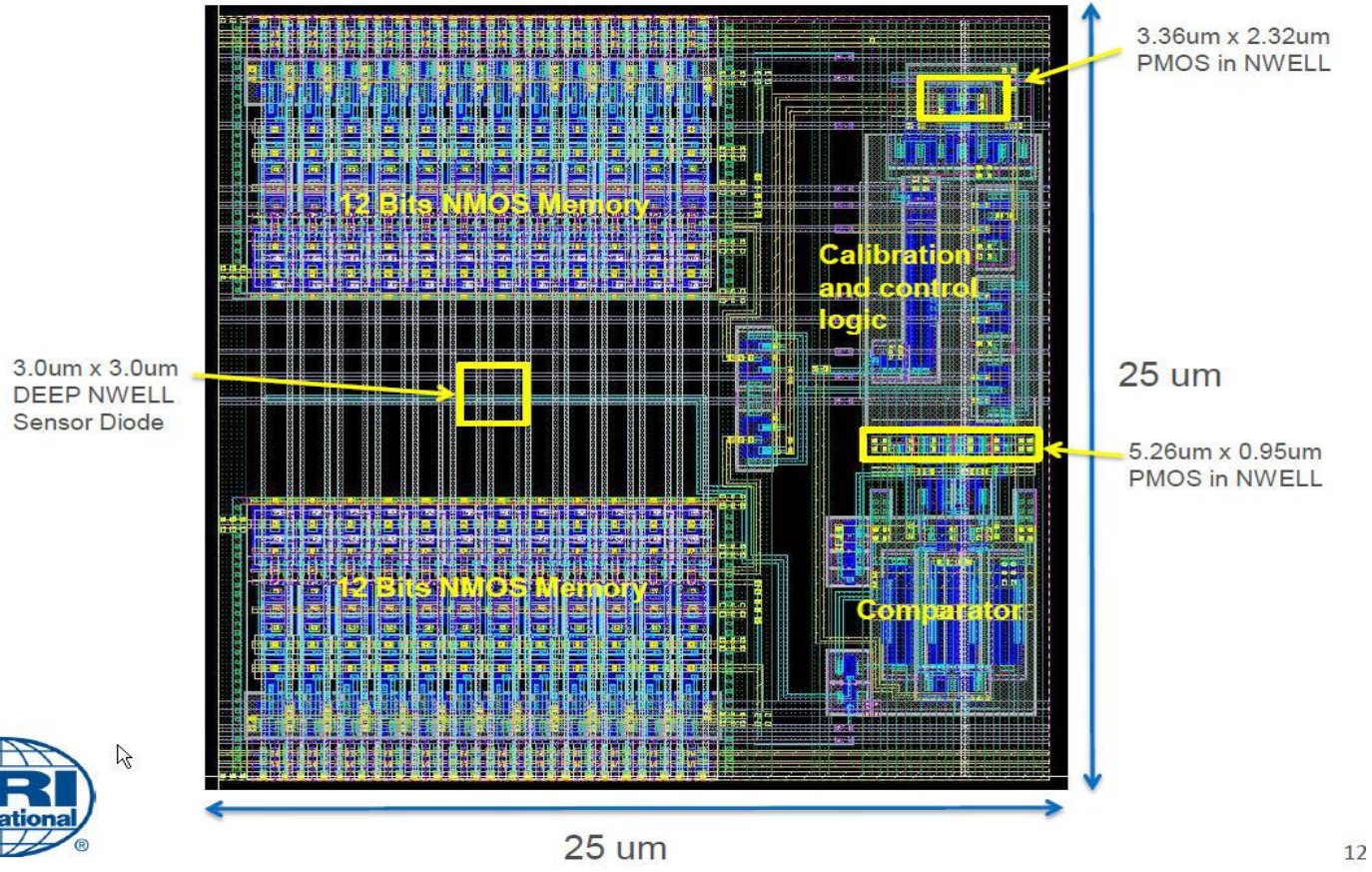
Proposed dynamic latch (memory cell) has technical problem in achieving very low power consumption. The problem is in the fact, that NMOS loads can't have very low current in conducting state – lower practical limit is 3-5μA. This necessitate in the use of very short pulses for refreshing to keep power within specified limit. However, we have suggested solution to this problem, which allows to reduce average current to required value without need for short pulses.

Prototype 2 chip



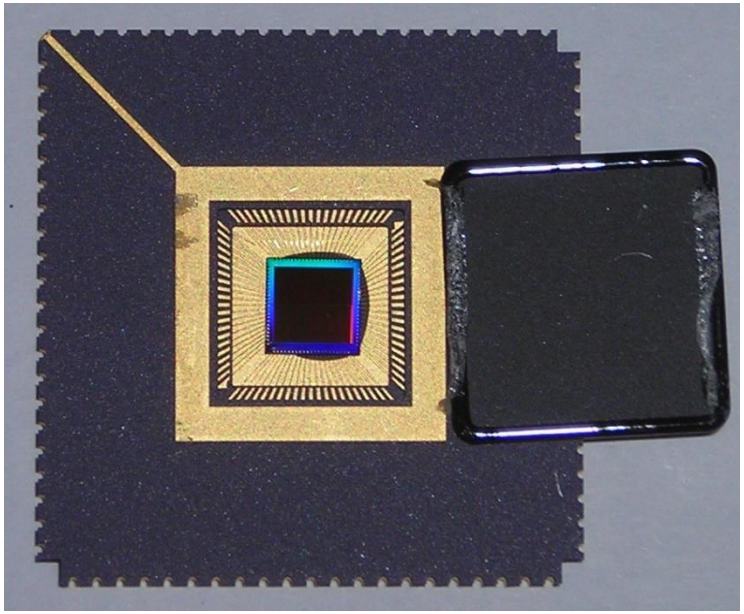
One of the technical problems was in the size of the chip – to make production cheaper we agreed to limit chip size to 1.2x1.2 mm^2 . This limits the number of pads on the chip to not more than 40. And that leads to the need of multiplexing some signals – for example, 12 bit time stamp is provided via 6 bit Radr_Cval bus with most significant bits on the high phase of CntLat signal and least significant – on low, with de-multiplexing in Count Buffer.

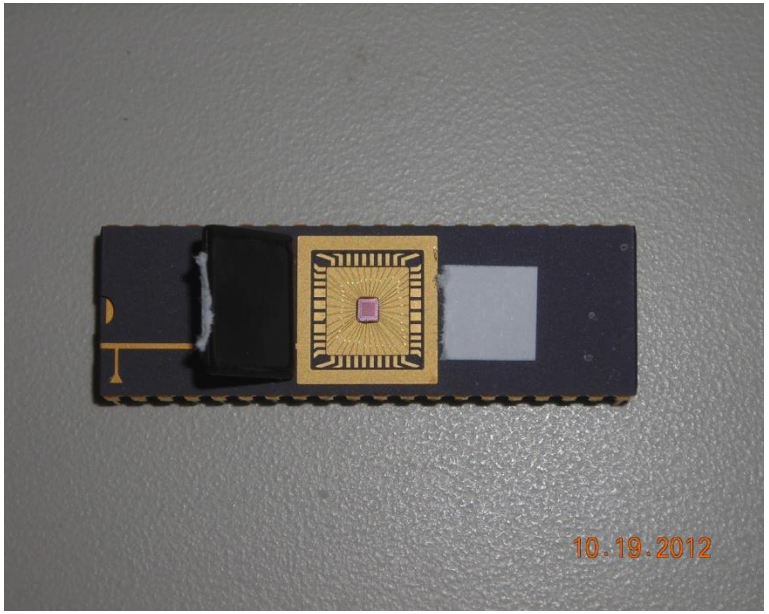
Prototype 2 pixel layout



All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to 4x5.5 μ^2 .

Prototypes 1 and 2





- **Because of much smaller chip size for prototype 2, there is not enough room on chip periphery to make 84 pads, as it was in prototype 1. So, 40 pads and 40 pins package were used.**

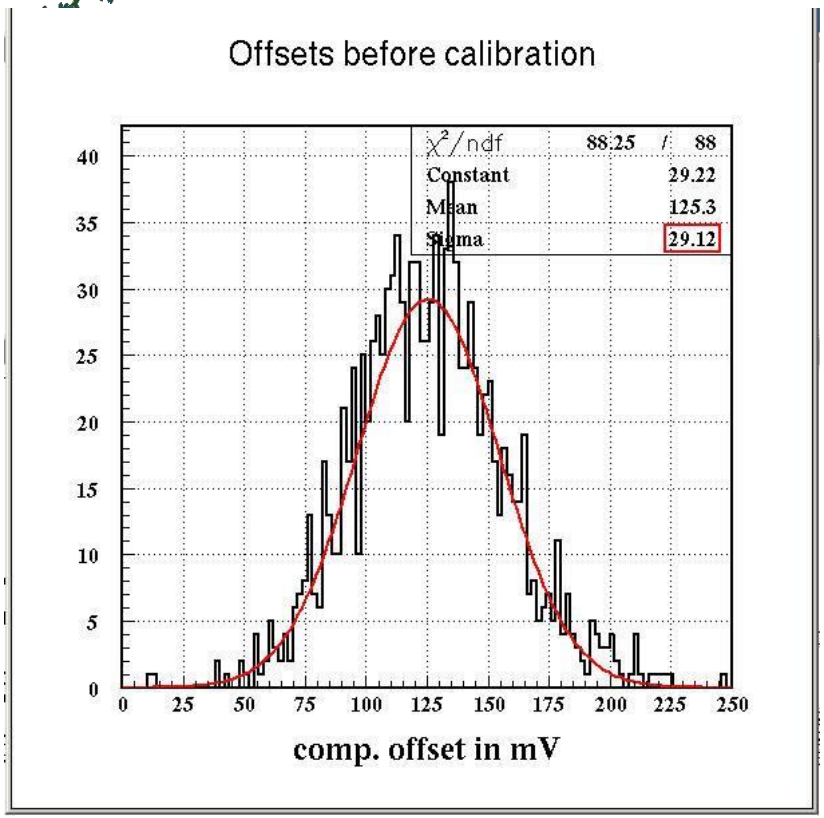
Price for allowing PMOS in pixels

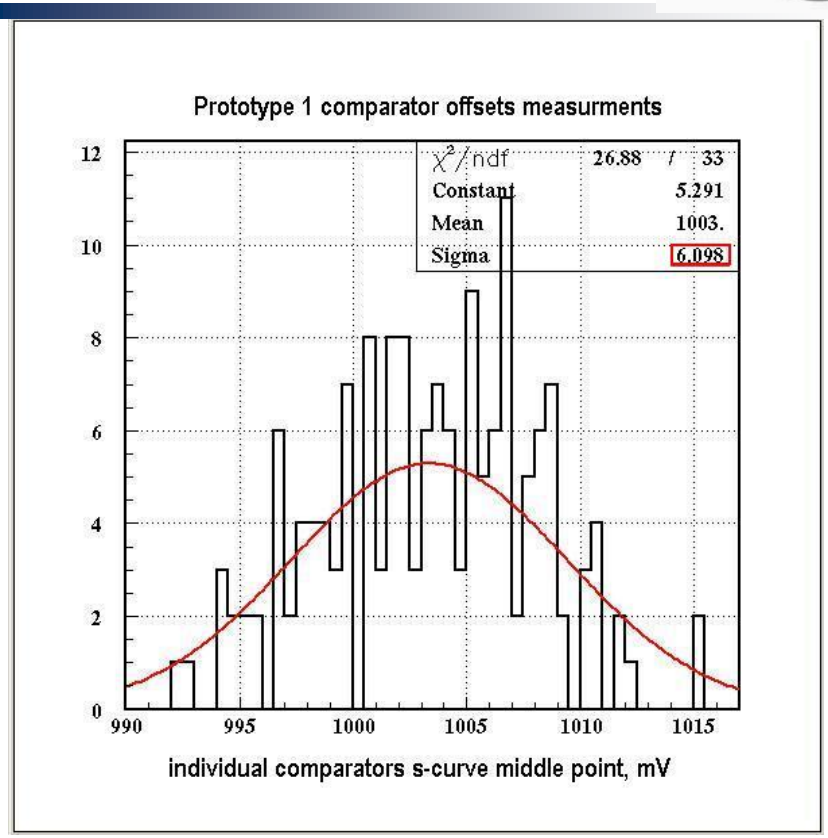
- Because of shorter channels and lower voltage in 90 nm technology, it is very difficult to build comparator with large gain and low power consumption, using only NMOS transistors.
- So, we decided to allow use of PMOS transistors inside pixels, but minimize their use only to comparators.
- It will reduce charge collection efficiency to $S_{se}/(S_{pm}+S_{se})$, where S_{se} is sensor electrode area and S_{pm} is the area of all PMOS transistors in the pixel. We hoped to have the S_{pm} to be around $1\mu^2$. However in the final Sarnoff design this area appeared to be close to $12\ \mu^2$. To reduce noise we want to reduce S_{se} from about $100\ \mu^2$ as it was in the first prototype to something like $25\ \mu^2$.
- From this, we can expect our charge collection efficiency be only about 67.5%.
- However, we need to add width of depleted layer to electrode areas. It will reduce area ratio and reduce charge collection efficiency. But taking into account larger depth of the signal charge collection electrode will increase efficiency.
- Next slides show simulation of prototype 2 performance

Pixel variations

- As soon as Sarnoff design manager gave me final schematics, I started SPICE simulation of it performance to double check their simulations. Suggested by them comparator design did not pass my check – it appeared very sensitive to the rise time of the latch signal. So I insisted that they use old (prototype 1) comparator, which did not have such a problem. But they also wanted to test their new design as they believed that with additional latch signal shaping it should work and it have better switching characteristics. So, we agreed to have half of the pixels have their new design.
- They wanted to have charge collection electrode only 3x3 μ^2 to have low noise level. However, with 12 μ^2 of PMOS transistors in the pixel would lead to charge collection efficiency less than 50% . From my calculations of noise and charge collection efficiency the optimal (providing maximum signal/noise ratio) charge collection electrode should have about 22 μ^2 area. So, we decided to have half of the pixels with 9 μ^2 charge collection electrode area (to check how much it helps with noise reduction), and half – with 22 μ^2 .
- That leads to 4 different variants of the pixel, which will be implemented in each chip.

Test results - calibration

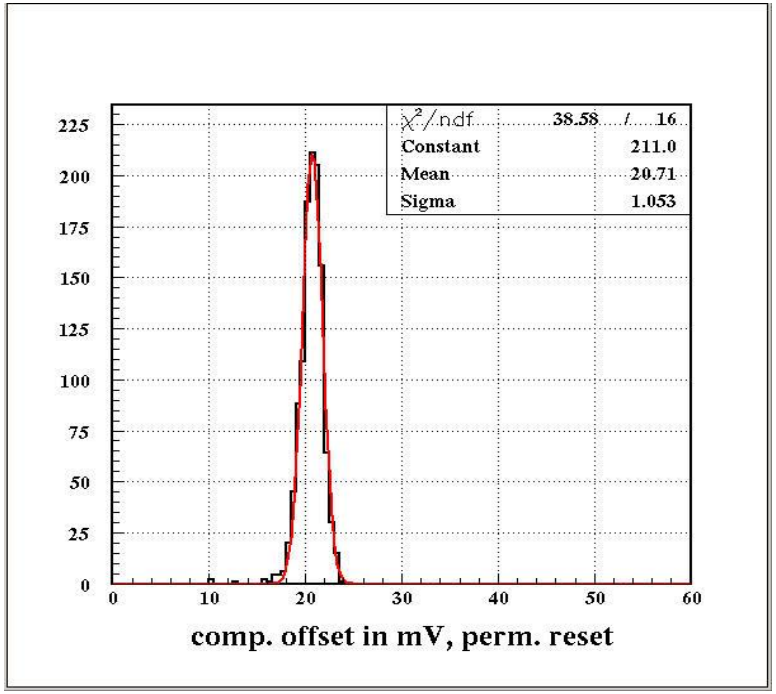


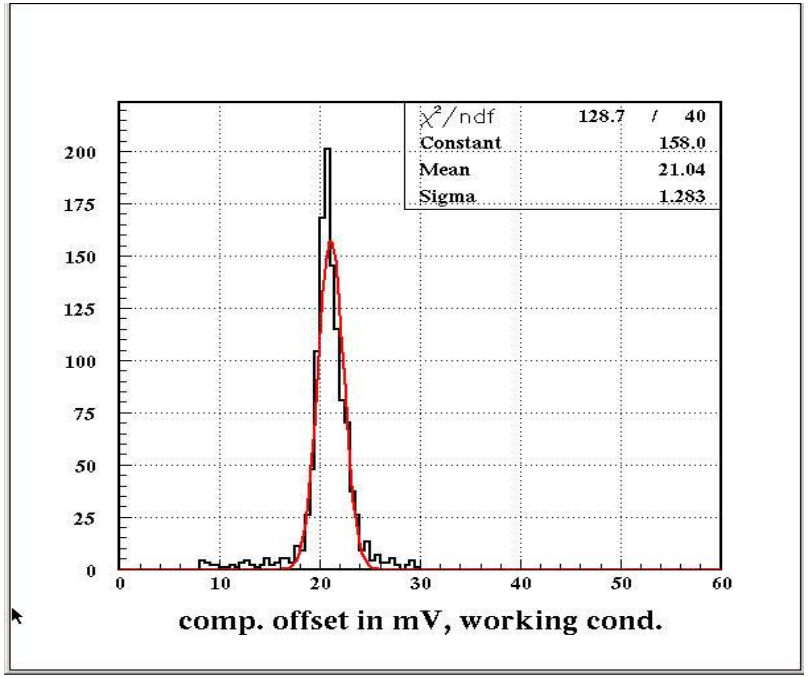


Prototype 2 **Prototype 1**

Comparator offsets spread comparison. Because of smaller feature size, it is more difficult to keep transistor parameters close to design values and different transistor with same design parameters in reality behave differently. This leads to the comparator offsets spread in prototype 2 almost 5 times larger than in prototype 1

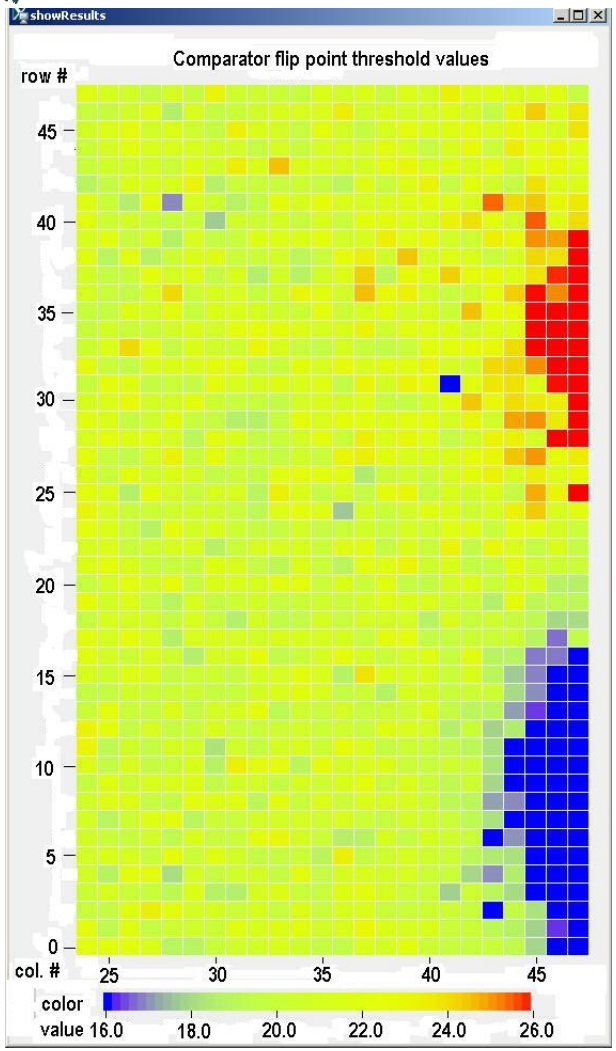
Comparator offsets calibration





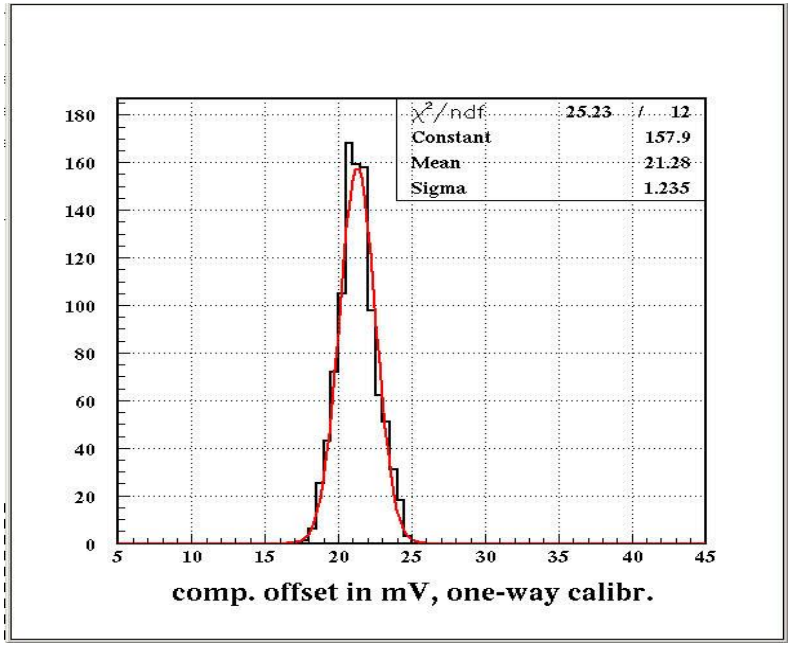
- To test how well comparator offset calibration (compensation) works, we first tried it with sensor permanently in reset state (connected to photodiode bias voltage). For convenience of measurements, we used pulse with 25 mV amplitude to simulate signal during offsets measurements. Plot at right shows offsets compensation in working conditions – sensor photodiode is connected to bias voltage only for short period of time during each measurement period.

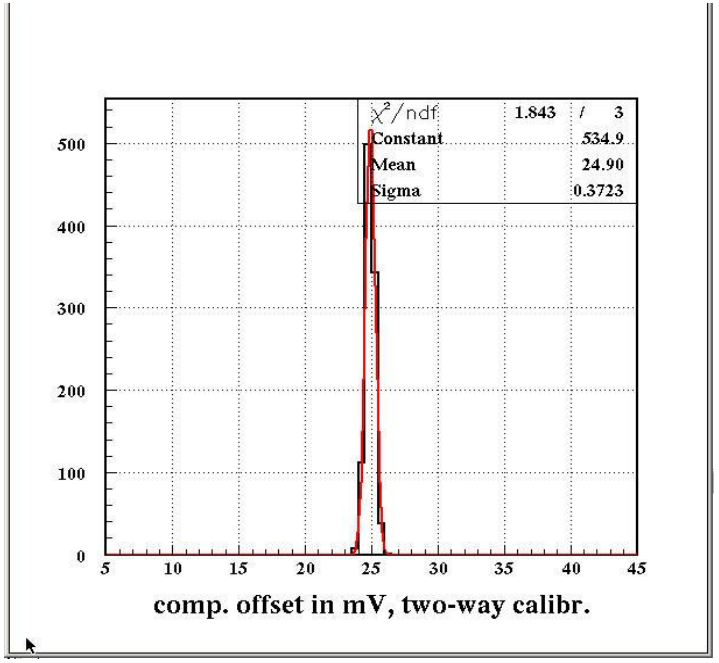
Test results - calibration



- On the right plot on previous slide we could see long tails of the offsets distribution. If we look at the picture how offsets values vary across chip area we can see two blobs of the pixels with large deviation of offsets from the average value (red and blue areas). These are pixels, close to clock drivers. So, there are some cross-talks from drivers.

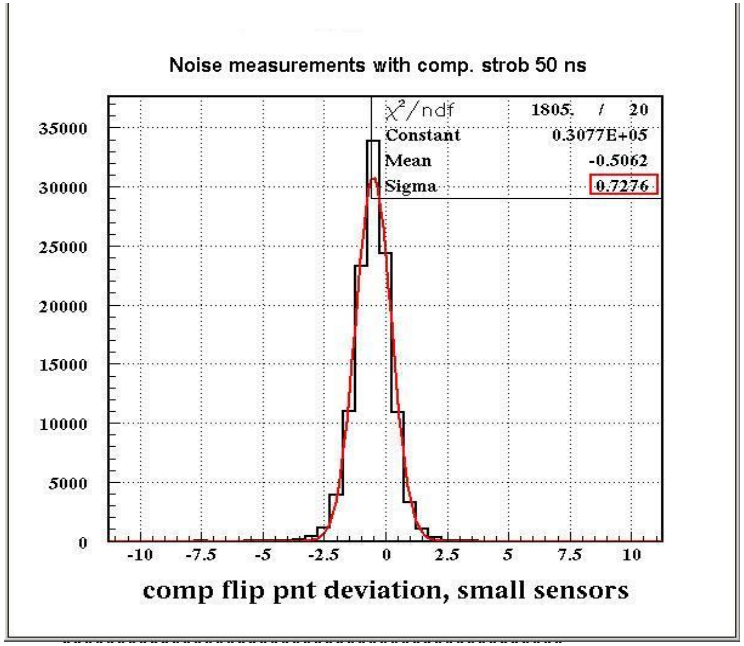
Deficiency of one-way calibration

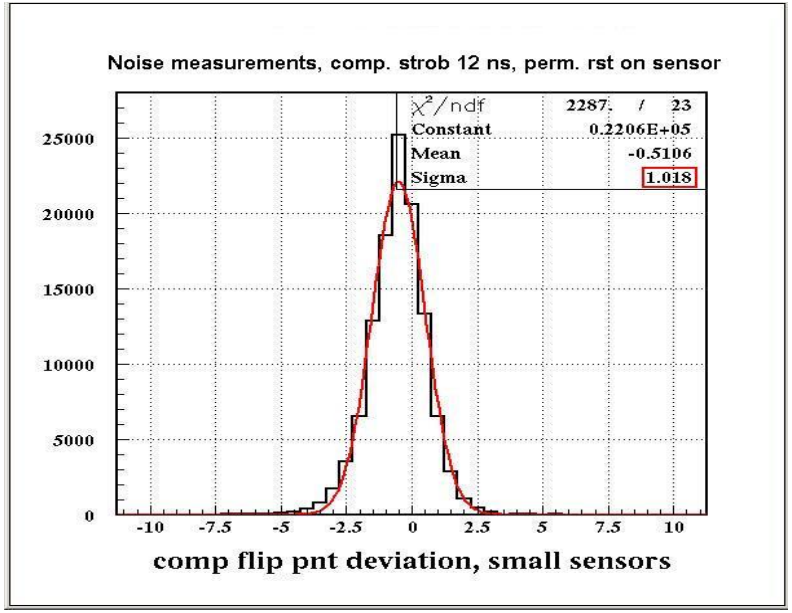




- **Sarnoff designer simplified calibration process. Originally it was thought, that during calibration, every calibration cycle voltage on the calibration capacitor is changing in two directions – if comparator got fired, voltage decreases, if not – increases. But designer decided that calibration can be done if we guarantee that initial calibration voltage exceeds any possible value of calibrated offset, and during calibration only decreases if comparator got fired, and do not changes otherwise. Result of such simplification you can see on the left picture. (Here on both pictures simulation results are shown).**
- **For the next prototype we requested implementation of 2-way calibration.**

Cross-talks problems

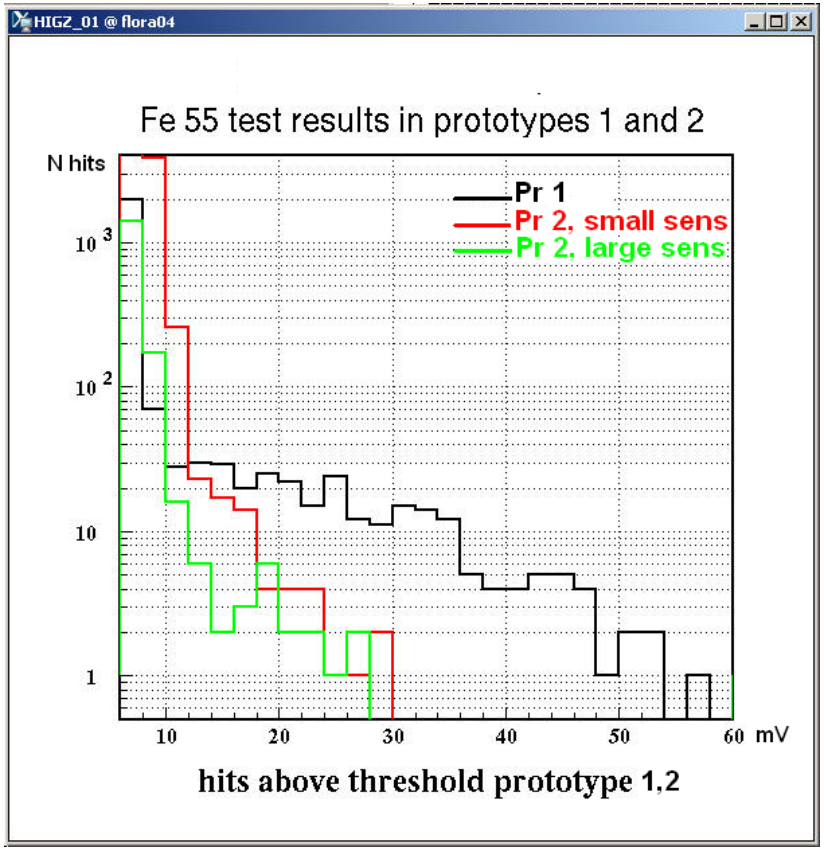




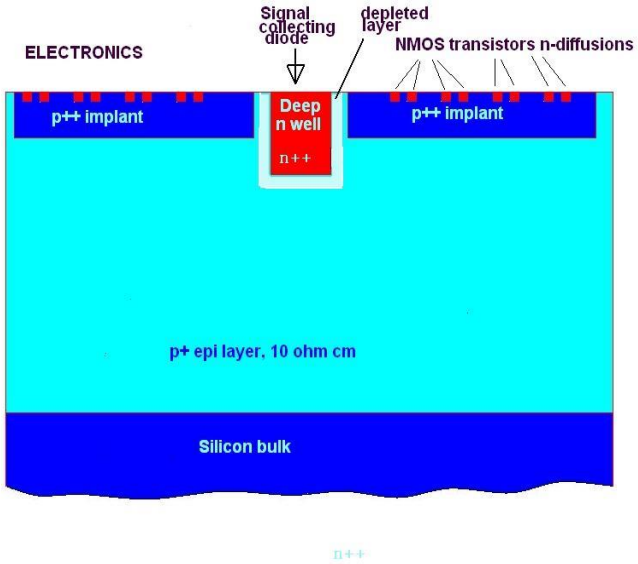
- I was originally puzzled with noise measurements. With increasing duration of comparator strobe pulse noise distribution became narrower. It appeared it was effect of cross-talks. As soon as many comparators on the chip start firing, the ringing on the not yet fired comparators inputs encourages them fire also. It artificially narrows distribution of flip points. There are more evidences that cross-talks also shift the comparator threshold depending on number of memory bits changing value during time stamp recording.

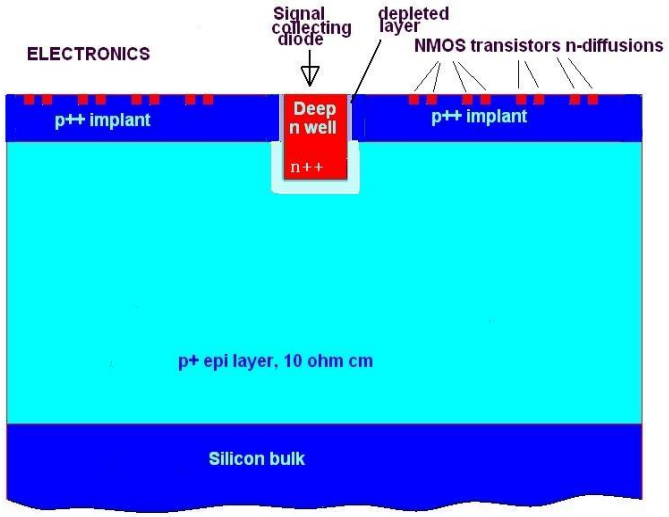
Test results – sensor capacitance

- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – 9 μ^2 and 22 μ^2 ("small" and "large" on the plot) . The maximum signal value is roughly in agreement with expected capacitance difference , though we would expect larger difference in maximum signal values here. But capacitance of the sensor from this measurements (~7.5 fF) appeared much larger of our expectations (~1-2 fF).



What got wrong?

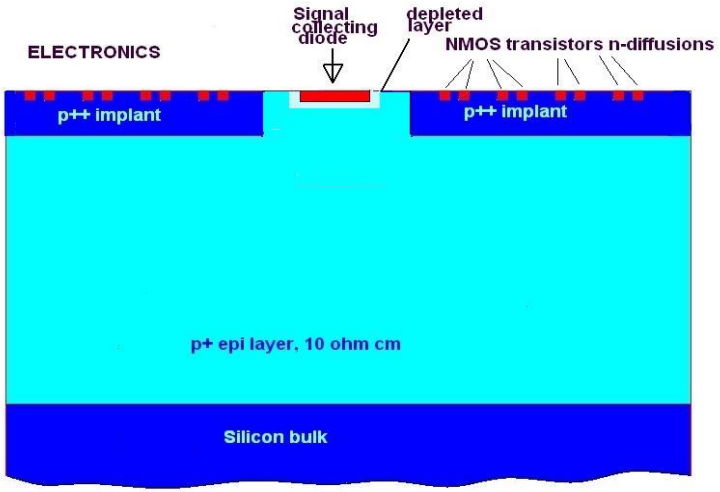




- We hoped, that pixel cross-section will look like what is shown on left picture. But it appeared, that in 90 nm design rules it is not allowed to have window in the top p++ implant around deep n-well, which forms our sensor diode. Resulting pixel cross-section is shown on right picture. Very high doping concentration of p++ implant leads to very thin depletion layer around side walls of deep n-well, which creates additional large capacitance.

Suggestions for prototype 3

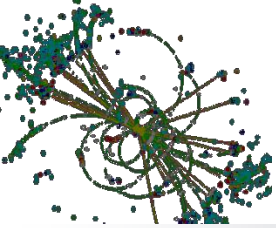
- It appeared, that prohibition of creating windows in top implant does not apply if we want make not deep n++ well for sensor diode, but create so-called native diode on the epitaxial layer – n+ implant in p+ epi layer, as shown on the picture. Simulation, made by Sarnoff people, claims 10-fold decrease in the sensor capacitance in that case.
- Fighting cross-talks is always a challenge. But what was done wrong in prototype 2 – common power supply for analog and digital part of electronics. It need to be fixed.



Power dissipation

Circuit	I total (mA)	I/pixel (nA)	P/pixel (nW)	Reduction strategy	Expected P/pix (nW)
1.2 V mem	0.46	200	240	Keep power only when hit	2.4 - 50
0.7 V mem	0.13	56.4	39.5	Keep power only when hit	0.4 - 8
1.2 V comp	0.53	230	276	Power only during BT	2.8
2.5 V SF	0.12	52.1	130.2	Power only during BT	1.3
Total			685.7		6.9 – 62.1
Spec			34.		

Design specification calls for 0.15 mW/mm^2 (100Wfor entire vertex detector), or 34nW/pixel assuming 15x15 μ^2 pixels.



Conclusions and plans

- From both, first and second prototype tests we have learned:
  - 1. We can build pixels which can record time stamps with 300 ns period (1 BC interval) - prototype 1
  - 2.We can build readout system, allowing to read all hit pixels during interval between bunch trains (by implementing sparse readout) - prototype 1
  - 3.We can implement pulsed power with 2 ms ON and 200 ms OFF, and this will not ruin comparator performance - both prototype 1 and 2
  - 4. We can implement all NMOS electronics without unacceptable power consumption - prototype 2. We don't know yet if all NMOS electronics is a good alternative solution to deep P-well option.
  - 5. We can achieve comparators offset calibration with virtually any required precision using analog calibration circuit.
  - 6. Going down to smaller feature size is not as strait forward process as we thought.
- As for the plans: contract for prototype 3 is signed in April 2013. Expected submission to MOSIS in September 2013.This prototype main goal will be to achieve smaller sensor capacitance. Problem with cross talks also should be addressed, and we hope 2-way calibration will be implemented also. We want to stay with 90 nm technology for prototype 3.