R&D status of FPCCD VTX and its cooling system

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Outline

- FPCCD R&D
  - Prototype sensors
  - Beam test plan
- 2-phase CO2 cooling system
  - Motivation
  - Circulating system using a compressor

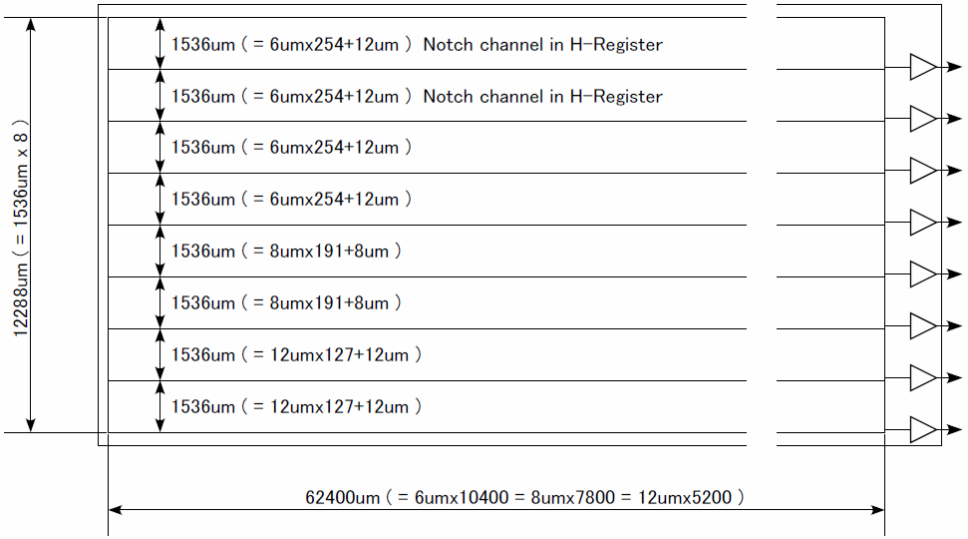
FPCCD R&D

FPCCD sensors

- Small prototype in FY2012
  - 6mm square image area
  - 6um pixel size
  - 4ch/chip with different horizontal shift register size: 6x6, 6x12, 6x18, 6x24 um^2
  - It works except for the channel with 6x6um^2 horizontal shift register
  - Thin wafer (50um) in package with hole for beam test

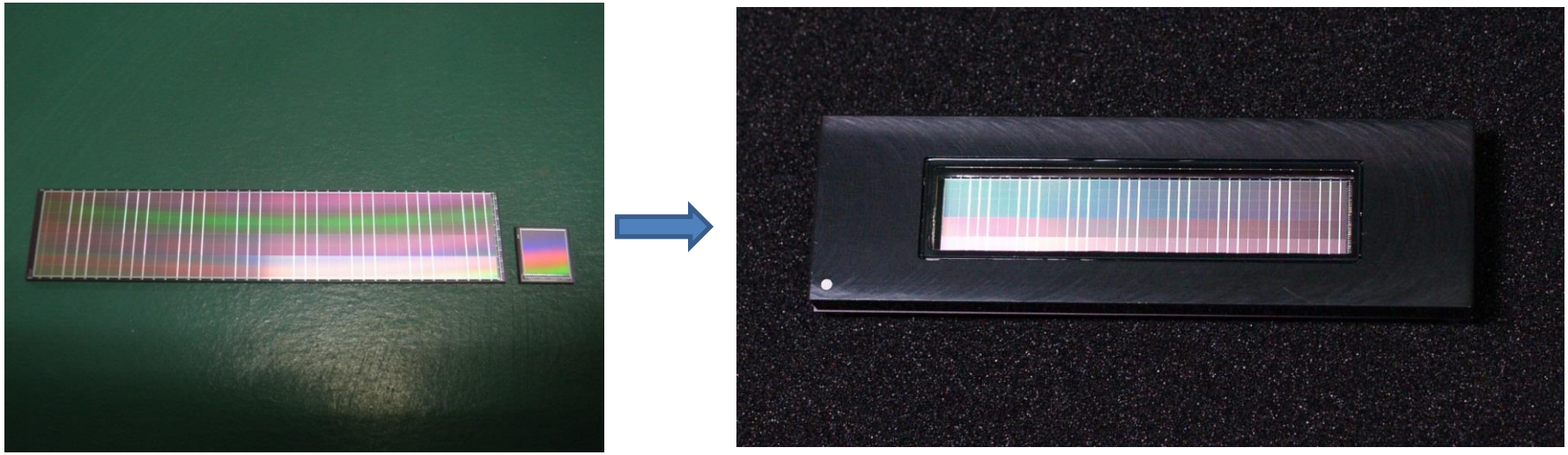
FPCCD sensors

- Large prototype
  - 62.4x12.3mm^2 image area ~ Real size prototype for inner layers
  - 8ch/chip with several pixel sizes: 4chx6um, 2chx8um, 2chx12um
  - Large area is achieved by stitching technique: 8 steps with 3 kinds of masks



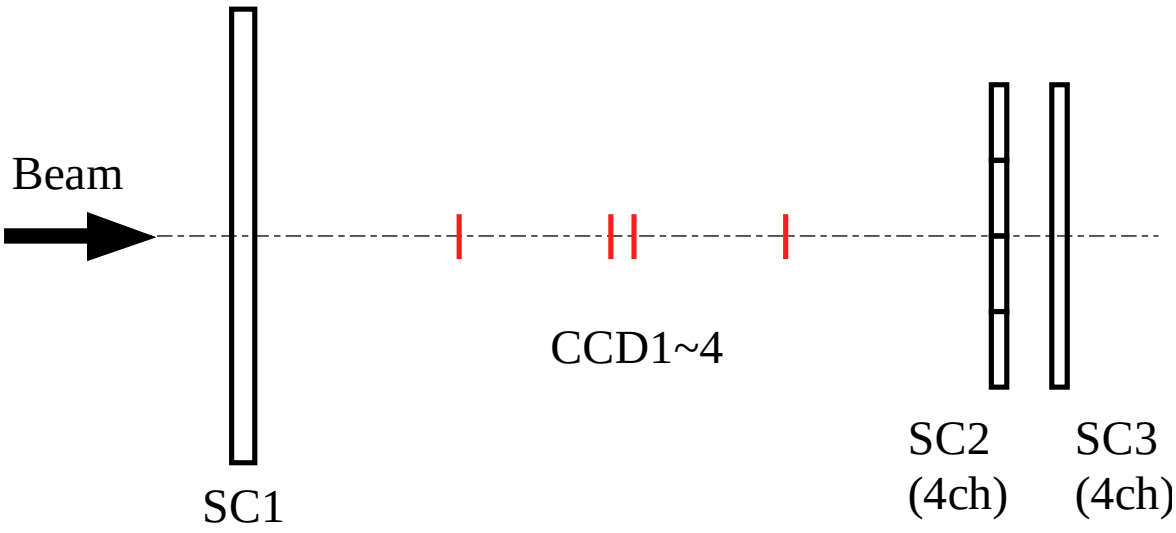
FPCCD sensors

- Large prototype
  - Packaged sensors have been delivered
  - Test boards have been prepared
  - Two channels (out of 8ch) which have 6umx6um horizontal shift register do not work properly
  - Full-well capacity is still small (~6k electrons) for 6um pixels



Beam test plan

- Test beam at J-PARC in June
  - 1 GeV/c pion
  - 3.2mm distance between central 2 layers → Minimize multiple scattering effect
  - Small prototypes with thin (50um) wafers will be tested
  - Study items: Spatial resolution, S/N ratio, charge spread, etc.
  - Could be delayed due to the trouble at J-PARC on May 23



FY2013 plan

- Study of 2012 prototypes
  - Source test / Beam test
  - Radiation damage test
- Improved small prototypes
  - Increase full-well capacity
  - Smaller pixel size: 6um → 5um
- Large prototypes
  - Thin large wafer → Prototype ladder in FY2014
- Readout electronics
  - Improvement of front-end ASIC
  - Development of a part of peripheral circuits (clock driver, ser-des, timing generator, or data compression circuits)

2-PHASE CO_2 COOLING SYSTEM FOR FPCCD VTX

Why we need CO2 cooling?

- Power consumption

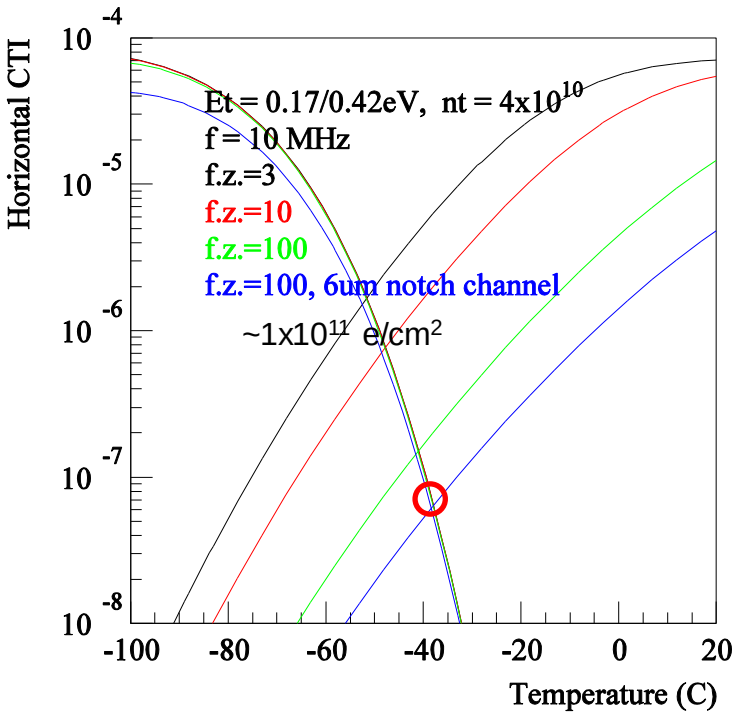
Readout frequency	10 Mpix/s
Readout time	200 ms
Clock timing	Same for inner and outer layers
Vertical shift time	40 us/line
Power consumption	15 mW/ch (On-chip amp + FE ASIC)
Chip size (in/out)	11x62.5mm^2 / 22x125mm^2
Number of chips (in/out)	40 (=10x2x2) / 112 (=(11+17)x2x2)

Pixel size (in)	Pixel size (out)	# of ch/chip (in)	# of ch/chip (out)	# of ch (total)	Power consumption
5 um	5 um	28	56	7392	111 W
5 um	10 um	15	15	2280	**34 W**

Power consumption in aluminum gate lines should be added
→ We should assume >50W power consumption

Why we need CO2 cooling?

- Operation temperature
  - Optimization for radiation tolerance
  - Charge transfer inefficiency (CTI) due to radiation damage is a function of temperature
  - A simple simulation of CTI based on Shockley-Read-Hall theory shows around -40℃ is optimal
  - 2-phase CO2 cooling gives constant temperature cooling



Why we need CO2 cooling?

- Material budget / dead region
  - 2-phase CO2 can go through very thin cooling tube (OD 2mm or less) → Only 0.3%X_0 increase of material budget of the end-plate
  - Gas cooling requires much thicker tube → Dead space between FTD and beam pipe

Advantages of CO2 cooling

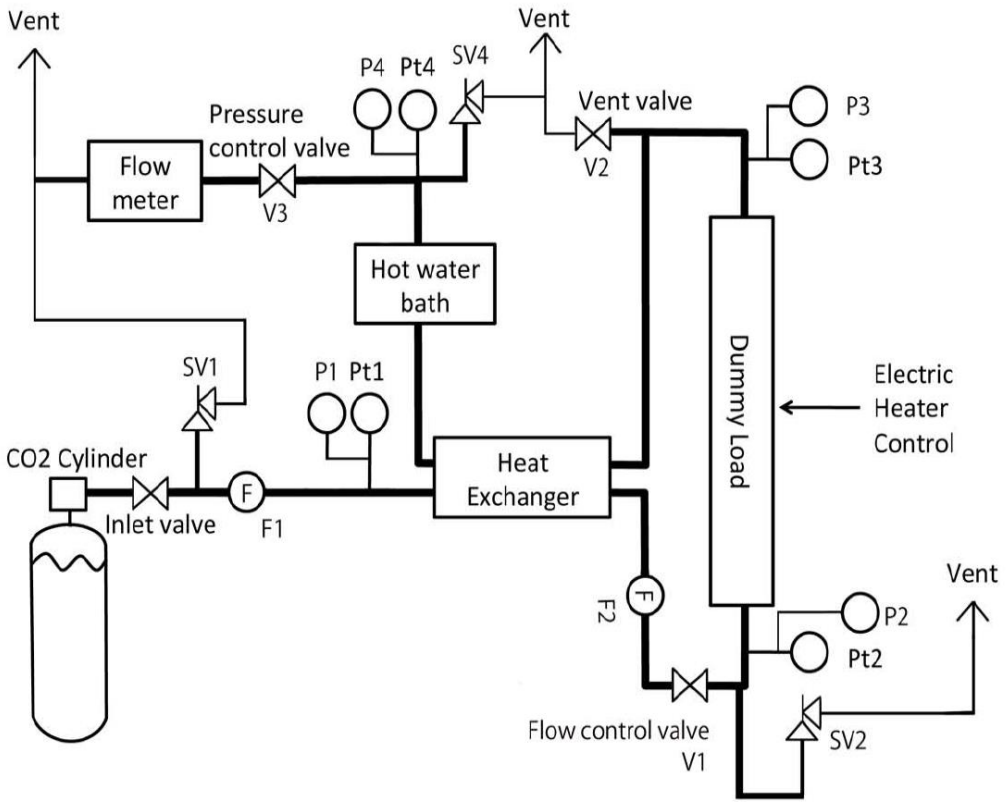
- Large latent heat ~300 J/g (x3 of PFC)
- High pressure ~1 MPa @-40℃
  - Less evaporated gas volume
  - Less temperature drop due to pressure drop

  ➔ We can use thin cooling tube
- Much less Global Warming Potential

	CO2	C2F6	C3F8
Latent heat @-40C	321 J/g	~100 J/g	~110 J/g
Critical point	31.1℃	19.7℃	71.9℃
Pressure @-40C	1 MPa	~0.5 MPa	~0.1 MPa
GWP	1	9200	7000

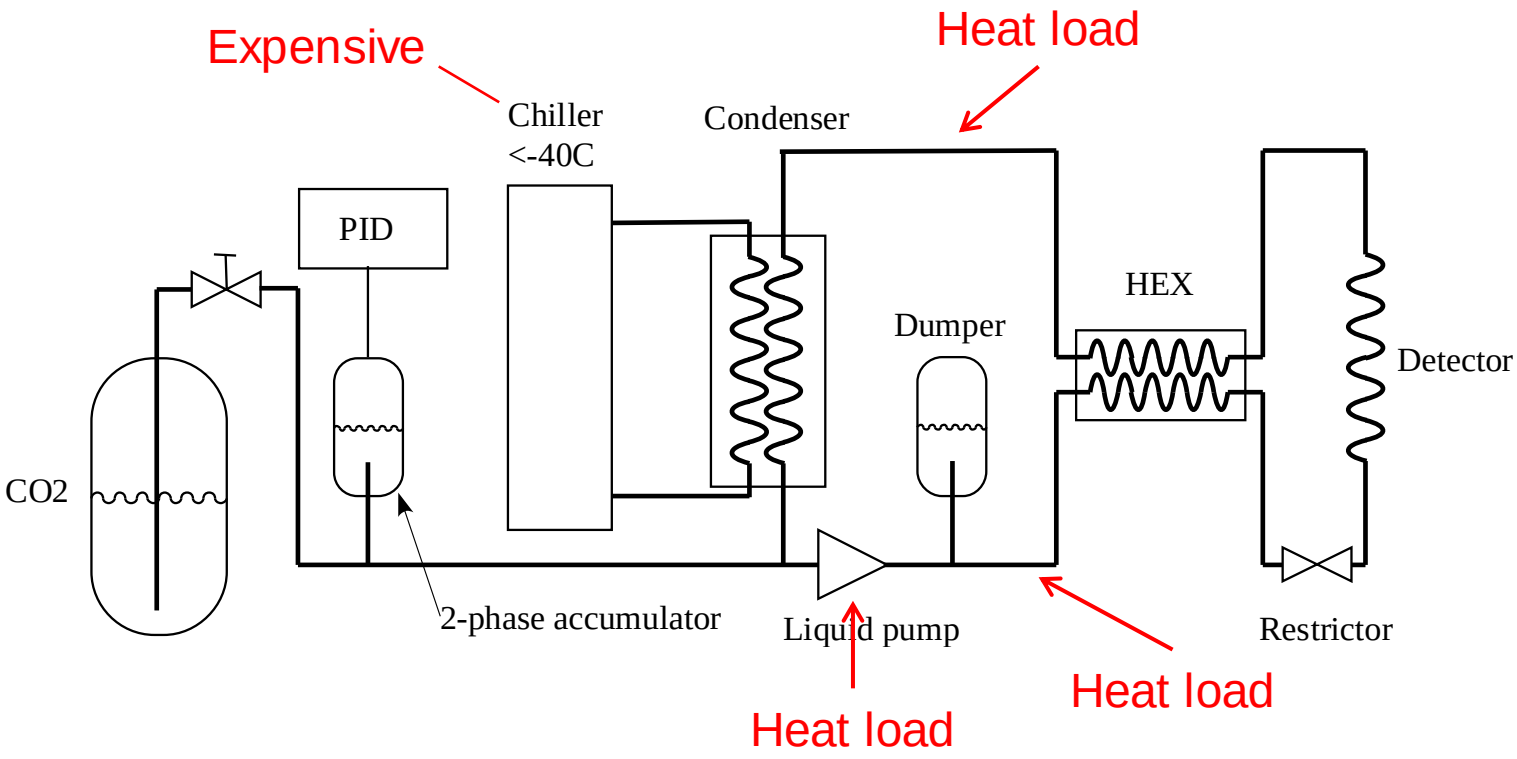
CO2 blow system

- First step towards circulating system
  - We constructed “blow system” and temperature was successfully controlled between -40℃ and +15℃



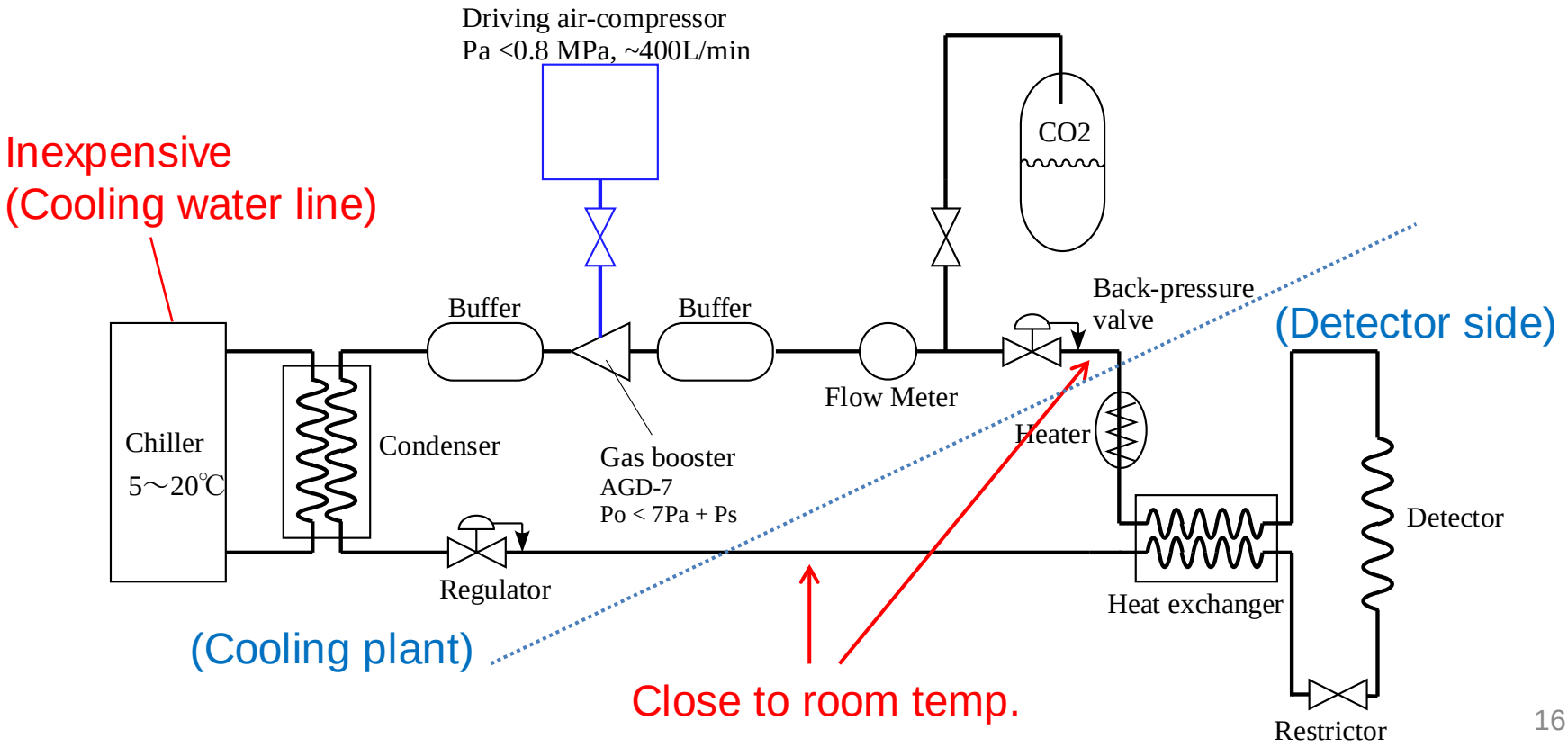
Circulating system

- Circulating system using a liquid CO2 pump
  - Getting popular in HE physics experiments
  - Disadvantages in low temperature application



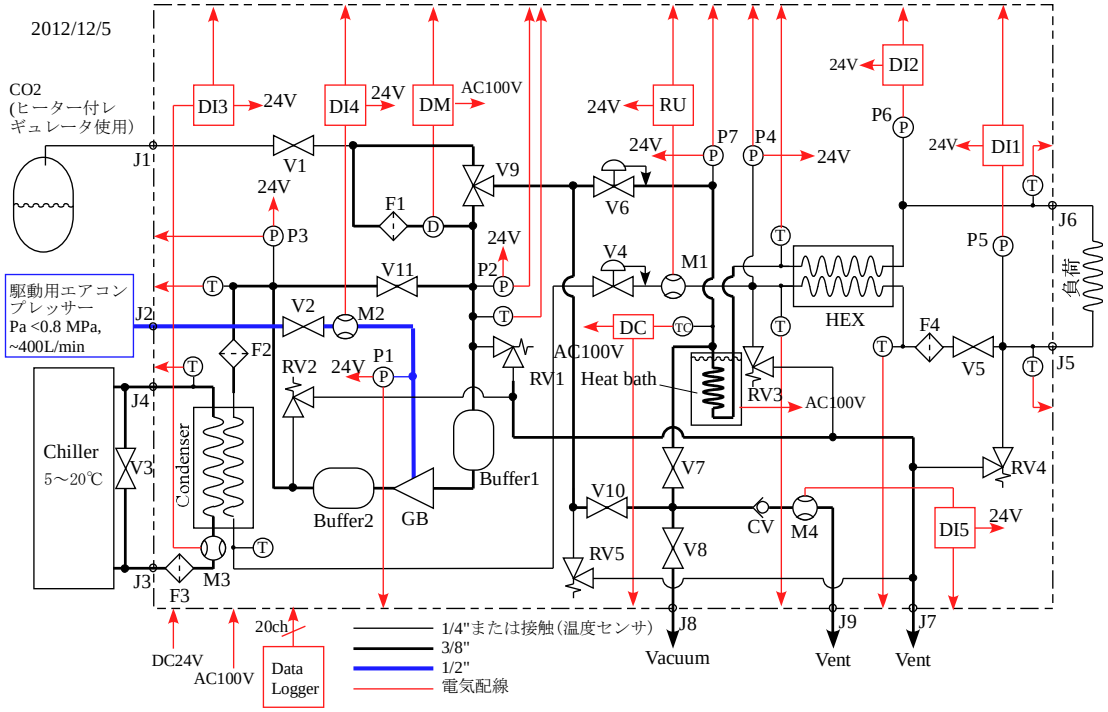
Circulating system

- Circulating system using a CO2 gas compressor
  - Less expensive for low temperature application



Development of circulating system

- Cooling plant for R&D → many sensors attached
- Assembly completed → to be tested after July



SUMMARY AND PLAN

Summary

- FPCCD small prototype with 6um pixel size has been developed and worked well if the horizontal shift register size is 6umx12um or larger
- Large prototype of FPCCD has been developed and the packaged prototype sensors have been delivered

- FPCCD VTX will be operated at -40℃ with 2-phase CO2 cooling system
- Circulating CO2 cooling system using a CO2 gas compressor seems attractive
- A test system for the circulating CO2 cooling system with a gas compressor has been designed and assembled

Future prospect

- R&D goal for coming 3 years
  - 5um pixel
  - Demonstration of performance
  - Peripheral circuits for demonstration
  - Prototype ladder
  - Engineering prototype of support structure
- Plan for 2016-2017 (after approval of ILC project)
  - Very large size prototype for outer layers
  - Peripheral circuits for real detector
  - Engineering prototype of support structure
  - ILD proposal and VTX TDR