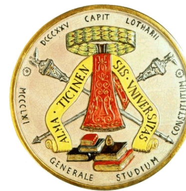
3D Deep N-well CMOS pixel sensors for the ILC vertex detector

V. Re[a,c], L. Gaioni[c], A. Manazza[b,c], M. Manghisoni[a,c], L. Ratti[b,c], G. Traversi[a,c]



[a] Università degli Studi di Bergamo

[b] Università degli Studi di Pavia

[c] Istituto Nazionale di Fisica Nucleare

Deep N-well CMOS sensors for the ILC and 3D integration

- ✓ Deep N-well (DNW) CMOS pixel sensors were devised with the goal of achieving **"hybrid pixel-like" functionalities in monolithic devices** (pixel-level sparsification and time stamping).
- ✓ A prototype chip **SDR0** was designed according to **ILC-driven** specifications; it was fabricated in a **130 nm CMOS process** by STMicroelectronics and successfully tested.
- ✓ Technology studies in the 3D-IC Consortium promoted by Fermilab provided an opportunity to develop a new chip **SDR1, exploiting 3D integration** to overcome some limitations of the 2D version, also providing a demonstrator of 3D design solutions.
- ✓ This talk will discuss status and plans for future 3D CMOS pixel developments.

From my own talk at LCWS '08: The way forward for DNW MAPS

- Next generation of DNW MAPS has to provide devices that approach actual experiment specifications more closely

  Several issues have to be addressed to meet ILC Vertex Detector specifications (pixel pitch, detection efficiency):

  - Binary readout: ILC VTX demands a **pixel pitch** < 20 μm to achieve required single point resolution < 5 μm.
  - **Detection efficiency** does not meet requirements (> 99 %) because of competitive n-wells (PMOS) decreasing the fill factor
  - Capability of **handling multiple pixel hits** has to be included without degrading efficiency and pitch

- Two different ways to approach this goal:

1) ***A gradual performance improvement***
   ⇒ better sensor layout, optimize interconnections and pixel cell

2) ***A technology leap***
   ⇒ Vertical integration

Deep N-Well (DNW) sensor concept

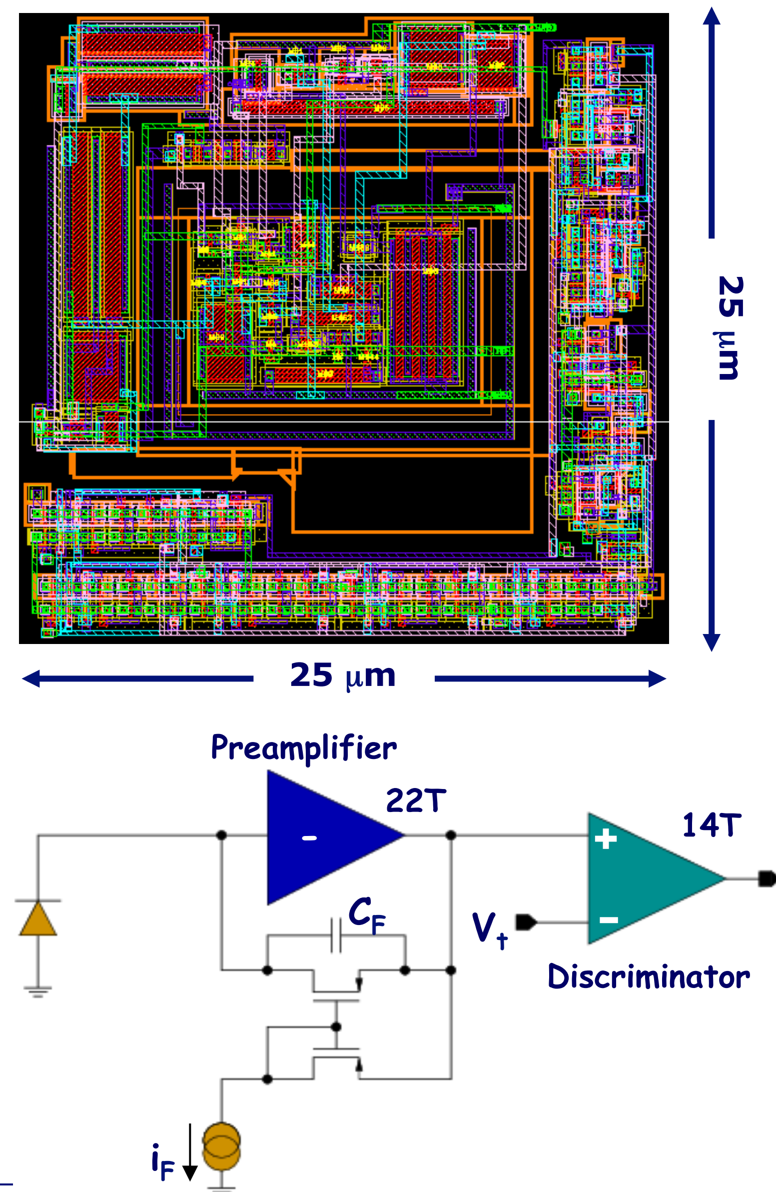
New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential

Classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located

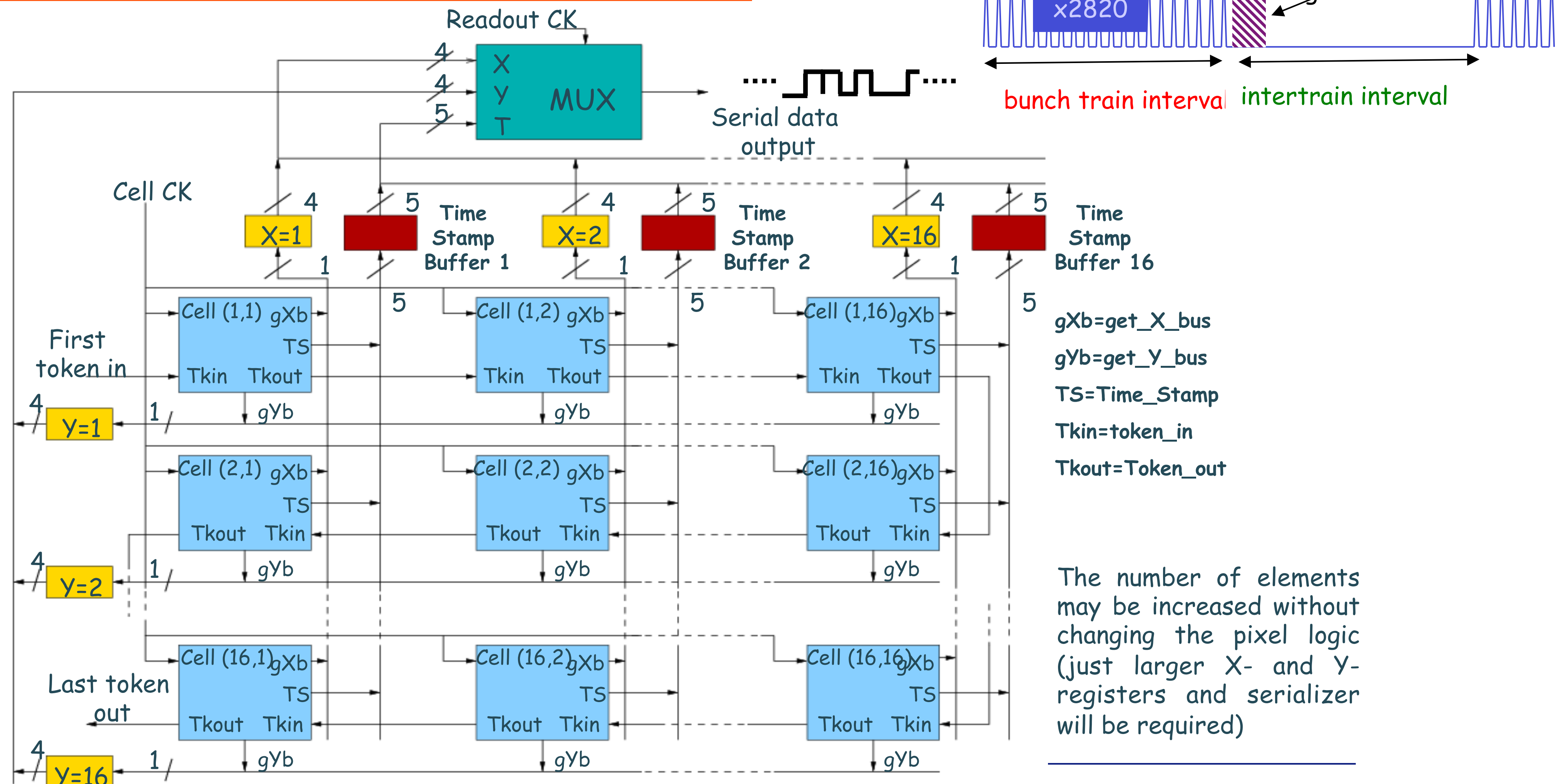
SDR0, a prototype DNW MAPS for the ILC VTX

- Sensor operation tailored on the structure of the ILC beam
  - detection phase - corresponding to bunch train interval
  - readout phase - corresponding to intertrain interval → EMI insensitive system
- Test chip including a number of different structures, among which a 16x16 DNW MAPS matrix
  - sparsification based on a token passing scheme
  - single-hit storage and 5-bit time stamping
  - "shaperless" analog front-end
- STMicroelectronics 130 nm CMOS



Intertrain Readout Architecture for SDR0

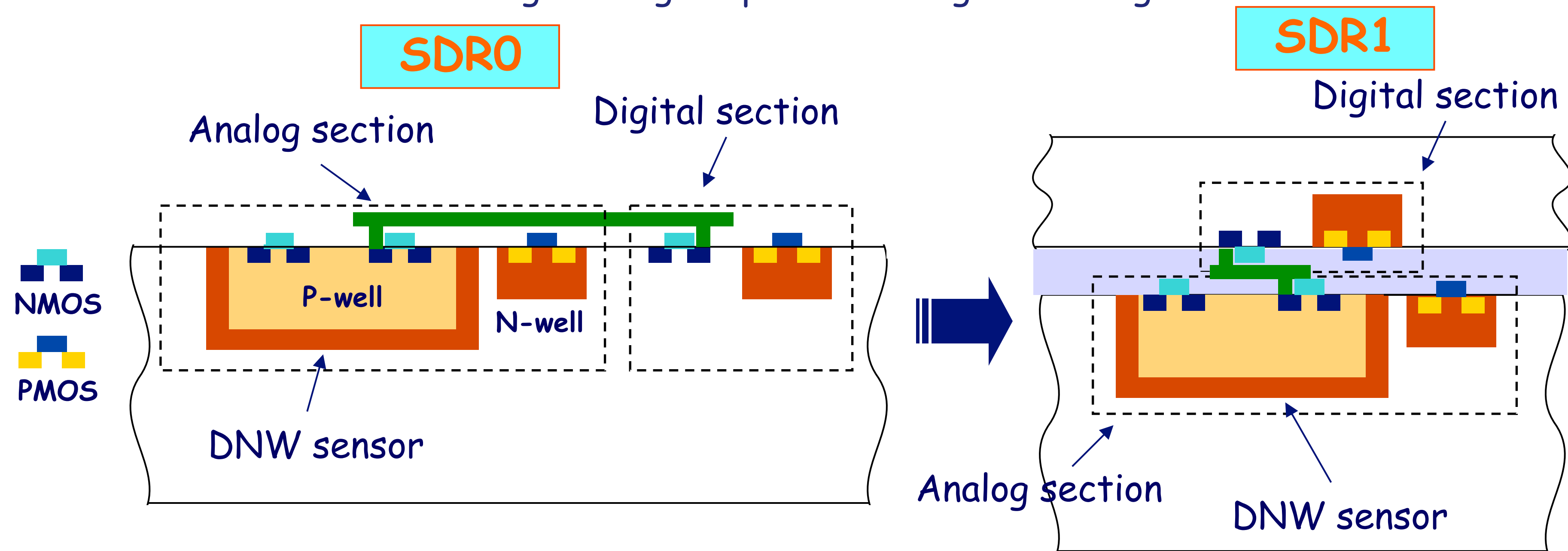
Suggested by FNAL IC design group, first implemented in the VIP chip



The number of elements may be increased without changing the pixel logic (just larger X- and Y- registers and serializer will be required)

What can be gained from going 3D: from SDR0 to SDR1

- sensor and analog front-end can be integrated in a different layer from the digital blocks
- less PMOS in the sensor layer → improved collection efficiency
- more room for both analog and digital power and signal routing

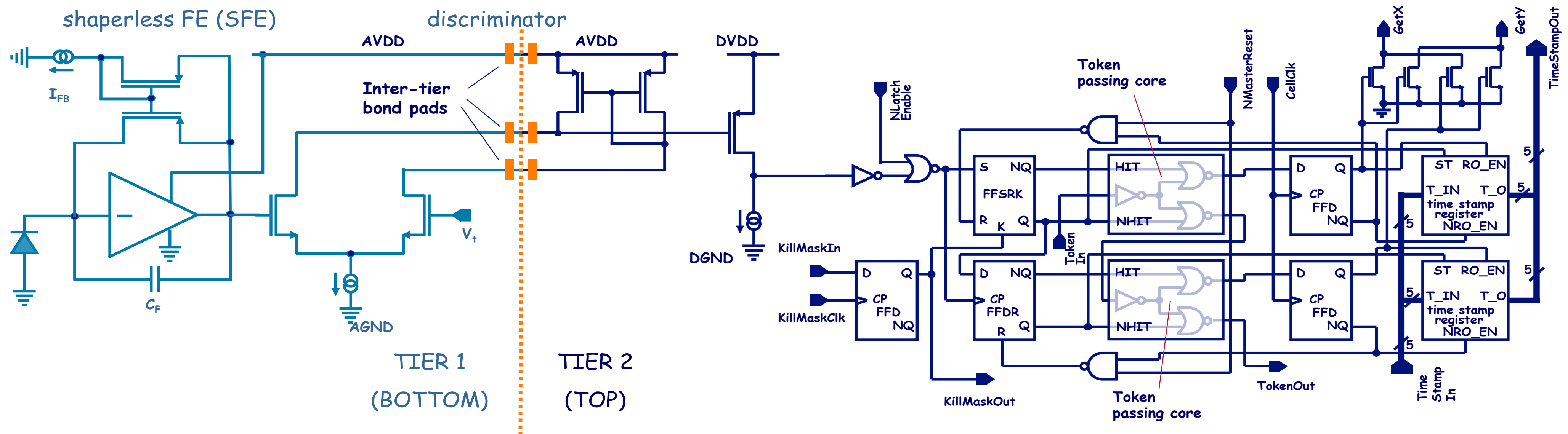


- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Advantages of going 3D for "ILC-like" DNW MAPS

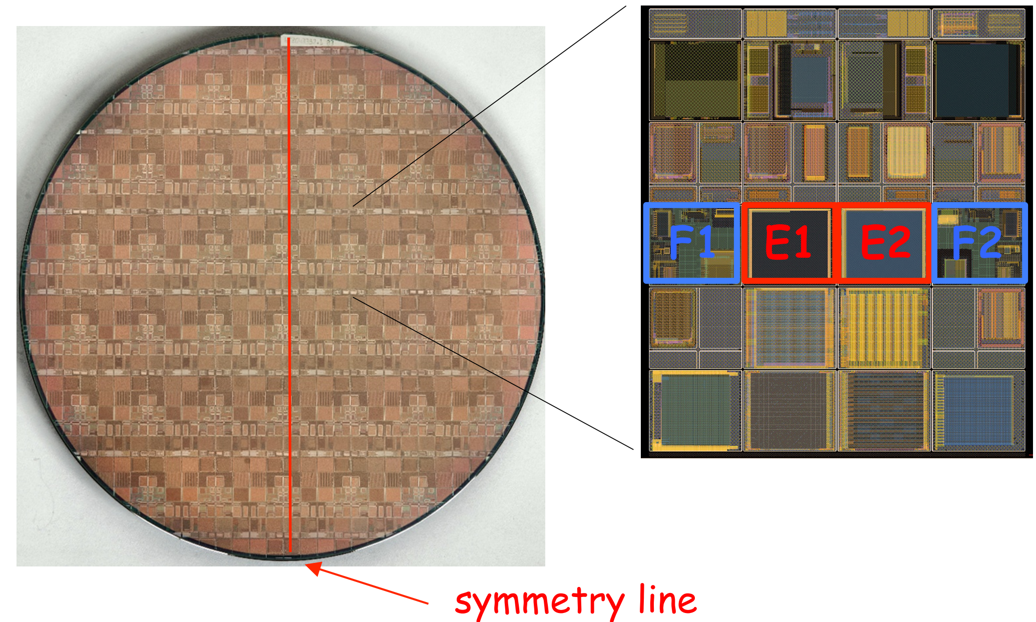
- Pixel-level functionalities: a double-hit detection capability (two flip-flops) is included (also a "power-enable" control signal)
- Pixel pitch: reduced from 25 μm to 20 μm
- Pixel "fill factor": increased by a sizable reduction of the area of PMOS N-wells in the sensor layer

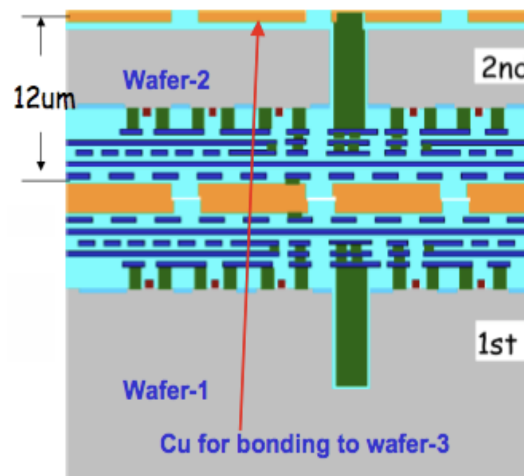
The SDR1 pixel readout cell



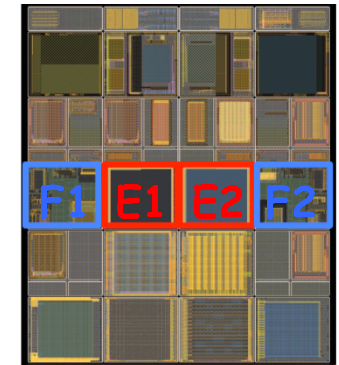
First MPW run of the 3D-IC consortium

- Several groups from US and Europe have been involved in the first 3D MPW for HEP (pixel and strip readout chips for ATLAS, CMS, B-factory, ILC) and photon science applications (X-ray imaging)
- Single set of masks used for both tiers to save money
  - identical wafers produced by Chartered (now **GlobalFoundries**) and face-to-face bonded by **Tezzaron**
  - backside metallization by Tezzaron



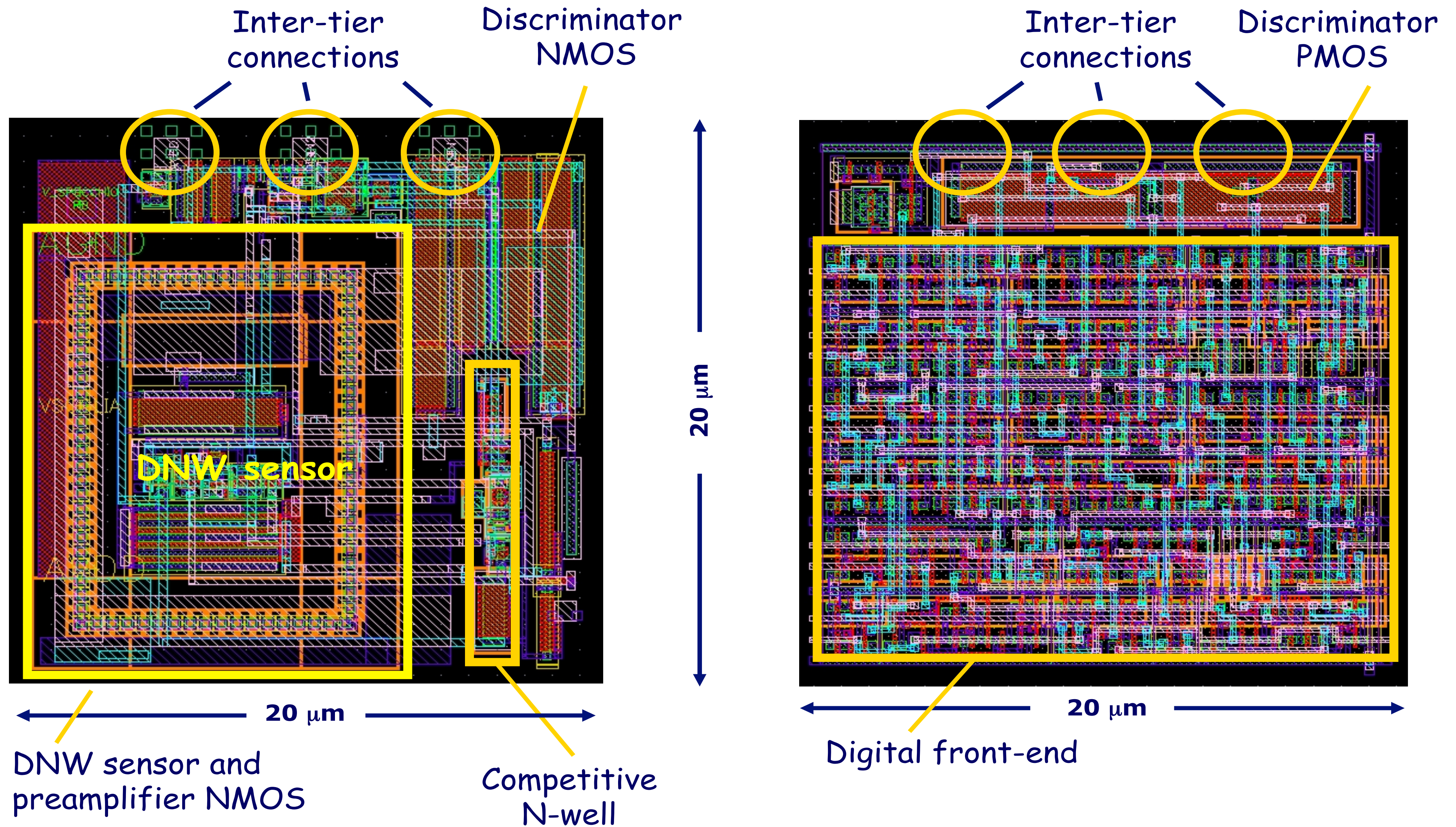


Top layer flipped over



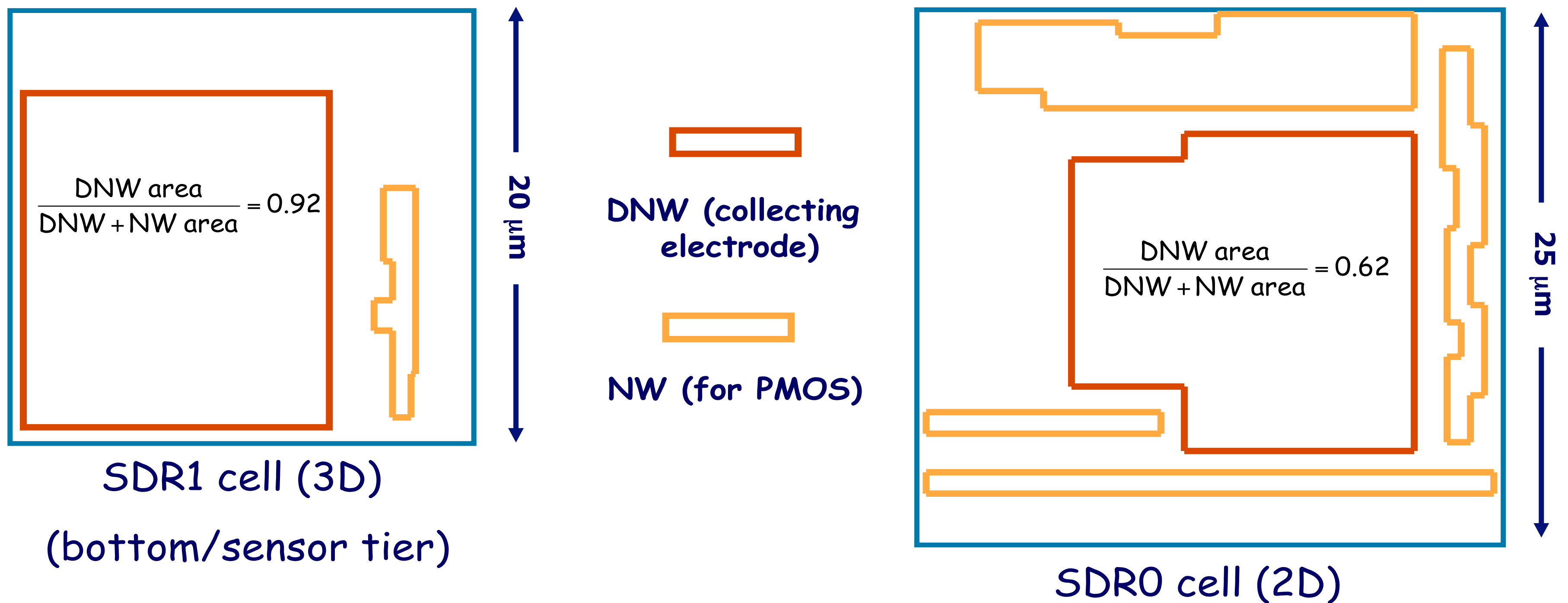
Bottom layer

Layout of the 2-tier pixel cell of SDR1



Collecting electrode layout

- Moving most of the PMOS transistors to the top (digital) tier may significantly improve the detector collection efficiency
- The DNW covers about 35% of the cell area in the SDR0 chip, more than 50% in its 3D release



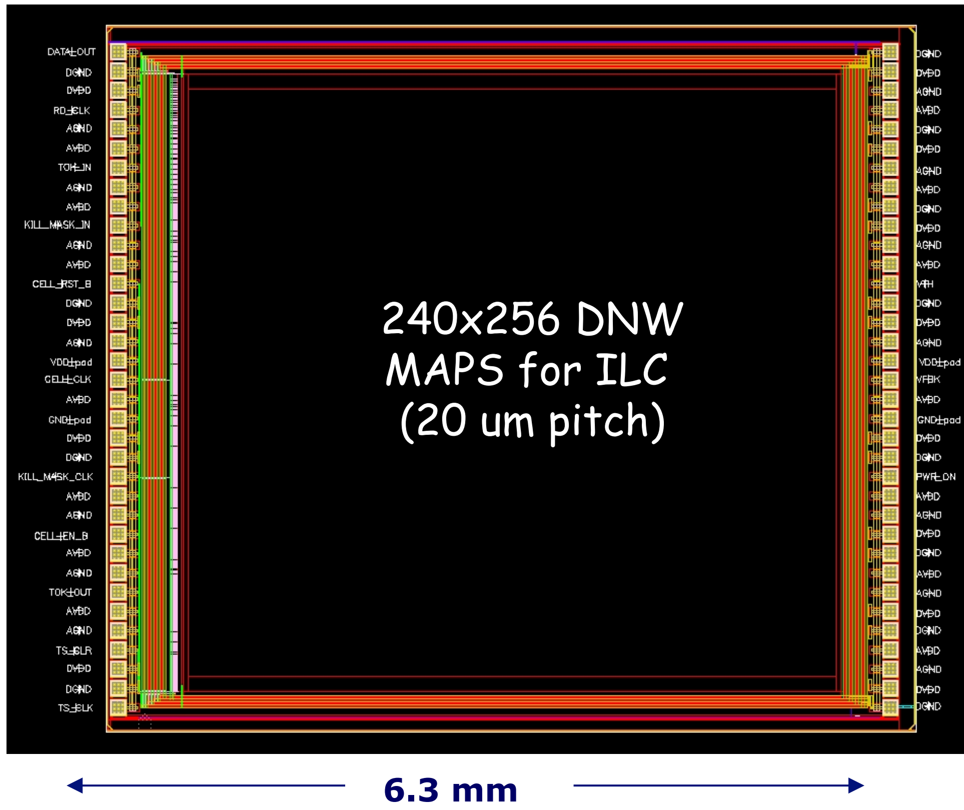
SDR1 cell (3D)

(bottom/sensor tier)

SDR0 cell (2D)

DNW MAPS in the 3D-IC run

The SDR1 chip

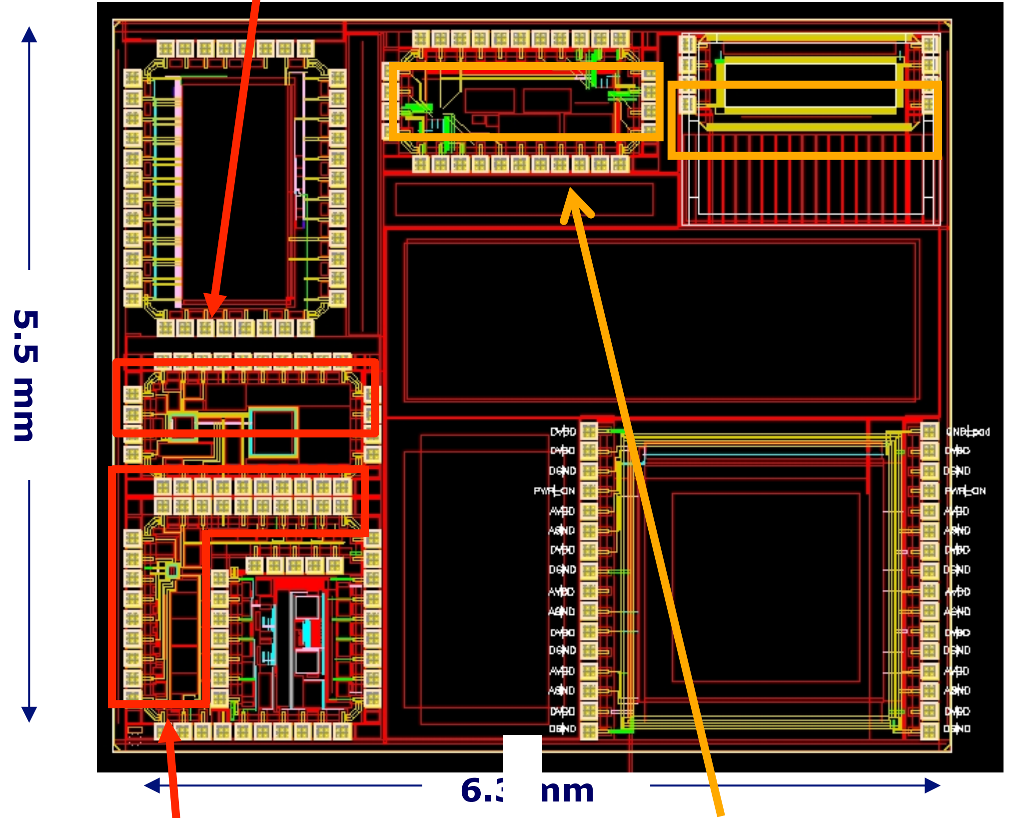


6.3 mm

5.5 mm

8x8 and 16x16 DNW MAPS for ILC (20 μm pitch)

32x8 DNW MAPS matrix for SuperB (40 μm pitch)



6.3 mm

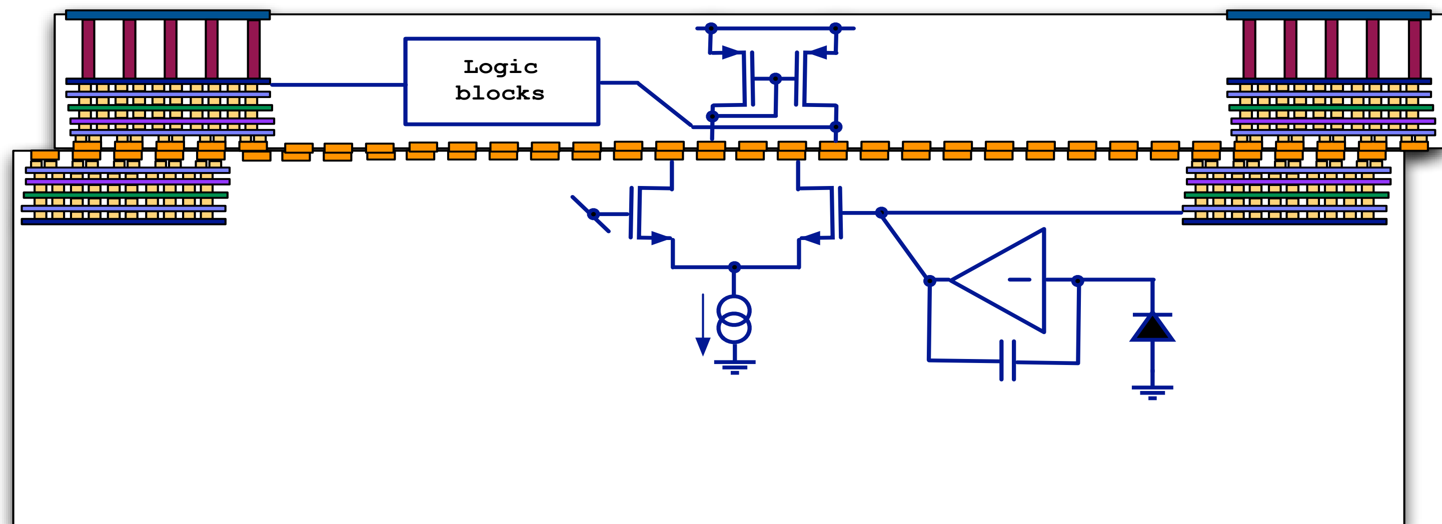
5 test structures of DNW MAPS for ILC (3x3, single channels with different C_D 20 μm pitch)

Test structures of DNW MAPS for SuperB (2 3x3 one with ELT input device, 40 μm pitch)

The first 3D DNW CMOS sensors: experimental results

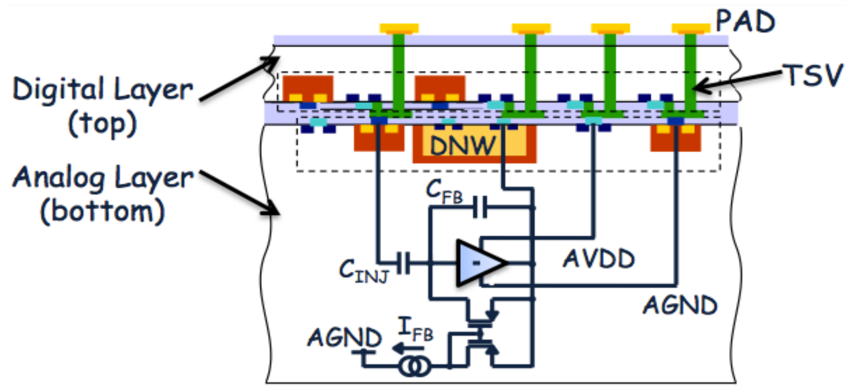
- The processing of 3D devices started about 3 years ago at Tezzaron/ GlobalFoundries and, after many technical problems, only **recently (summer 2012) fully functional chips were delivered**. This is a signature that advanced 3D technologies have not yet reached a full maturity.

An example of what can go wrong: misalignment in inter-tier connection pads

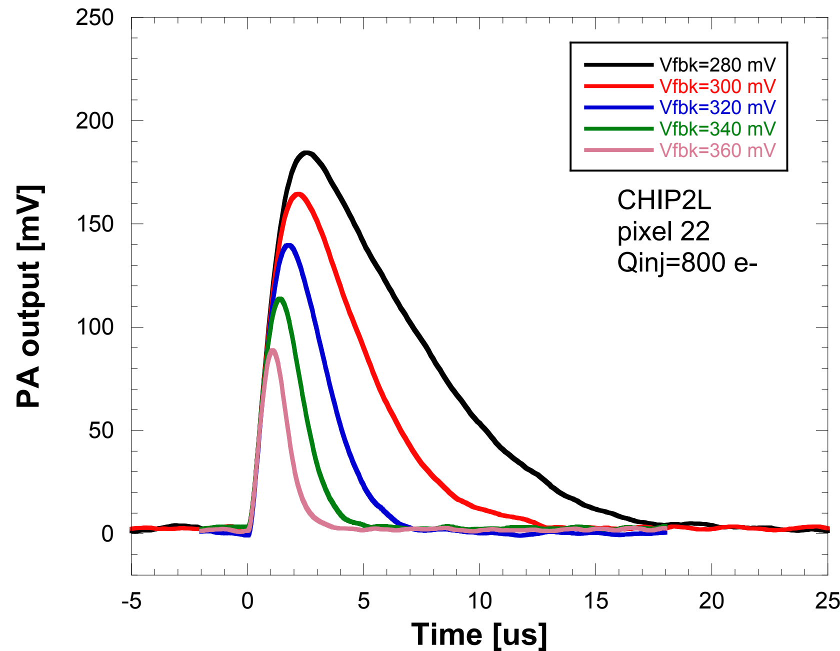


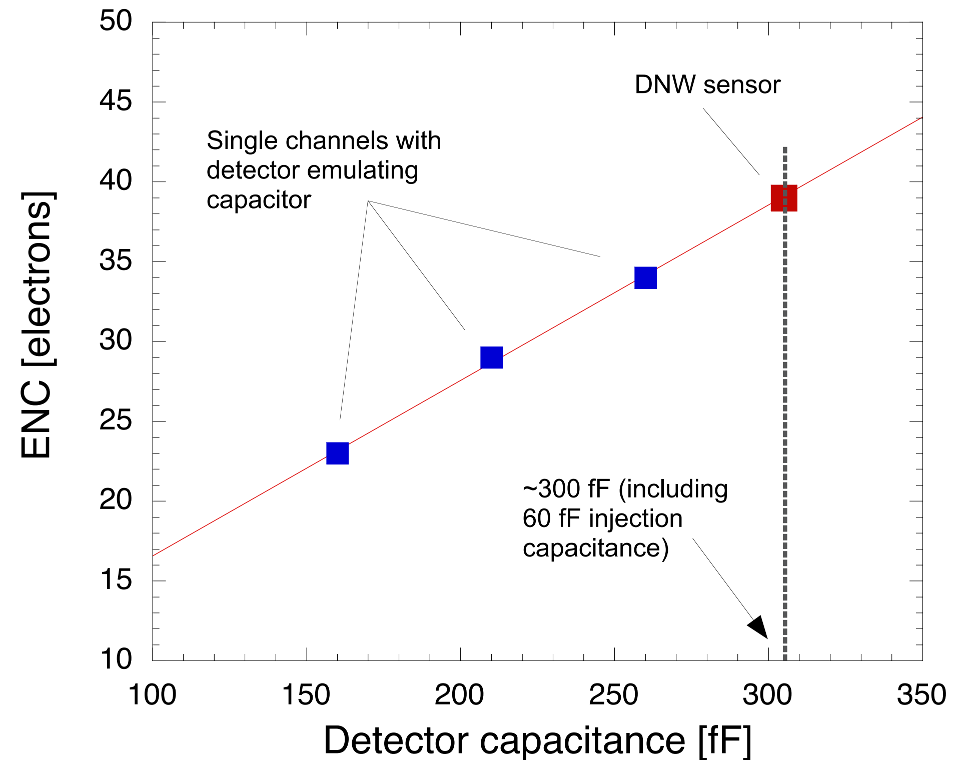
- However, eventually **very good test results on fully working 3D chips provide a demonstration of the potential of 3D integration**, and stimulate further work.

SDR1: analog front-end characterization

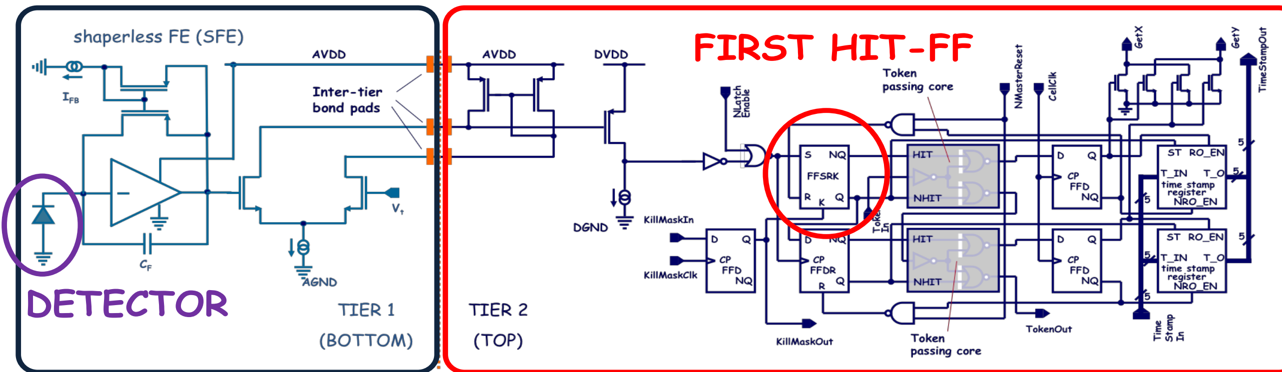


- *Charge sensitivity: 700 mV/fC*
- *Input linear dynamic range: 2500 electrons*
- *ENC: 40 electrons rms*
- *Power dissipation: 5 μW/pixel*

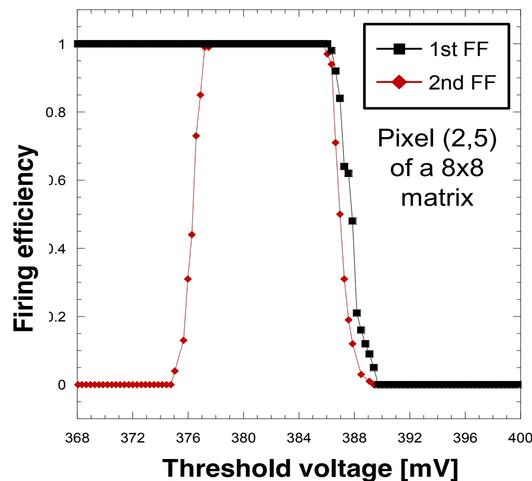


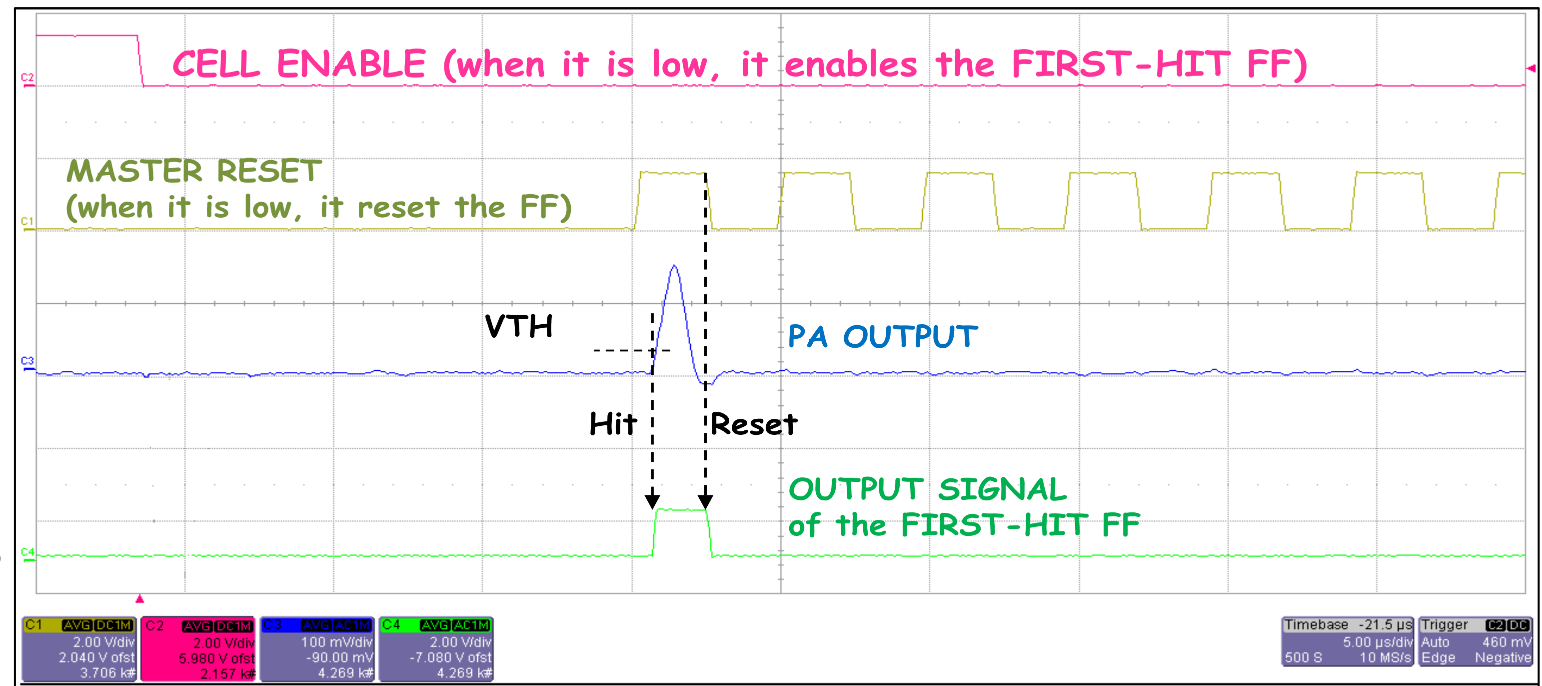


Tests on digital and analog section of SDR1



- Tests on SDR1 digital circuits show the full functionality of vertically integrated chips

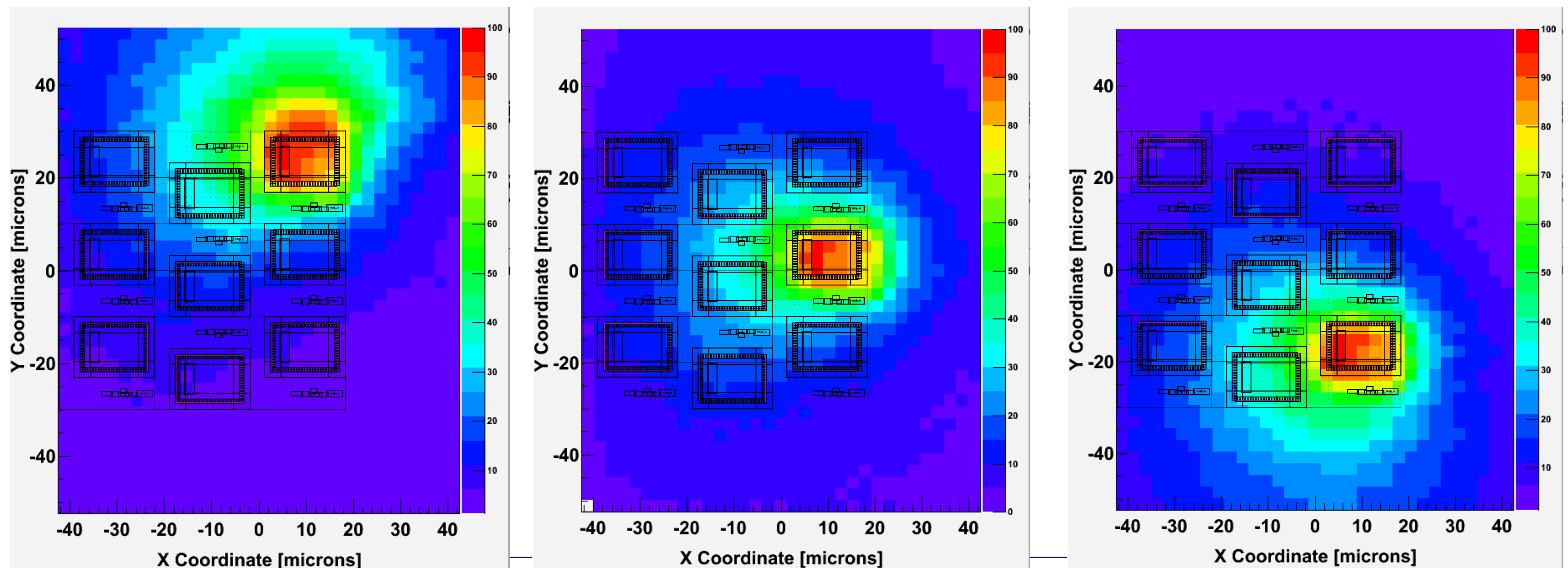




SDR1 characterization with laser scan

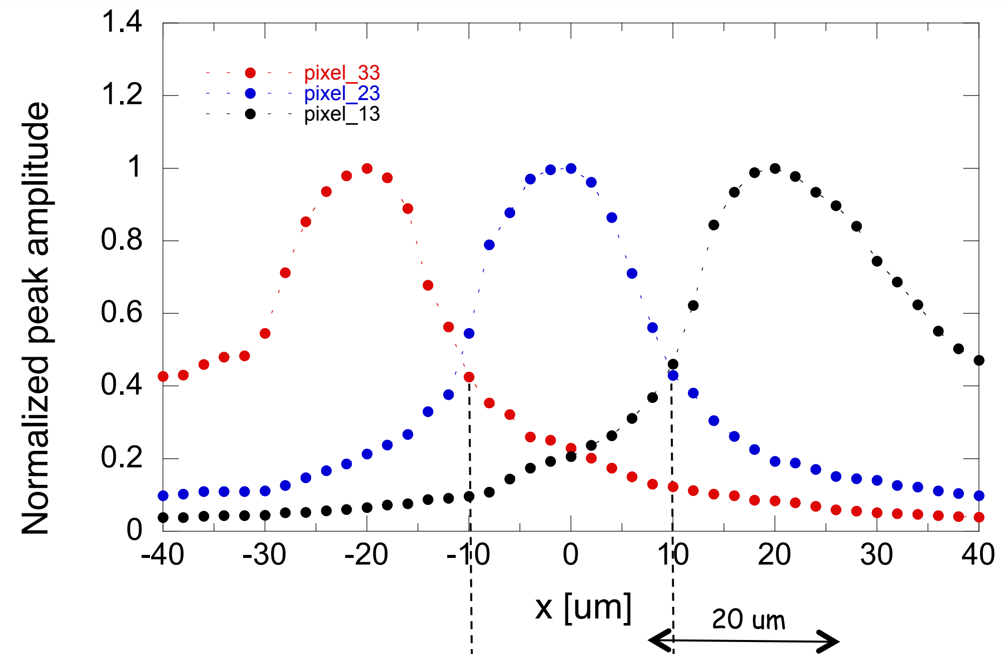
Laser measurements for characterization of gain uniformity, identification of dead pixels, ….

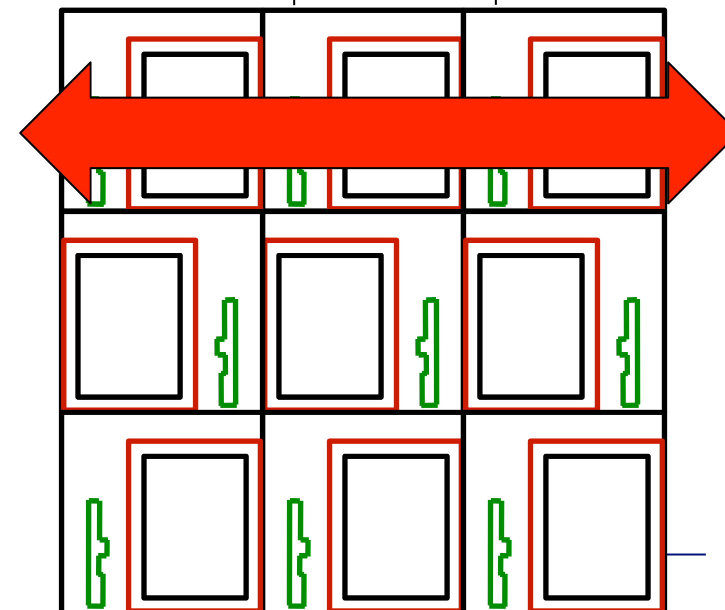
- collected charge (expressed as percentage of the peak value) as a function of the laser beam position
- obtained by retro-illumination with an infrared laser (1060 nm wavelength)
- 2.5 um step in X and Y
- the layout of the Deep N-well layers and competitive N-wells has been superimposed (exact position unknown)
- intensity profile of the laser beam has a Gaussian shape with $\sigma_{xy} \approx 1.3$ um
- measurement results show the relative charge collection versus position (the amount of charge that is deposited has not been calibrated) and the impact of the standard N-wells on the charge collection



SDR1 characterization with laser scan

- Peak amplitude of pixel 13, 23, 33 measured at the same time for each laser spot position
- Adjacent pixels collect slightly less than 50% of the charge when the laser spot is above the competitive N-well
- 2 um step in X



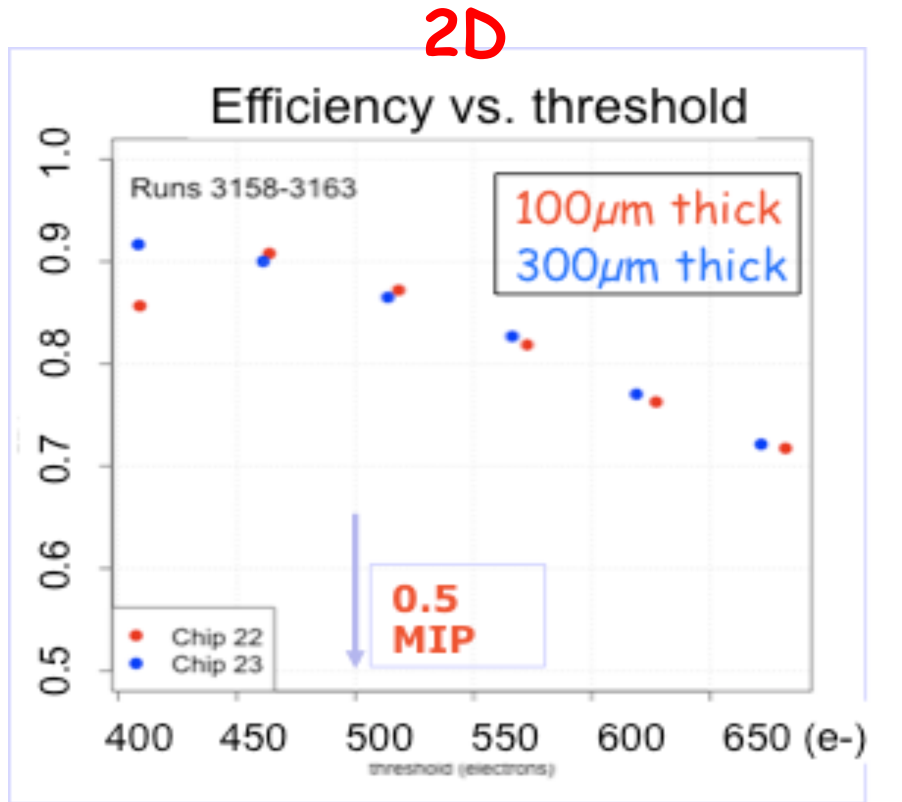


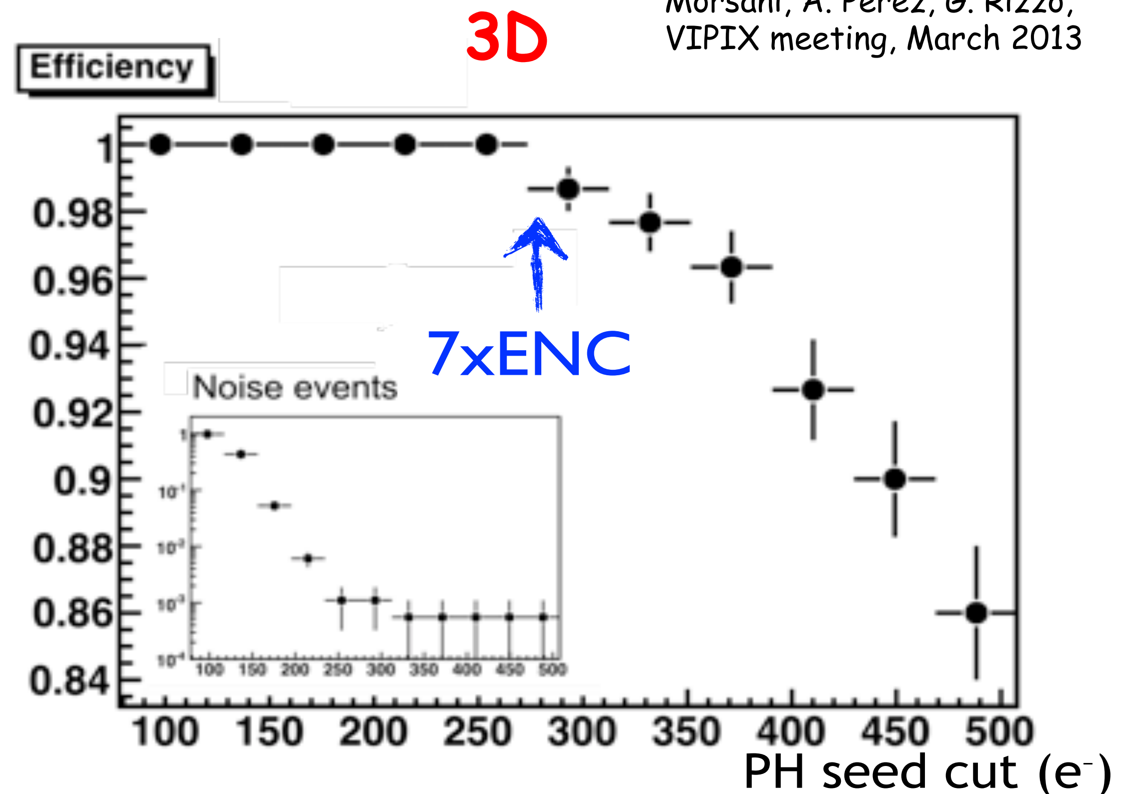
Dep N-well
N-well
Competitive N-well

3D integration improves efficiency of DNW CMOS sensors

- In the first 3D-IC run, besides "ILC-like" devices, we had also DNW CMOS sensors with continuous sparsified readout (originally developed for SuperB, which was then cancelled), called APSEL.
- Beam test results on these 3D APSEL prototypes confirm the advantage in charge collection efficiency with respect to previous 2D versions, because of the reduction of the area of competitive PMOS N-wells.

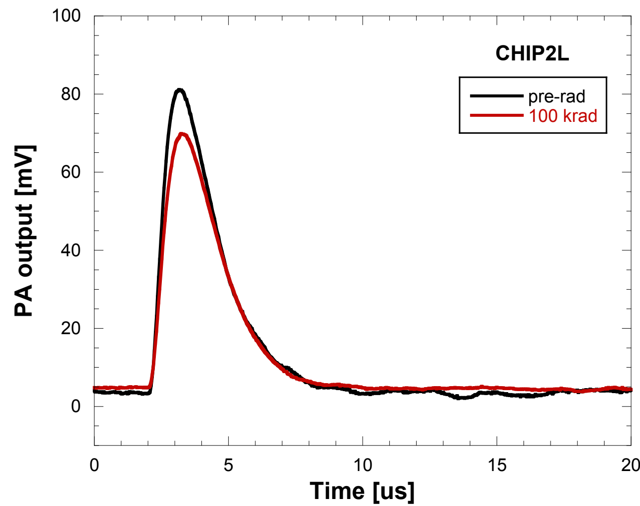
S. Bettarini, G. Casarosa, F. Morsani, A. Perez, G. Rizzo, VIPIX meeting, March 2013



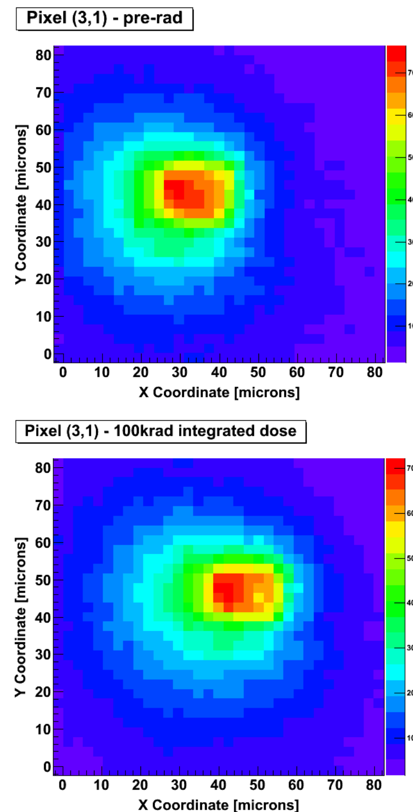


Radiation hardness tests

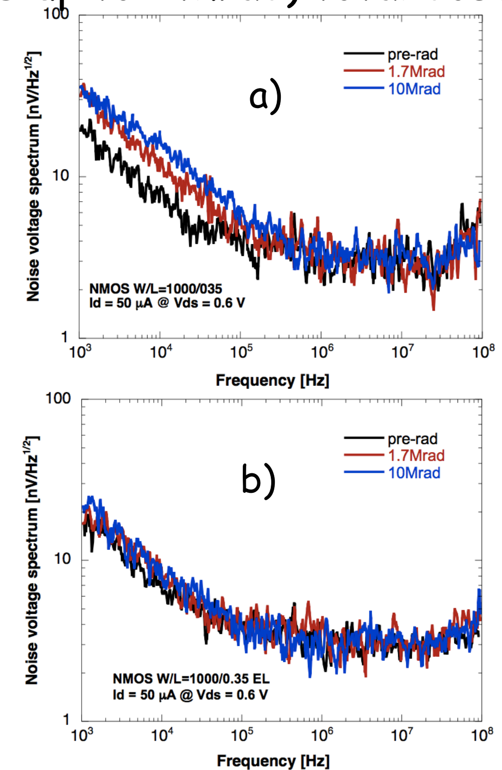
- The characterization campaign is carried out to verify that 3D fabrication steps do not result in a degradation of the radiation tolerance.
- CMOS transistors were irradiated up to 10 Mrad(SiO_2) (DNW MAPS up to 1 Mrad) total dose with γ-rays from a ^{60}Co source



Decrease of the charge sensitivity probably due to threshold voltage shifts in the PA transistors



No sizeable variation in the profile and amount of the collected charge -> bulk damage from TID exposure is negligible as expected



Noise voltage spectra for different values of the total ionizing dose in a standard multifinger or enclosed layout NMOS transistor. a) 1/f noise of the lateral parasitic devices which are turned on the irradiation; b) in enclosed layout devices lateral leakage path between source and drain are removed.

A new generation of 3D chips

- The yield, reliability and turnaround time of the aggressive 3D process we used so far still seem to be an issue.
- Since an experimental proof of 3D-related performance advantages was provided by the first 3D-IC run, there are plans for submitting two new 3D chips, whenever a viable access is provided to the technology.

Main analog features	3D APSEL	SUPERPIX1
Charge sensitivity [mV/fC] @ DAC out	700	50
peaking time [ns]	300	250
ENC [e rms]	40 @ C_D=300 fF	180 @ C_D=150 fF
Threshold dispersion before/after correction [e rms]	106/15	560/65
Pitch [μm]	50	50
Matrix size	128x100	128x32
Power/pixel [μW]	36	13.5

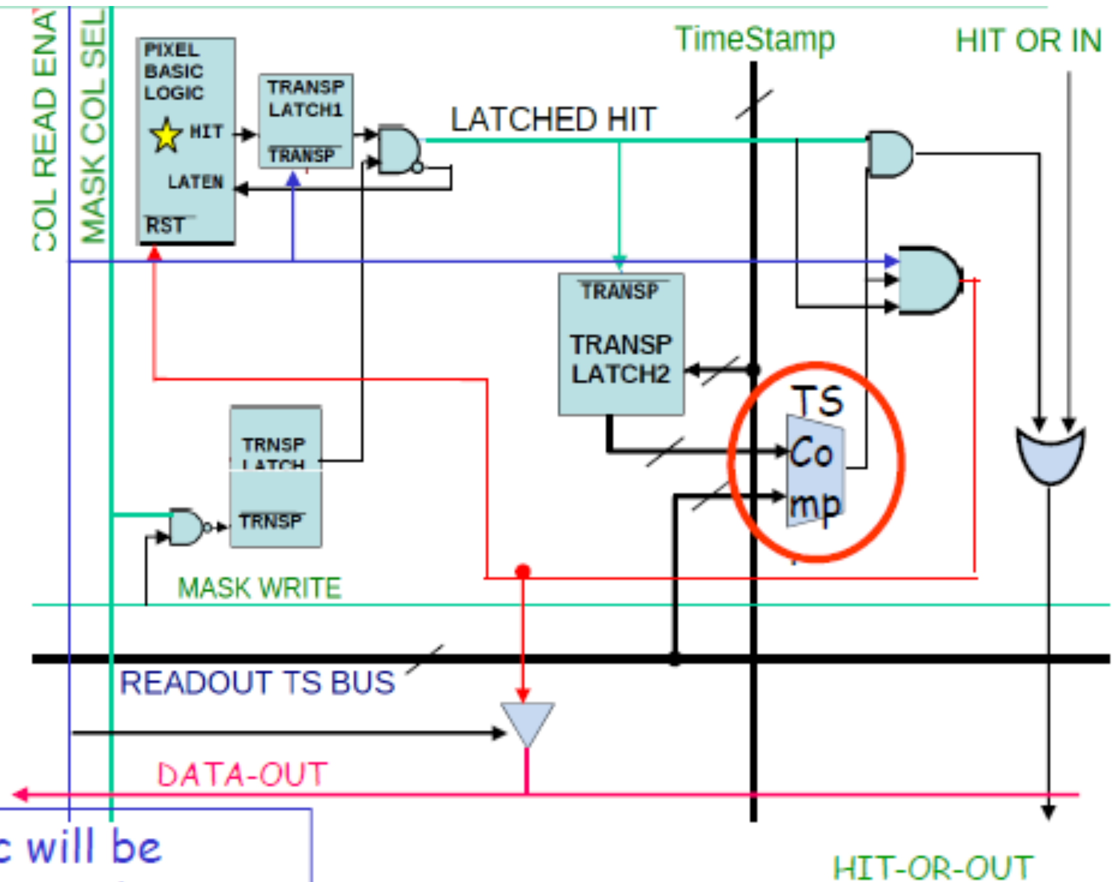
1) **Large-scale 3D deep N-well MAPS (3D APSEL)**

2) **3D readout chip for high resistivity pixel sensors (SUPERPIX1)**

Both chips share a new flexible readout architecture (pixel-level zero suppression and time stamping): data push & triggered version, with time-ordered readout

Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS

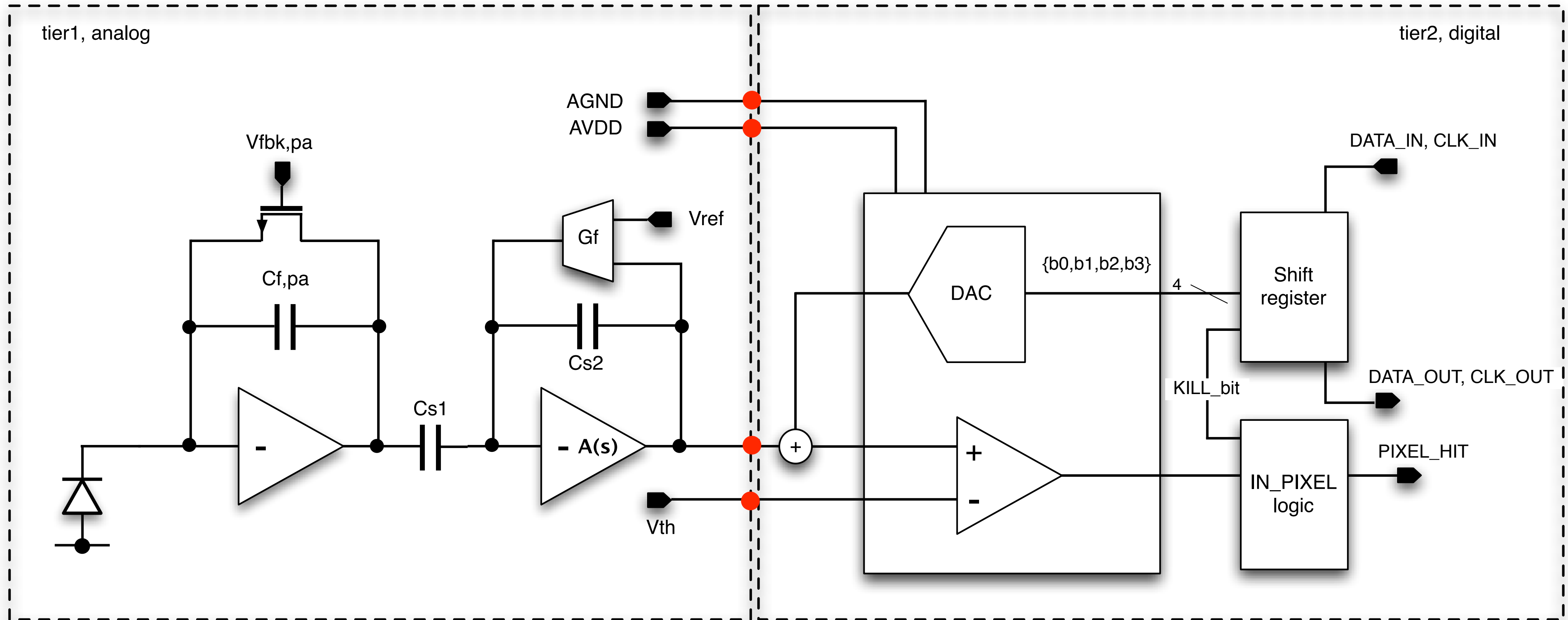


- This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency even improving the readout performance *(readout could be data push or triggered)*

VHDL simulation of the data push chip (100MHz/cm² input hit rate)

- Readout Effi > 99 % @ 50 MHz clock with timestamp of 200 ns.

ApselVI front-end architecture

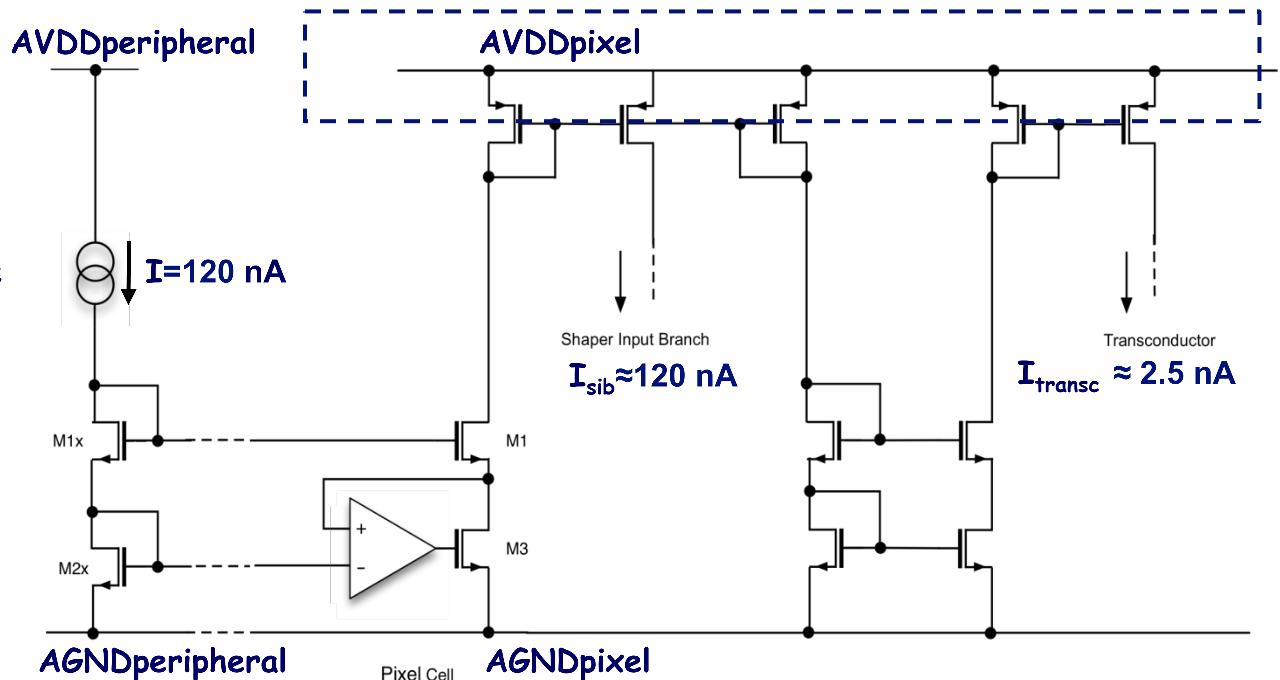


Thanks to 3D integration, the addition of a shaping stage in the analog tier makes it possible to independently optimize noise and threshold dispersion (also with a DAC for local threshold adjustment), achieving a high charge sensitivity in a reliable way

Compensation of power supply voltage drops in a large matrix

- 3D Apsel features:
  - I_{analog_cell}=25 µA
  - 128x100 pixels matrix for the next run
  - Considering the case of a larger matrix, supplied from both sides, we obtain the following voltage drop on AVDD and AGND:

ΔV_d=15/20 mV (typ/max)



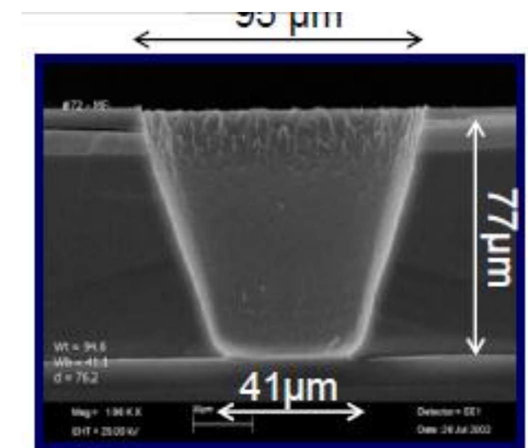
M. Manghisoni, E. Quartieri et al.,"High Accuracy Injection Circuit for Pixel-Level Calibration of Readout Electronics" presented at the *2010 IEEE Nuclear Science Symposium Conference*, Knoxville, USA, October 30 - November 6 2010.

- Voltage drop on the AVDD and AGND lines causes changes in some pixel current sources, in particular in the **shaper input branch** and in the **transconductor**. These current changes lead to a degradation of the front-end performance (i.e. charge sensitivity and peaking time).

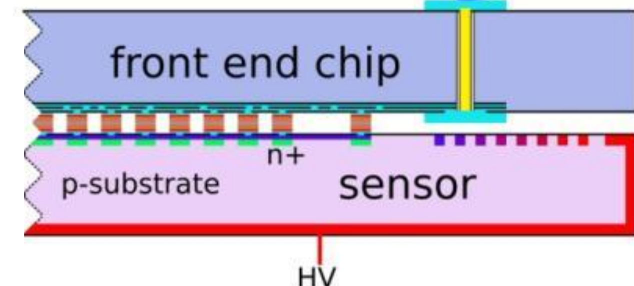
- **This problem is overcome by distributing a reference voltage to each pixel according to the schematic above.**

Perspectives and support to 3D integration in the semiconductor detector community

- 3D integrated circuits based on homogeneous layers (same CMOS technology) and high density TSVs and interconnections are a very promising approach to advanced pixel detector readout and other applications.
- The **AIDA WP3** project is supporting the less aggressive **"via last"** variant of 3D integration, where **low-density TSVs are etched in fully processed CMOS wafers**. It is a mature technology, presently available at various vendors.



- This technique makes it possible to **use heterogeneous layers** (different technologies) for sensors and front-end electronics and to fabricate four-side buttable devices with minimal dead area.
- A high-resistivity, fully depleted sensor can be combined in a low-mass assembly with a readout chip designed in an aggressively scaled CMOS generation (usually not available in the typical MAPS "Opto"processes), both with excellent radiation hardness (among other properties).
- Low-density peripheral TSVs can be used to reach backside bonding pads for external connection. The interconnection technology can be chosen according to the pixel pitch.



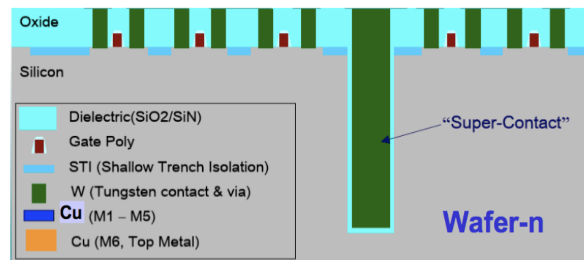
Conclusions and future plans

- Characterization of SDR1 is still in progress
  - Tests of SDR1 with radioactive sources
  - Test of the readout architecture on large (240x256) matrix
  - Conclude the radiation hardness evaluation
  - Test beam of the 240x256 matrix
- **The first 3D-IC run provided demonstrators of 3D CMOS chips, and confirmed potential advantages of 3D integration. The problems associated with this run do not have to prevent us to continue pursuing 3D as a way of devising advanced pixel detectors, also in an ILC perspective.**
- Even with not very aggressive 3D technologies, significant advantages may be gained by designing a 2-tier readout chip (for example, analog layer + digital layer)
- Ultimately, 3D integration may allow designers to avoid using sub-50 nm processes for analog and digital circuits in very small pixel readout cells.

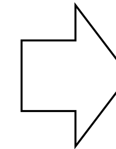
Backup slides

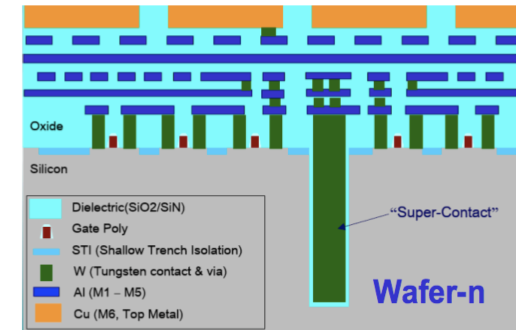
Tezzaron vertical integration (3D) process

Tezzaron uses a "via middle" approach for the fabrication of 3D chip

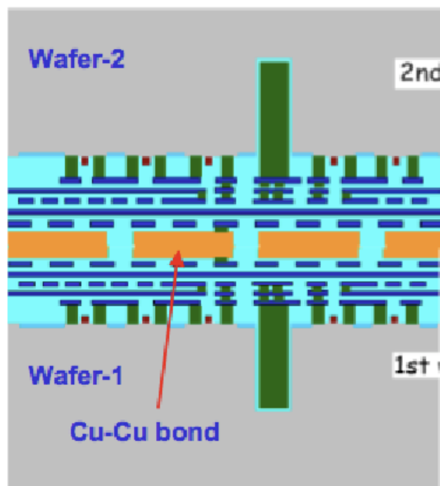


Step 1: On all wafer to be stacked complete transistor fabrication, form TSV, passivation and fill TSV at same time connections are made to transistors

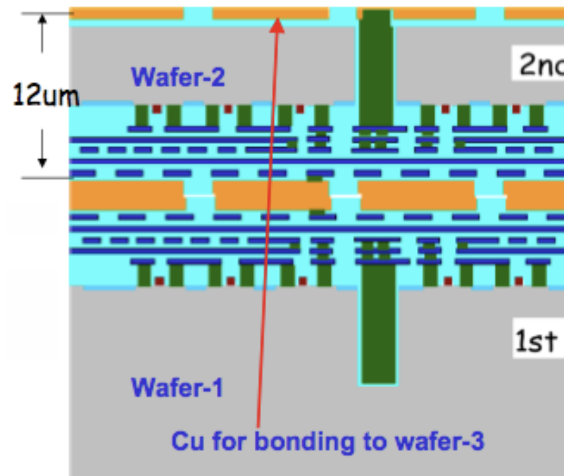




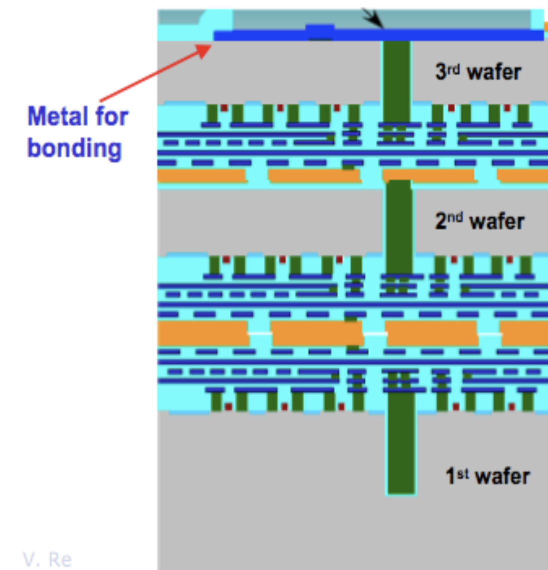
Step 2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7um)



Step 3: bond wafer 2 to wafer 1 (Cu-Cu thermo-compression bond)



Step 4: thin the wafer 2 to about 12um to expose TSV. Add Cu to back of wafer 2 to bond wafer 2 to wafer 3 OR add metallization on back of wafer 2 for bump bonding or wire bonding



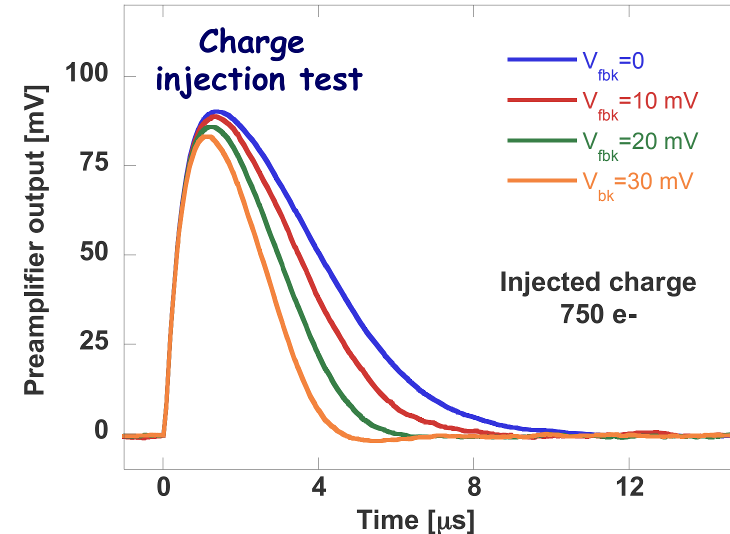
V. Re

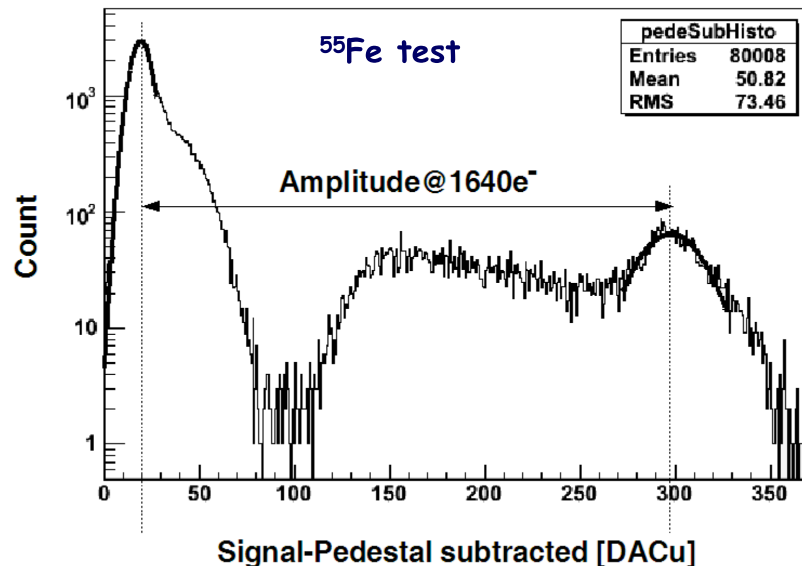
Step 5: stack wafer 3, thin wafer 3 to expose TSV, add final passivation and metal for bond pads.

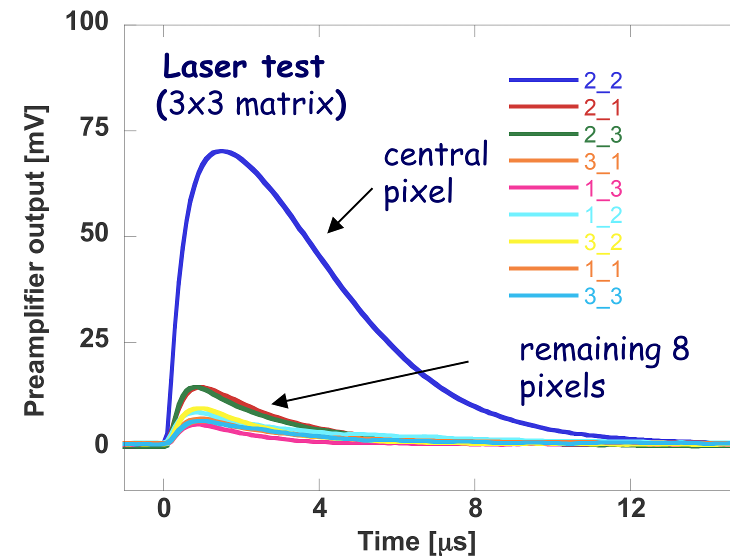
SDR0, a prototype DNW MAPS for the ILC VTX

Main design features and experimental results

- W/L=22/0.25
- I_D=1 μA, power dissipation=5 uW
- C_D=100 fF
- ~1 μs peaking time
- Power cycling capabilities
- Charge sensitivity (G_Q): 650 mV/fC
- Equivalent noise charge (ENC): 50 e-
- Threshold dispersion (DQ_t): 50 e-
- Digital readout fully functional at 50 MHz

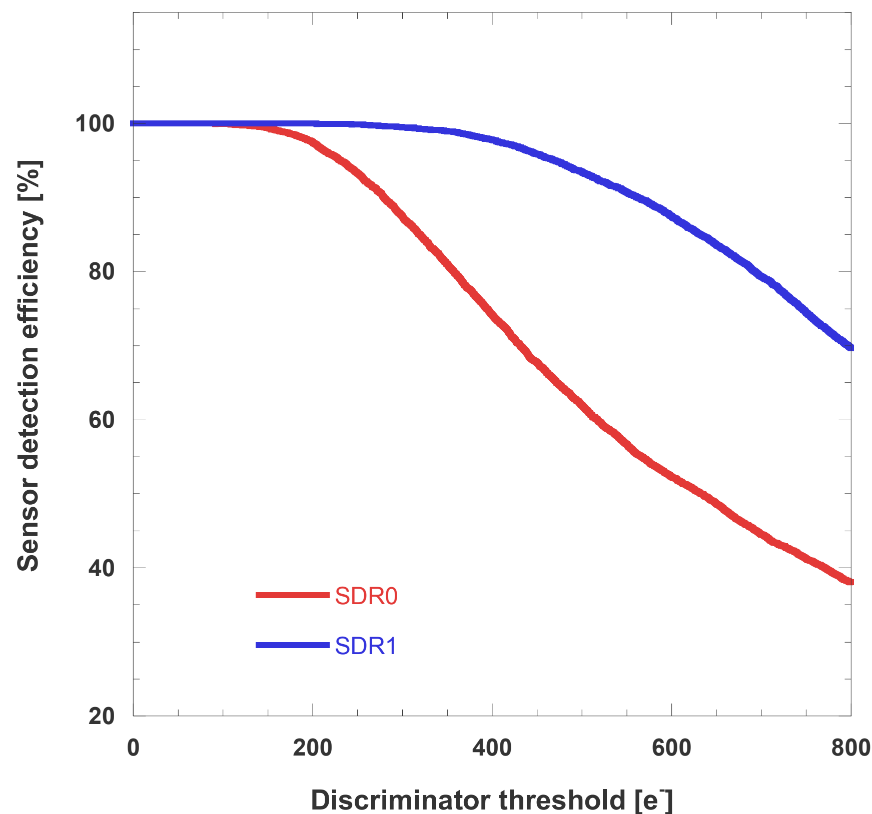


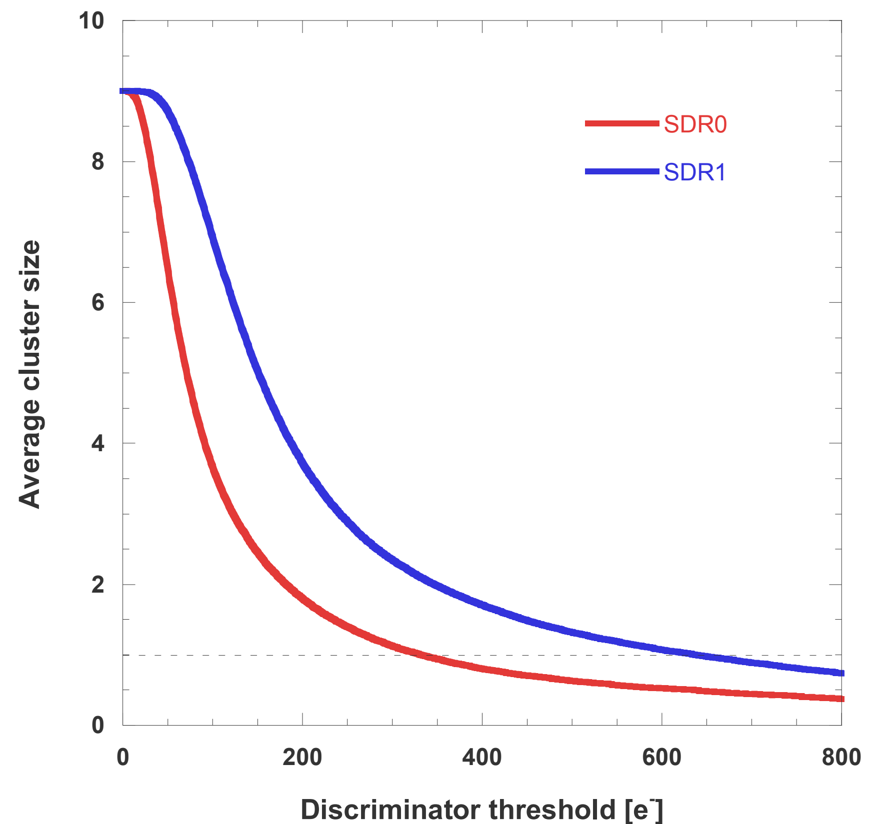




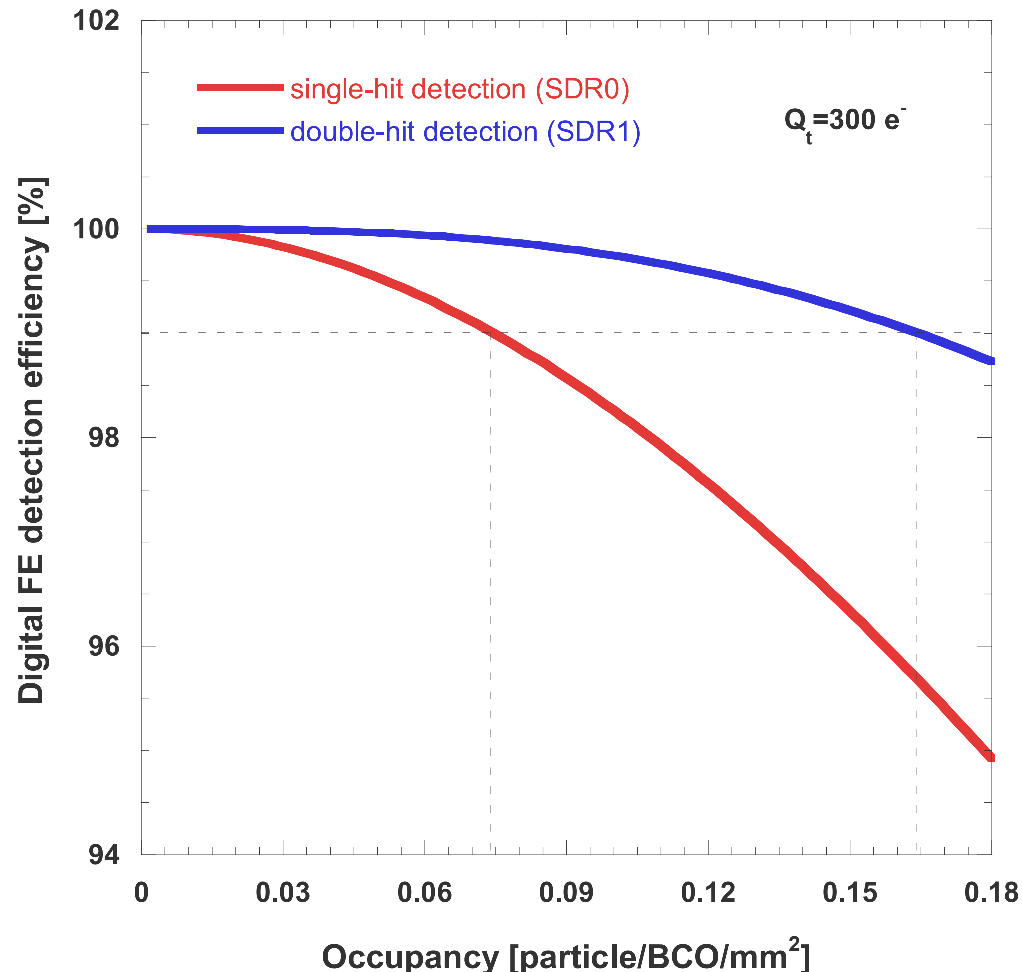
Sensor detection efficiency and cluster size

- Monte Carlo simulations on matrices of 3x3 DNW MAPS featuring the layout of the SDR0 and SDR1 sensors (10000 experiments, 80 μm thick substrate)





Digital FE detection efficiency

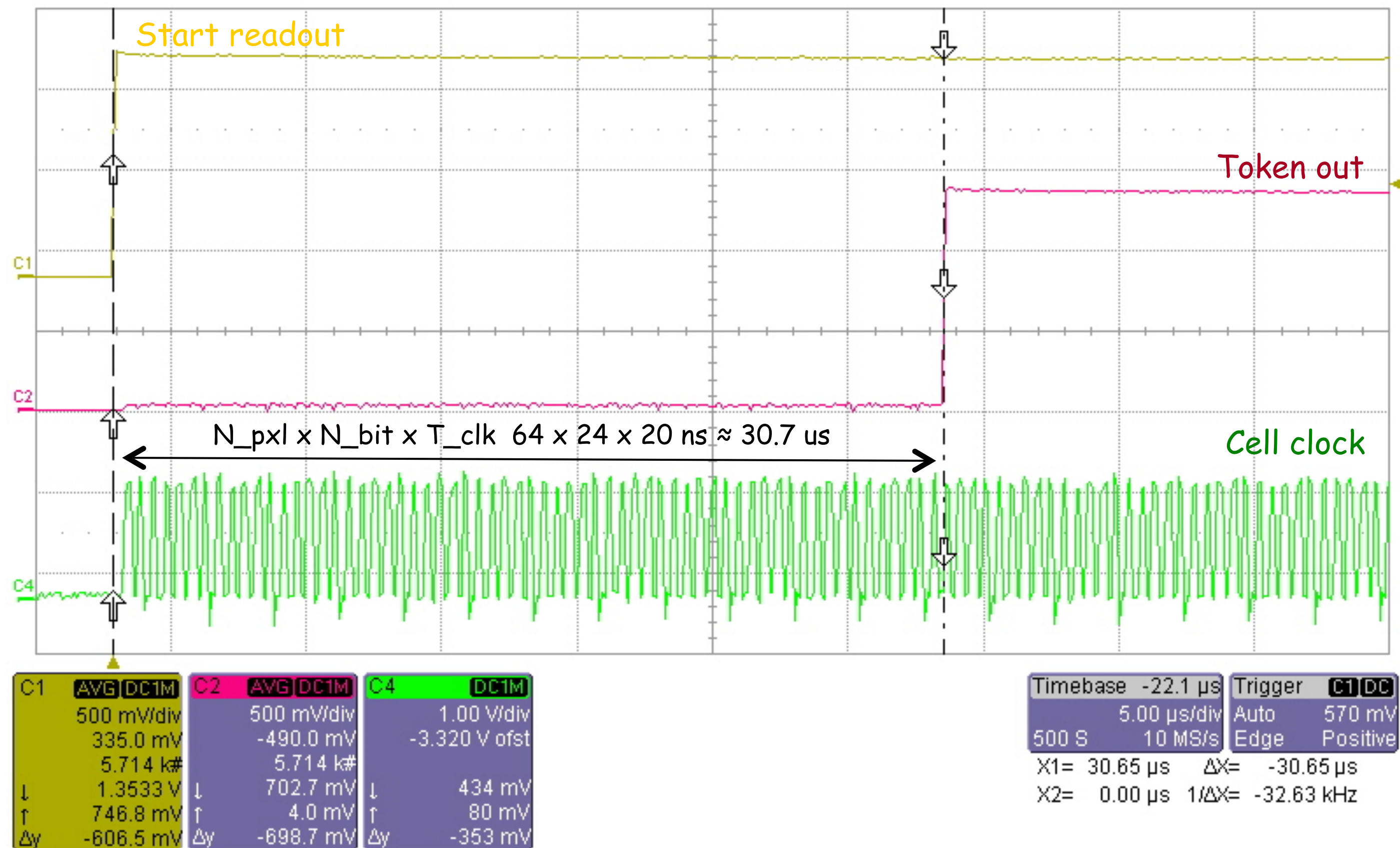


- Increased functional density in the digital FE section improves the detection efficiency
- Curves obtained by taking into account the average cluster size (1.13 for SDR0, 2.35 for SDR1) at a discriminator threshold of 300 e-

Digital readout test

Signals from an 8x8 matrix at 50 MHz readout clock

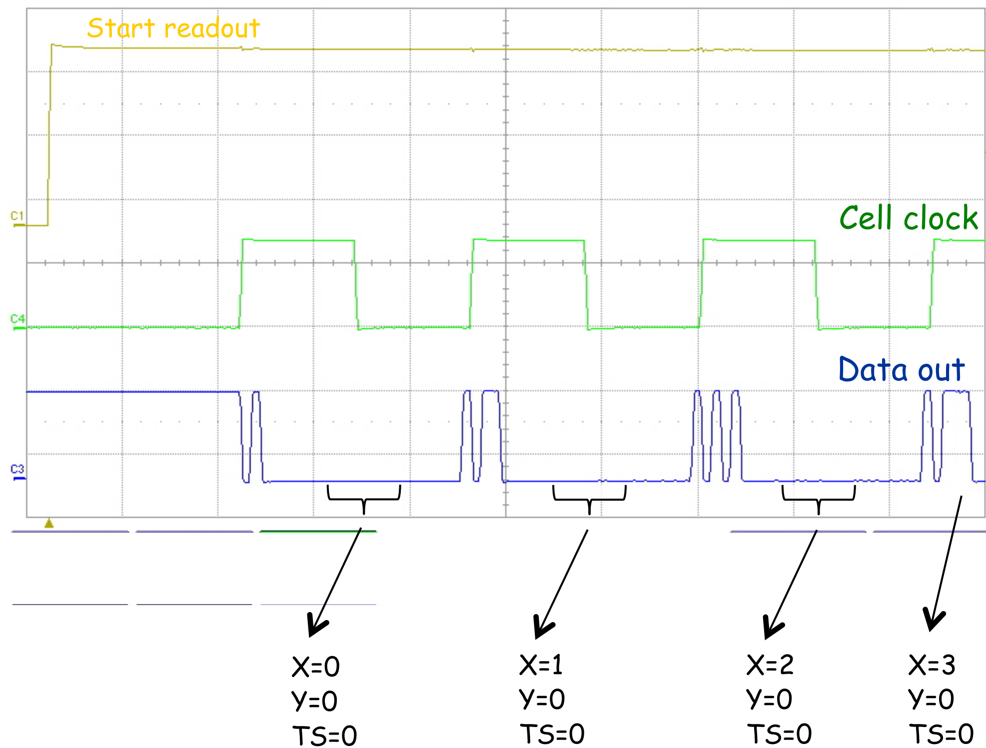
Vth < PA output DC level -> all the pixels are read out

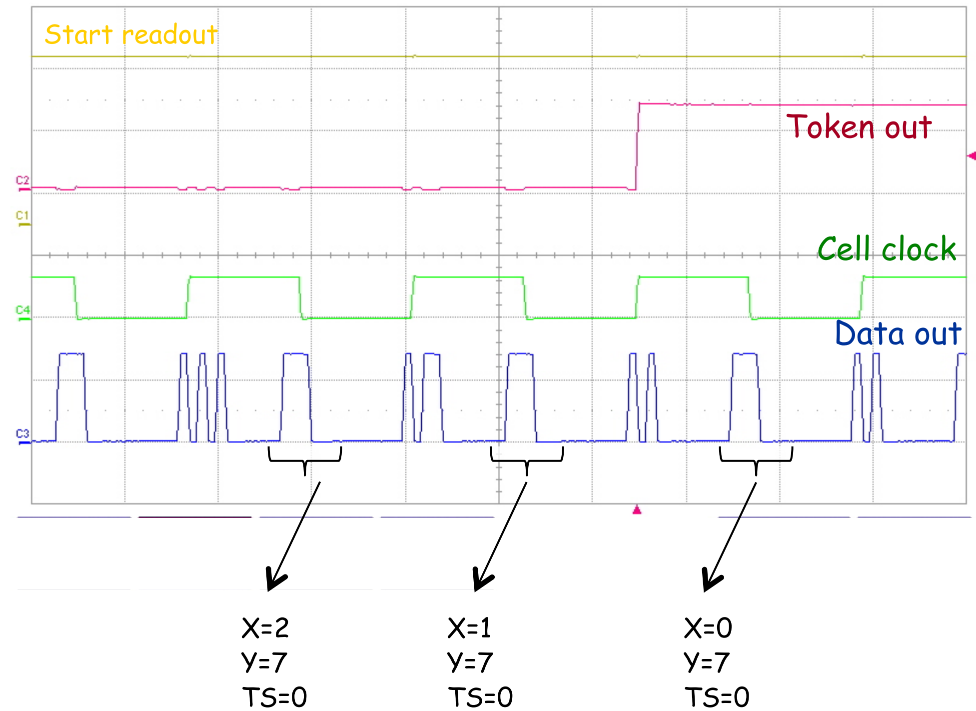


Digital readout test

Signals from an 8x8 matrix (details of the first and last read out cells, f_{CK}=5 MHz)

Vth < PA output DC level -> all the pixels are read out



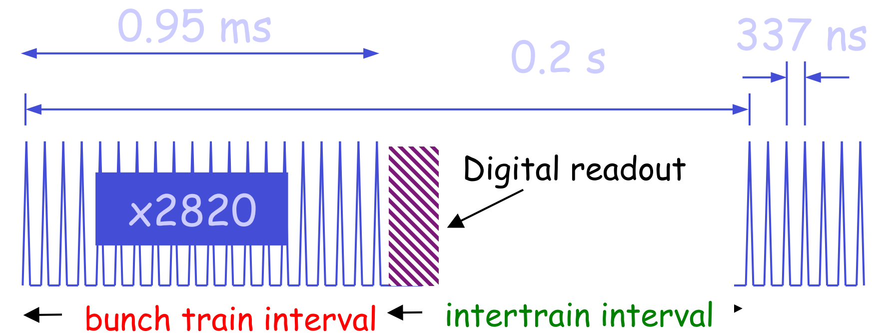


Digital front-end

The digital tier includes a number of digital blocks (double hit detection and double 5-bit time stamp, data sparsification and pixel masking)

Chip operation tailored on the ILC beam structure

- detection phase, corresponding to the bunch train interval
- readout phase, corresponding to the intertrain interval



- During the detection phase, the SR FF (FFSRK) is set, and the relevant time stamp register gets frozen, when the pixel is hit for the first time
- Upon a second hit, the D FF (FFDR) is set and the relevant time stamp register gets frozen