AGH University of Science and Technology

Readout electronics for LumiCal detector
Present status and new developments

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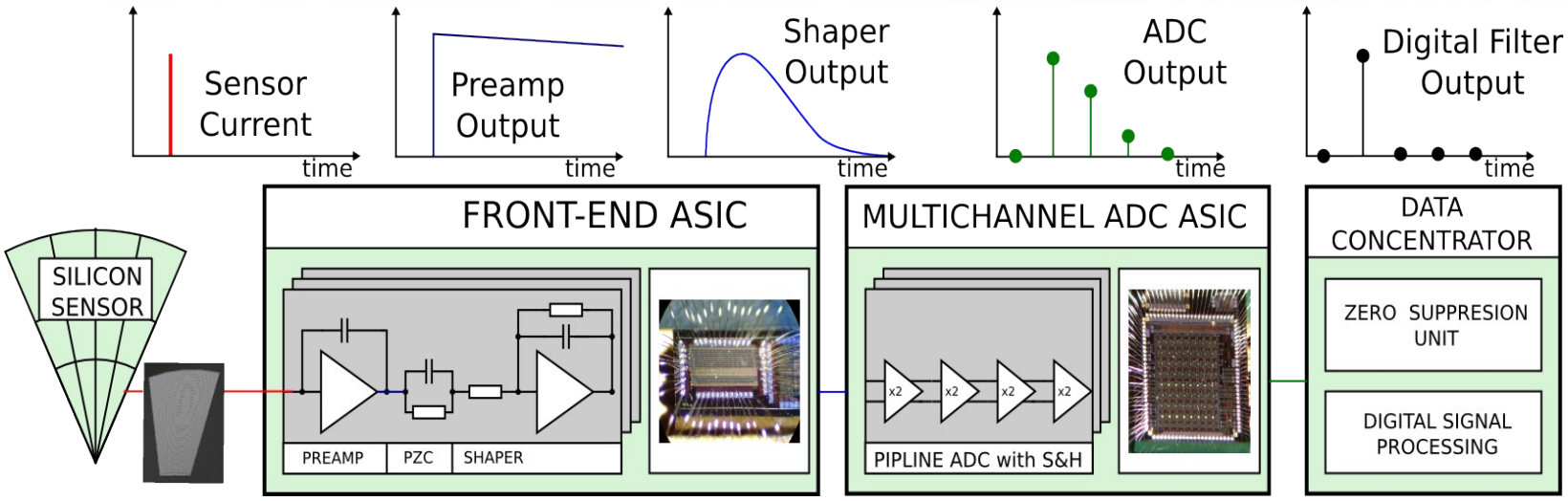
AGH University of Science and Technology

ECFA Linear Collider Workshop 2013 27 – 31 May 2013, DESY in Hamburg, Germany

Agenda

- **Present LumiCal Readout**
- **ASIC developments in IBM CMOS 130nm:**
  - Front-end electronics
  - 10b SAR ADC
  - PLL, Single Ended-to-Differential converter
- **Preliminary measurements of prototypes**

Present LumiCal Readout
LumiCal detector readout chain
Status and plans



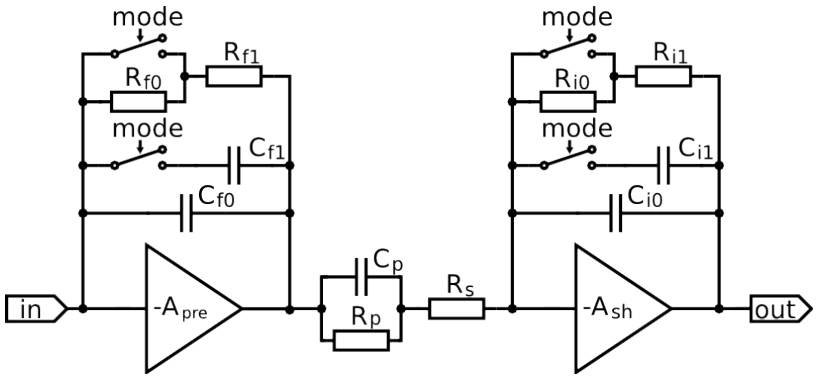
Existing LumiCal detector readout comprises:

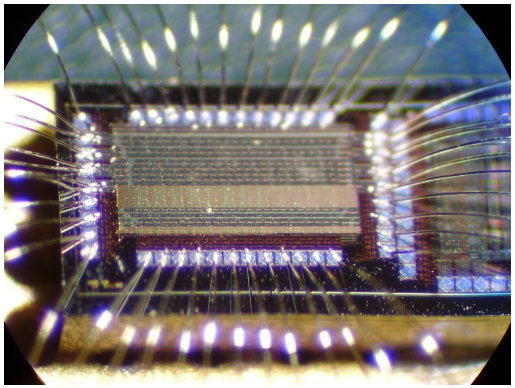
- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

New developments for LumiCal detector readout:

- Prototype front-end ASIC **in IBM 130 nm under development…**
- Prototype SAR ADC ASIC **in IBM 130 nm under development…**

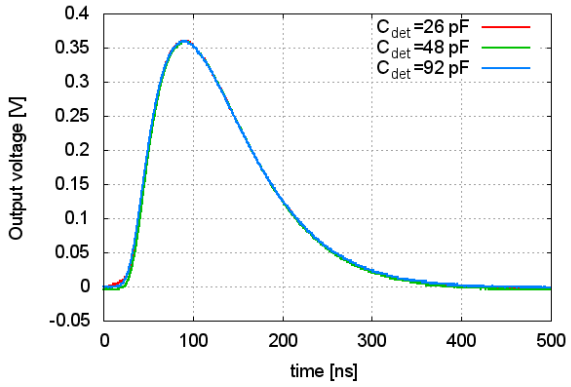
Present LumiCal Readout
Front-end Electronics for LumiCal detector in AMS 0.35um





Existing prototypes:

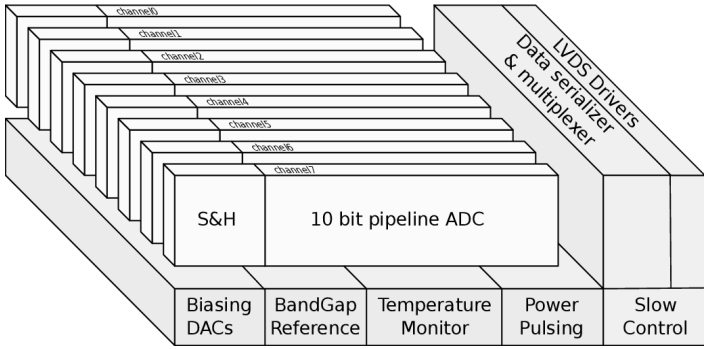
- 8 channels in AMS0.35um
- Cdet ≈ 0 ÷ 100pF (in new specs: Cdet<30pF)
- 1st order shaper (Tpeak ≈ 60 ns)
- Variable gain:
  - calibration mode - MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC
- Prototypes fabricated and tested
  - power consumption 8.9 mW/channel
  - event rate up to 3 MHz
  - Crosstalk < 1%

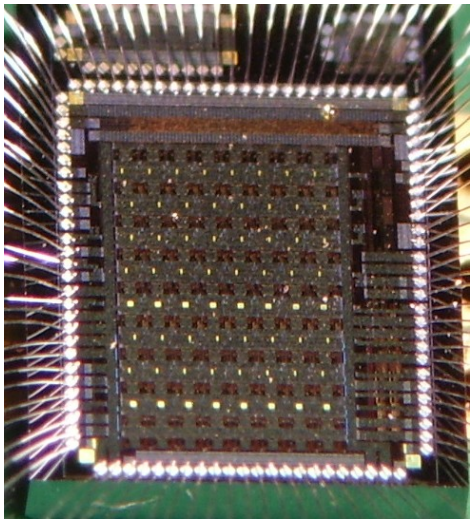


M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminosity detector at ILC", NIM A 608 p.169-174, 2009

Present LumiCal Readout
Multichannel digitizer in AMS 0.35um architecture

- Specs & impleentation issues:
  - 8 channels of 10-bit pipeline ADC
  - Technology AMS 0.35um
  - Fully differential ADC
  - Layout with 200um ADC pitch
  - Multimode digital multiplexer/serializer:
    - Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
    - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
    - Test mode: single channnel output (max fsmp ~50 MSps)
  - High speed LVDS interface (~1GHz)
  - Bootstrapped S/H switches
  - Power pulsing
  - Low power DACs for internal settings
  - BandGap reference source
  - Temperature sensor

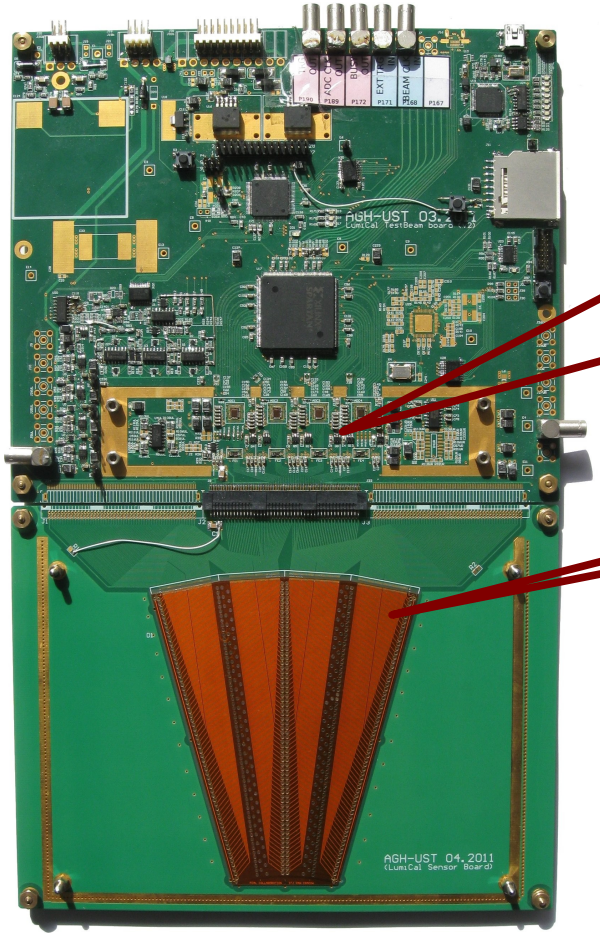




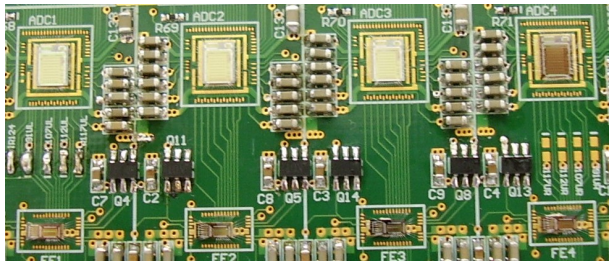
2.6mm x 3.2mm

M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. vol. 59 pp. 294-302, 2012

Present LumiCal Readout
LumiCal detector readout module (ASICs in AMS 0.35um)



4 pairs of Front-end + ADC

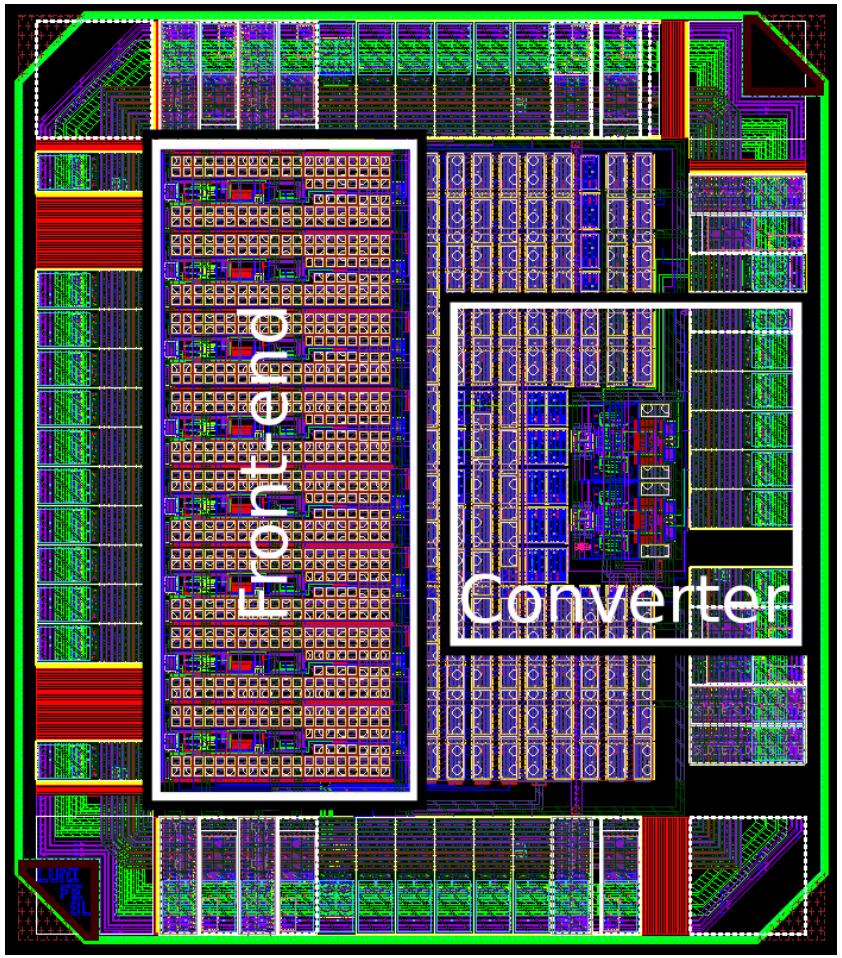


Sensor (IFJ PAN)

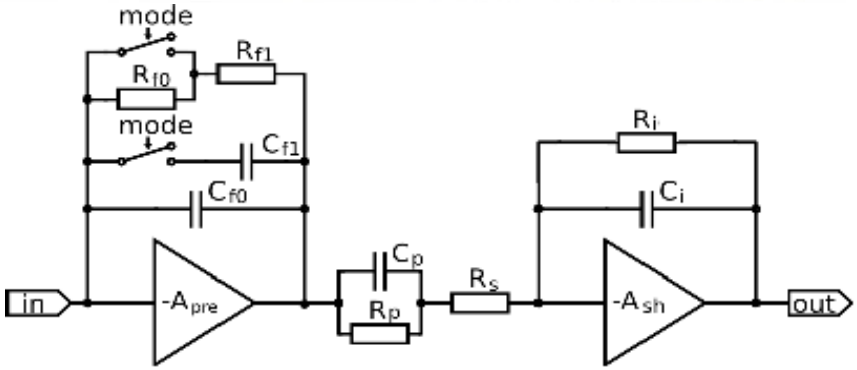
- LumiCal detector module with 32 fully equipped channels (Front-end +ADC ASICs) plus FPGA data concentrator is regularly used during FCAL Collaboration test-beams

S. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", JINST 7 T01004 2012

Developments in IBM CMOS 130nm
Front-end: Preamplifier & Shaper



Design submitted in February 2013



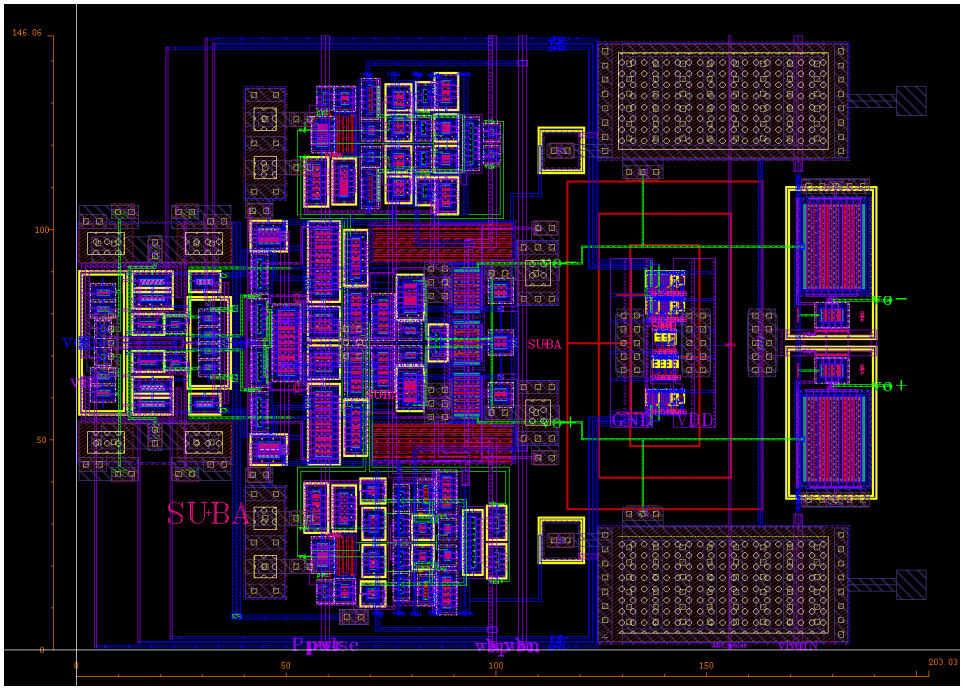
Design specs:

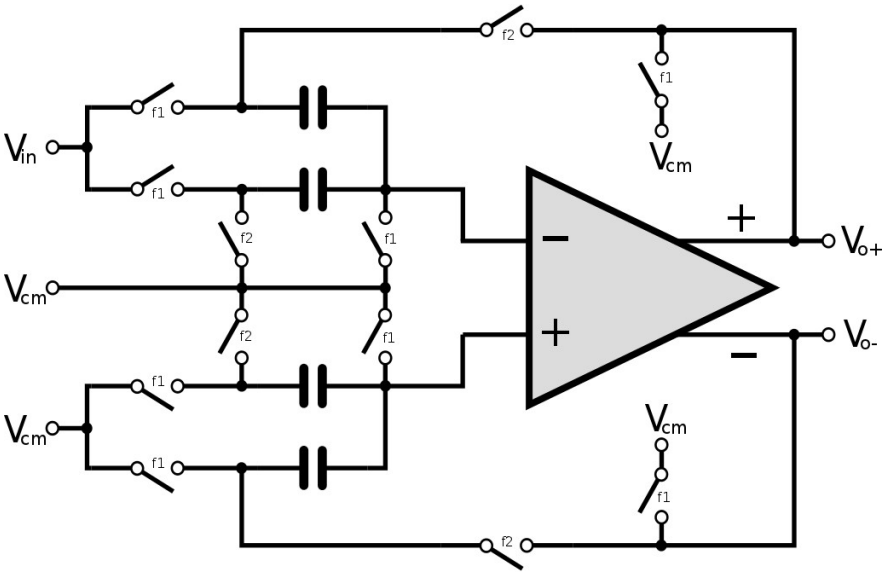
- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~6 pC
- Power pulsing implemented
- Simulated power consumption ~1.5 mW/channel

Developments in IBM CMOS 130nm
Single Ended-to-Differential converter

Single Ended to Differential converter

- Dynamic input range ~600 mV
- Differential output range ~1.2V
- Maximum frequency ~ 50 MHz

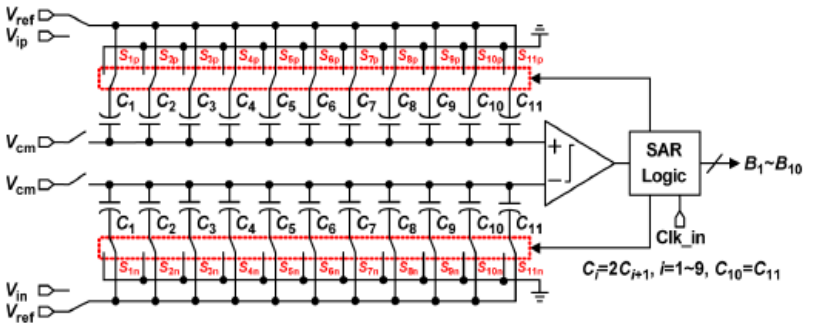




Design submitted February 2013

Developments in IBM CMOS 130nm
SAR ADC: General features & design considerations

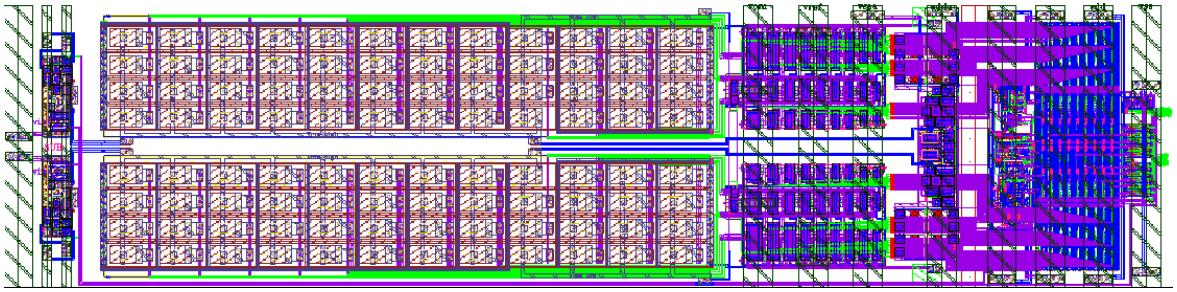
- Power and area-efficient architecture – the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage
- Only one comparator, two DACs and SAR logic needed – fits well to modern digital CMOS
- Limited sampling rates - but with modern CMOS technology (~100nm) up to ~100MSps 10-bit ADCs were reported
  - next conversion cannot be started before completion of previous one
  - sampling time adds to conversion time (not like in pipeline)



- Comparator – the only analog block
- DAC network serves as sampling capacitance
- Simple digital logic
- Fully differential implementation increases the resistance to disturbances

Developments in IBM CMOS 130nm
Design of 10-bit SAR ADC

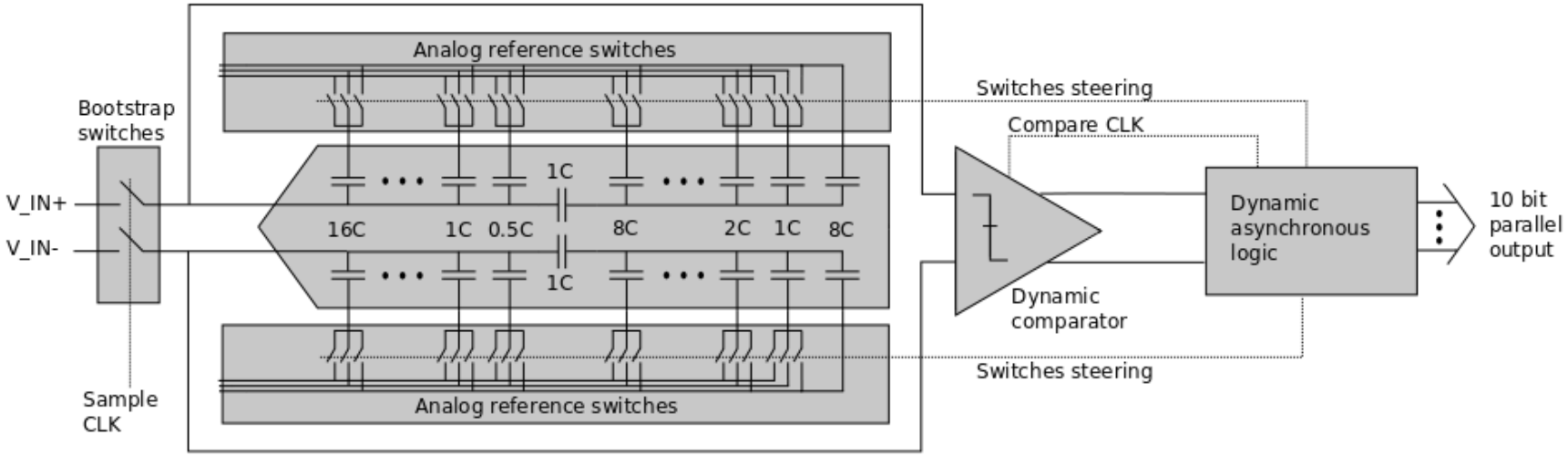
SAR channel 600um x 146um



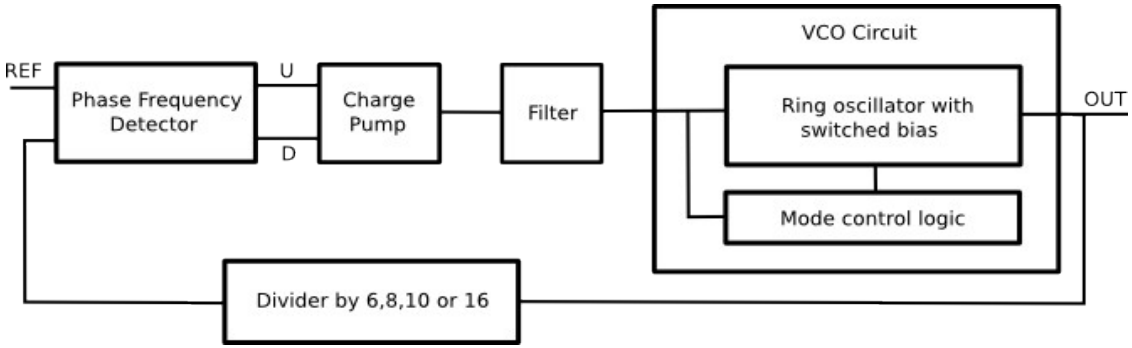
Designs of 10-bit ADC

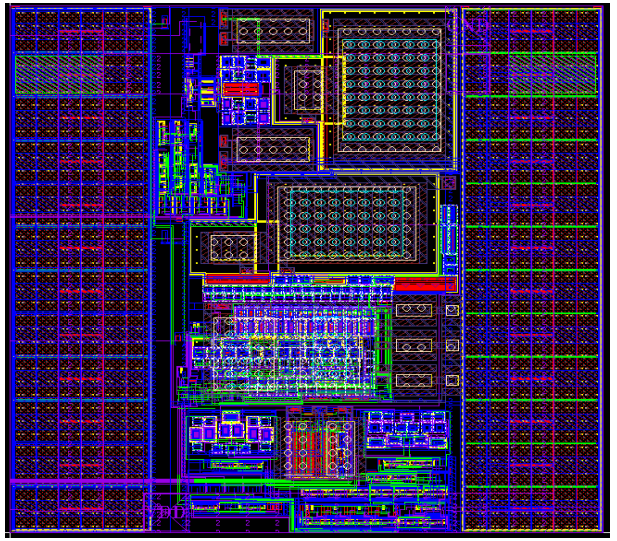
- Architecture: SAR ADC with segmented/split DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- Asynchronous SAR logic – No bit-clk

- 1-2 mW at 40 MS/s
- 146um pitch
- Fabricated in 2012 (2 prototypes)



Developments in IBM CMOS 130nm
Design of PLL for data serialization



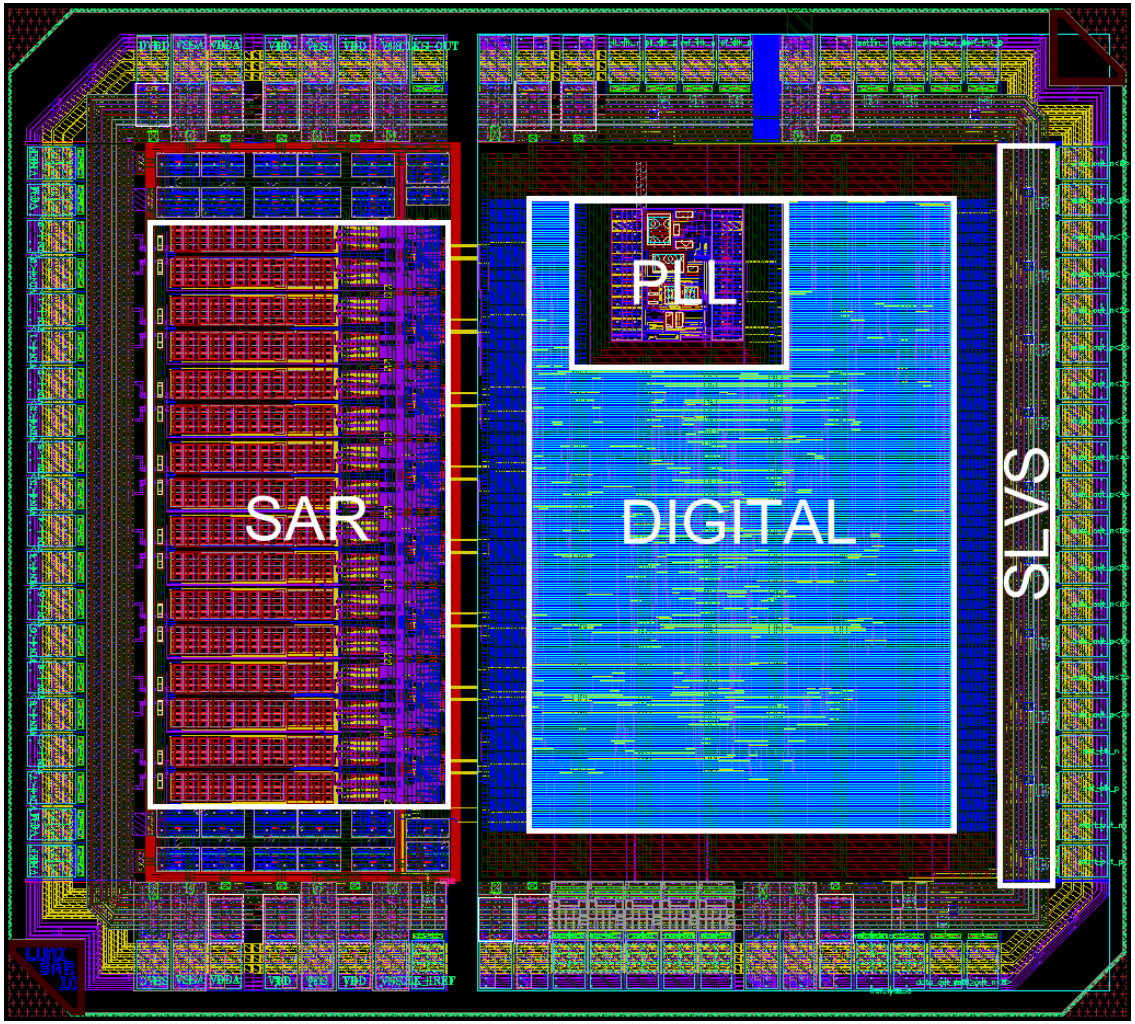


300 x 300 um

Design specs:

- Architecture: type II PLL with 2nd order filter
- Scalable frequency & power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- ***Submitted and fabricated in 2012, the tests have just started…***

Developments in IBM CMOS 130nm
Layout of 8 channel 10-bit SAR ADC



ASIC comprising:

- 8 channels of 10-bit SAR ADC,
- Multimode digital multiplexer / serializer
- PLL for data serialization
- High speed SLVS interface

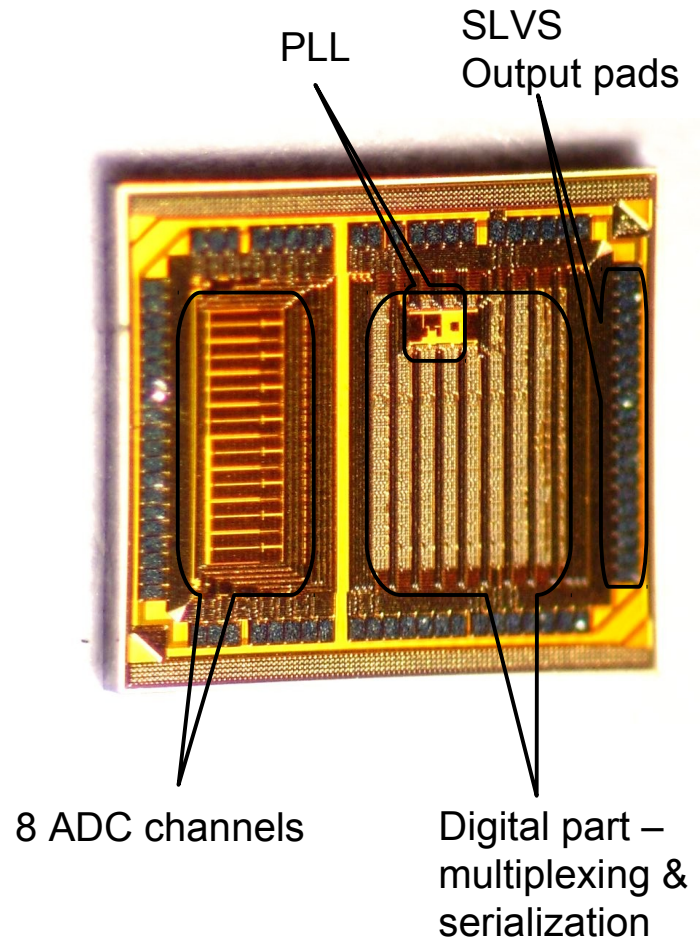
Design submitted and fabricated in 2012

2200um x 2000um

Preliminary measurements
First prototypes in IBM 130nm under tests
10-bit ADC, PLL, SLVS

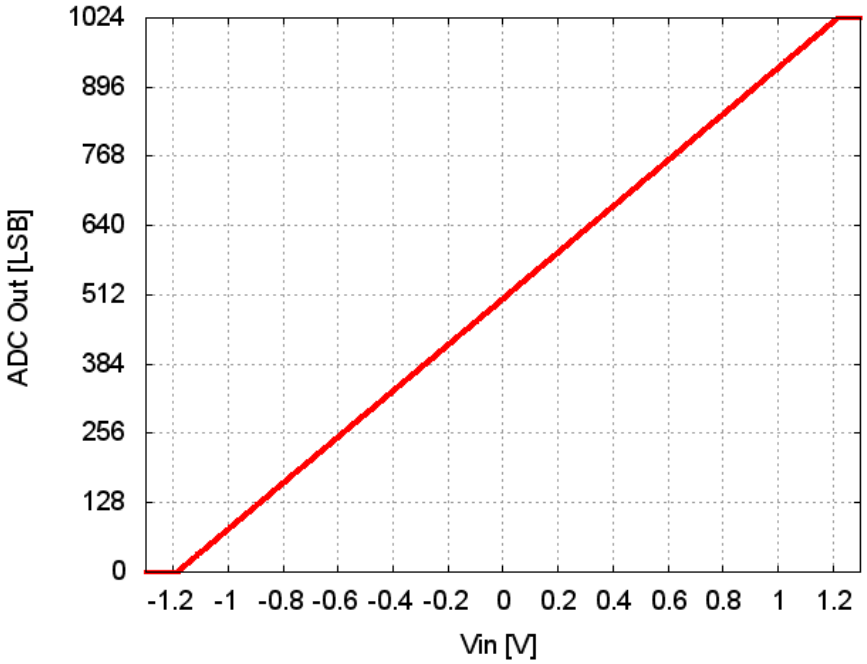
Prototype ASIC contains:

- 10-bit SAR ADC
- PLL
  - Systematic tests are just starting. PLL output clock signal was observed with scope.
- SLVS interface
  - No dedicated tests of SLVS interface were done, but looking at ADC and PLL differential outputs it was verified that SLVS driver operates at least up to 700 MHz.

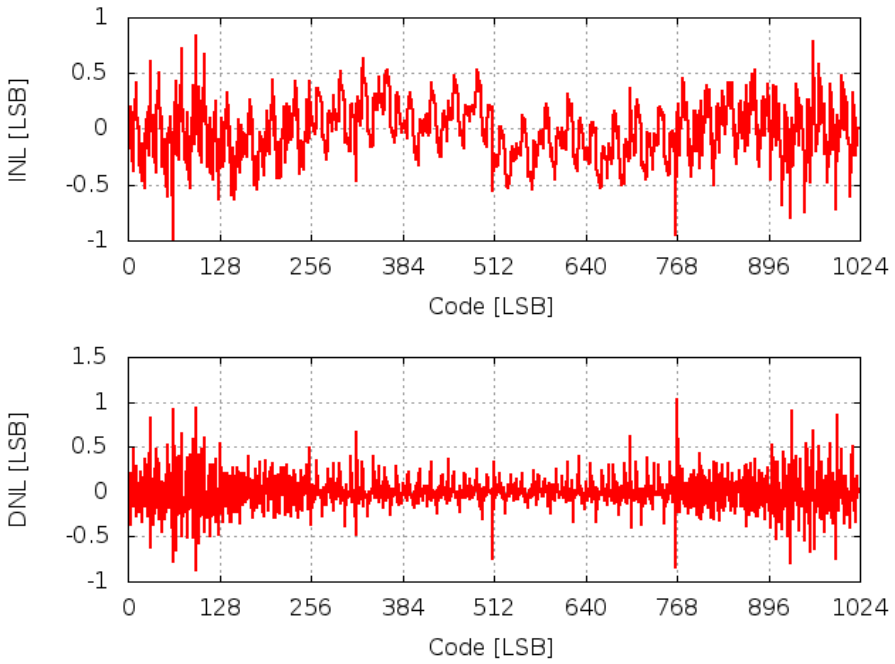


Preliminary measurements
10-bit SAR ADC - Static measurements

Transfer function

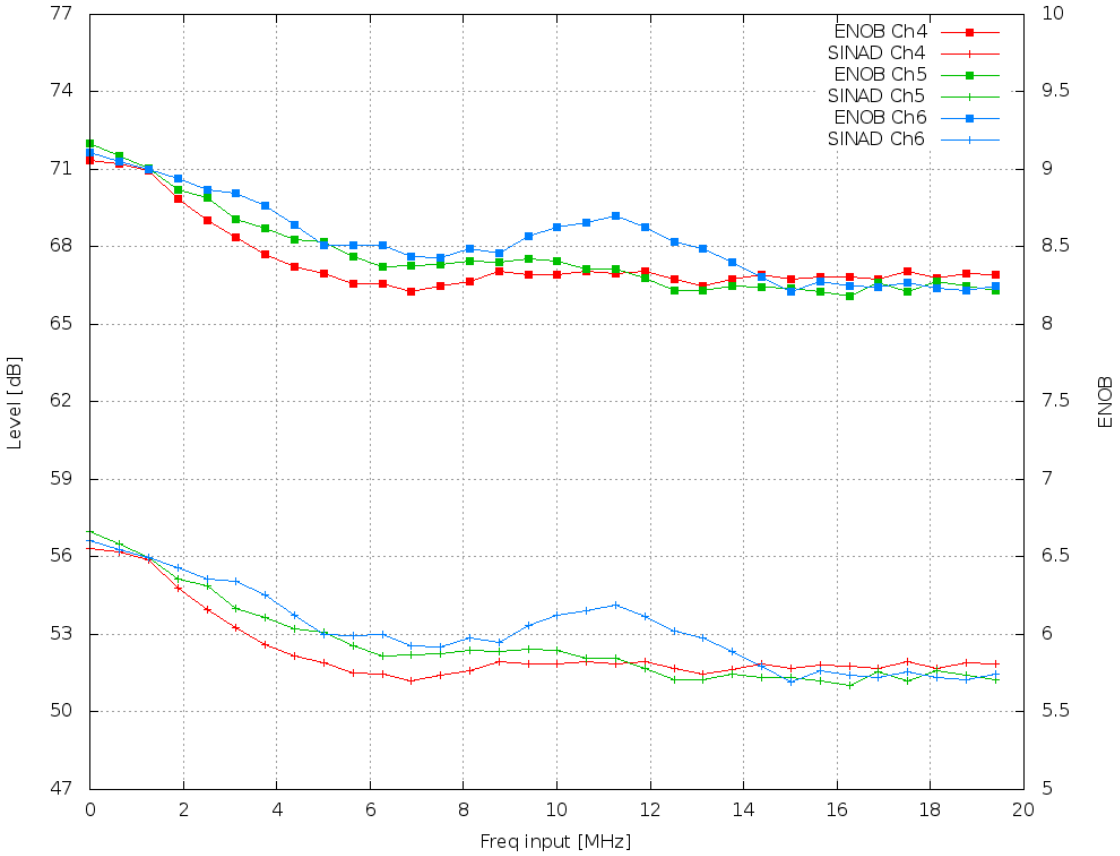


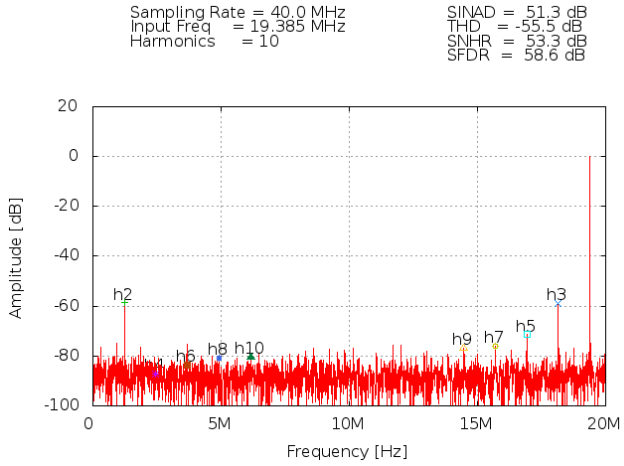
INL/DNL measurements



- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (to be investigated...)

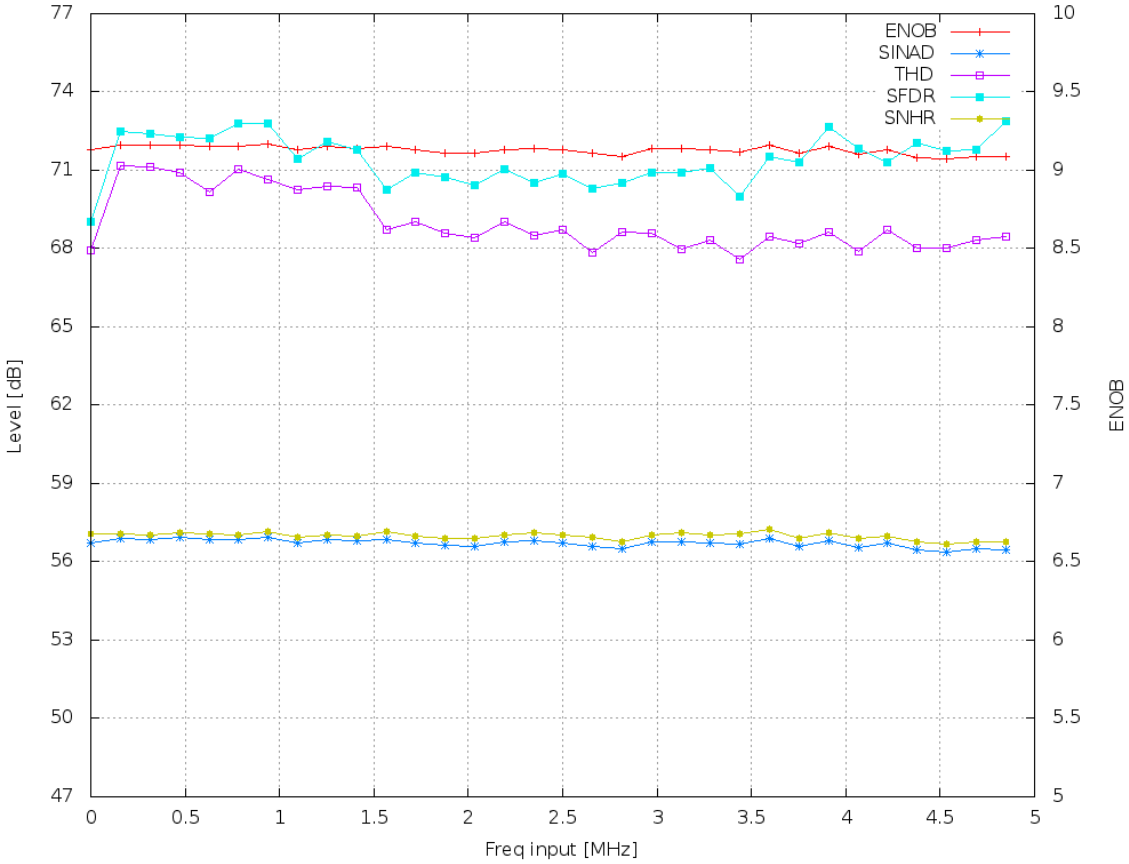
Preliminary measurements
10-bit SAR ADC - Dynamic measurements – different channels

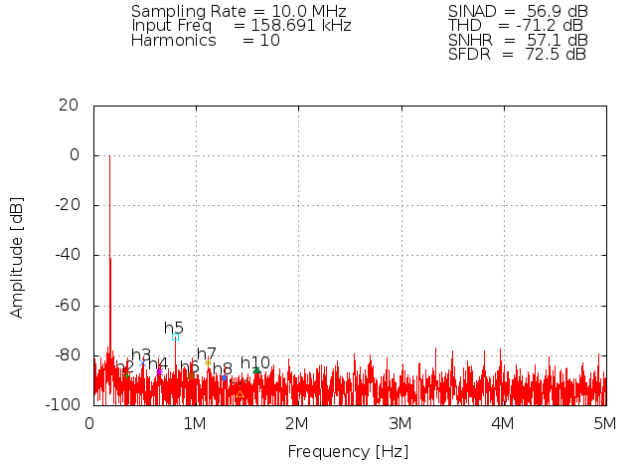


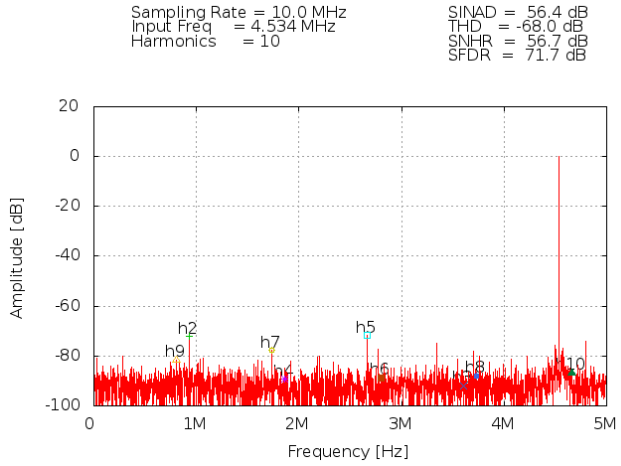


- Results for different channels (only one channel ON during measurements) are similar
- It was suspected that ENOB decrease with f_{in} is partially/mainly due to setup

Preliminary measurements
10-bit SAR ADC - Dynamic measurements – f_{in} scan



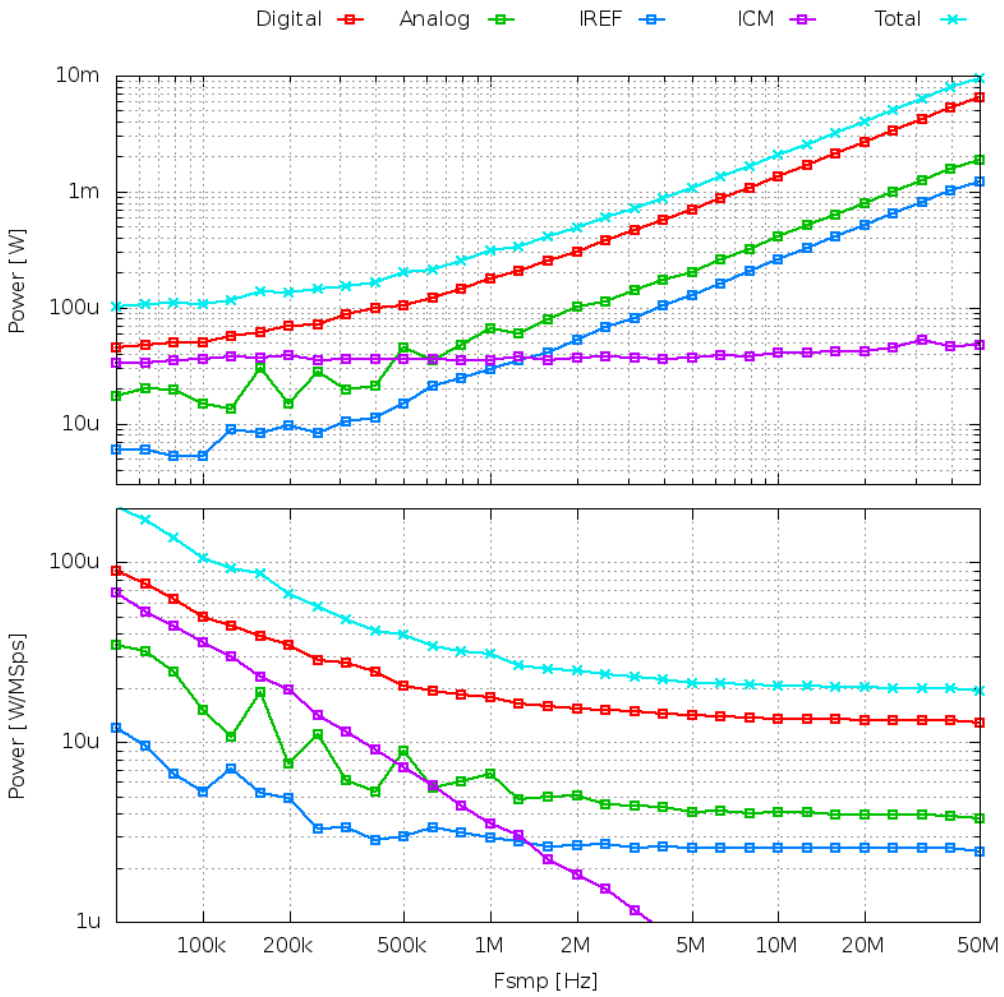




- ENOB of >= 9.2 was measured up to Nyquist frequency after improving test setup – more improvement needed?

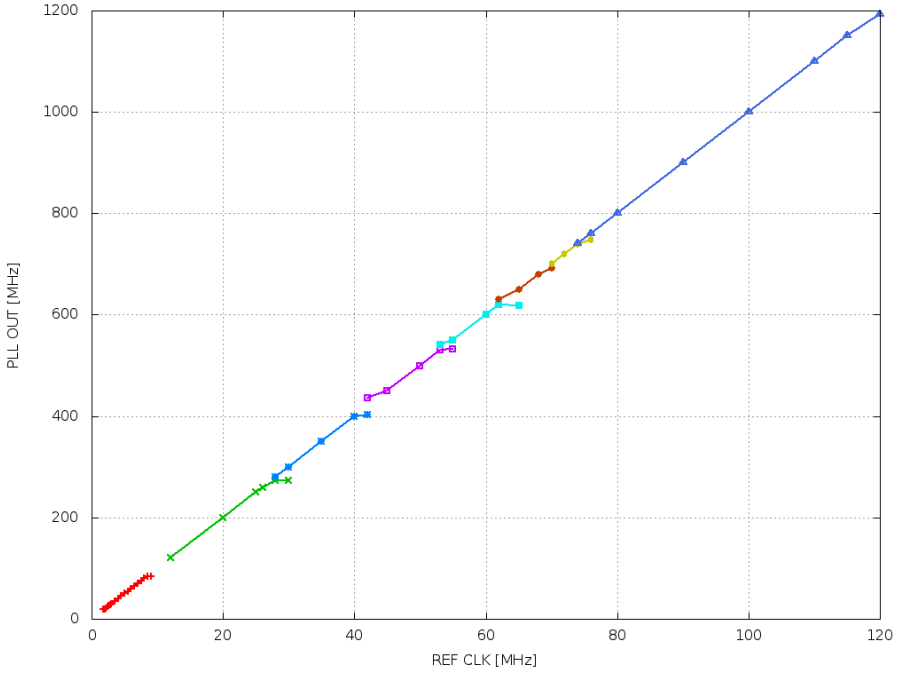
Preliminary measurements
10-bit SAR ADC - Power consumption vs sampling frequency

- Power measured for 8 ADC channels
- At 40MS/s power consumption is about 1 mW per channel – in agreement with simulations

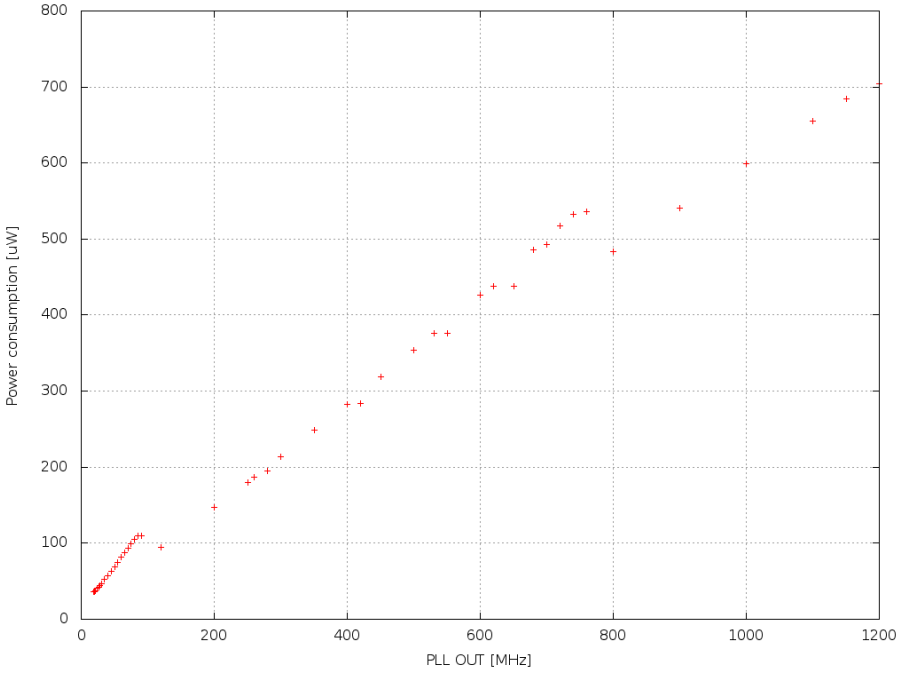


Preliminary measurements
PLL – Transfer function, power consumption

PLL transfer function – CLK out vs CLK in



Power consumption measurements



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

Summary and Plans

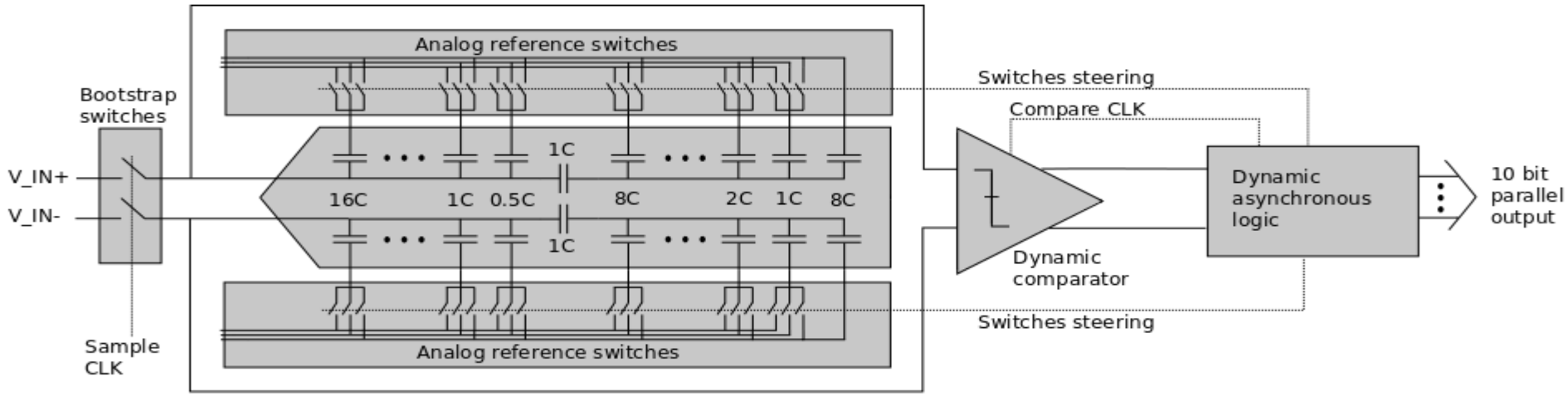
- Presently FCAL uses in test-beams the readout modules based on developed at AGH-UST ASICs in CMOS AMS 0.35um
- Development of new ASICs for LumiCal readout in IBM 130 nm in progress:
  - First prototype of front-end electronics submitted and should be available in ~June 2013
  - First prototypes of 10-bit SAR ADC, PLL, SLVS already produced and presently under test:
    - 10-bit SAR ADC: first results show its functionality, the effective resolution slightly less than simulated - quantitative measurements in progress...
    - PLL tests just started...
    - SLVS interface works well
  - Depending on test progress and results we plan next submission at the turn of 2013/2014

Backup slides

Developments in IBM CMOS 130nm
Design of SAR ADC - Implementation issues

- Asynchronous logic
  - no fast clock needed for bit cycling
  - only sampling pulse needed
  - sampling pulse (trigger) does not need to be periodic
- Dynamic comparator
  - alows to obtain zero static power consumption and so "power pulsing" is given for free

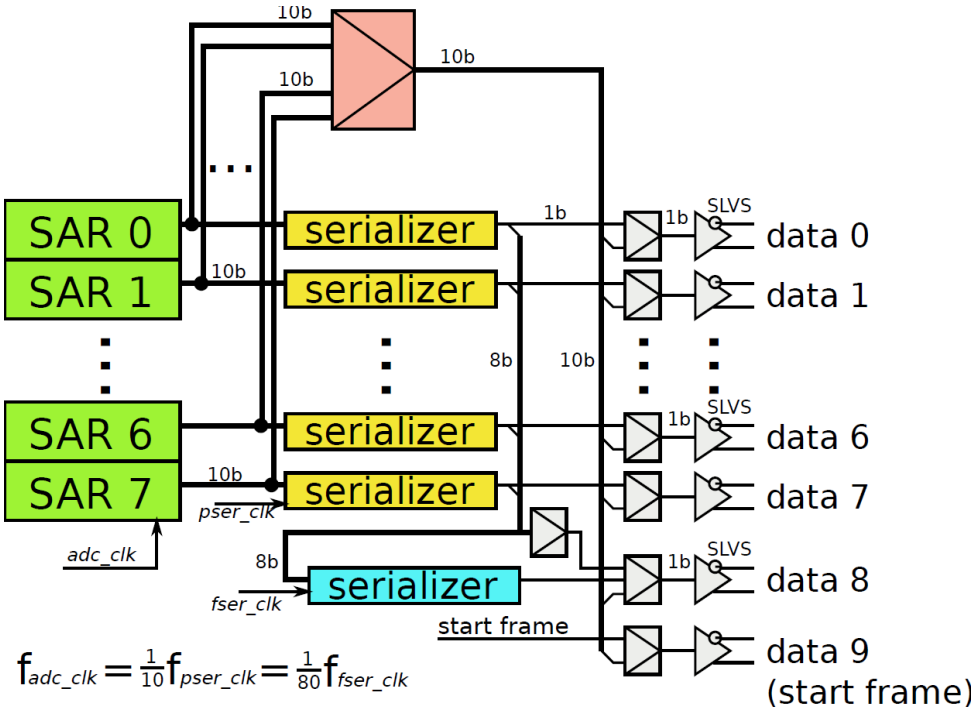
- Split DAC architecture
  - allows using higher unit capacitance for the given total DAC capacitance. It helps to bypass the problem of relatively high C_{min} available in CMOS technologies – allows to decrease the effective "LSB capacitance" and so power consumption



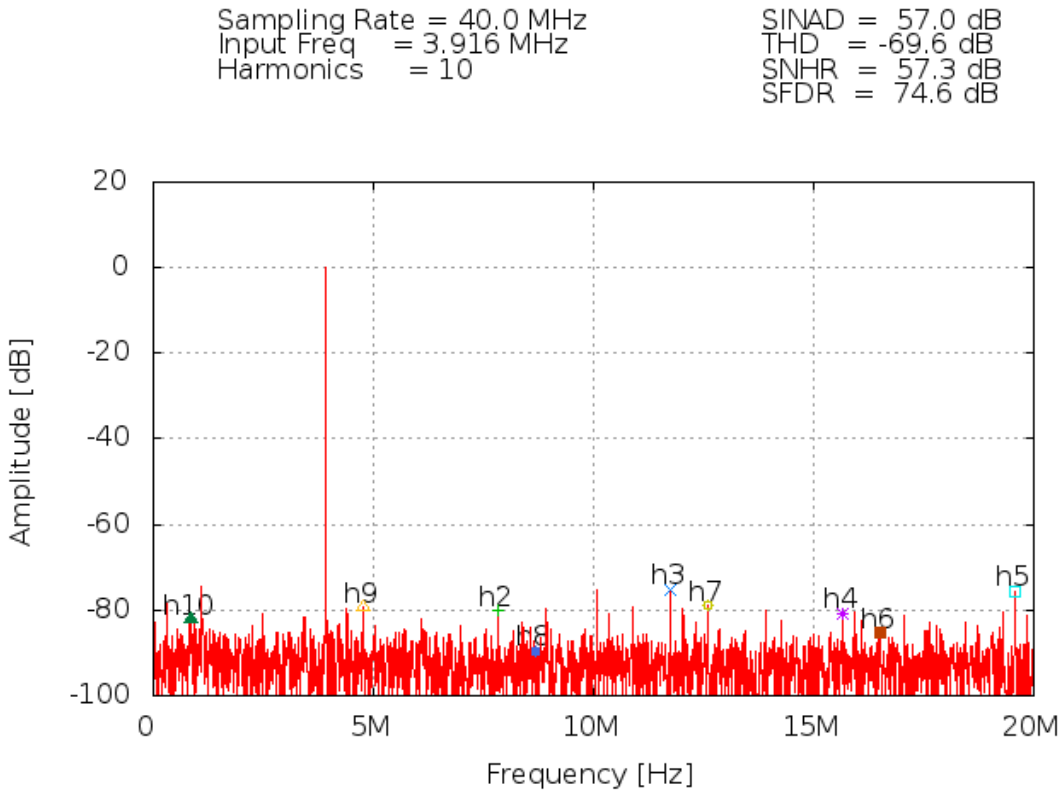
Developments in IBM CMOS 130nm
Development of multichannel SAR ADC

Specifications :

- 8 channels of 10-bit SAR ADC
- Technology IBM 130 nm
- Layout with 146um ADC pitch
- Multimode digital multiplexer/serializer:
  - Serial mode: one data link per all channels (external clk division or PLL clk generation)
  - Parallel mode: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channnel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing

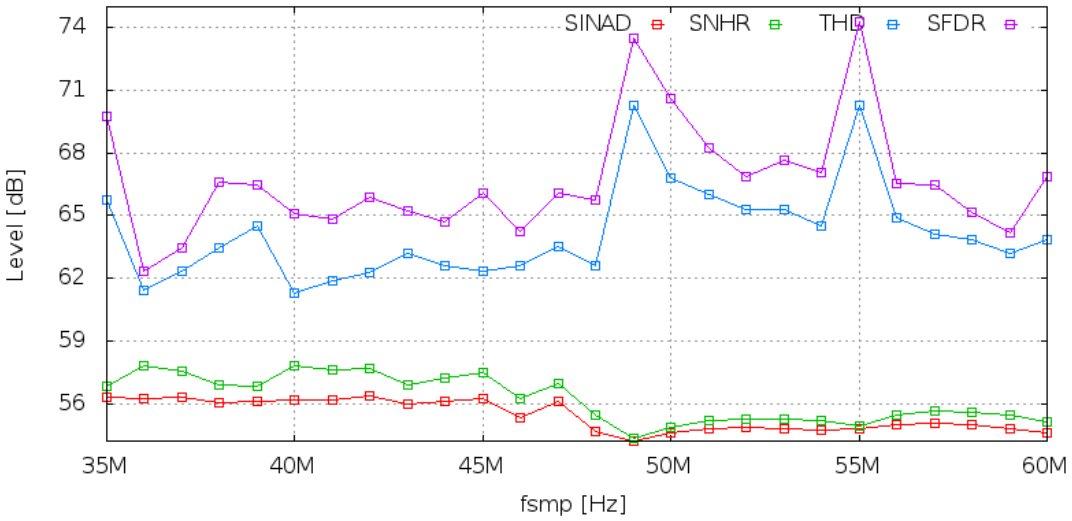


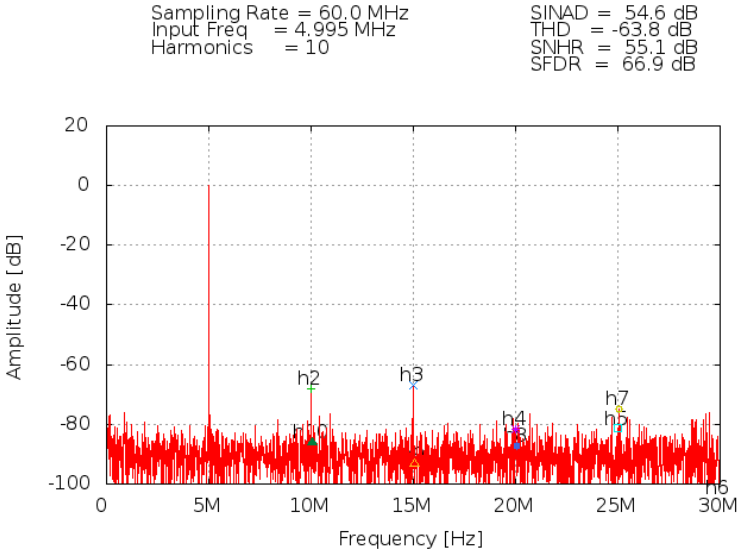
Preliminary measurements
10-bit SAR ADC - Dynamic measurement at 40Ms/S



- First dynamic measurements show that ADC is fully functional and gives reasonable resolution results
- Quantitative measurements in progress...

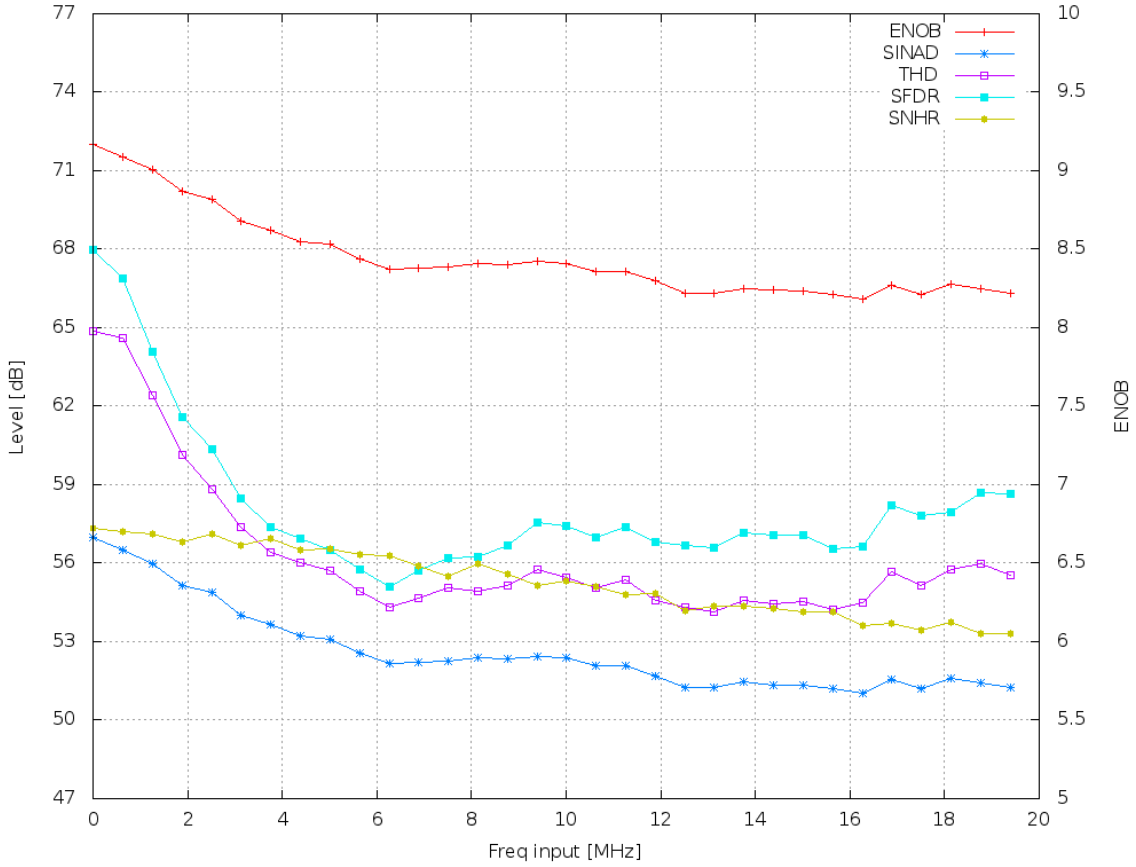
Preliminary measurements
10-bit SAR ADC - Maximum sampling frequency

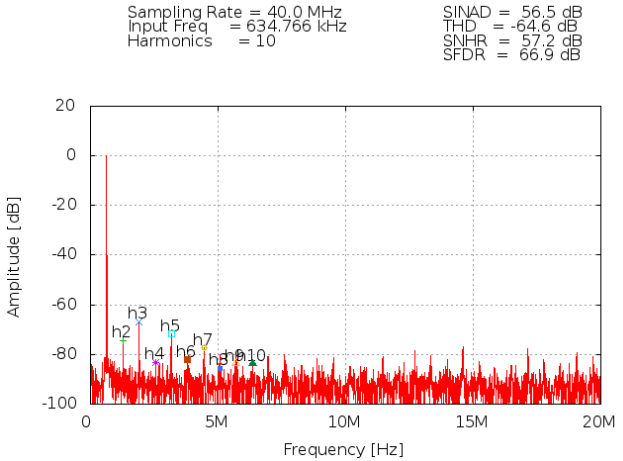


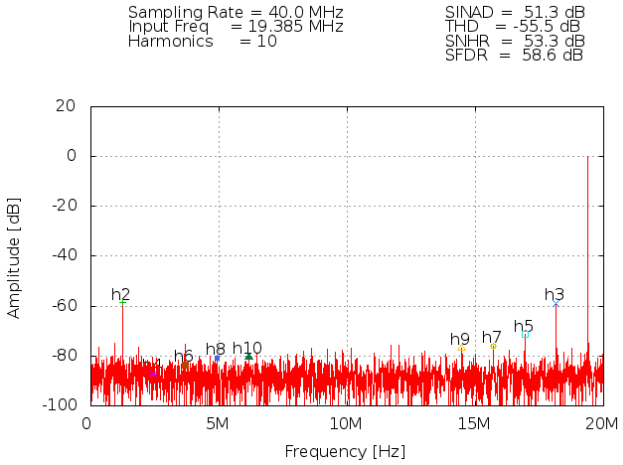


- SINAD decreasing above 45 MHz
- It is suspected that measured ENOB was limited by the setup

Preliminary measurements
10-bit SAR ADC - Dynamic measurements – f_{in} scan



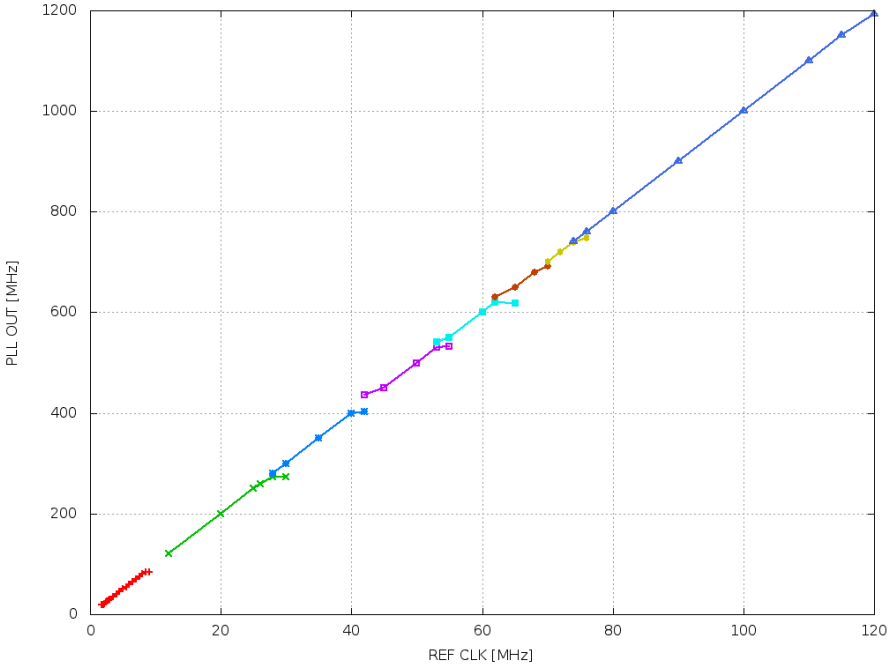




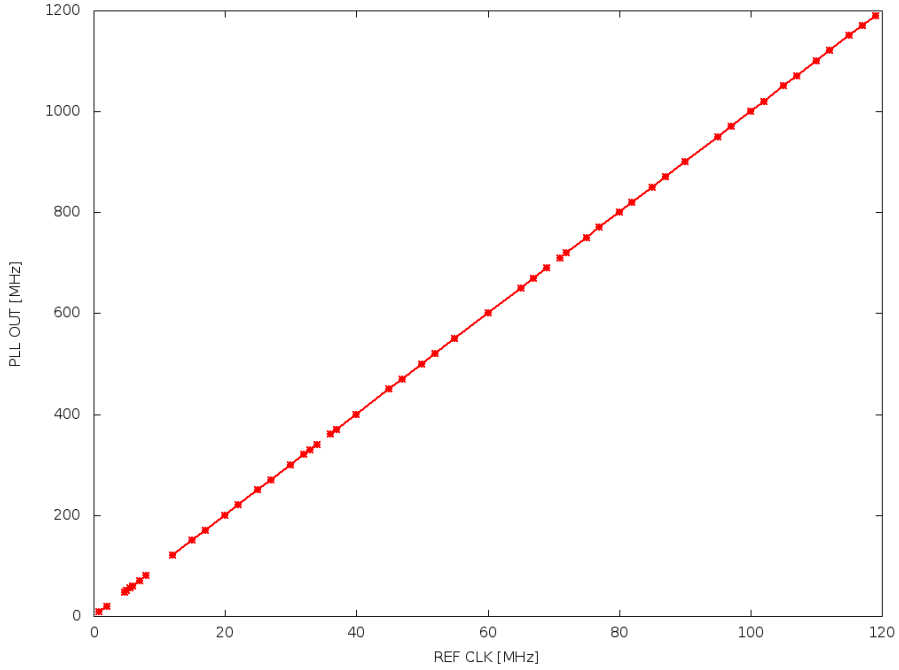
- For low f_{in} ENOB of >= 9.2 was measured
- It is suspected that ENOB decrease with f_{in} is partially/mainly due to setup

Preliminary measurements
PLL – Transfer function (CLK out vs CLK ref)

Manual mode setting

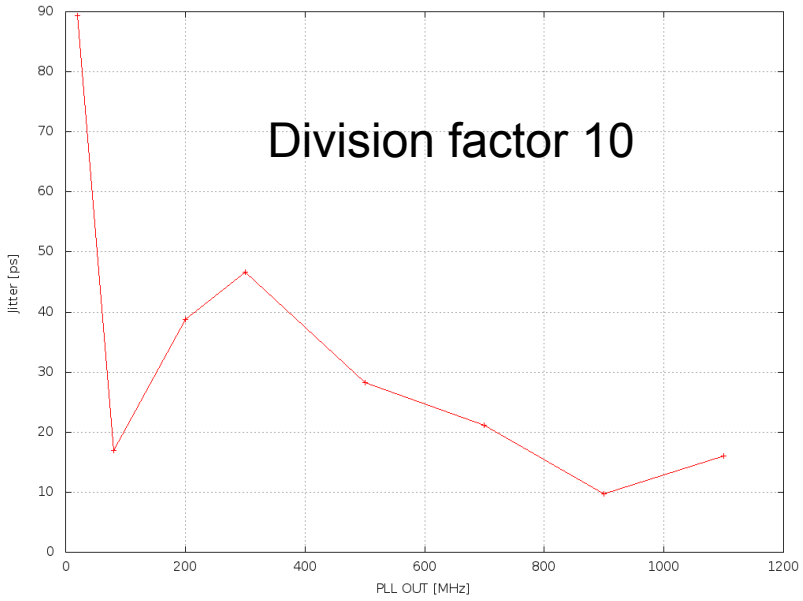


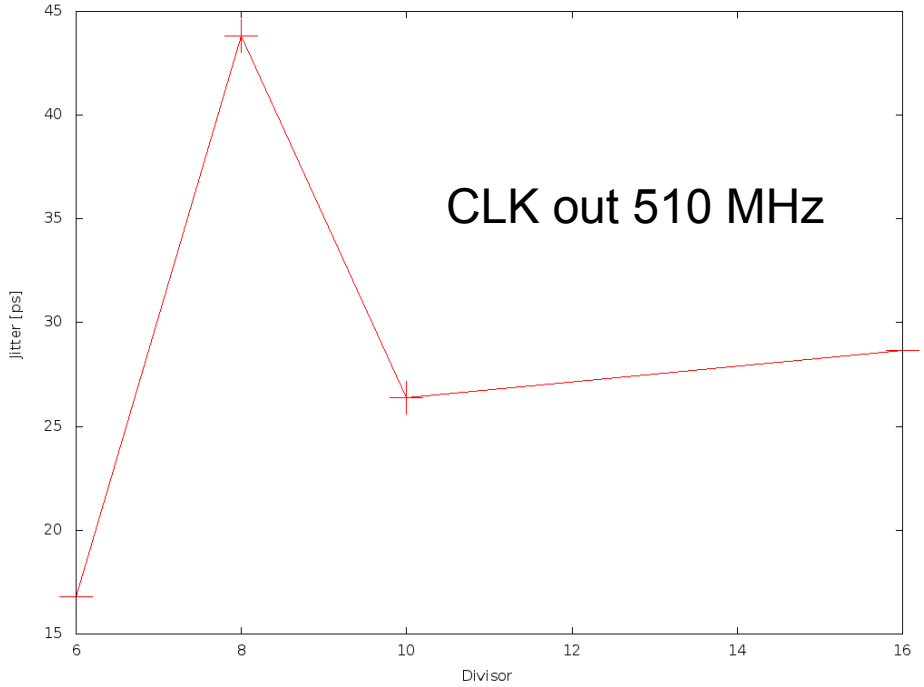
Automatic mode setting



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

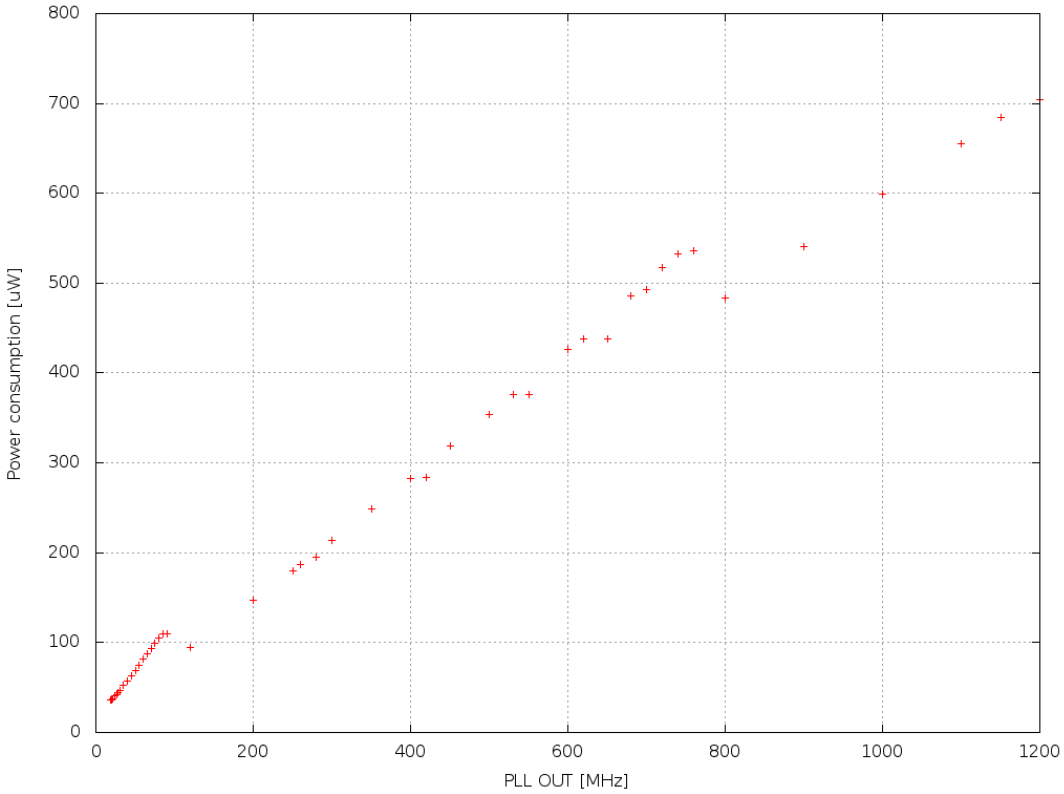
Preliminary measurements
PLL - Jitter





- Measured jitter at least few times higher than simulated (to be verified...)

Preliminary measurements
PLL - Power consumption



• Power consumption seems to be higher than simulated (to be verified...) but anyway very low