Power pulsing scheme based on a back-end current source for the analog electronics of the vertex detectors at CLIC

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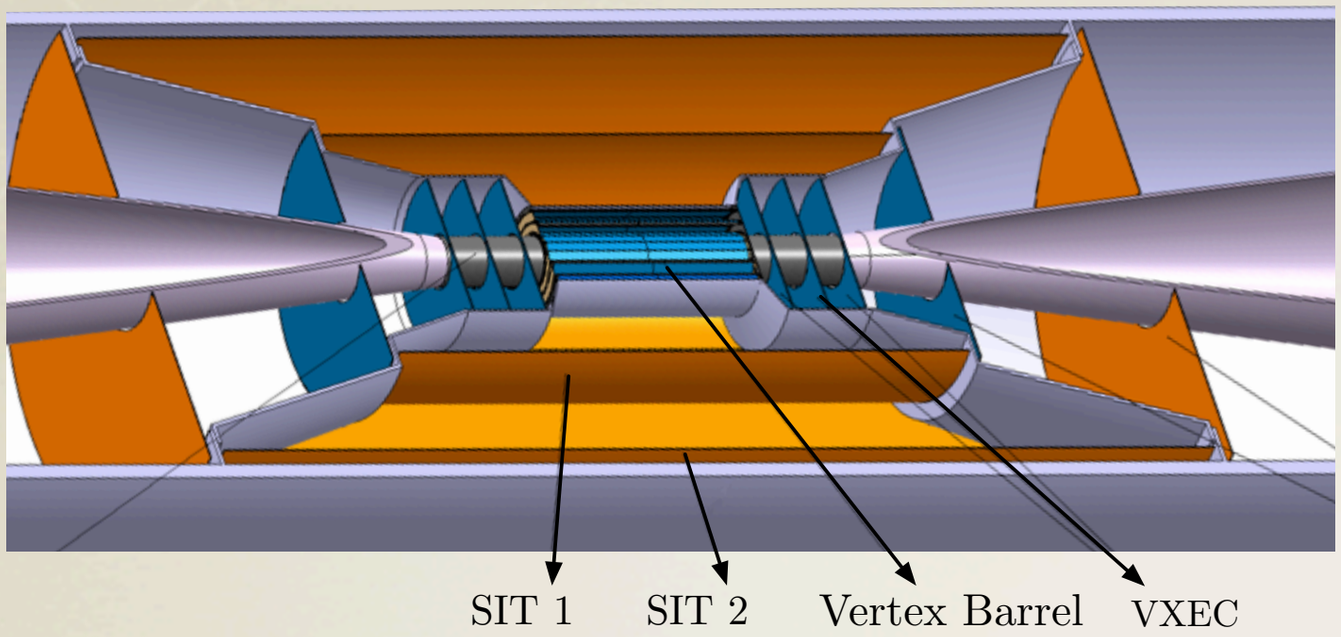
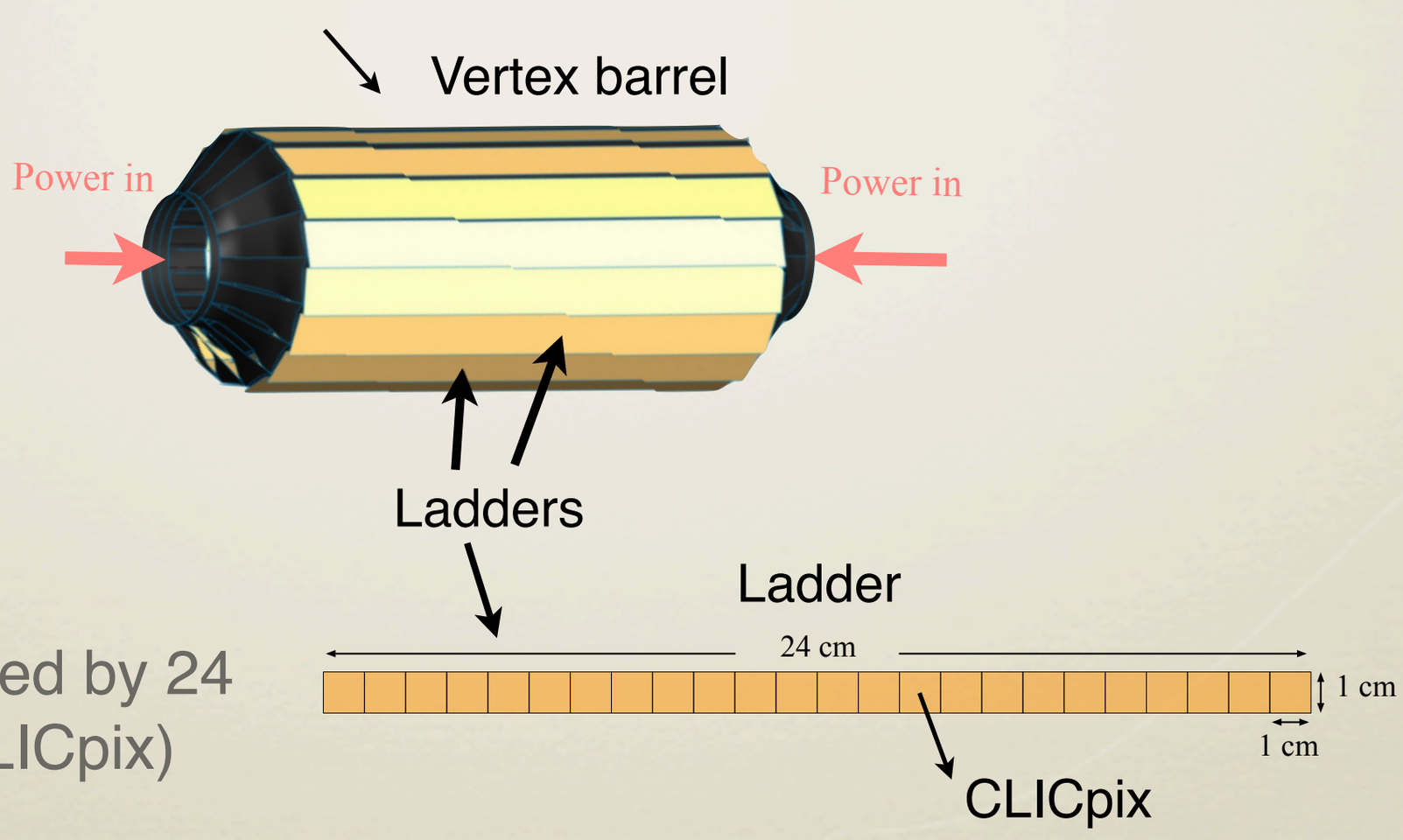
Vertex barrel, ladder and CLICpix

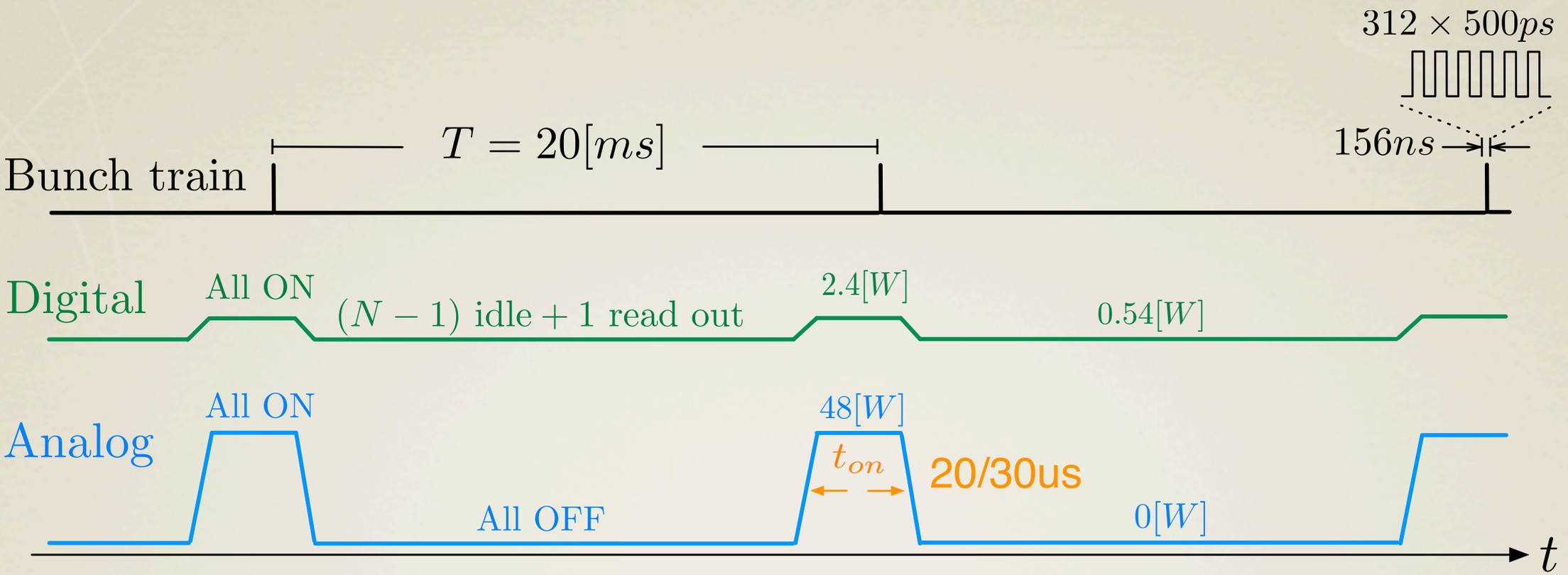
CLIC_ILD inner tracking region





The ladder is formed by 24 readout ASICs (CLICpix)

Power consumption of a Ladder



➡ Analog and digital electronics have a very different power consumption.

➡ The analog electronics could be completely turned off after the acquisition.
While the digital electronics need to be powered during the whole period.

➡ Analog voltage is 1.2V while the digital is expected to be 1V.

For these reasons they will be powered separately. In that way the analog and digital powering schemes could be optimized independently, in order to achieve the requirements (next slide).

This presentation shows results on the Analog power scheme. The digital is currently being studied.

Restrictions

1) Low losses: < 50 mW/cm^2 in the sensor area, as the heat-removal solution is based on air-cooling to reduce mass. (must be shared among analog and digital electronics)

2) Material Budget: < 0.2%X_0 for a detection layer, leaving less than 0.1%X_0 for cooling and services. (must be shared among analog and digital electronics)

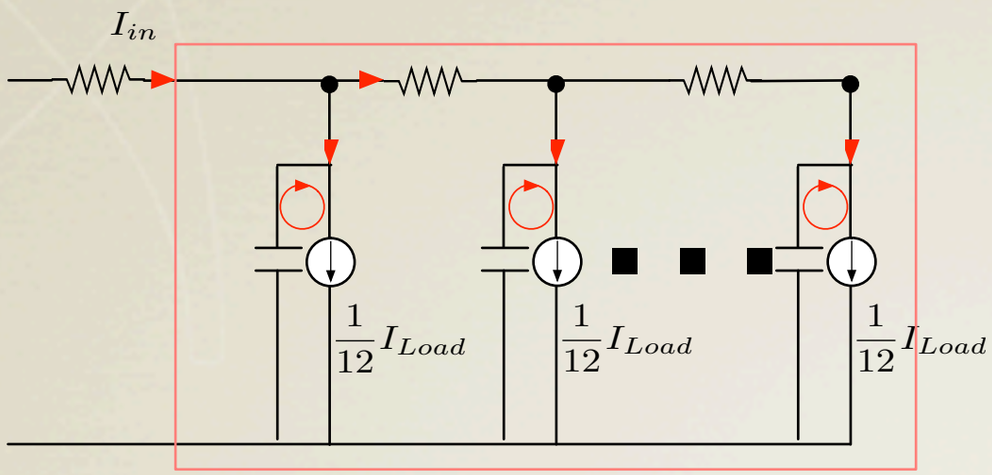
3) High magnetic Field: 4 to 5 [Tesla] restricting the use of ferromagnetic material.

extra challenge for analog electronics

4) Regulation: within 5% (60 mV) on the ASIC during the acquisition time, expected to be close to 20-30 μs (CLICPIX specifications).

Powering half a ladder (analog)

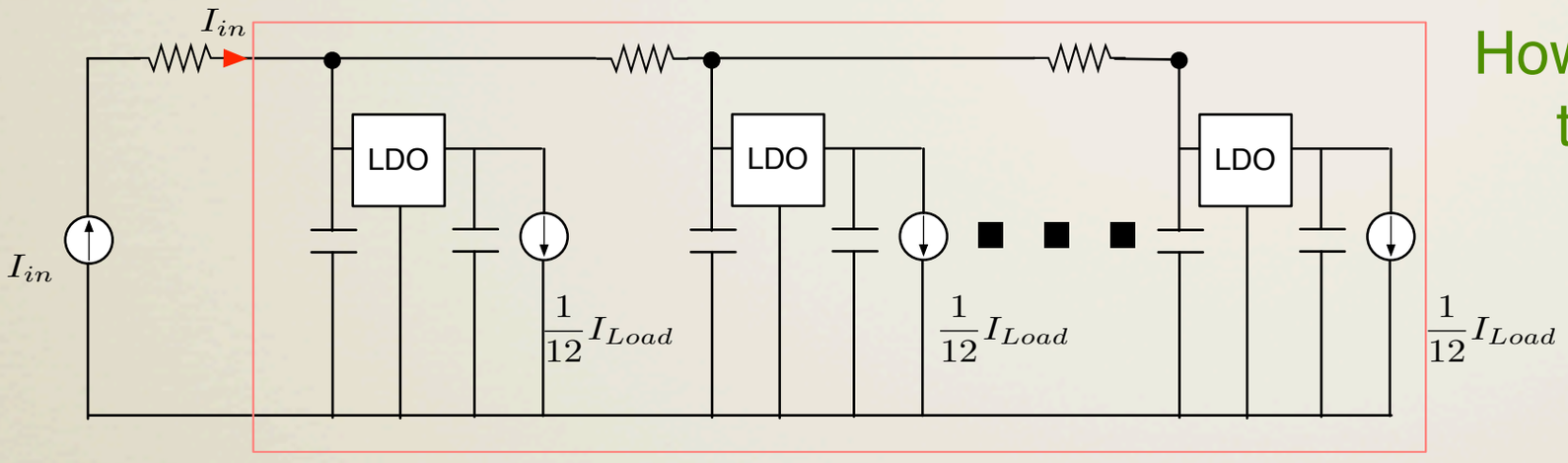
Small capacitors close to each ASIC at the FE: (10 μF)



✔ The current loop is very small.

✖ But there's need of regulation, as the capacitor discharges when the load is active.

Low dropout (LDO) voltage regulators added per ASIC:



The capacitor still discharges..
How do we charge it back to its level to be ready for the next cycle?

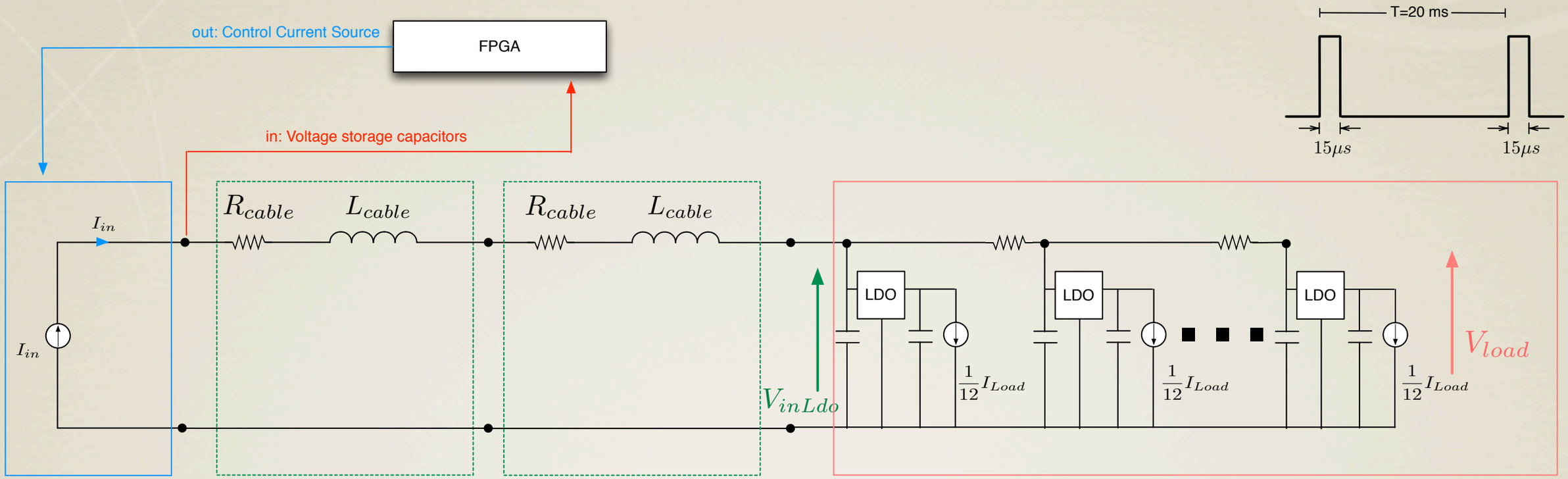
The best way is using a constant current source at the back-end.

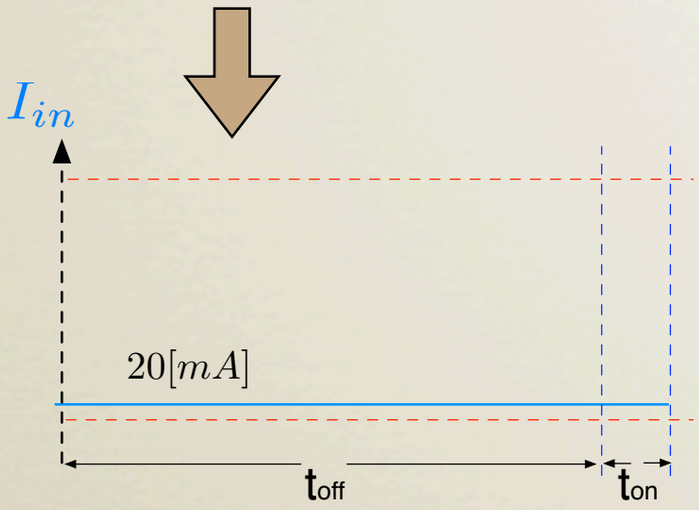
An estimation of the current at the BE, using the whole period to charge the capacitor, is:

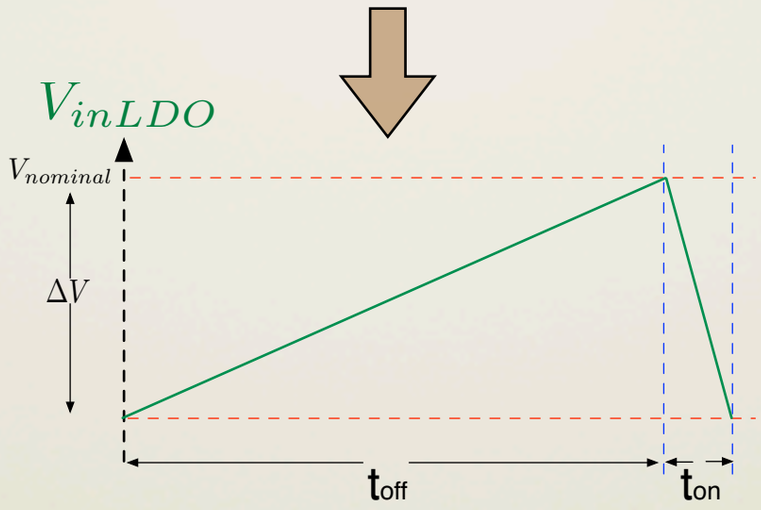
$$I_{in} = I_{load}\frac{t_{on}}{T} \approx I_{load}\frac{20\mu s}{20ms} \approx \frac{I_{load}}{1000} \approx 20mA$$

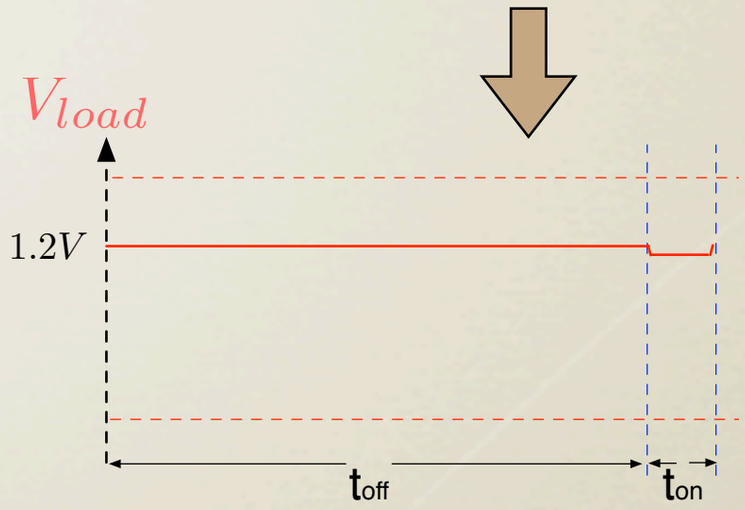
✔ The cables from the back-end to the capacitors @ FE can be really light in terms of mass.

Principle and waveforms of the scheme









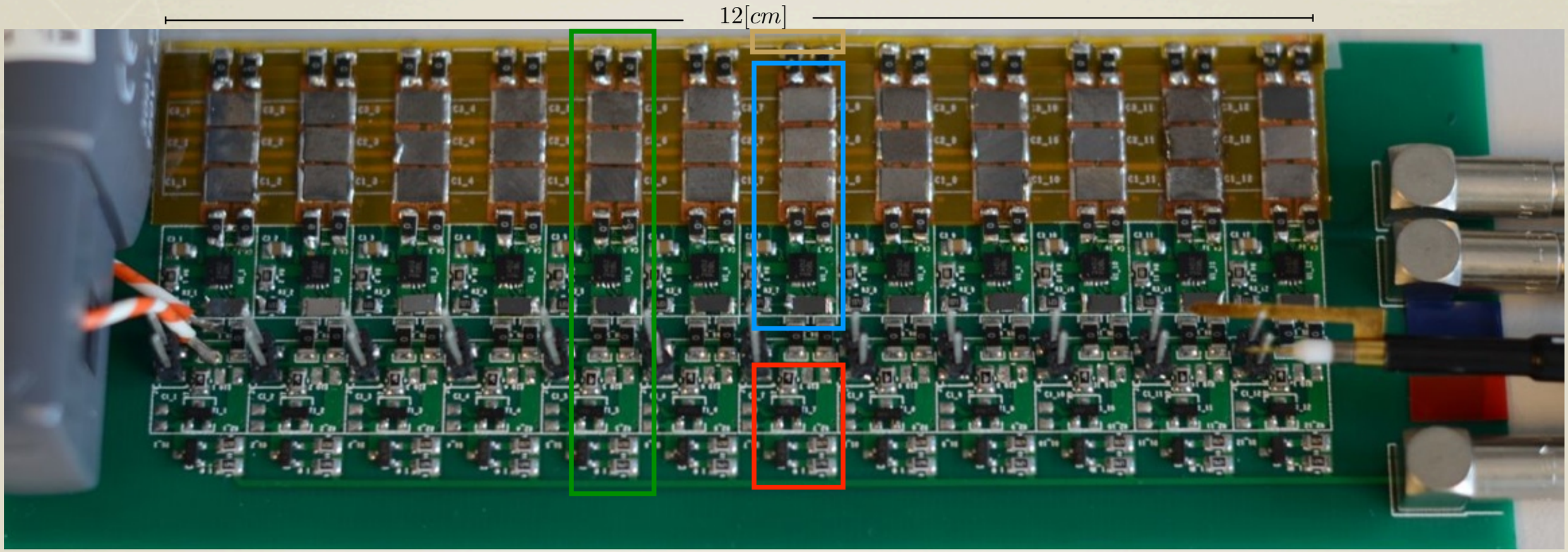
In order to work, the following condition has to be fulfilled:

$$V_{inLDO}(t) > V_{load} + V dropout$$

$$V_{nominal} - \Delta V > V_{load} + V dropout$$

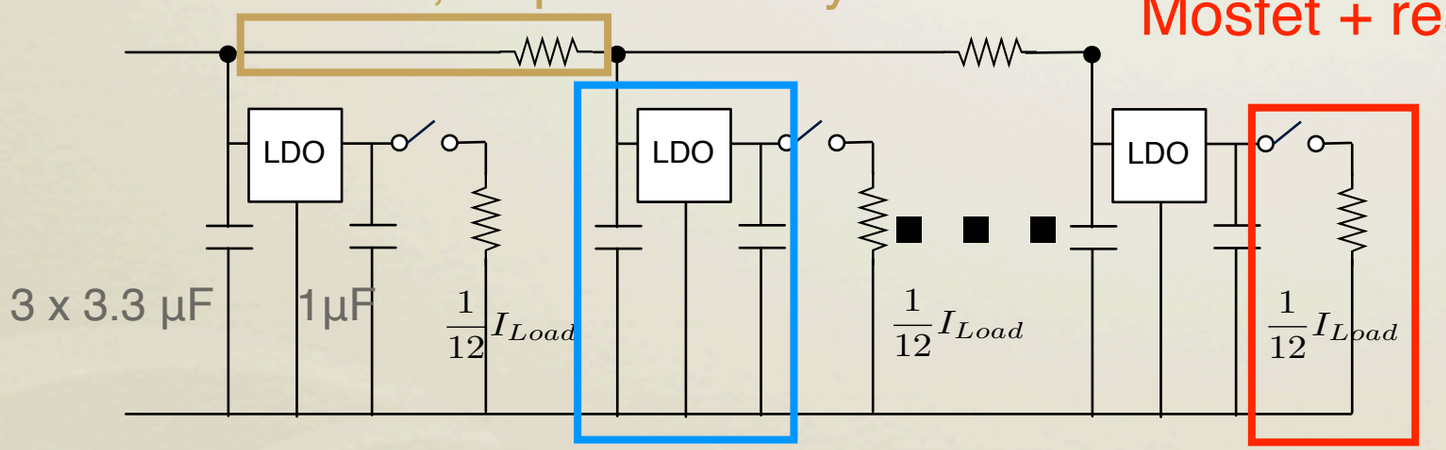
Analog Dummy Load / test board

The CLICpix is being developed, so in order to test the scheme we need a dummy load.



Two layers Aluminium Flex Cable
1mm wide, 20µm thick/layer

Dummy load:
Mosfet + resistor



This duplicates 12 times,
representing the 12 ASICs,
the power storage,
regulation and cabling.

Power storage and regulation:
input Si cap (3 x 3.3 µF) + LDO (out: 1.2V) + output Si cap (1µF)

Why aluminium cables?

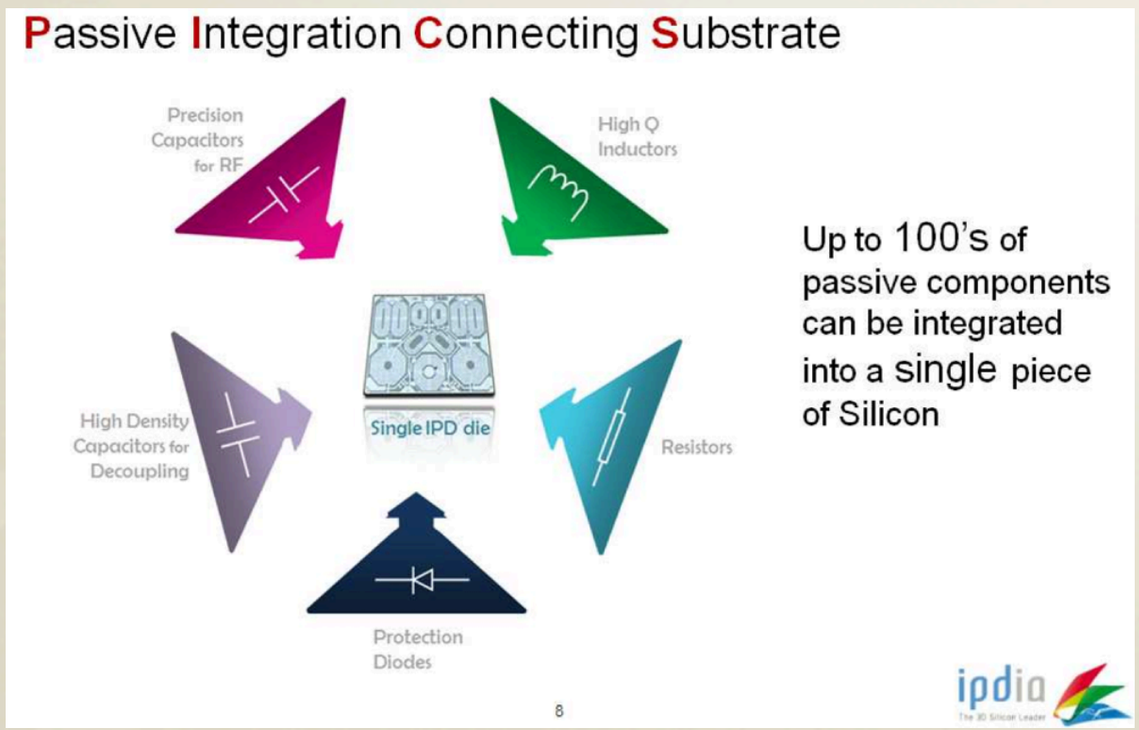
For the same resistance than a copper cable, aluminium cables have around 4 times lower material contribution. The aluminium flex cables were made at the CERN PCB shop.

Why silicon capacitors?

Low mass and flat. They can have a thickness down to 80 µm.

Ceramic capacitor of small smd package (0402 or 0201) can have comparable material. Nevertheless, their capacitance change dramatically (more than 80% of their value for some conditions) with the voltage applied (V_{bias}), making them impractical for our application.

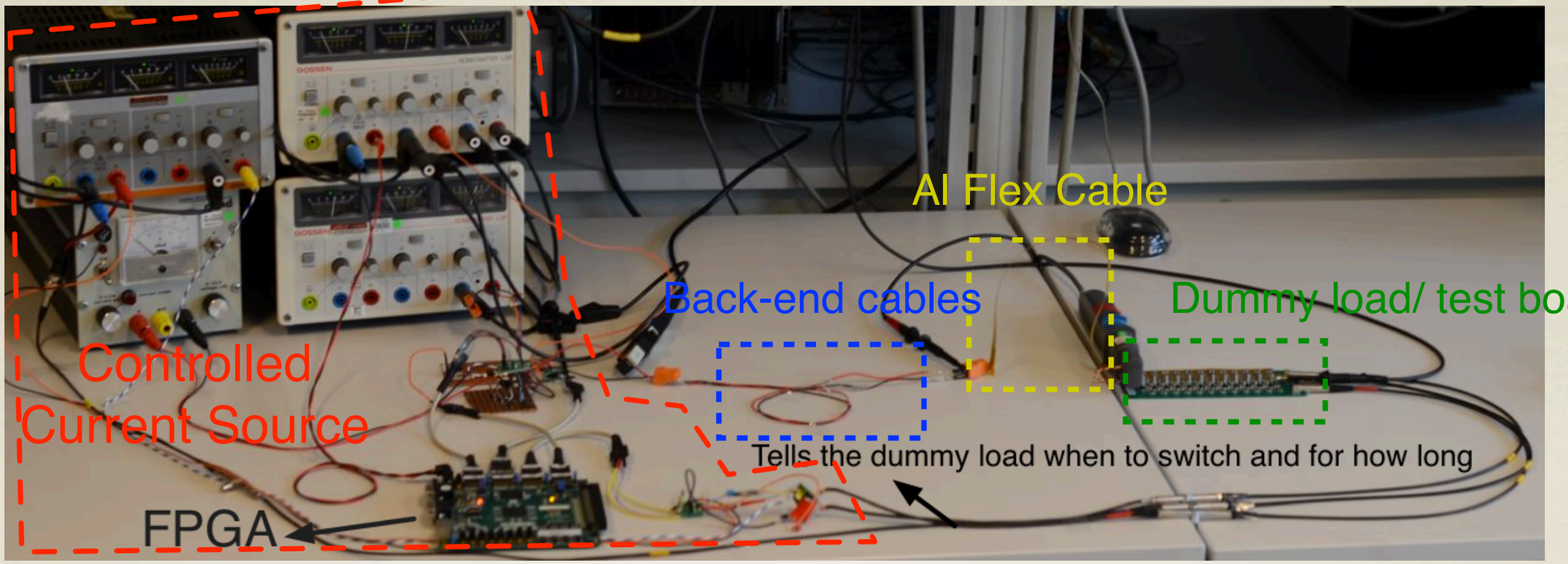
IPDiA company can integrate all the necessary passive components into a single die

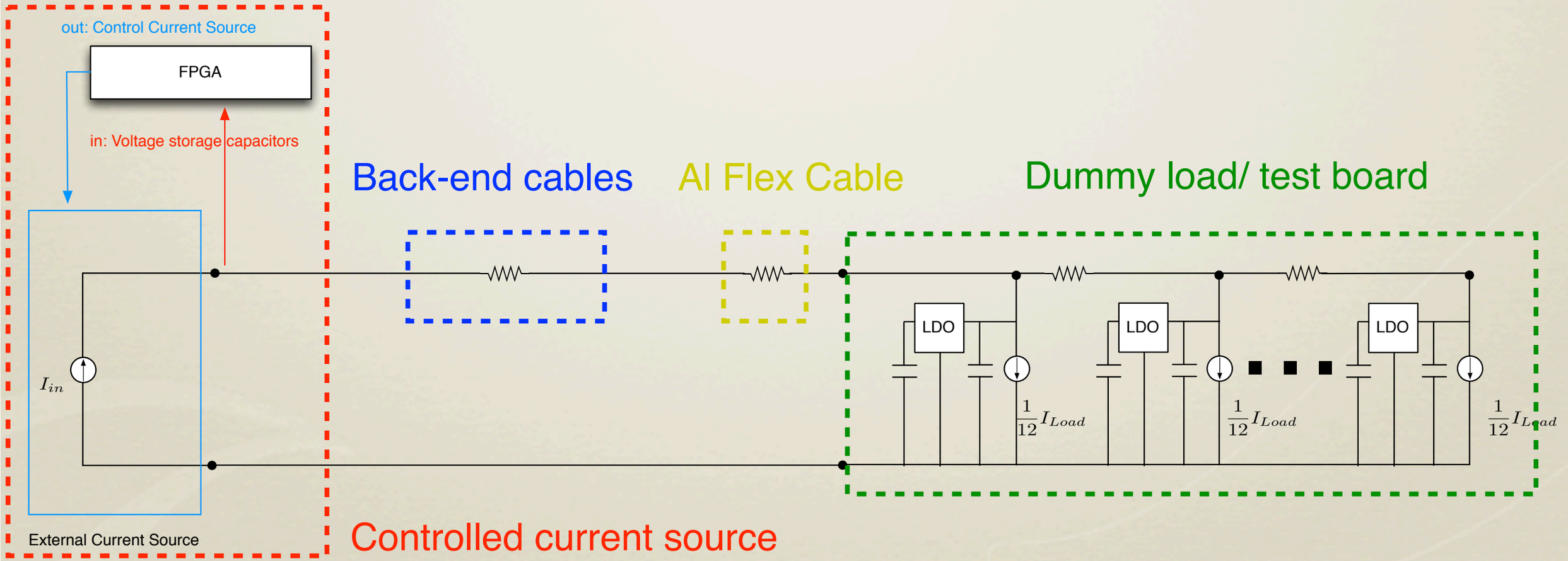


Which can be afterwards connected to the CLICpix chip using TSVs (Through Silicon Vias).

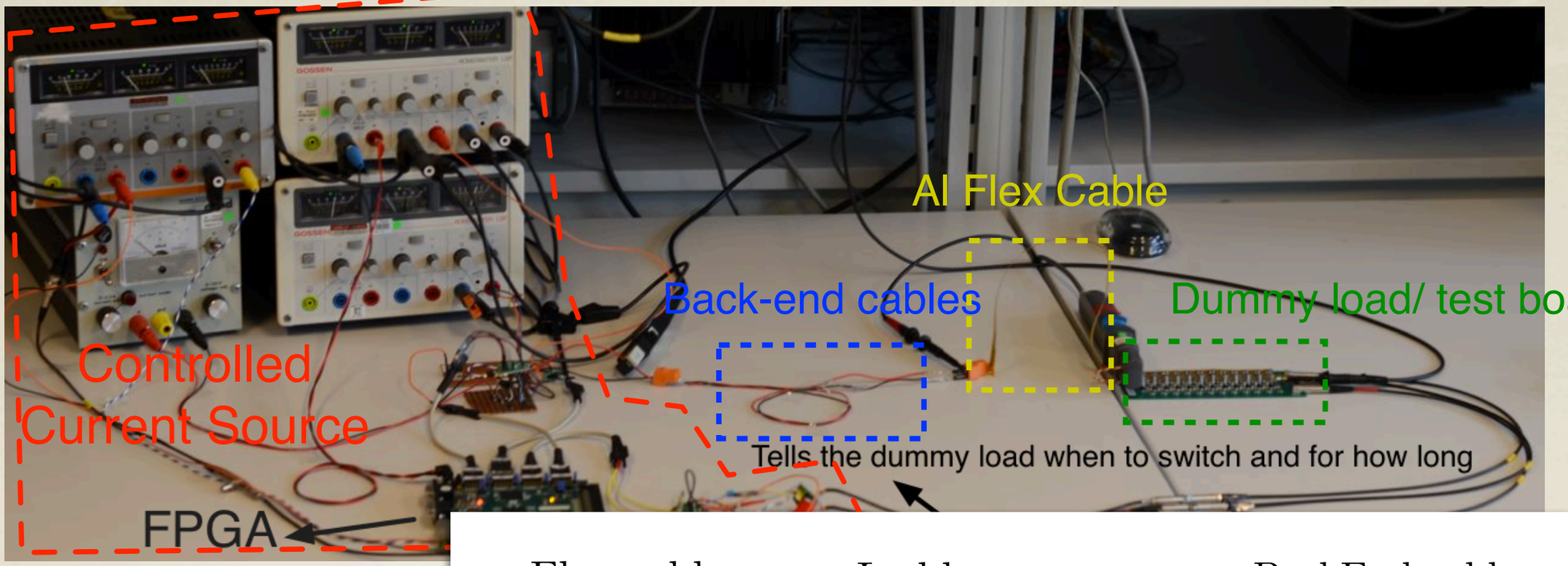
This is just a preliminary idea, and might be explored in the following months.

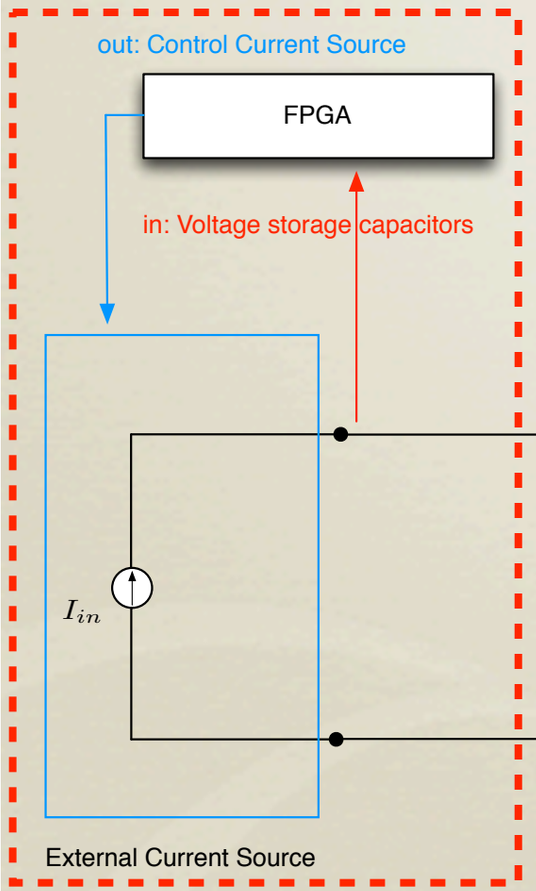
Implementation @ Lab





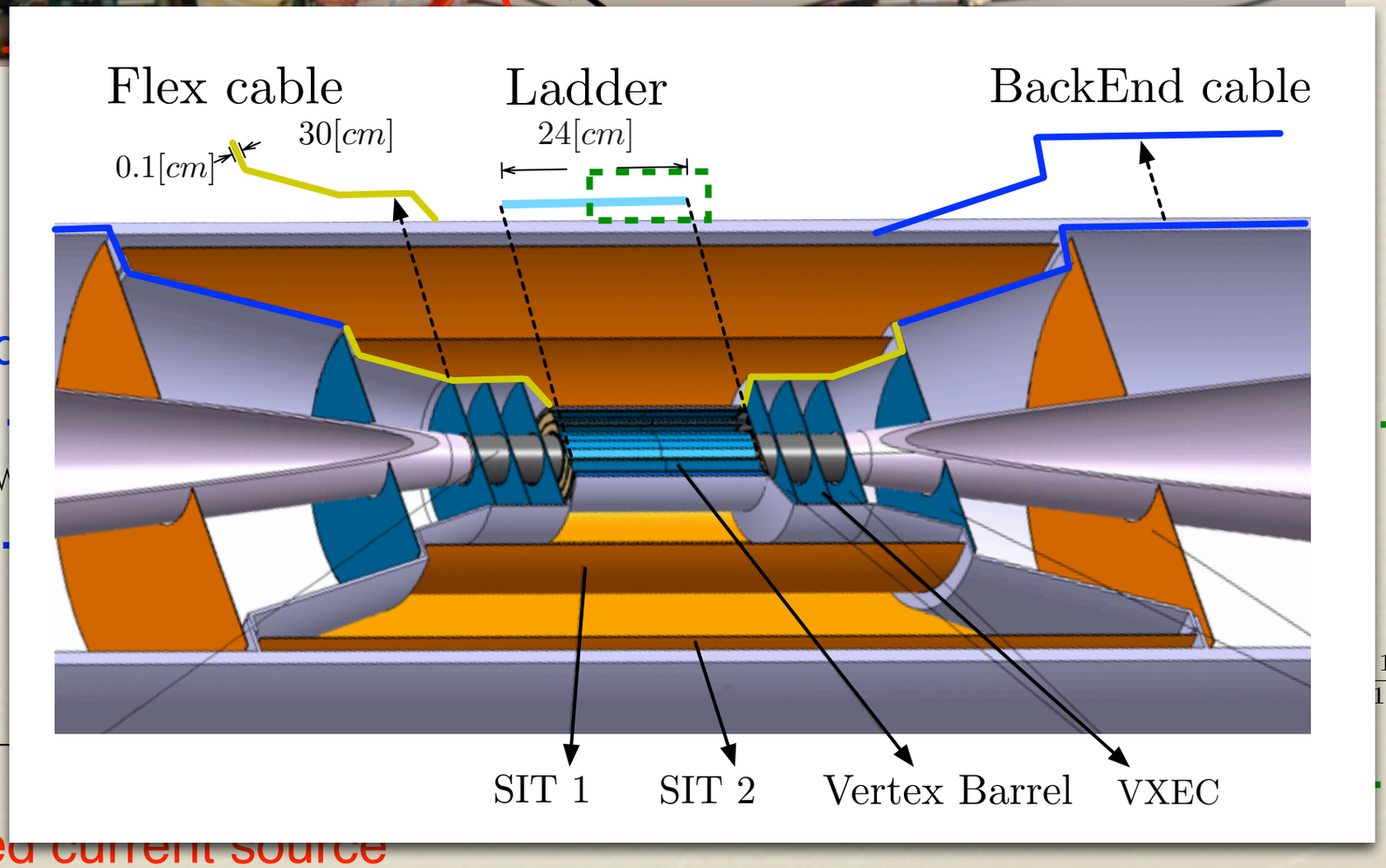
Implementation @ Lab





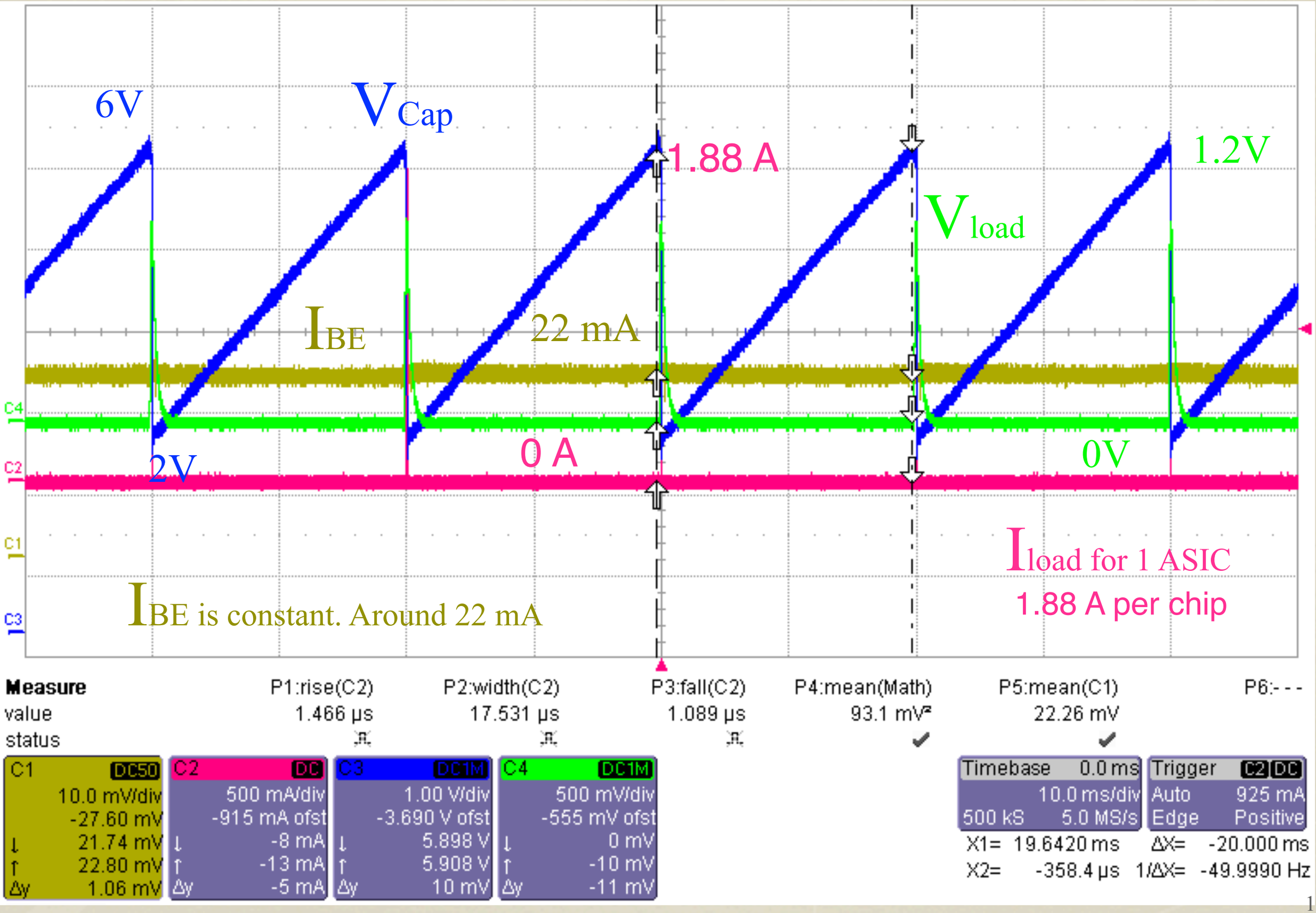
Back-enc

Controlled current source

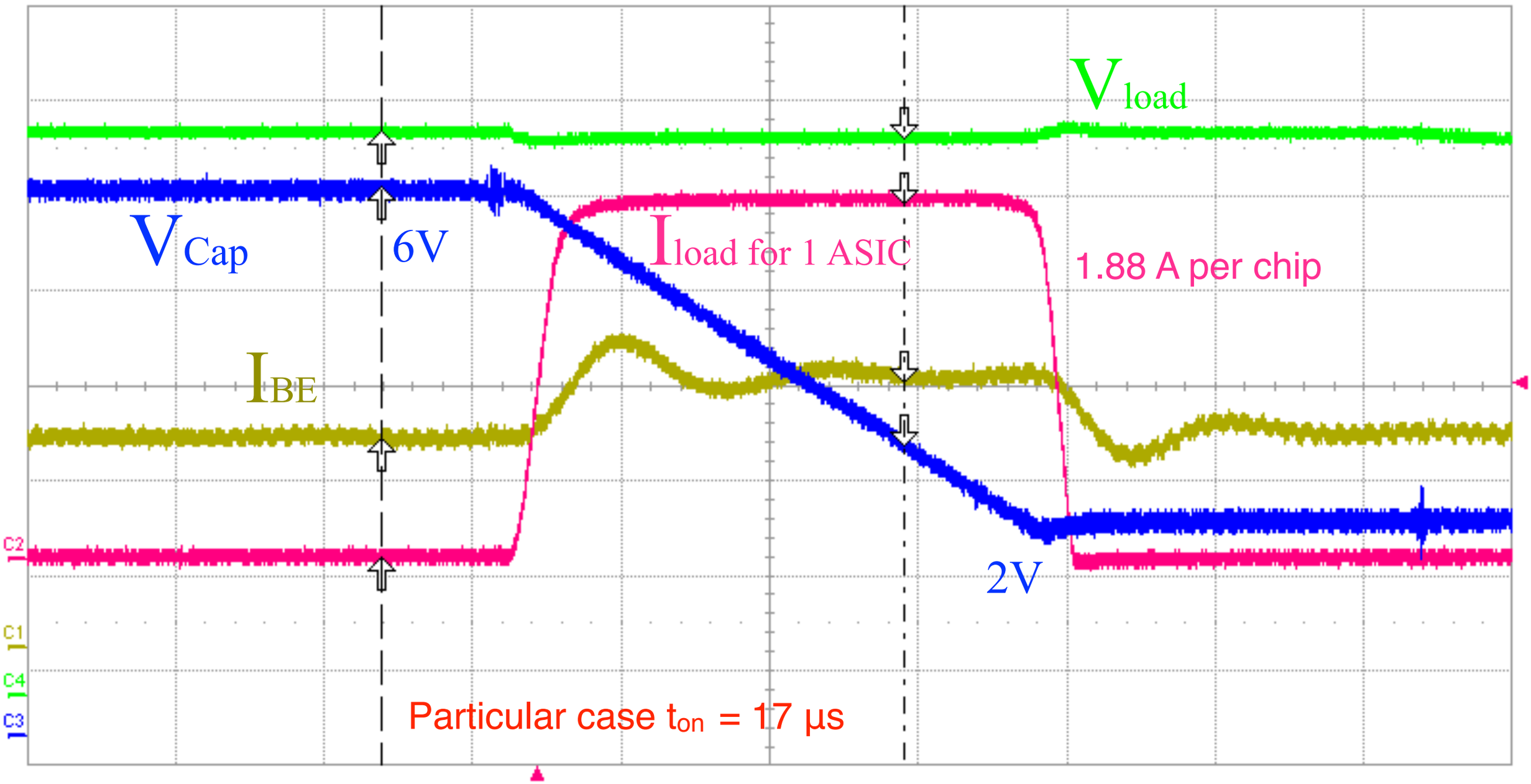


$\frac{1}{12} I_{Load}$

Measurements for the same load value



Regulation during t_{on} < 50 mV



Measure	P1:rise(C2)	P2:width(C2)	P3:fall(C2)	P4:mean(Math)	P5:mean(C1)	P6:- - -
value	1.345226 µs	17.420000 µs	918.890 ns	97.7 mV²	24.61 mV	
status	✔	✔	✔	✔	✔	

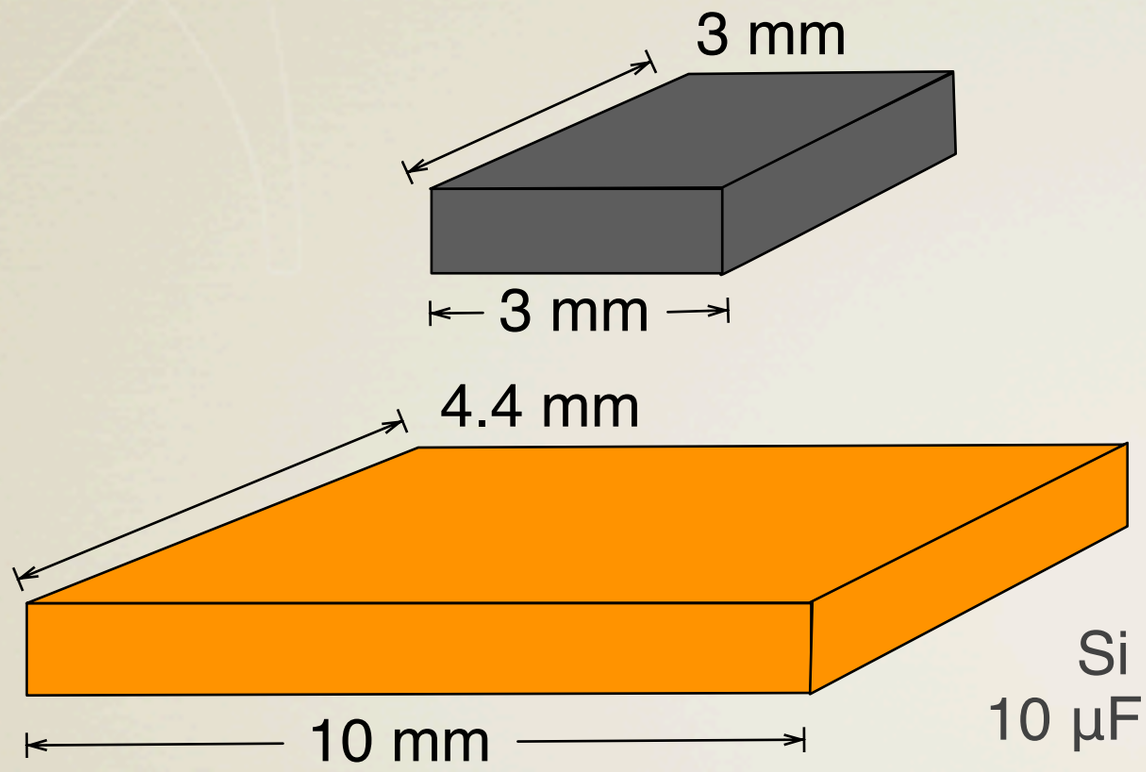
C1 DC50	C2 DC	C3 DC1M	C4 DC1M
10.0 mV/div	500 mA/div	1.00 V/div	200 mV/div
-27.60 mV	-915 mA ofst	-3.690 V ofst	-652.0 mV
↓ 28.08 mV	↓ 1.879 A	↓ 3.074 V	↓ 1.1736 V
↑ 21.84 mV	↑ -1 mA	↑ 5.770 V	↑ 1.1848 V
Δy -6.24 mV	Δy -1.880 A	Δy 2.696 V	Δy 11.1 mV

✔ 11 mV voltage drop

Timebase -7.8 µs	Trigger C2 DC
5.00 µs/div	Stop 925 mA
125 kS 2.5 GS/s	Edge Positive
X1= 12.3444 µs	ΔX= -17.6136 µs
X2= -5.2692 µs	1/ΔX= -56.774 kHz

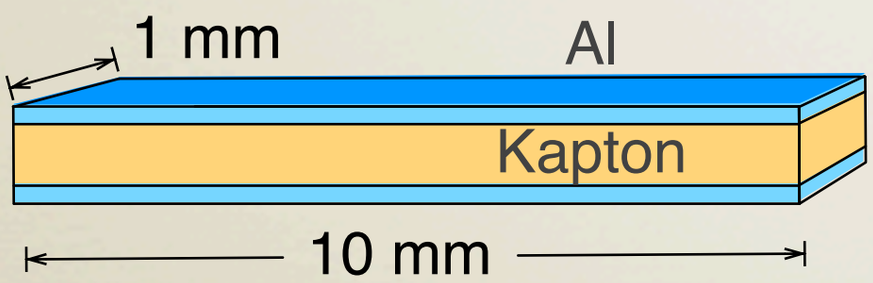
Material Budget Today

Silicon capacitors (today 25 μF/cm²):

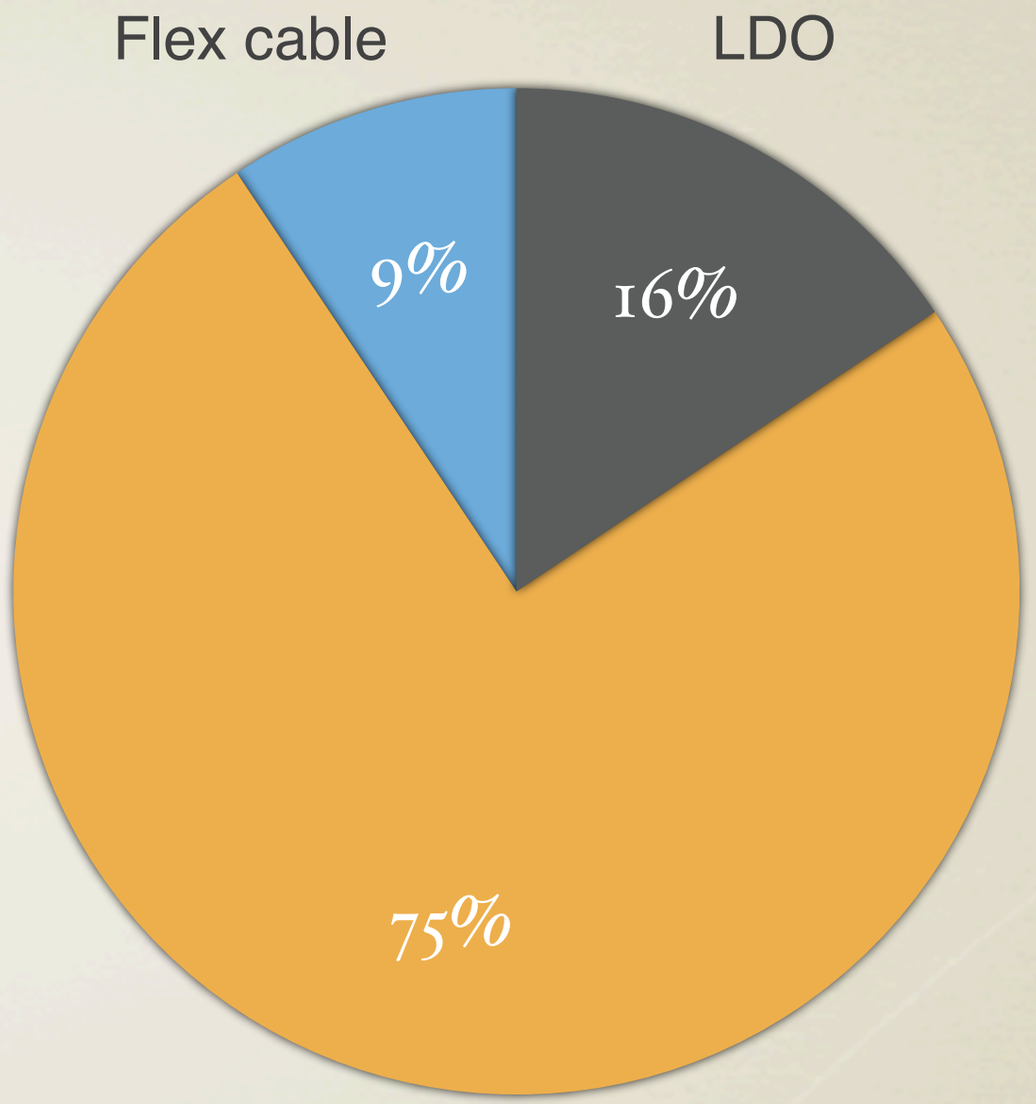


LDO

Si cap
10 μF + 1 μF



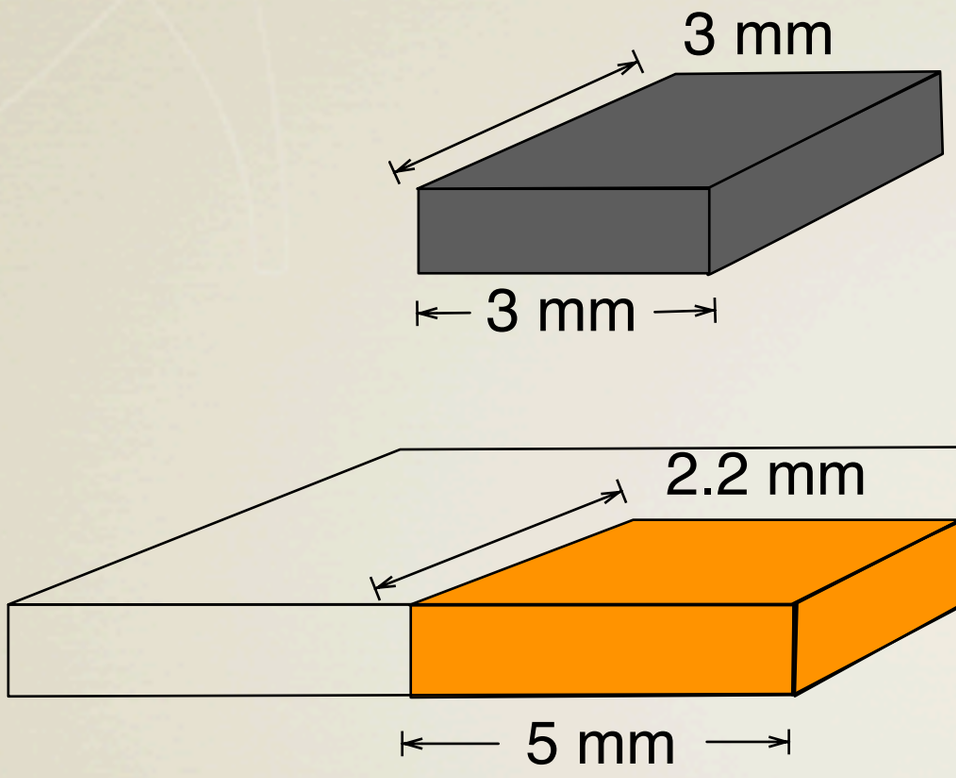
Flex cable



Contribution: 0.064 % X_0

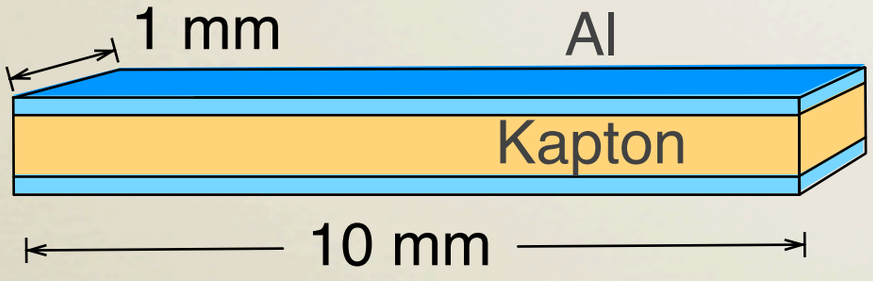
Material Budget ~~Today~~ Tomorrow

Silicon capacitors (~~today 25~~ 100 µF/cm²):

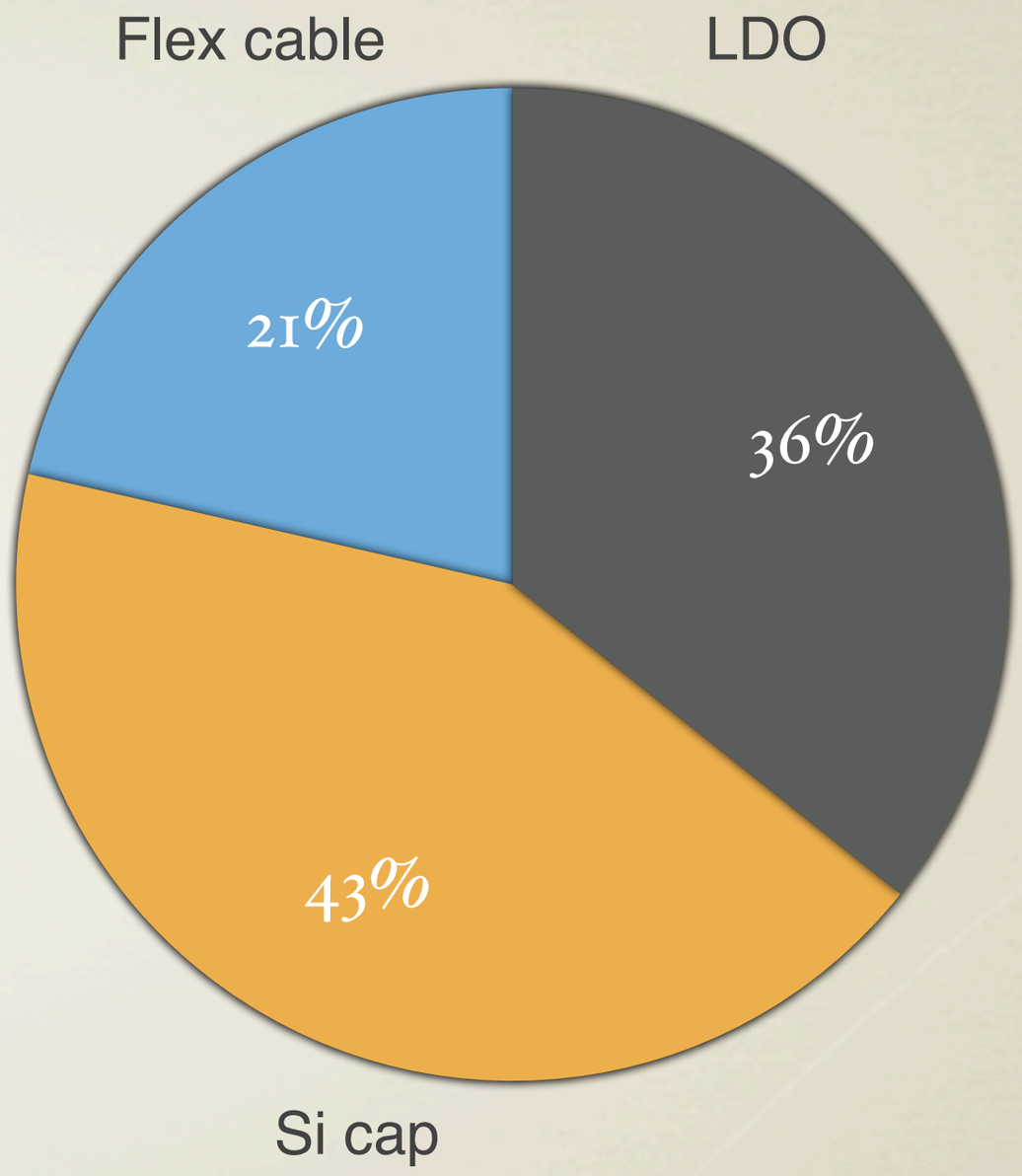


LDO

Si cap
10 µF + 1 µF



Flex cable



We are considering the possibility of integrating the LDO inside the ASIC.
Allowing a further reduction

Contribution: 0.028% X_0

Conclusions

During this talk we presented a power-pulsing scheme to power the analog electronics of the future vertex read-out ASIC CLICpix.

The scheme counted with regulation and silicon capacitors in the front-end, which were charged up using a back-end current supply of less than 100 mA.

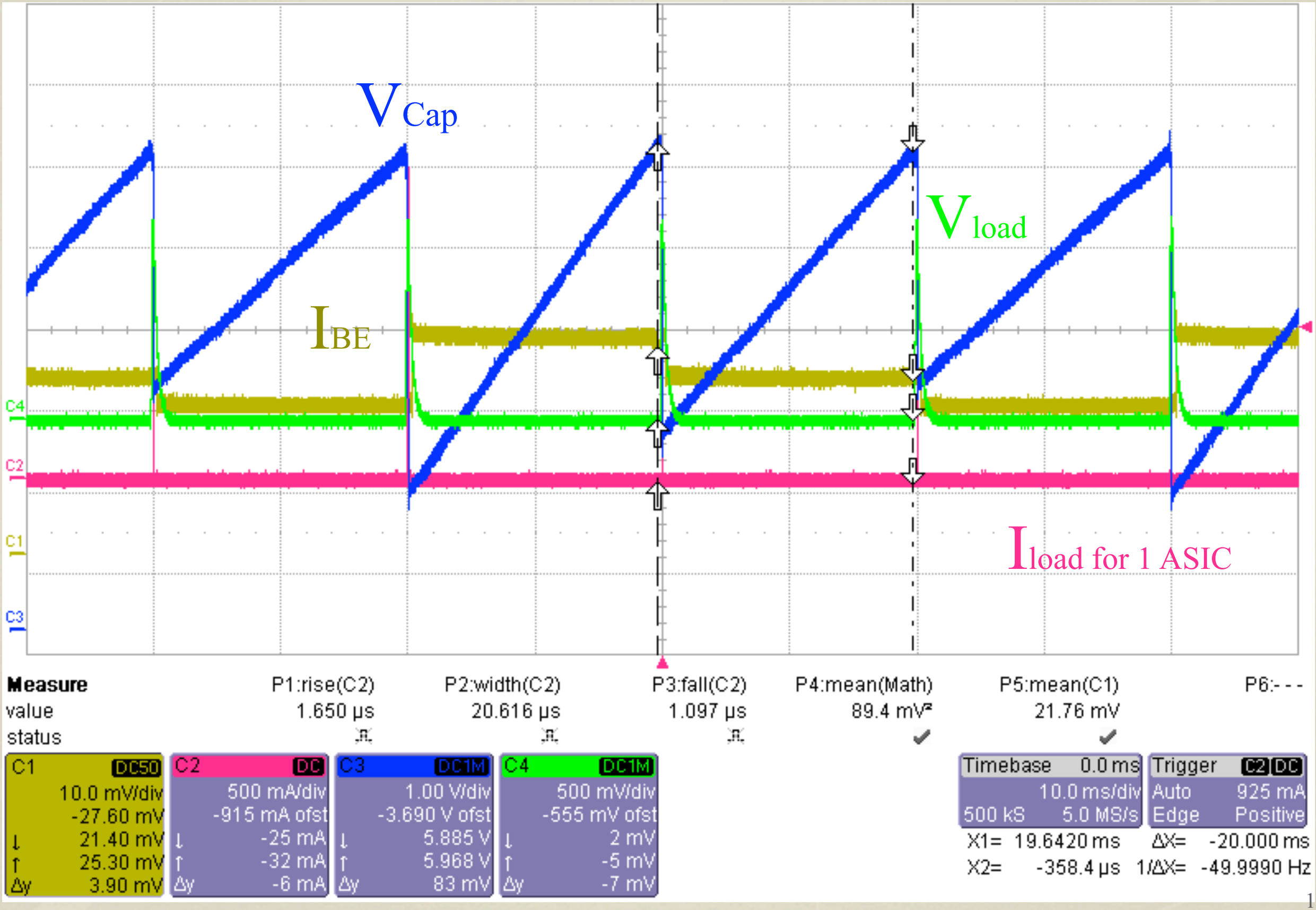
Some of the achieved results were:

- Good regulation (11 mV)
- Power losses/dissipation lower than 10mW/cm^2(leaving more than 40mW/cm^2 to the digital part)
- Small current (20mA to 60mA) through the whole cable depending on the load consumption. => Low material cables
- No DCDC needed. (Everything is in the back-end)
- Today's Material Budget 0.064 %X_o, which is expected to be less than 0.028 %X_o. (after improvements of silicon capacitors technology).

Future work: To try a similar scheme for the digital electronics and to compare it with a scheme based on DC/DC converters.

Thanks for your attention :)

Change in the load consumption



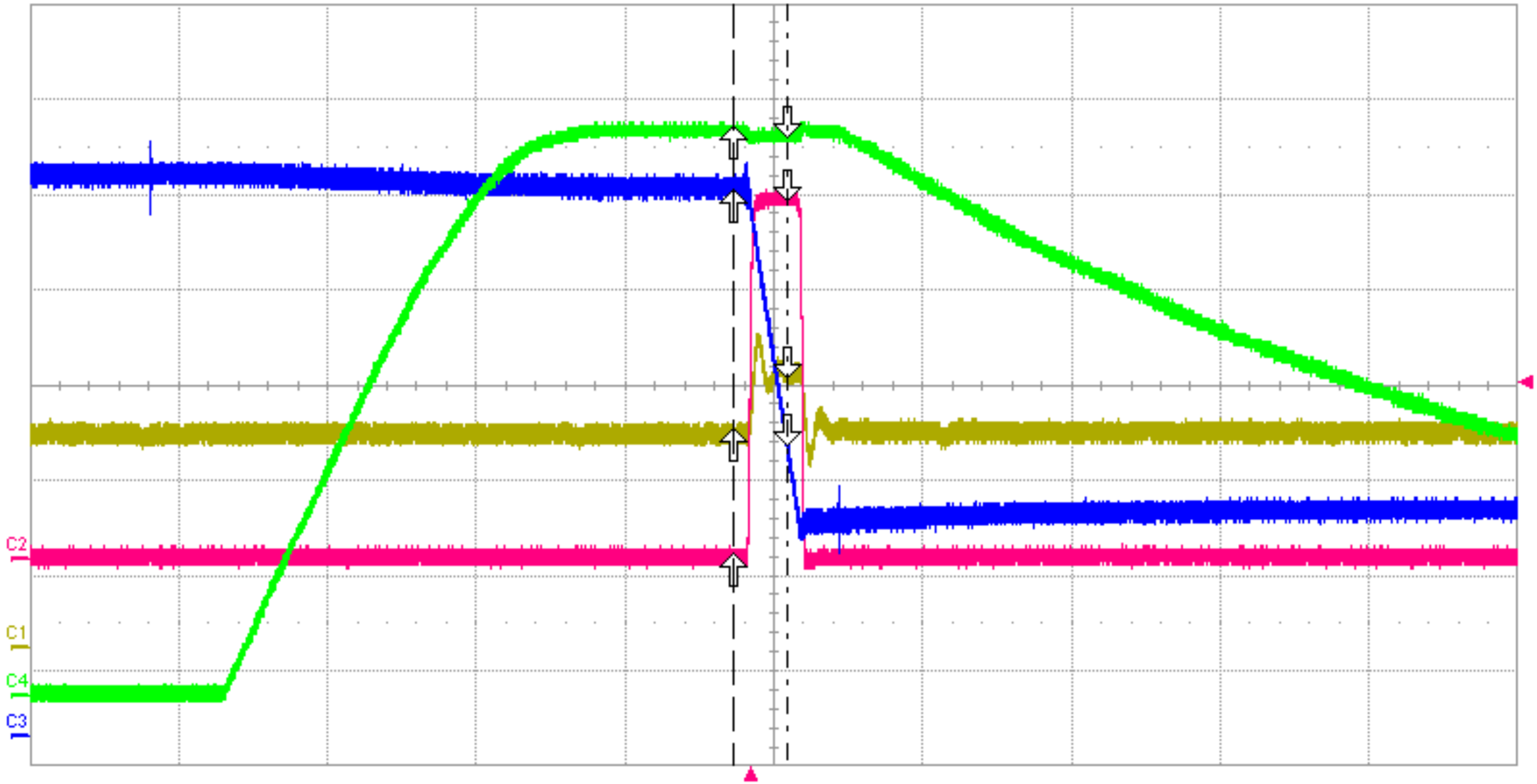
Measure	P1:rise(C2)	P2:width(C2)	P3:fall(C2)	P4:mean(Math)	P5:mean(C1)	P6:- - -
value	1.650 µs	20.616 µs	1.097 µs	89.4 mV	21.76 mV	
status				✓	✓	

C1 DC50	C2 DC	C3 DC1M	C4 DC1M
10.0 mV/div	500 mA/div	1.00 V/div	500 mV/div
-27.60 mV	-915 mA ofst	-3.690 V ofst	-555 mV ofst
↓ 21.40 mV	↓ -25 mA	↓ 5.885 V	↓ 2 mV
↑ 25.30 mV	↑ -32 mA	↑ 5.968 V	↑ -5 mV
Δy 3.90 mV	Δy -6 mA	Δy 83 mV	Δy -7 mV

Timebase 0.0 ms	Trigger C2 DC
10.0 ms/div	Auto 925 mA
500 kS 5.0 MS/s	Edge Positive

X1= 19.6420 ms ΔX= -20.000 ms
X2= -358.4 µs 1/ΔX= -49.9990 Hz

Backup: En/Dis voltage regulator



Measure	P1:rise(C2)	P2:width(C2)	P3:fall(C2)	P4:mean(Math)	P5:mean(C1)	P6:- - -
value	1.38831 µs	17.52466 µs	940.41 ns	92.9 mV²	22.79 mV	
status	✔	✔	✔	✔	✔	

C1 DC50	C2 DC	C3 DC1M	C4 DC1M
10.0 mV/div	500 mA/div	1.00 V/div	200 mV/div
-27.60 mV	-915 mA ofst	-3.690 V ofst	-652.0 mV
↓ 28.56 mV	↓ 1.887 A	↓ 3.082 V	↓ 1.1754 V
↑ 22.80 mV	↑ 19 mA	↑ 5.720 V	↑ 1.1896 V
Δy -5.76 mV	Δy -1.868 A	Δy 2.638 V	Δy 14.2 mV

Timebase -8 µs	Trigger C2 DC
50.0 µs/div	Stop 925 mA
500 kS 1.0 GS/s	Edge Positive

X1= 12.344 µs ΔX= -17.613 µs
X2= -5.269 µs 1/ΔX= -56.776 kHz

Material Budget

Silicon capacitors (today 25 µF/cm²):

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	1	0.05	1	1.00	0.005	0.002
Flex cable layers	Aluminium	88.9	120	1	0.020	2	1.00	0.004	0.004
Input LDO Capacitors	Silicon	93.6	10	4	0.1	12	1.00	0.040	0.043
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.0641

Silicon capacitors (few years 100 µF/cm^2):

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	1	0.05	1	1.00	0.005	0.002
Flex cable layers	Aluminium	88.9	120	1	0.020	2	1.00	0.004	0.004
Input LDO Capacitors	Silicon	93.6	10	4	0.1	12	1.00	0.040	0.011
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.0320

Power losses

7 mW/cm² leaving 43 mW/cm² for the digital electronics.