Silicon-Tungsten EM calorimeter

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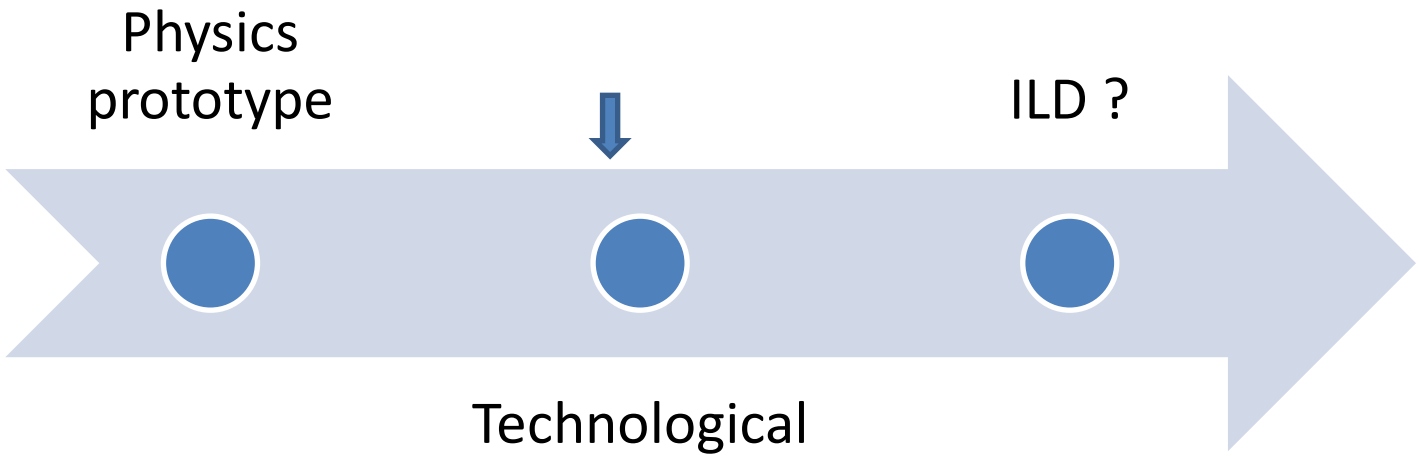
Time line



Proof of concept
- Linearity
- Resolution
- Sensors
- Very front-end

Feasibility of design options
- Compactness
- Granularity
- Front-end
- Demonstrators

Construction
- Integration
- Environement
- Services
- Industrialization
- Logistics

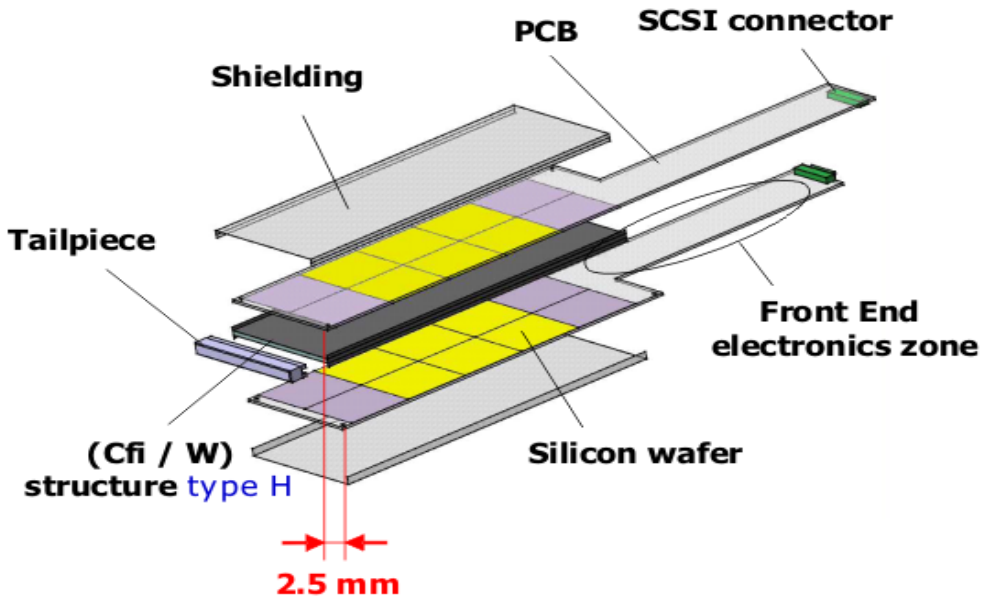
First prototype (2006) : Concept OK✓

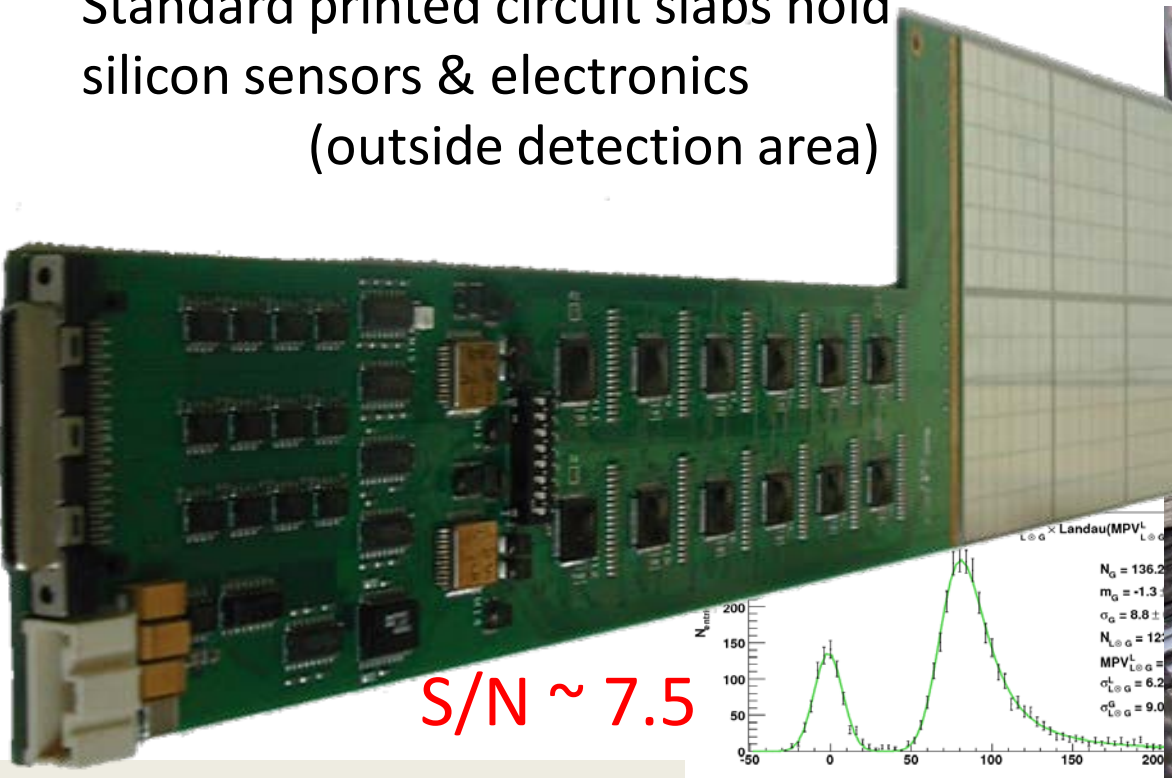
First generation prototype
and tested on beam 2006-2008

30 layers - ~4000 channels

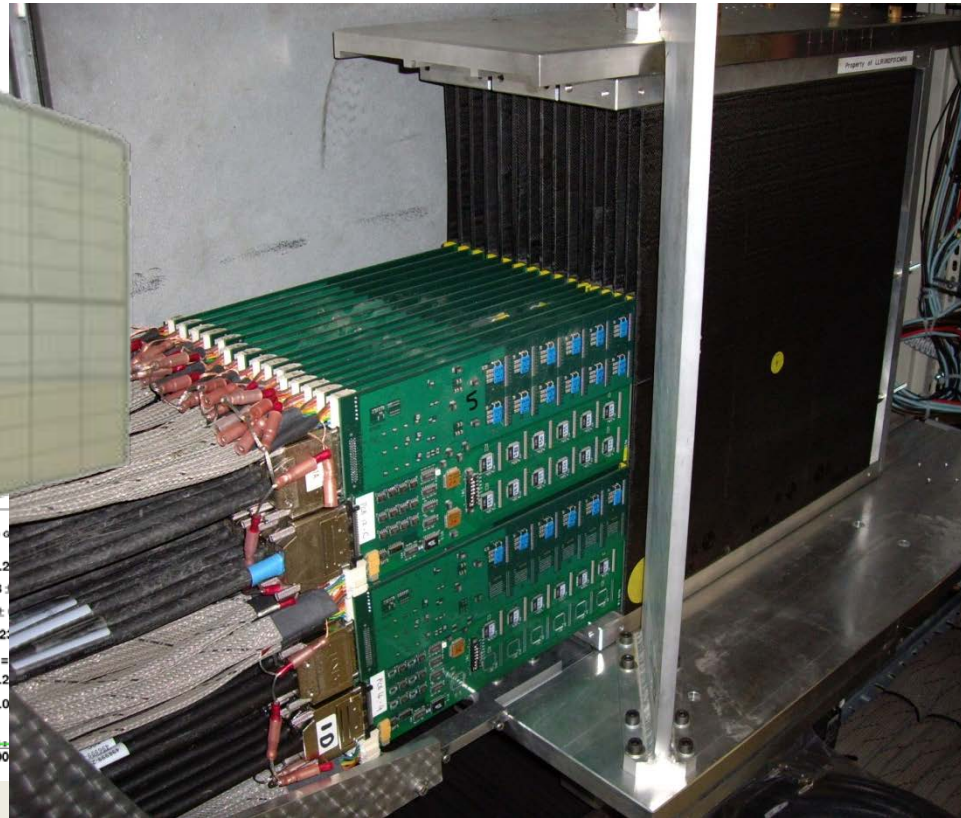
Mechanical structure: carbon fibre composite, incorporating tungsten layers

Standard printed circuit slabs hold silicon sensors & electronics
(outside detection area)





S/N ~ 7.5



ECAL for ILC

~24 X0, 20 cm thick

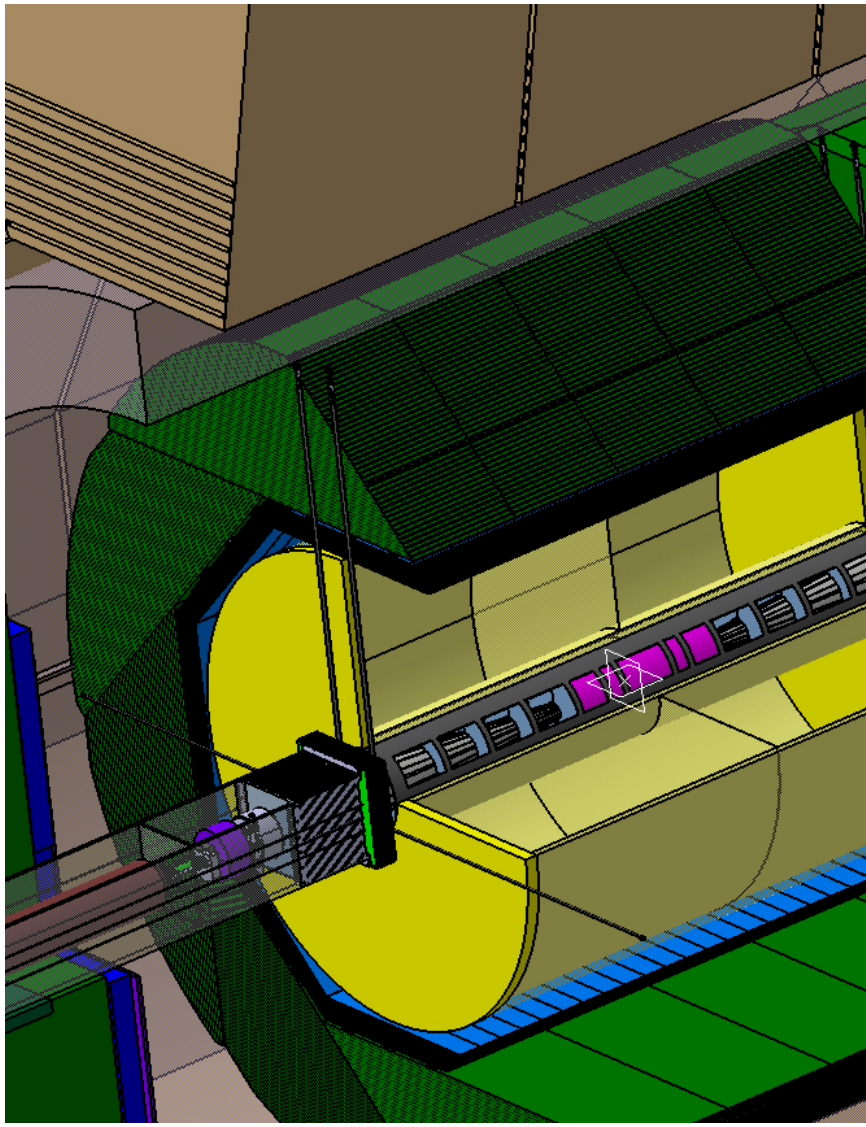
~2500 m^2 active detectors

~100M readout channels

Reduce dead material,

calorimeters inside coil,

Extreme compactness

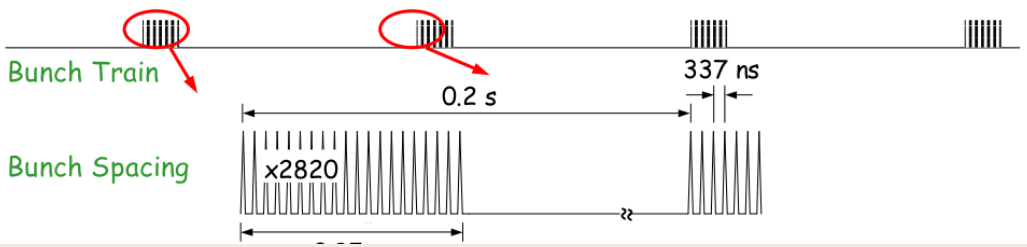


Designed for specific beam structure

ILC: 5Hz trains each of 3k bunches @ 340 ns

low occupancy, low noise : S/N >10

allow power pulsing then embedded VFE

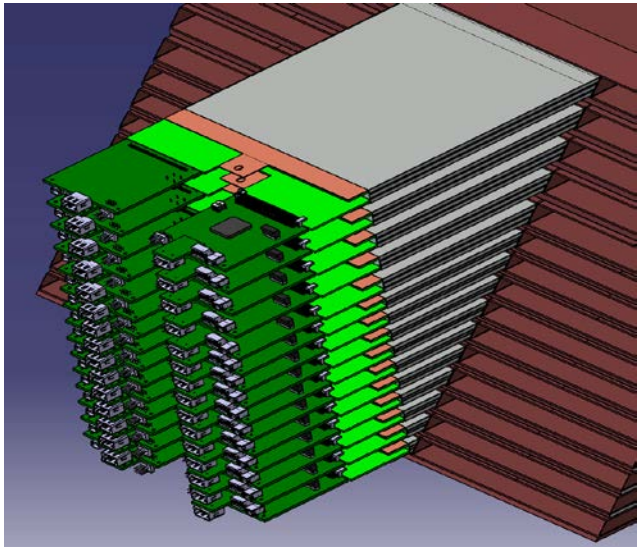


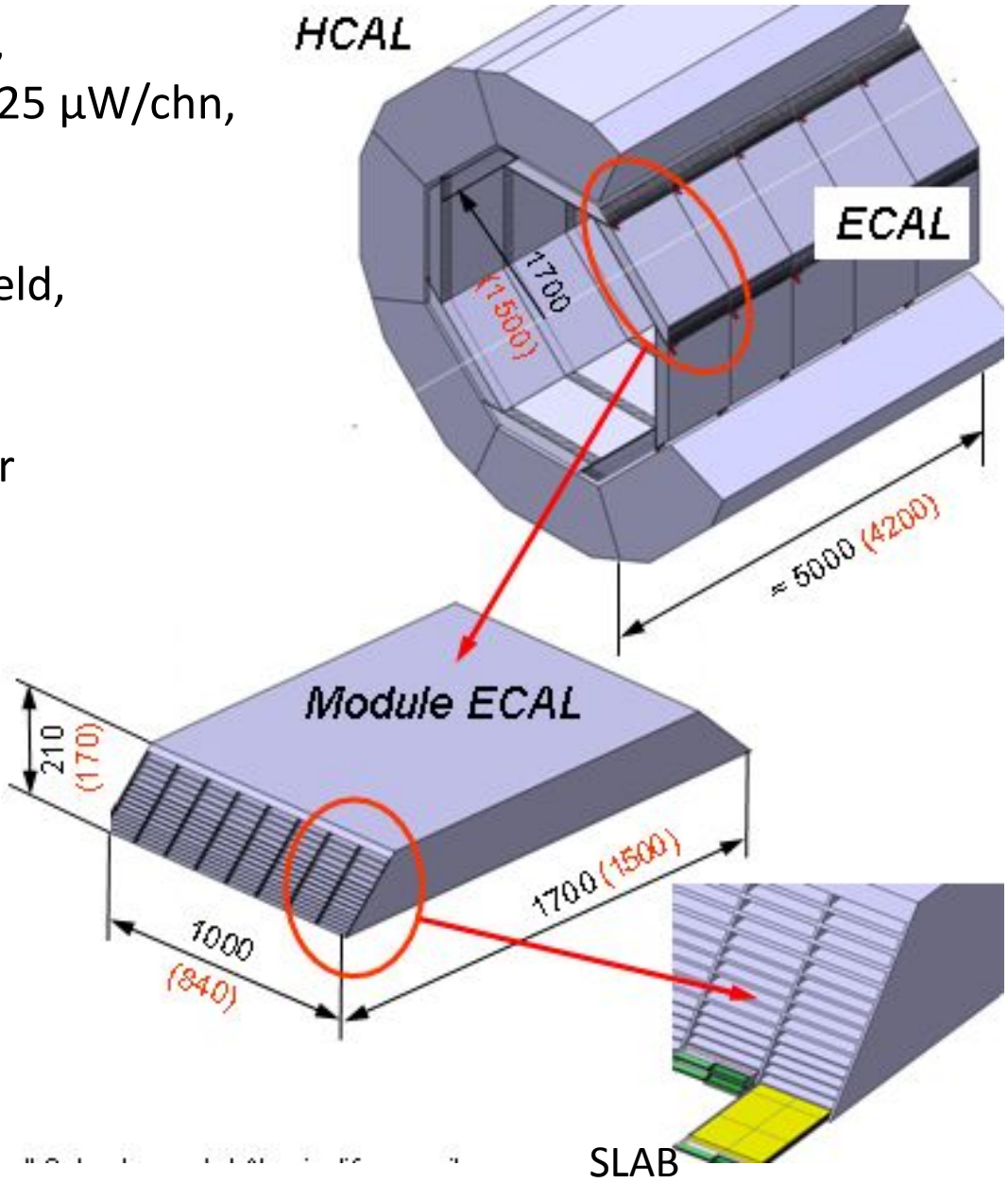
Technological prototype (2011) : Proof of feasibility

Engineering challenges :

→ embedded “system on chip” electronics,
→ extremely low power consumption typ. 25 µW/chn,
→ wide sensors (81 cm², pure silicon),
→ large composite mechanical structure,
→ readout technology insensitive to ~4T field,
→ integrated DAQ system

Goal : demonstrator of 1 instrumented tower
(40k channels, 20 cm^2 crossection, 1/300th of full detector)

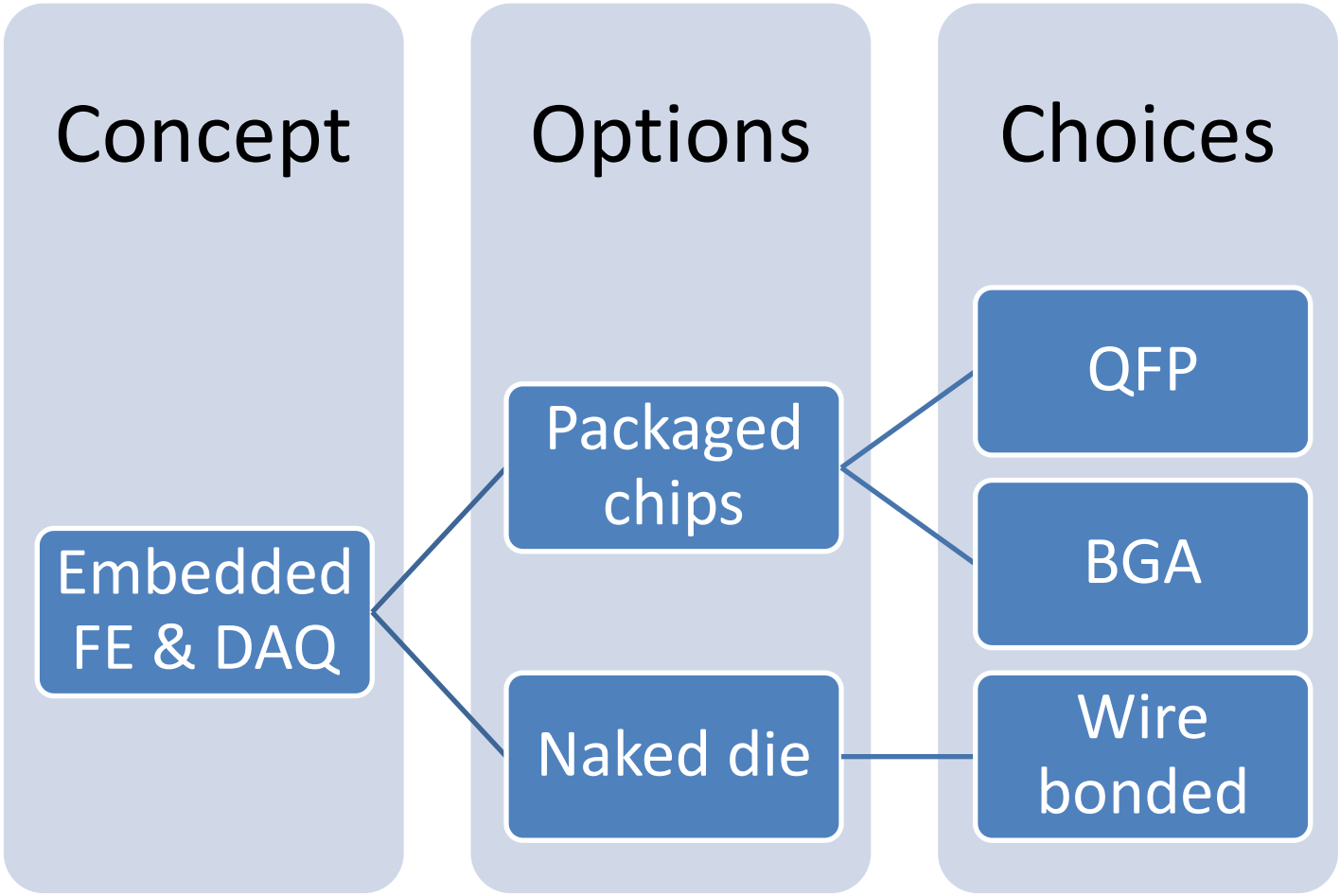




Even 1/300th is not easy to do

Prototyping phase includes several steps
Decision to explore alternative "branch" according to issues

- **Conservative option**
- **High-end Technological option**

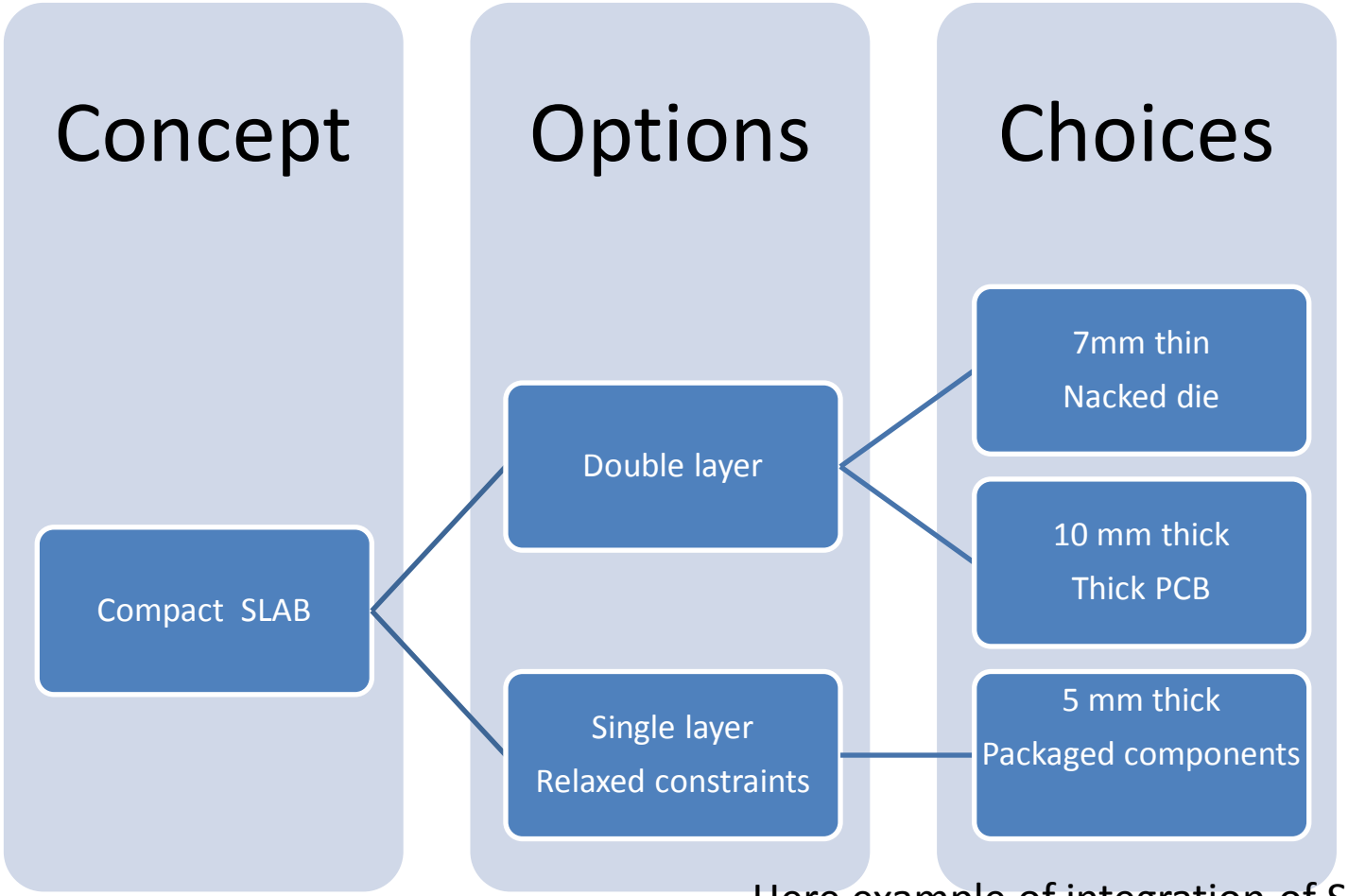


Here example of integration of microchips

Even 1/300th is not easy to do

Best option will be chosen according to

- **Actual feasibility at industrial level (mass production)**
- **Reliability & Maintenance**
- **Cost**
- **Physics performance**



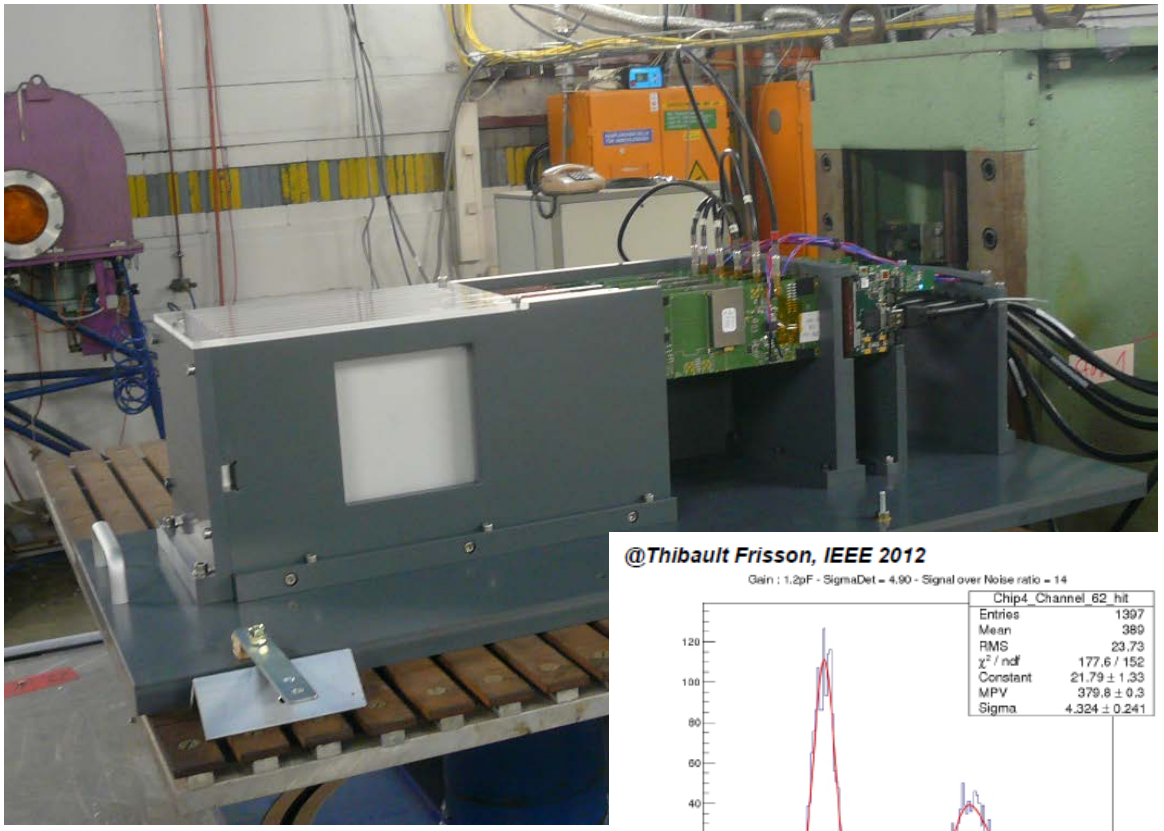
Here example of integration of SLAB

A conservative version

- **Single layer slabs**
- **¼ active area (4 chips = 256 chanels), 1/8 length**
- **QFP Packaged chips**

6 SLAB prototype : 1536 chn.
Test beam @DESY
S/N = [14..22] wrt. Chn# !

Intermediate compactness ✓
3 cables : LV, HV, DAQ&SC ! ✓
Qualification of sensors and VFE (analogue) ✓



- **Good result which highlight the amount of remaining work…**

PIN diode matrices design

The simplest design to control the cost

- Few thousands of m² needed for ILD
- Glued on PCB : Floating Guard Rings

Drawbacks :

- Large dead zone at the edges (>1 mm)
- Crosstalk with GR

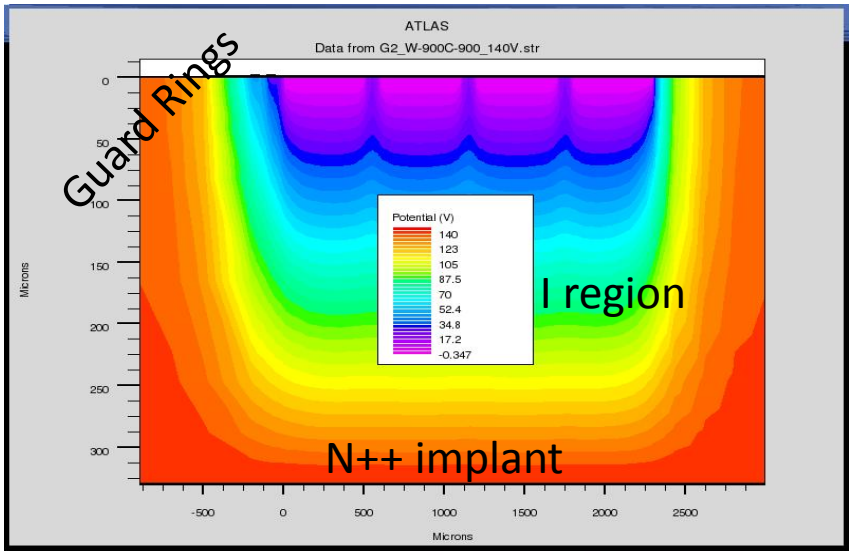
R&D in close collaboration with HPK

- Split GR and/or complete removal of GR
- Laser dicing : gain a factor 2 on dead zone
- Smaller size abutted matrices may improve yield

Also tried edgeless techno. from VTT

Large matrices, reduced dead zone ✓
Crosstalk ✗
Optimization (dimensions) ✗
Mass production & tests ✗

P++ implants (pixels)



HPK : 9x9 cm², 256 pixels

SKIROC chip

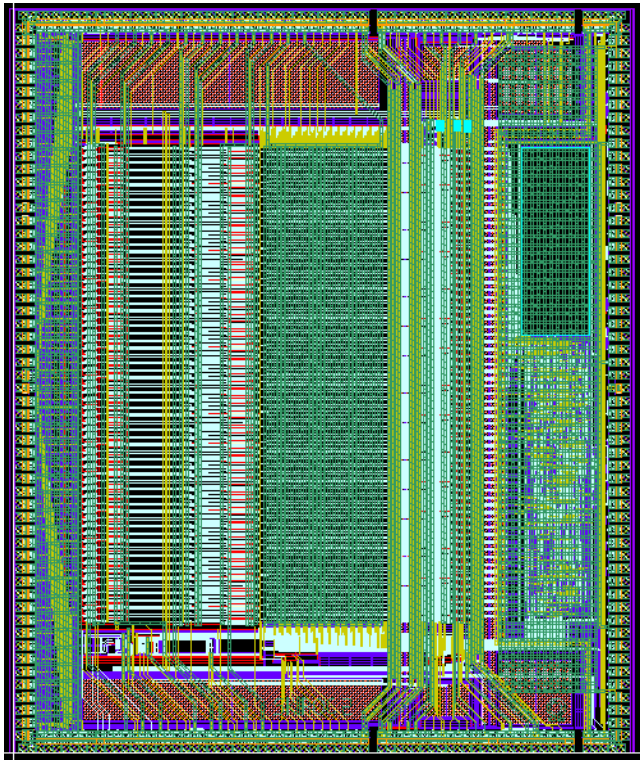
Silicon Kalorimeter Integrated Read Out Chip

- SiGe 0.35µm AMS, Production batch received Q3'10
- 64 channels, variable gain charge amp, 12-bit ADC, digital logic
- Power-pulsed → 25 µW/channel (goal)
- Linearity & 3000 MIPs dynamics

« Youth bugs » seen, fixed in next version

- Trigger logic to be improved
- Optimization of power-pulsing

VFE (Analogue) ✓
Trigger ✗
Digital functions, power-pulsing ✗
Trigger ✗

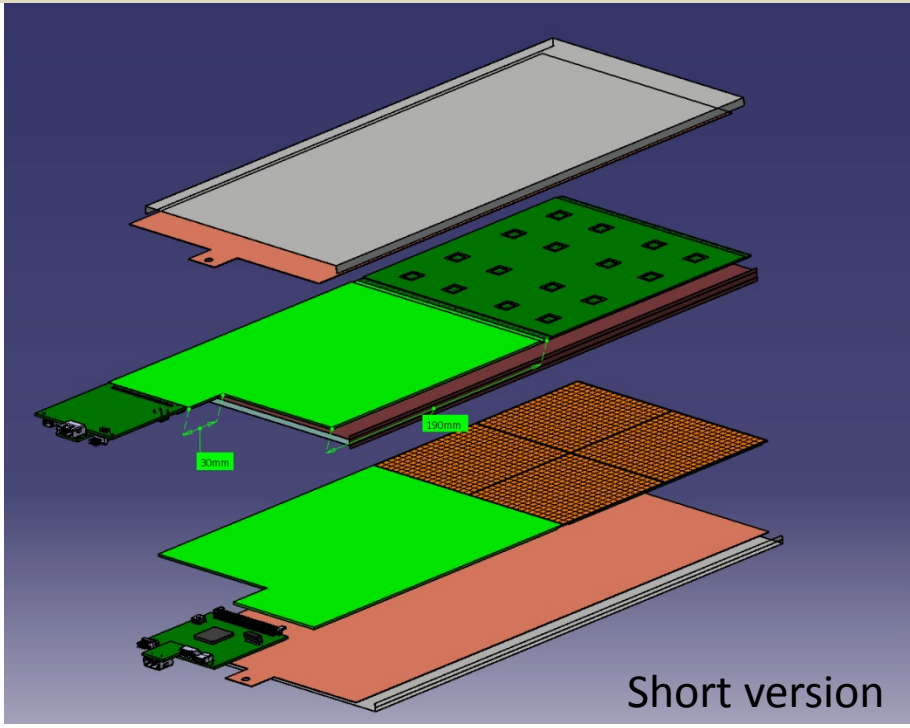


Detector slab : “extreme” design

Compact assembly of 2 layers of 1 to 8 Active Sensor Units (ASU)

1 ASU = 1 kapton (HV bias for PIN diodes)
+ 1 layer PIN diodes
+ 1 PCB with microchips embeded
+ 1 thermal drain (copper)

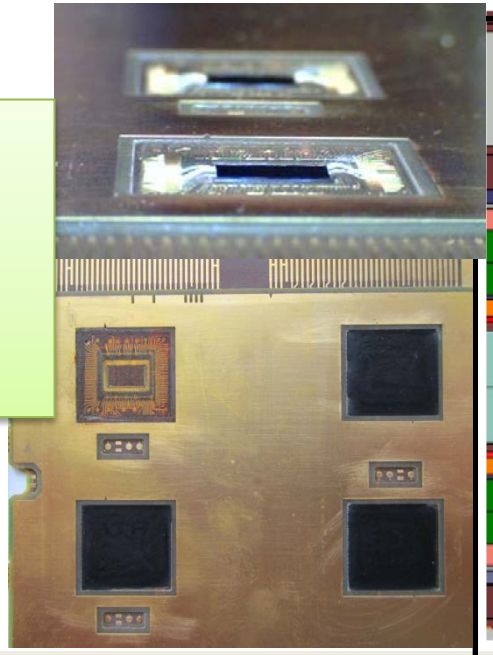
PCB is critical : 1 mm tick, 8 layers, 1% flatness , chips bounded *into* ✘

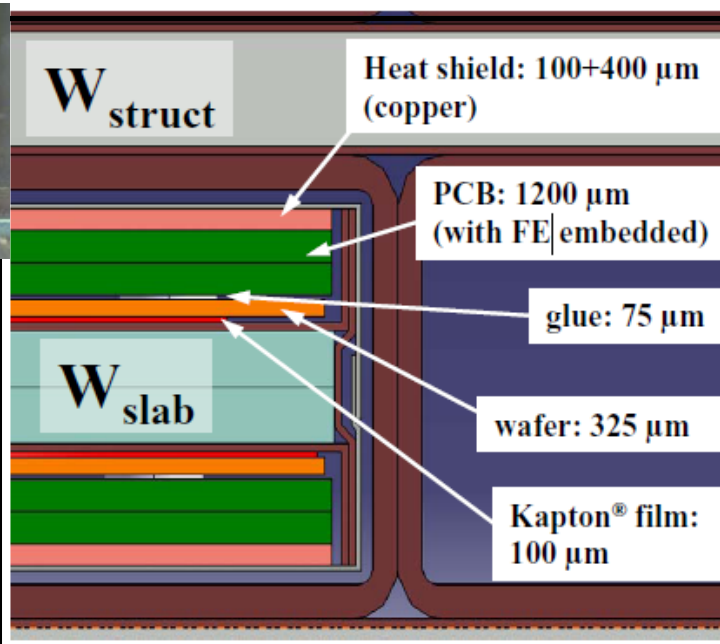


Prototyping ✓

Flatness ✘

Mass production & tests ✘

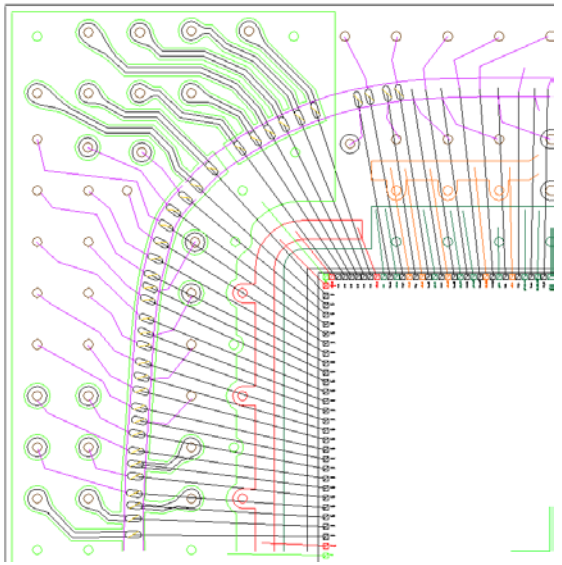


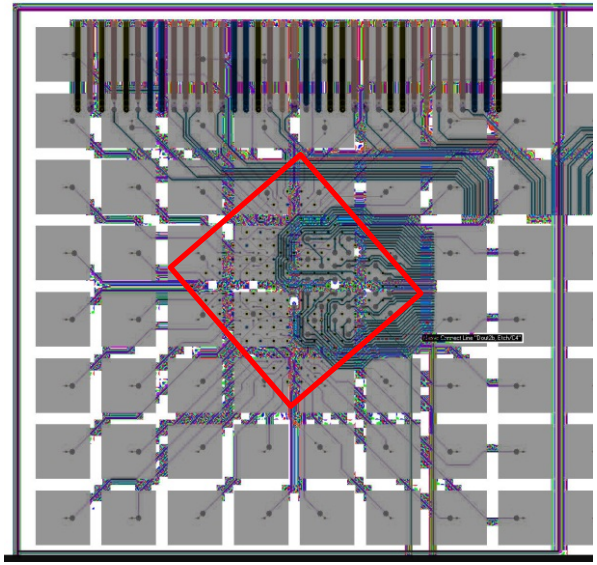


Detector slab : conservative design

Same concepts but with chips in package

- BGA design requires additional 3 mm in SLAB thickness
- Ultra thin BGA under study : promising
  - Thicknesses as low as 0.5mm
  - Feasibility of lidframe : done ✓
  - Length of pixel-chip traces divided by 2-3 w.r.t. PQFP design





BGA pattern : 1/16th of the PCB

Prototyping ✗

Impact on Xtalk, noise : to be studied

Expect easier testing & maintenance

Large mechanical structure

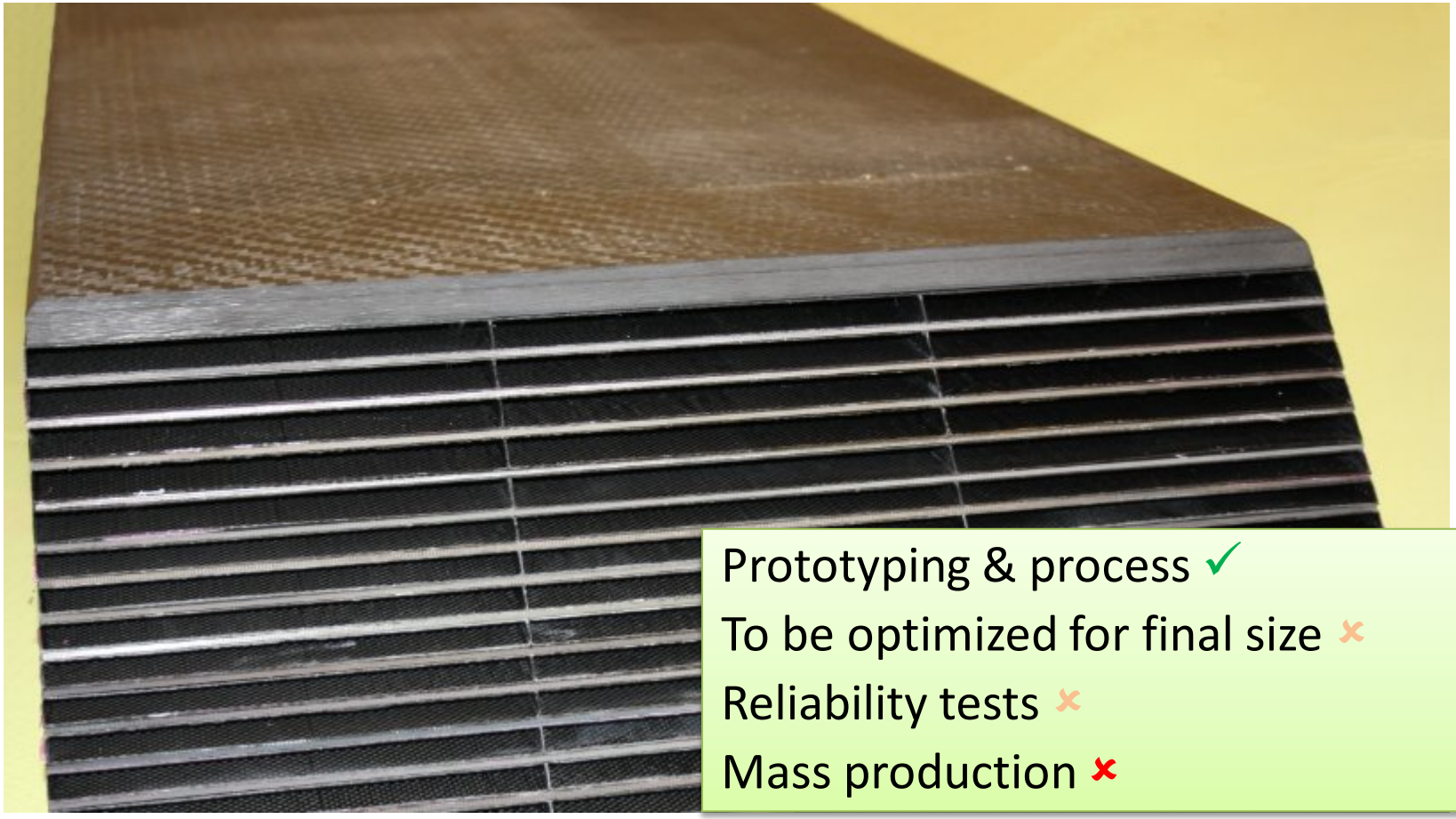
Each layer build separately then “cooked” together.

Deeply simulated : mechanical constraints, thermal behavior

Next step : wider assembly with 5 columns

Tungsten plates wrapped into carbon fibre: 15 layers

7 mm tick detector slab slided into alveola



Prototyping & process ✓

To be optimized for final size ✗

Reliability tests ✗

Mass production ✗

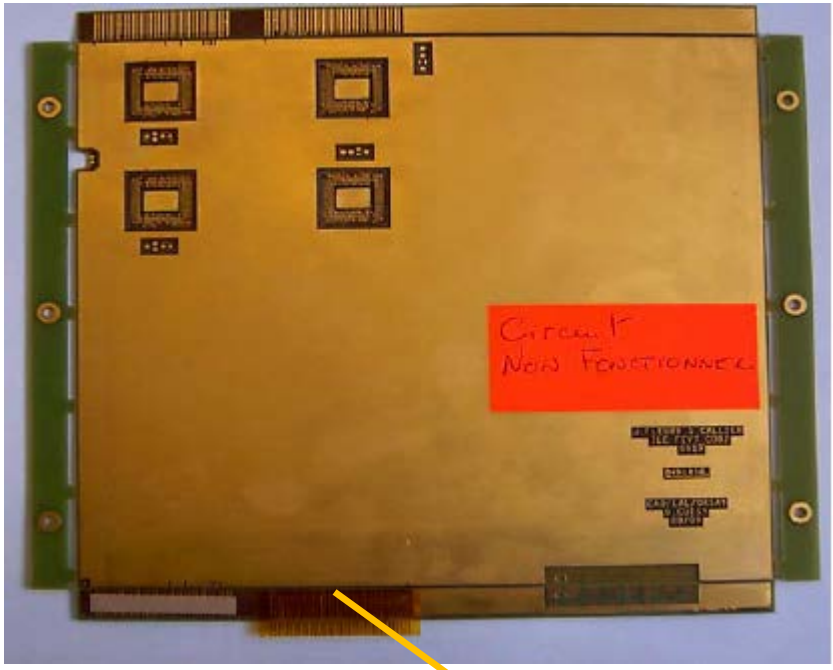
Long SLAB

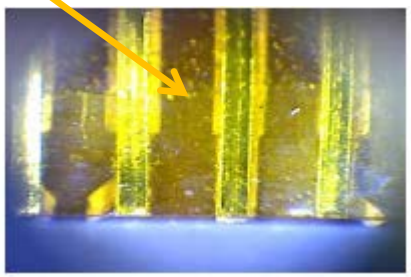
Up to 9 equipped PCBs interconnected to make detector slab

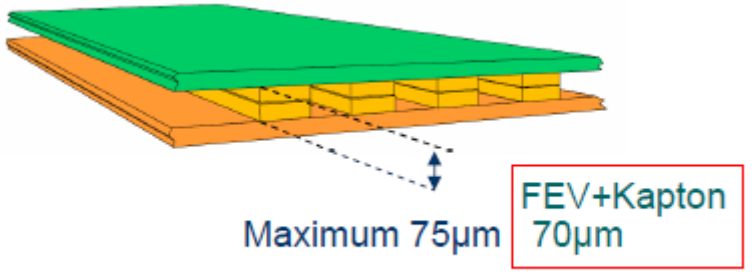
Electrical and mechanical connection made thanks to Kapton connecting cable

Technique under investigation

- Soldering with Flat Cable (Kapton)
- Easy for mass production







Prototyping & process ✘
B field ✘
Signal integrity ✘
Reliability tests ✘
Mass production ✘

18 cm, 4 slots of 36 pins each

DAQ : hardware and software

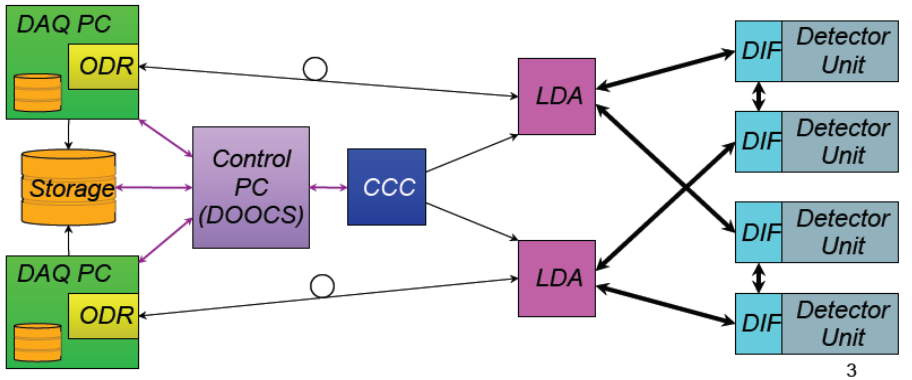
Scalable : Computing network architecture
Standard : Giga-Ethernet, Serial 8b10B

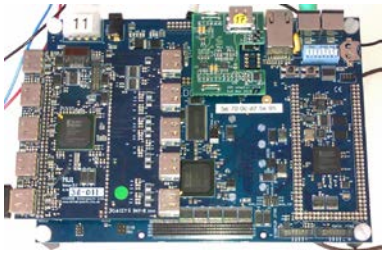
Compact

- "one cable for everything"

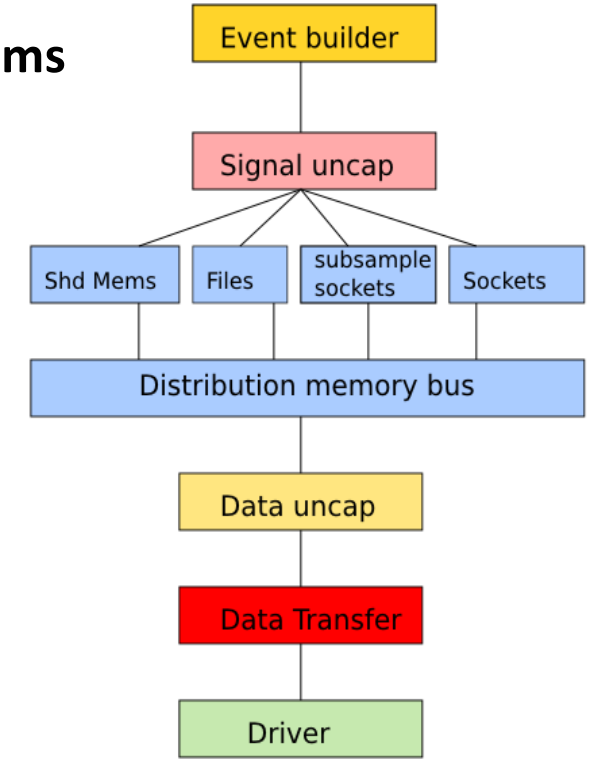
  Data Acquisition, Timing, Slow control

- Backplane-less : made for integration





Ran for test beams



Flexible and highly modular software

Multiple output formats

Files (offline), Shared memory (online High Perf.)
TCPSockets (remote online), Subsampling (real time processing)

Architecture & prototyping ✓
Reliability tests ✘
Coupling to supervisor/event builder (EUDAQ ?) ✘
Scaling to full detector size ✘

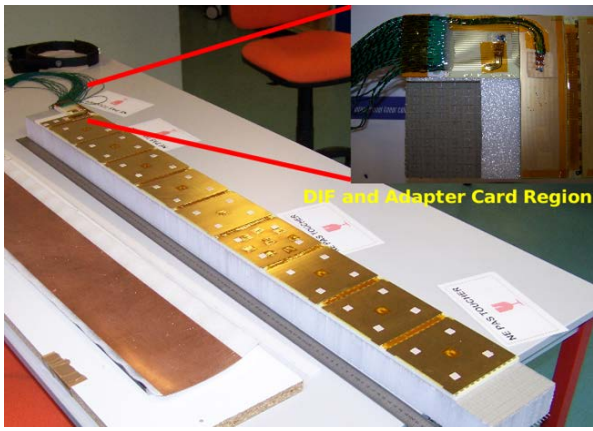
Developing a leak less water cooling system

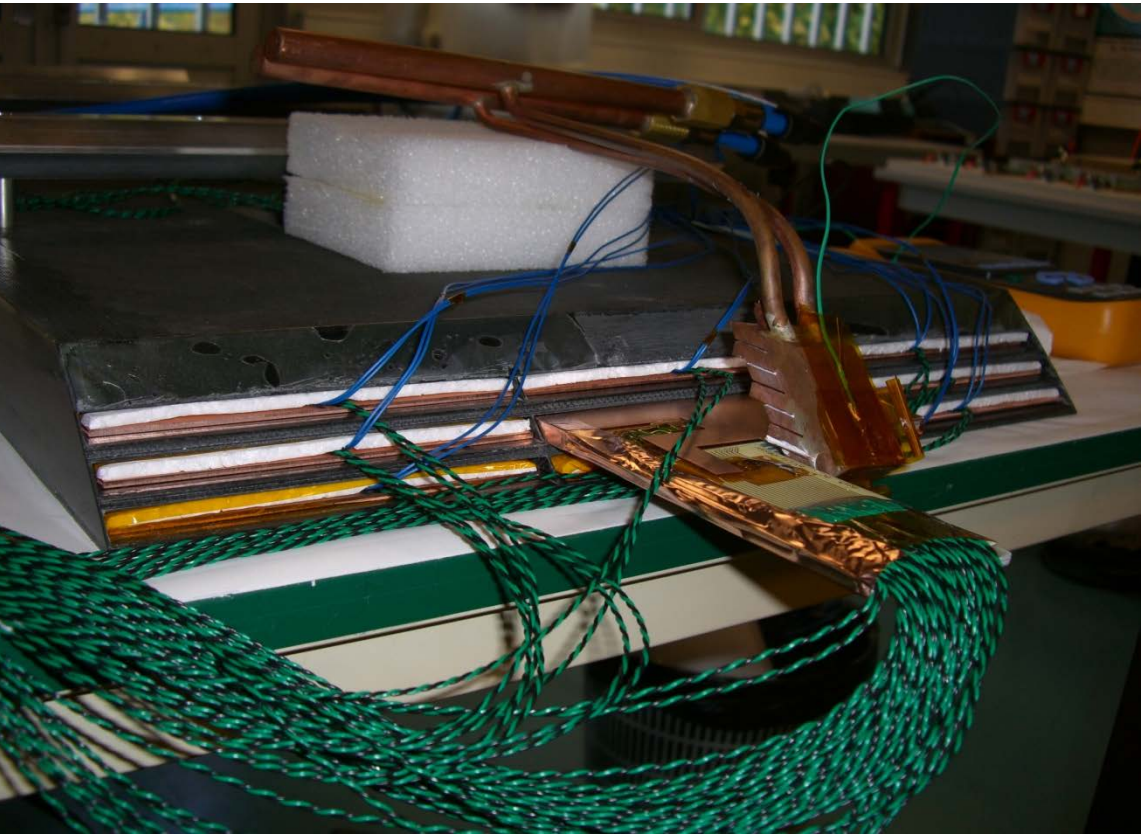
Total ECAL power dissipation O(10 kW) even at 25 µW/ch

Need active cooling system (cold water pipe + radiator)

Limit : temperature differences within ECAL

heat transfer to neighboring detectors





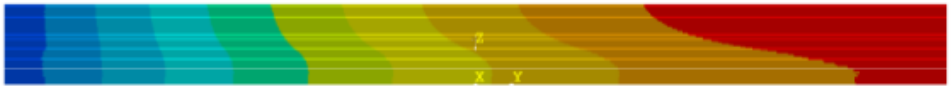
Cooling tests in demonstrator module

Results

Barrel : (1.5m)

ΔT = 2,2℃

End Cap : (2.5m)



ΔT = 6℃

Thermal simulations of detector

Priorities for next prototyping steps

It is urgent to increase our knowledge about :

- BGA packaging + 16 chips/ASU
- Power pulsing + B field
- Long slab & signal integrity (up to 2m long transmission lines)

Will look at this in 2013.

ANR grant (Project leader : R. Cornat)

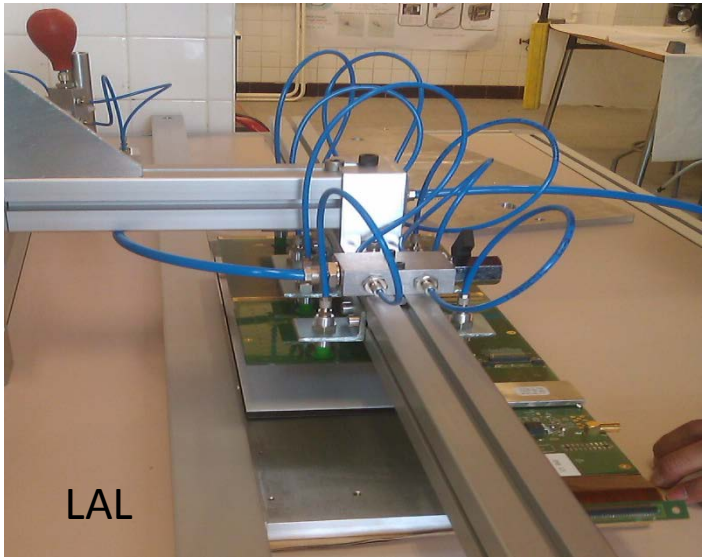
We should also have first thought about :

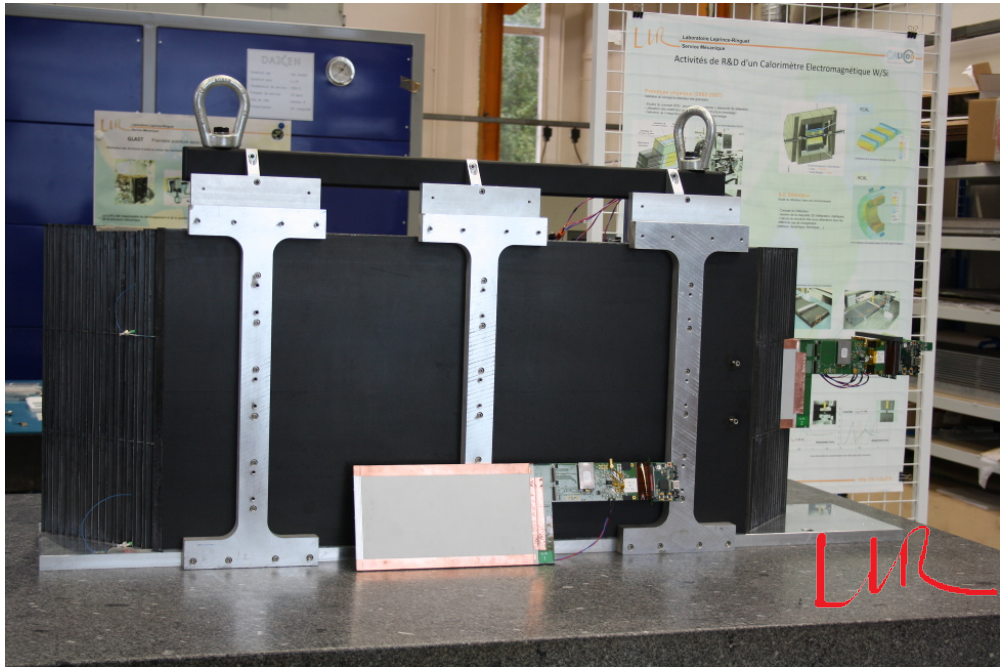
- Selection of components for a final design
- “Form factor” for integration
- Services
- End caps

Assembly of first SLABs

Most of technologies described above used to build first SLABs

First approach of an assembly procedure
Lot of effort required for automation
and industrialization

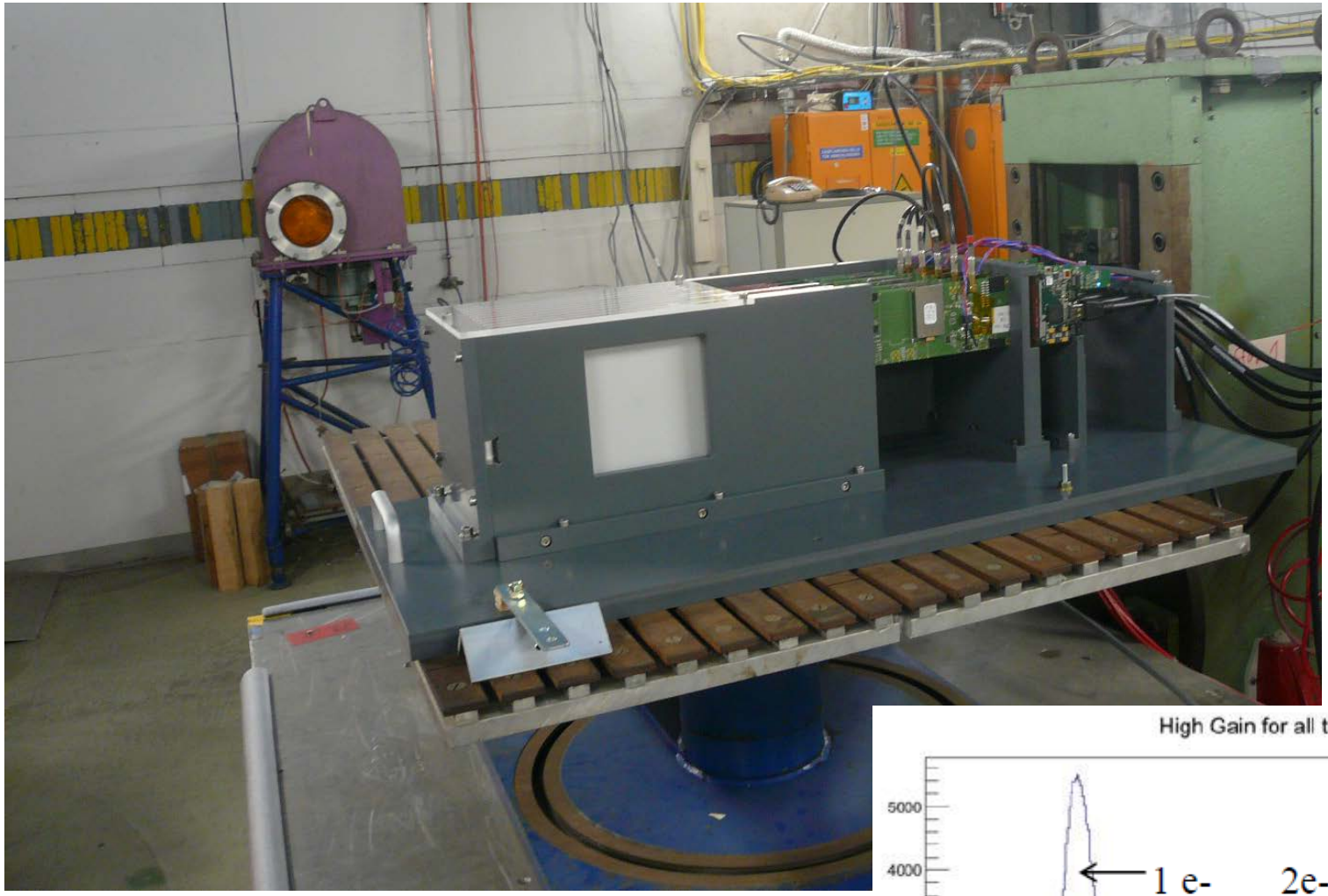


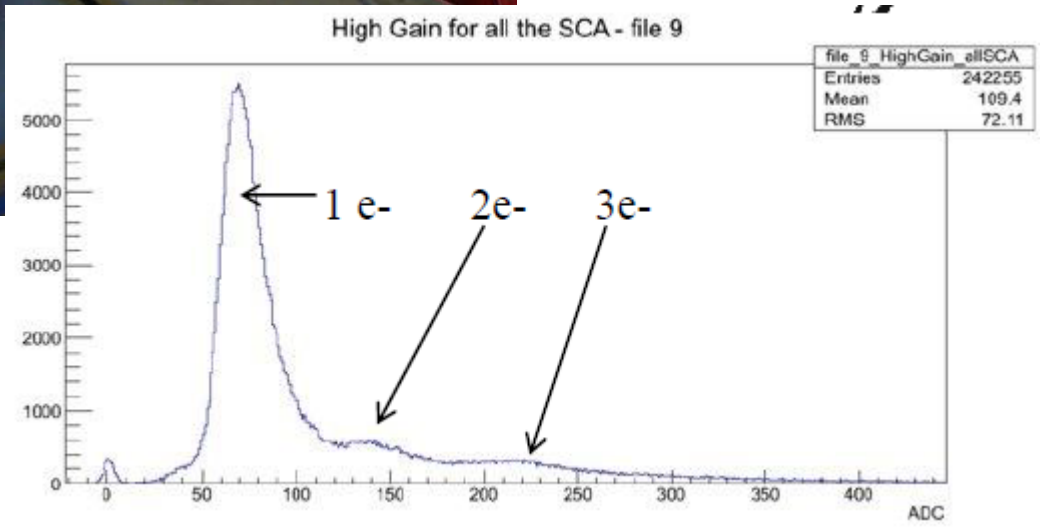


Simplified SLABS including
1 ASU with 4 SKIROCs in PQF package
1 Si Wafer (256 chn)

Successfully put into structure

First 6 SLABS tested @DESY (July'12)





Pending issues : toward a full scale detector

No serious R&D effort made about

- HV & LV distribution
- Redundancy (reliability)
- Environment monitoring & Security

‘Final’ design

Radiation hardness of specific components

Grounding

Cables & connectors

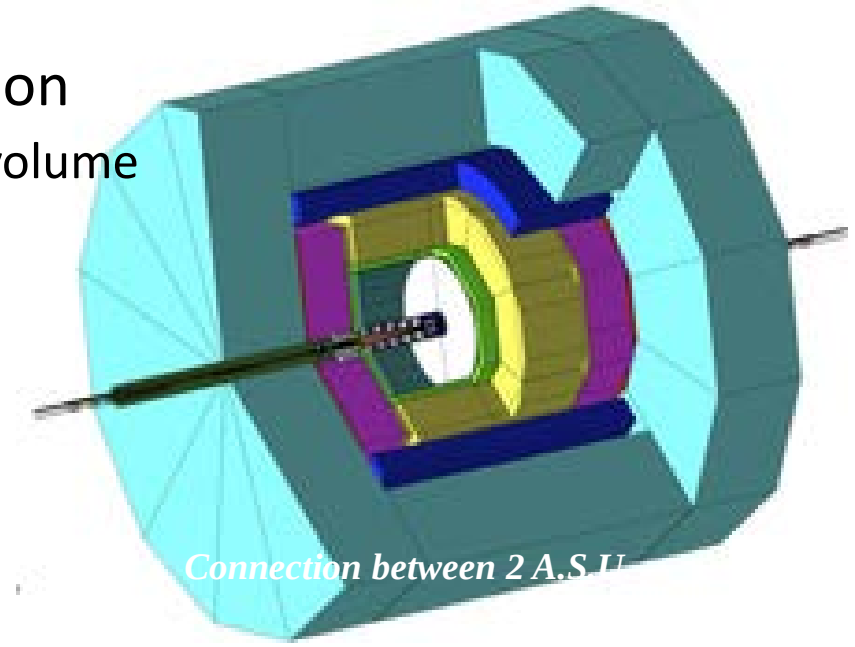
Quality insurance, procedures, logistics, commissioning, anything related to mass production, etc…

This is a good prototype…
…far away from the target.

Summary

CALICE Si-W ECAL technologies with emphasis on

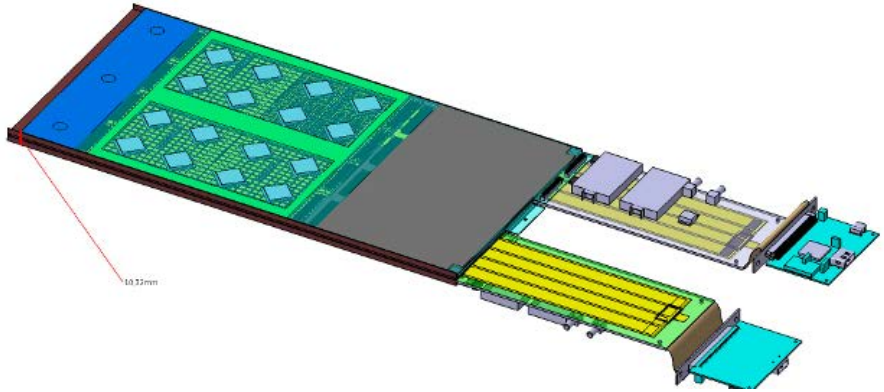
- Low power FE electronics incorporated in detector volume
- Integration (Structure, DAQ, cooling, services)
- Sensor improvements & industrialization



Step by step prototyping targeting
the best feasibility/cost compromise

Optimization of overall design is based on accurate physics simulations

- Number of layers
- Number of pixels
- Dead area
- Allowed material



Progress in having good understanding of how to build a complete ECAL with affordable technologies but big amount of remaining work.