LLR

PIN diodes matrices
Si-W ECAL

Activities at LLR

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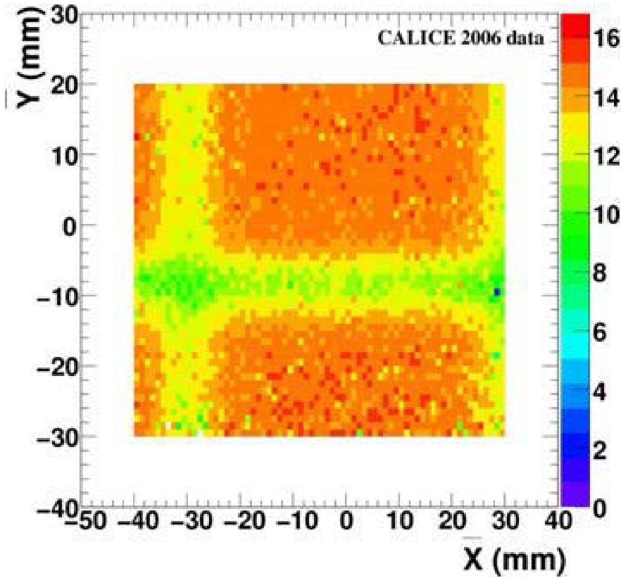
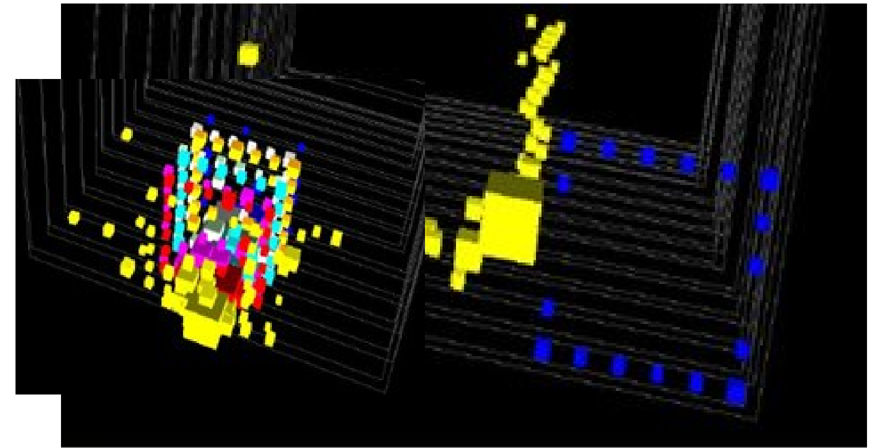
Activities at LLR

- Relations with subcontracters
- Electrical measurments
- Crosstalk measurments
- Design & (some) simulation

2 issues





Peripheral dead zone : -20% of detection efficiency due to GR and mechanical structure

Can be compensated (off line)

« square » events : crosstalk between guard rings and peripheral pixels

Should be reduced by a factor 50 to 100

Technological prototype

- Larger matrices : lower edge effects on reconstruction
- Smaller pixels : improve « imaging » (counting)
- Thiner detector : keep Cpix~constant (same electronics)

- Critical issue about COST
  - Enlarge potential manufacturers
  - Understand origin of cost (yield, maskset, commercial margin, raw material, processing, …)

Cost

- Basic ideas :
  - SORT wafers : keep as most as possible, equip non critical part of the detector with partly bad matrices
  - OPTIMIZE production yield
    - Smaller matrices (decrease sensibility to local defects)
    - Larger batches

- But : need to solve edge issue
- Crosstalk is secondary (may be suppressed with digital data filtering)

Batches

- Hamamatsu (9x9 cm2)
  - 2008 : 18x18 pixels, 1.2 mm edge (used on ecal slabs)
  - 2009 : 16x16 pixels, 750 um edge
  - 2011 : 16x16 pixels, 1mm – 200 um edges : laser dicing
  - 2012 : idem + baby wafers

Standard
Segmented GR 2 or 4 rings
No GR

Measurements at LLR (1)

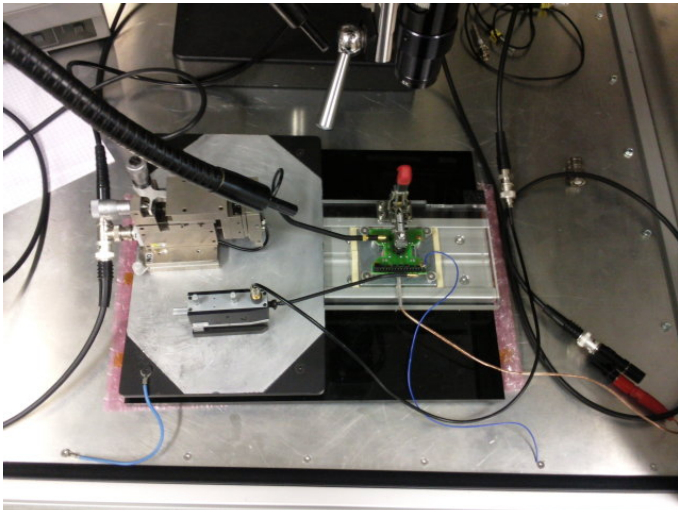
- I(V) & I(t, V, T, H) => long term
  - Global
    - « box » with contact to each pixel
    - sourcemeter
  - At pixel level (in preparation)
    - Adding a switch crate (256 switches, have 104 for the moment)
  - Useful for breakdown (> x3 bias voltage)
  - Check compatibility with ReadOutChip
    - Current = offset for the preaplifier = decrease of dynamic
  - Climatic chamber (T,H)

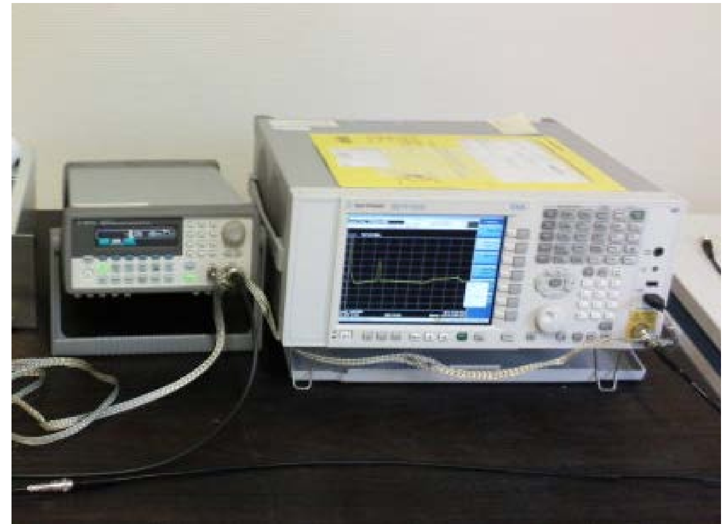
Measurements at LLR (2)

- C(V)
  - Global
    - « box »
    - Sourcemeter + RLC network analyser
  - Quality check
    - Full depletion voltage
    - Implant (with $1/C^2$)

Measurements at LLR (3)

- crosstalk
  - Verification of manufacturer's design
  - R&D (segmented guardring)
  - Measurments with sensibility of -100 dB





R&D

- Segmented GuardRings
  - « cut » GR into small pieces to avoid signal propagation
  - What about GR quality (leakage) ?
  - 2007-2008 (OnSemi)
  - 2012 (HPK)

- Edgeless sensors
  - VTT edgeless technology
    - Single diodes 0.25 cm2
    - Minimatrices : 3x3 pixels, 1 cm2
  - 2011
  - First batch received in September

Measurement results HPK'12

- Delay due to other tasks
- I(V) & C(V) as usual (no surprise)
- Baby wafers :
  - even with no GR, Vbreak ~350 V !
  - Segemented GR : ok.

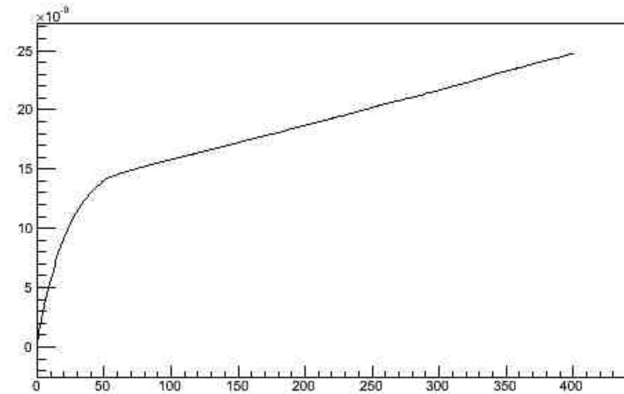
- ON GOING I(t, V, T, H), t up to several weeks, months

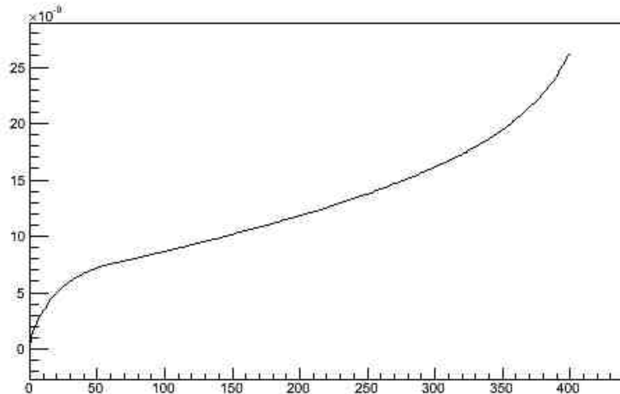
No GR !

- I(V) Slope slightly increased

May consider edge effect

Should check individual pixels





- Expect lower yield as breakdown appears at lower Vbias

Next steps

Individual pixel characteristics

Cross talk

Follow cost issues (search for more potential manufacturers)

R&D : urgent to organize Test Beam to test square events (require few 100s MIPs) and/or use of an IR laser (bought @LLR, test room being equipped)

Tools to share results ?

Discussion

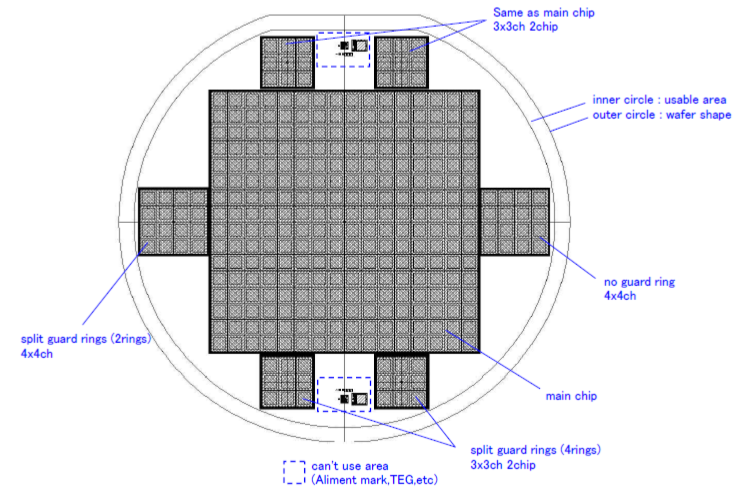
- 6 inches wafers :

Ok with 4 smaller sensors

Expect better yield

Compliant with 4 inches wafers : wider selection of manufacturers

- Need to confirm impact of dead zone



Note : Optimum use of overall surface with (4.9 cm)² => ~20 cm large slab and 0.61 large pixels