CALICE
Calorimeter for ILC

Peak Sensing ADC for SiPM readout

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Outline

- Motivation & Requirements of the ADC
- ADC structure
- Design details
  - parameter calculation and estimation
  - peak sensing T&H design
  - switch design
  - comparator design
- Summary & Time Plan

Motivation & Requirements

Motivation of the ADC

- Quatization (one ADC per channel):
  - charge integration
  - timing voltage ramp
- 3 types of signal to quantize:
  - calibration signal, only a few pixel fired
  - physical MIP-like signal, large fluctuation
  - timing voltage ramp

Motivation of the ADC

- Calibration signal

i. clearly seperated peak - < 1 mV electronic noise - 12 bits

ii. up to 10 pixels, range of ~300mV (small range)

iii. only a small portion of the total signals

- Physical signal - Much larger uncertainty - Less resolution

i. large fluctuation due to Landau Distribution

ii. signal uncertainty due to the detector pixel uniformity
4-5mV (15 pxls , MPPC 50um pitch device)

iii. most time, 8 bits sufficient - Quantization noise (3.7mV)

- TAC ramp signal

i. 10 bits - 400ps bin size - <100ps quantization error

ii. if ns resolution sufficient, only 8 bits required

Requirements

- Resolution : 8 bits for most of time
  12 bits for calibration only (shortly)
  10 bits necessary for precise timing

Other Requirements

Performance	*Parameter*
Area	~ 100μm * 700 μm
Sampling Rate	> 1 MHz
power	μW w/ pulsing
SNDR, SFDR	descent

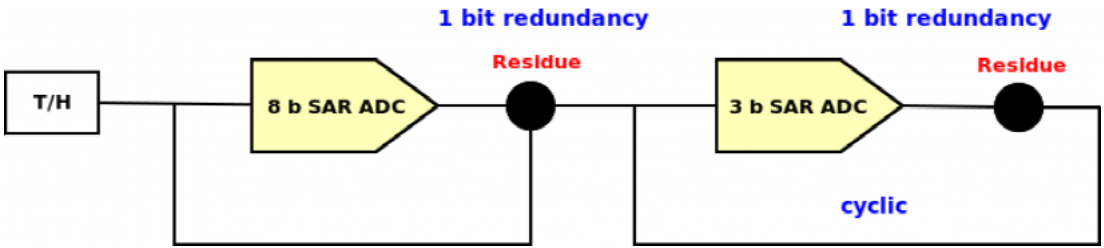
ADC Structure

ADC Structure

- 8 bits low power (!) , small size ADC, SAR is the perfect choice
- sampling rate easily exceeds 1 Mhz.

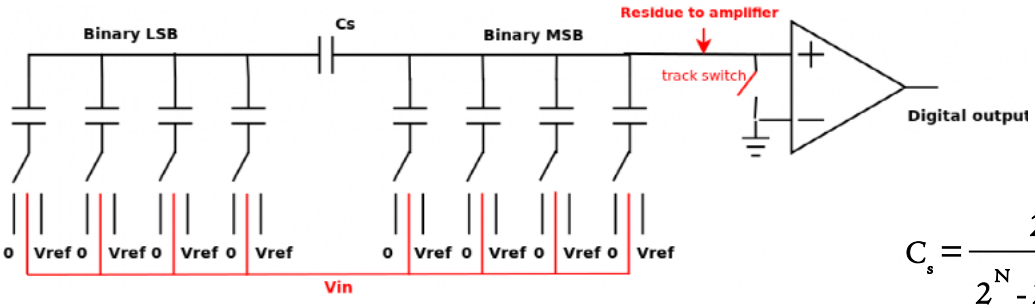
  only μs needed for analog memory, less distorsion
- the extra 2 bits (10bits) required by timing can be pipelined
- the additional 2 bits (12bits) can be cyclic

  (only shortly)



Design Details - 8b SAR C-array

8b C-DAC in SAR ADC



$$C_s = \frac{2^N - 2^L}{2^N - 2^M - 2^L + 1}$$

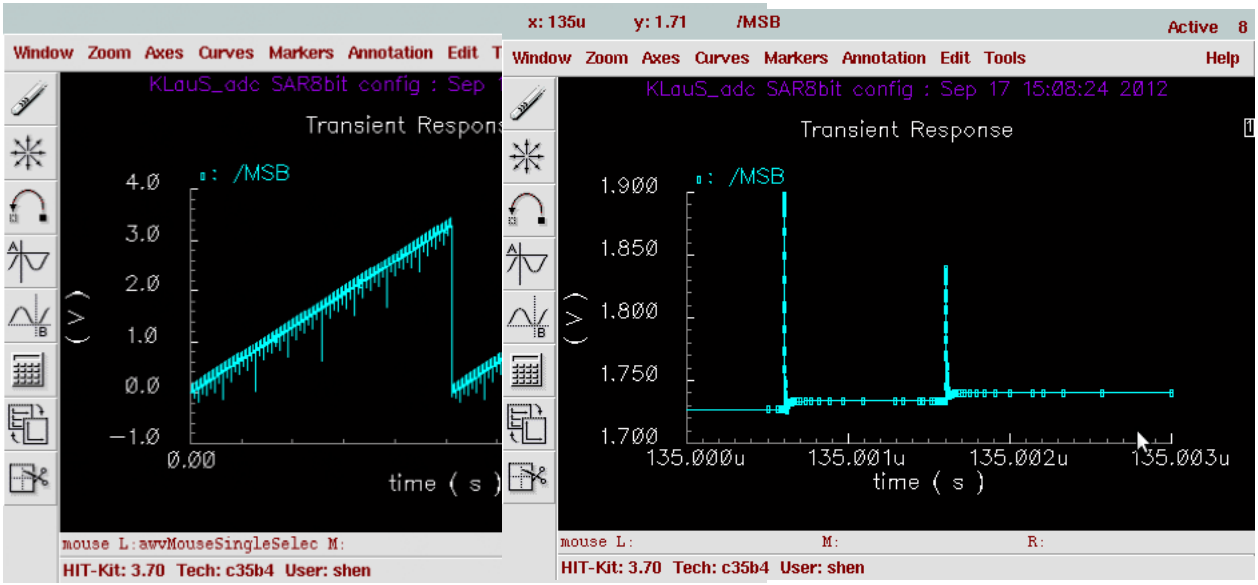
$DNL = (2^k - 1) \cdot dC/C \cdot LSB$

DNL < 1 LSB, dC/C < 0.4%, According to the AMS datasheet, for Cpoly W=L > 7um, 10um will be taken

- total size : 32um * 100um, differential 64um *100um
- KT/C noise around 0.2 mV

  Setting time < 10ns

Simulation for the 8b C-array



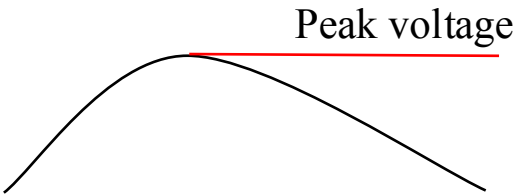
8 bits Scan MC
DNL/INL < 0.5 LSB

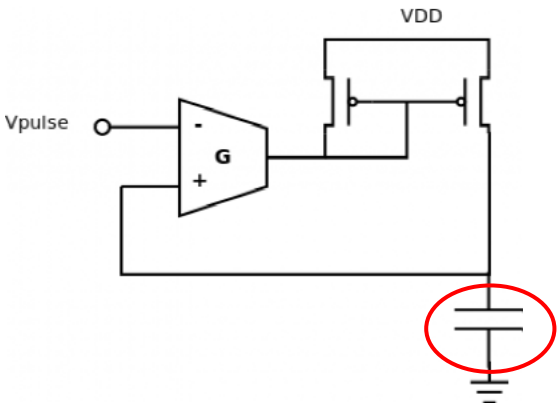
Zoom of each step,
response fast enough

Design Details - Track & Hold

Peak-sensing Track and Hold

Peak sensing using a **peak detector and holder (PDH)**





Peaking time is input pulse shape dependent, easier to control with PDH

Memory capa can be merged to SAR capa

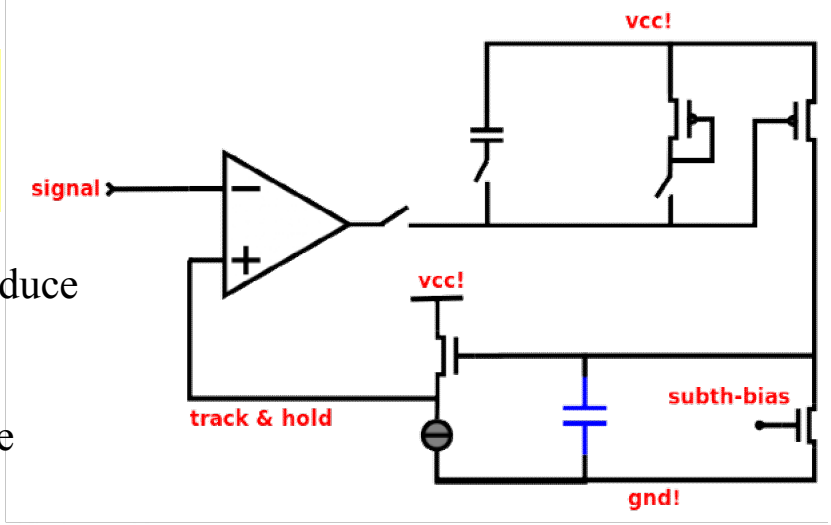
Peak-sensing Track and Hold

Small & large signal

P.S. Track and Hold

sub-threshold bias to reduce small signal error

Compensation to reduce droop rate

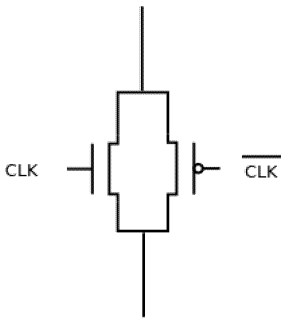


For rising time from 50ns up
signal from 10mV (error less than electronics noise)
Up to 1.2V (error less than 0.5%)
Bias current 50 uA

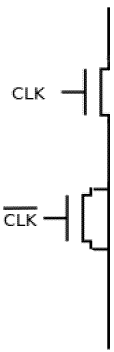
Design Details - Switches

Switch Design

- There are 3 types of signal to switch
- vcc, gnd, signal, 3 different switches need



gnd
switch



No complete cancellation

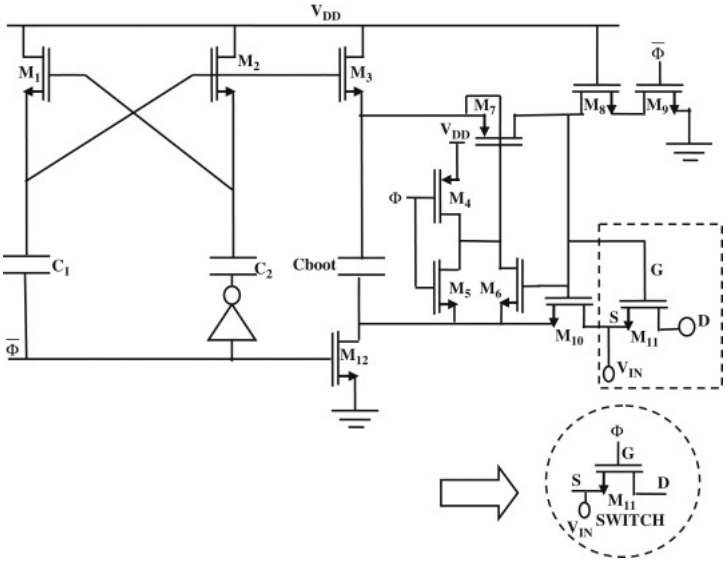
At all corners, error about 1-2mV in MC connected to Cmin,

Max error +/-125uV at comparator

Switch Design

- For signal, range range from 0.5V to 2.5V, switch with P/N mos is necessary, but the channel charge / clock feedthrough is dependent on input signal: Bootstrap Switch

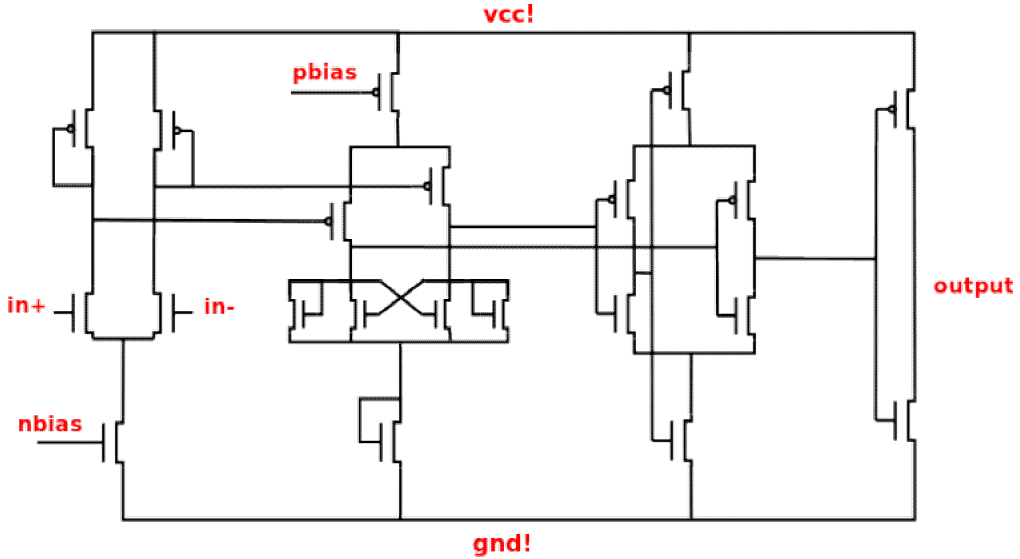
In progress



Design Details - Comparator

Comparator Design

- Comparator = preamplification + latch + CMOS converter



- Response Time ~5 ns, for ImV overvoltage
- Power, 20uA bias current

Summary

- SAR ADC structure chosen
- 8 bits for physical signal, 10 & 12 bits can be pipelined
- Size estimation 100µm * 300µm
- Pulsed power consumption µW
- Residue amplification, switch control logic, error analysis, careful layout needed
- Design started, Tapeout estimation Spring / Summer 2013