

AHCAL Electronics.

Experiences with the AHCAL testbeam prototype

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AHCAL main meeting

DESY

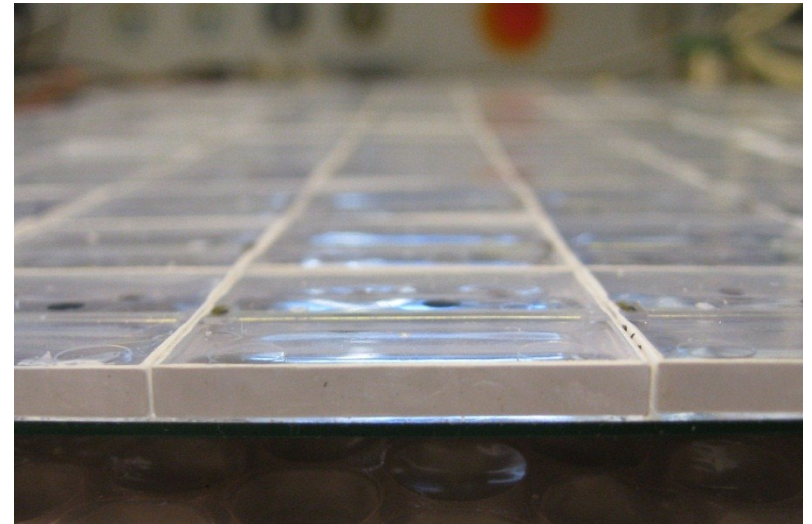
Dec. 10th to 12th, 2012



Outline

- > Hardware Experiences with respect to SPIROC3 specification
- > New topics

*I would like to apology for mainly listing up problems.
Lots of the problems have been solved already and the AHCAL detector delivers nice data (see later talks).*



Assembled tiles below HBU2

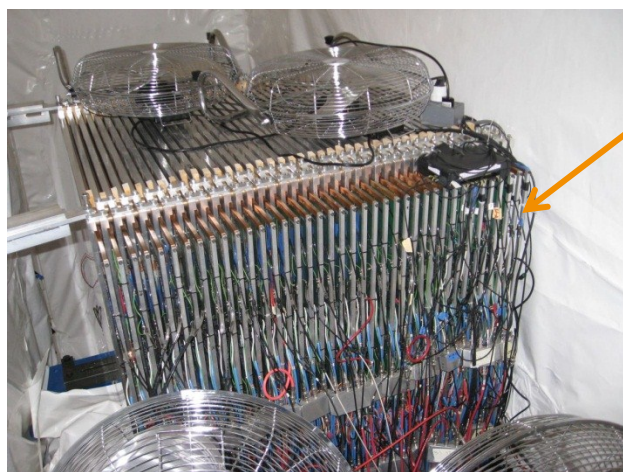
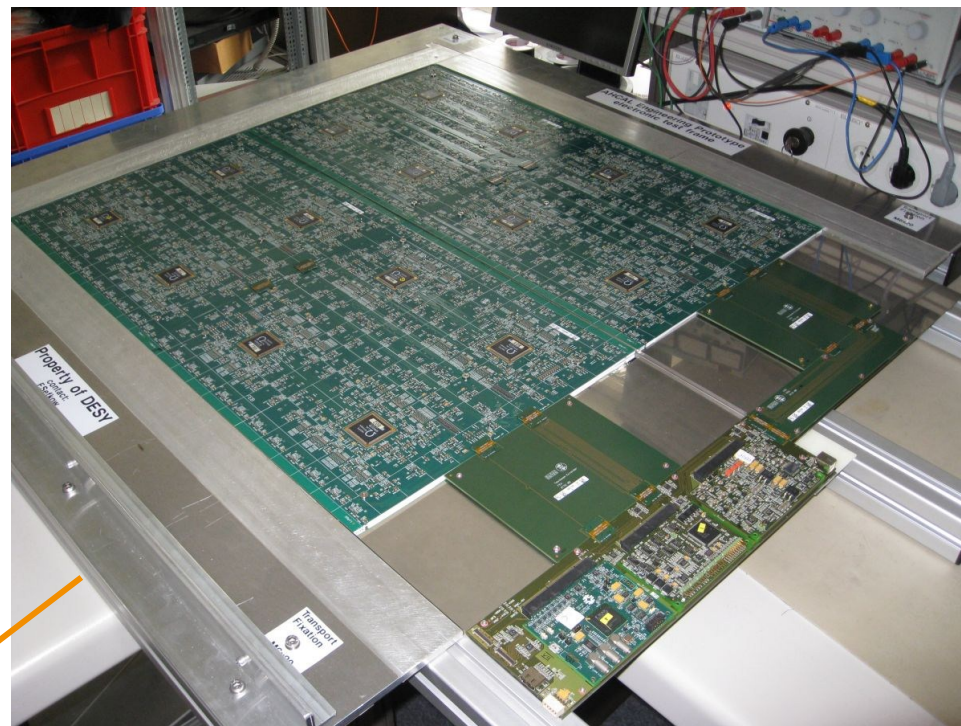
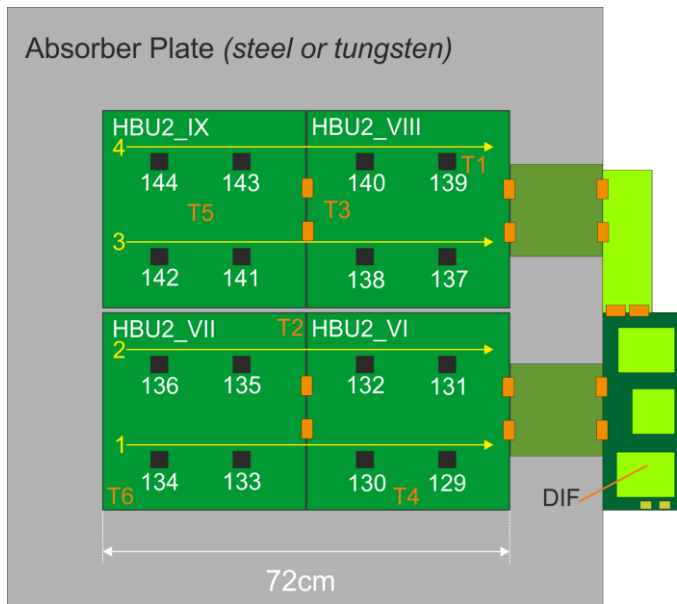
Topics to keep in mind for SPIROC3 specification.

- > Pedestal shift when too many channels have a high signal.
- > Memory cell dependent amplitude decay. Solved by compensation capacitors.
- > Feedback of channel-wise trigger thresholds on the global threshold.
- > Random zero events and zero-results for the first trigger.
- > Poor uniformity of the input DACs.
- > Holdscan is different for HG/LG.
- > Trigger threshold width increases with threshold height.

- > A lot of these topics have been addressed in SPIROC2c, but in SP2c: external trigger does not work.



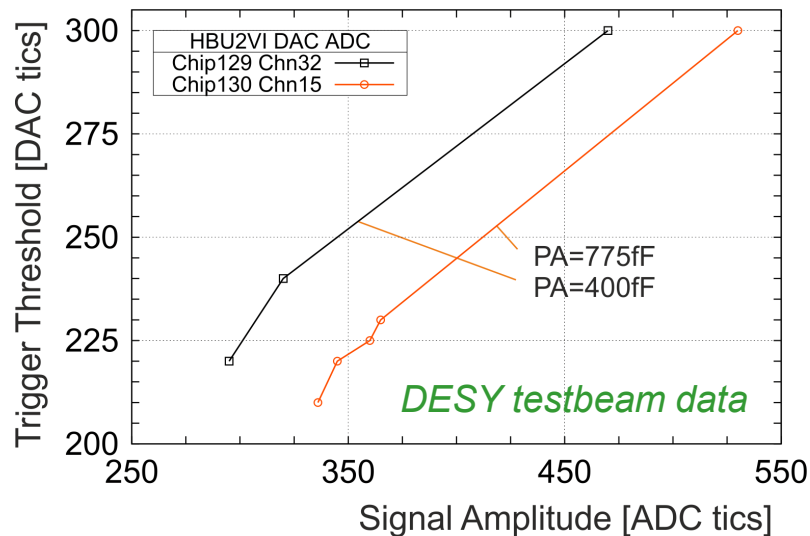
AHCAL testbeam module (CERN SPS)



See nice results in Oskar's and Sebastian's talks

Autotrigger Threshold

- In autotrigger mode, a **trigger threshold (DAC)** must be defined.
- Relation: trigger threshold DAC setting to ADC signal amplitude:

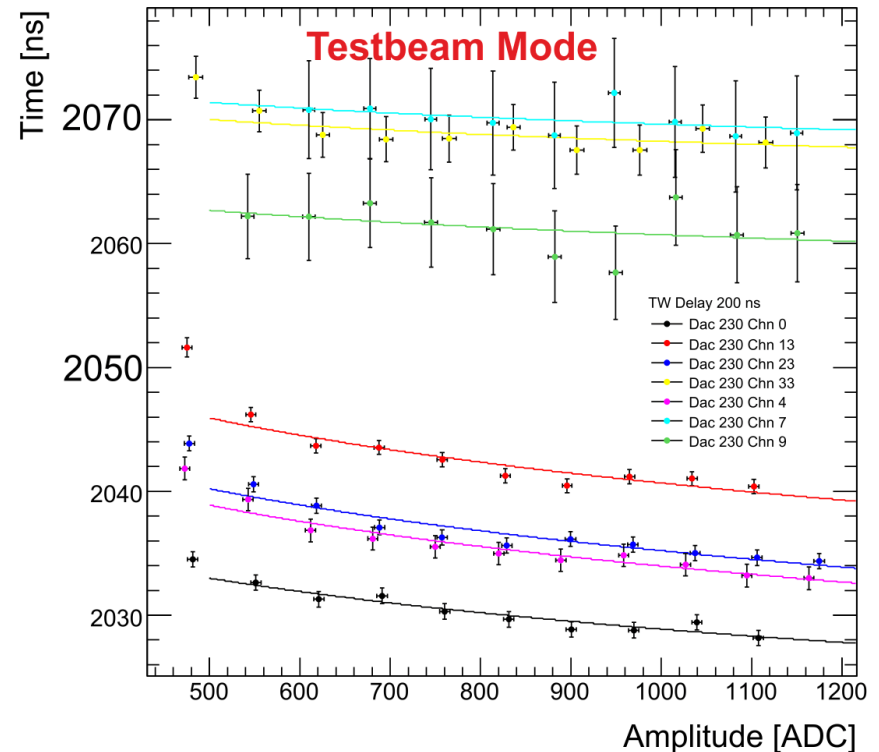
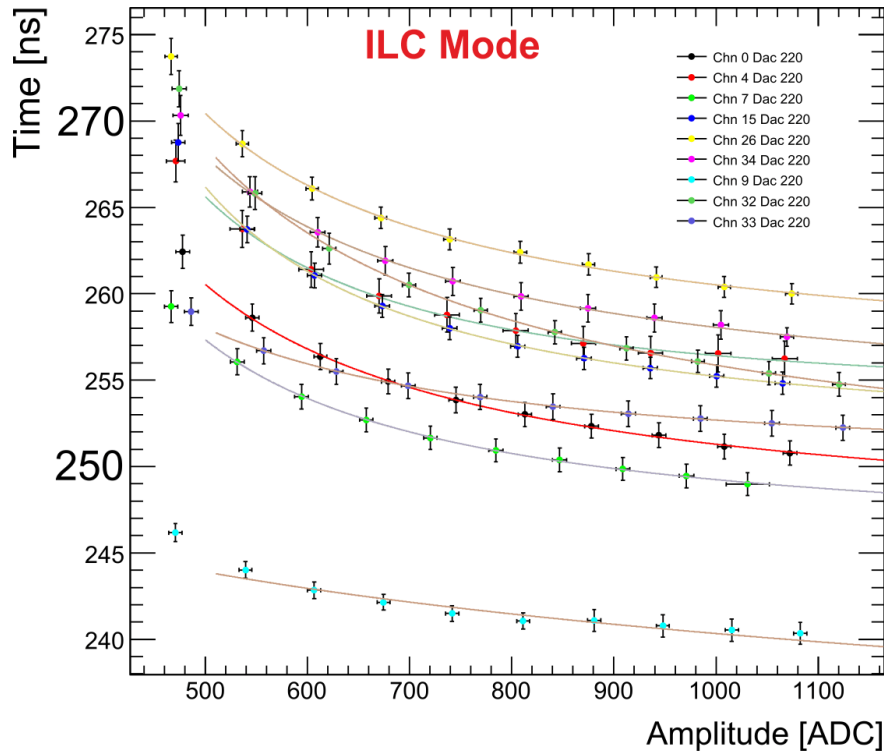


***Preliminary: MIP~500 ADC tics,
Pedestal ~240 ADC tics
⇒ 1/2 MIP ~ 370 ADC tics
⇒ Trig. threshold ~ 250 DAC tics***

- Problem: The ADC-DAC relation depends on the SPIROC2b preamplifier (PA) setting and the input pulse shape.



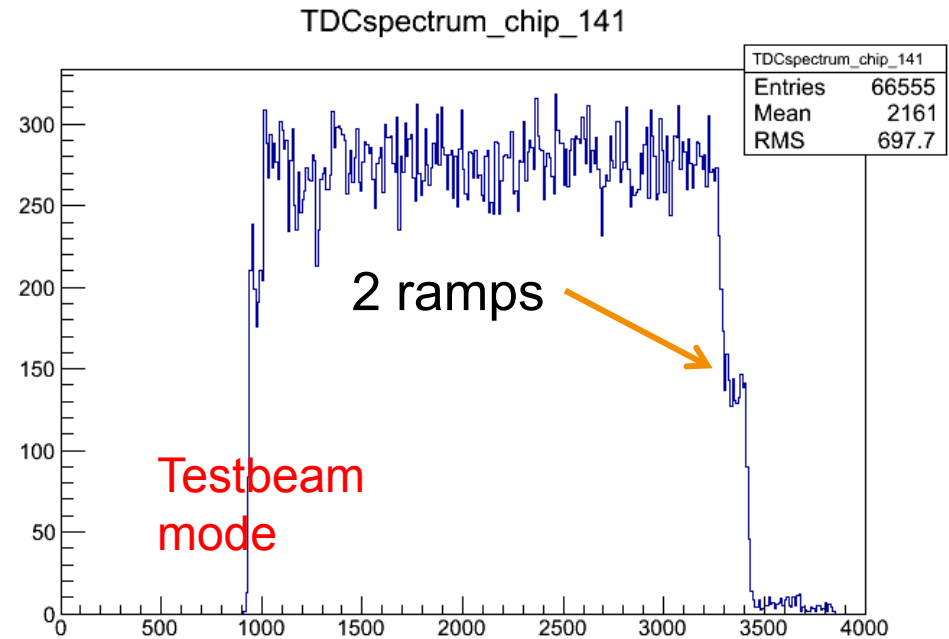
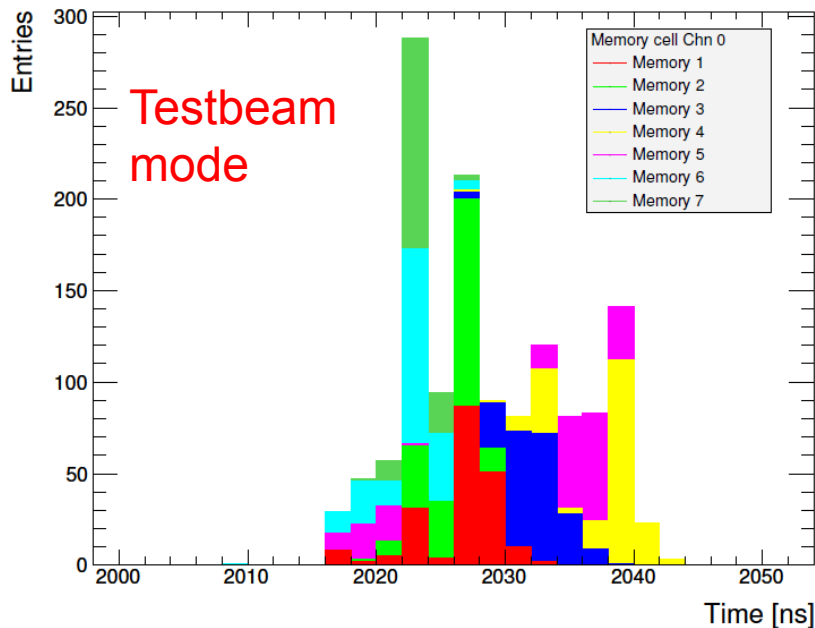
TDC: Time Walk and Channel-to-Channel Spread



- Amplitude-dependent time-shifts and channel-to-channel differences.
- Difficult to parameterize because of different behaviours. Channel-wise TDC calibration necessary as for ADC (MIP calibration)?



TDC: Memory Cell Dependence and „2-Ramp“ Problem

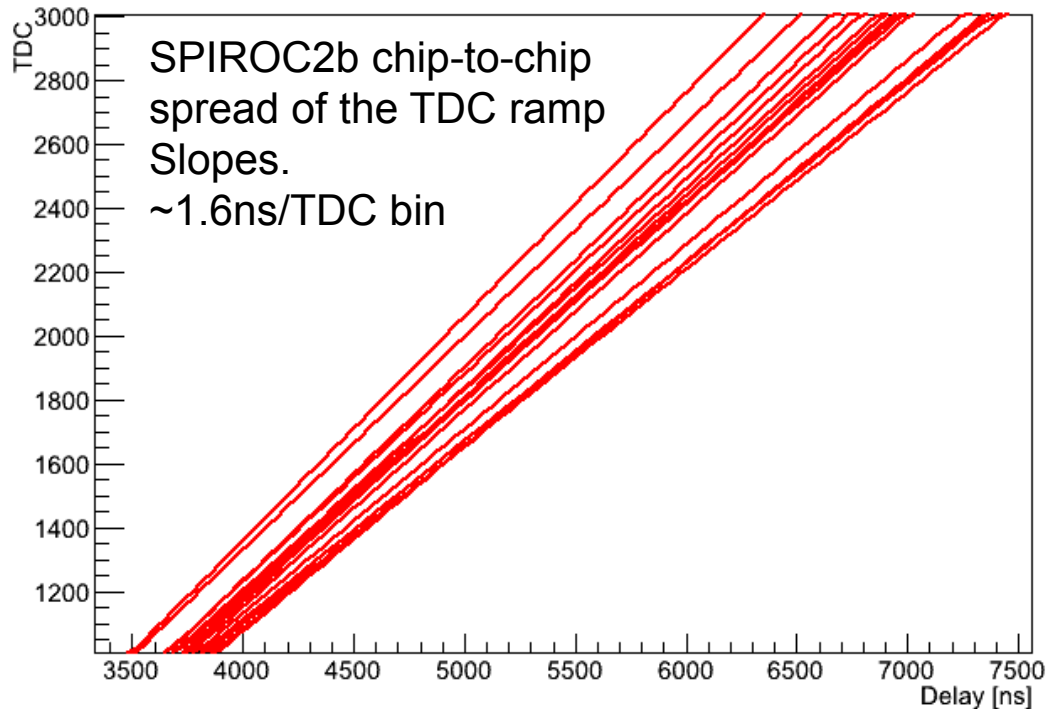


- TDC result depends on memory cell
- The SPIROC2b internal TDC ramps have different amplitudes and for a specific event it cannot be identified with which ramp the TDC result has been achieved (known problems).

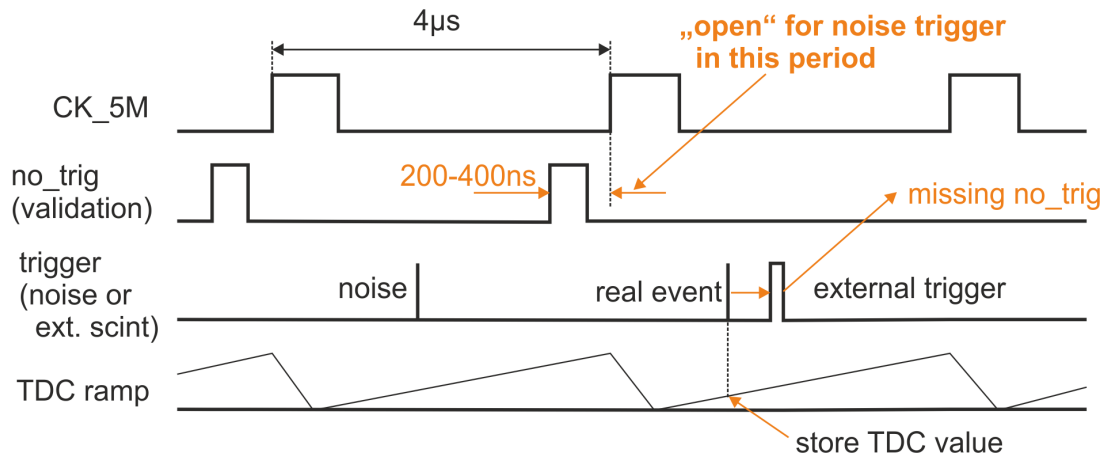


TDC Calibration – CERN Module

- Calibration of all 16 SPIROC2b ASICs of the CERN Testbeam-module with charge injection.
- Chip-to_chip spread of the TDC ramp slopes: Calibration necessary: TDC (time measurement!).

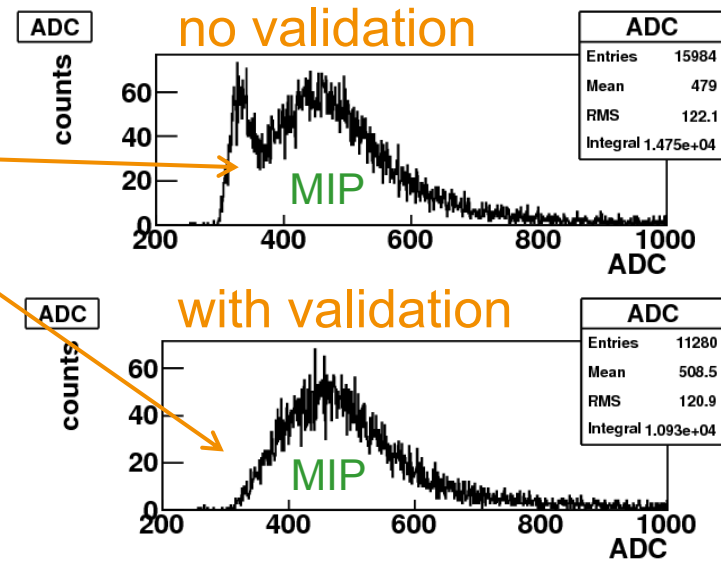


Trigger Validation



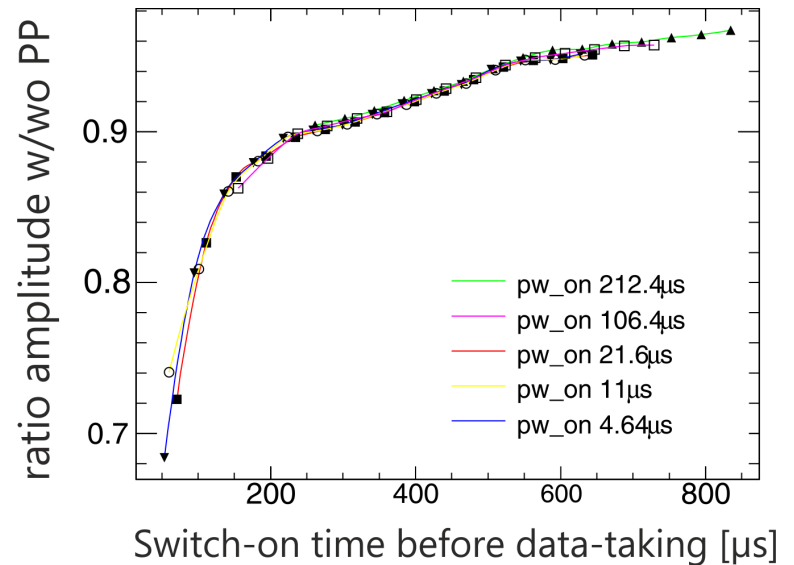
> Only stores events that are validated by an external trigger signal

- > **Validation works fine:** Histogram only shows MIP events without noise/pedestal contributions.
- > Problem: Validation does not work for noise hits between no_trig and rising CK_5M edge (200-400ns).
- > For no_trig 25ns before CK_5M, the validation did not work any more.

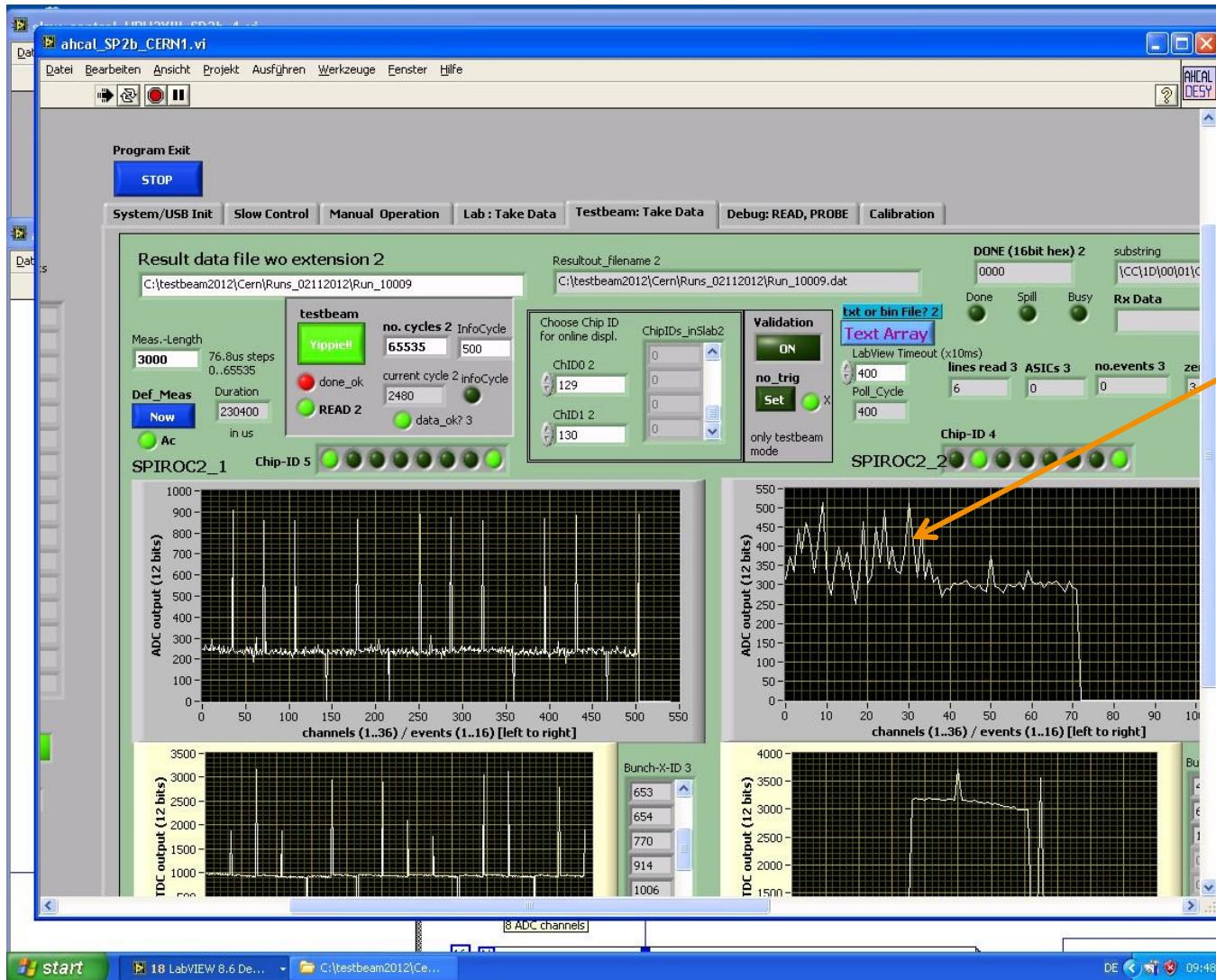


Power and Power Pulsing (PP)

- Aim: Switch on as short as possible before data taking starts (initial idea: $20\mu\text{s}$).
- Results with charge injection show a decreased amplitude response with PP.
- Single-Pixel Spectra measurements show a reduced amplitude with PP.
- Aimed power dissipation of $20\mu\text{W}$ per channel not reached yet.



Start-Run Problem



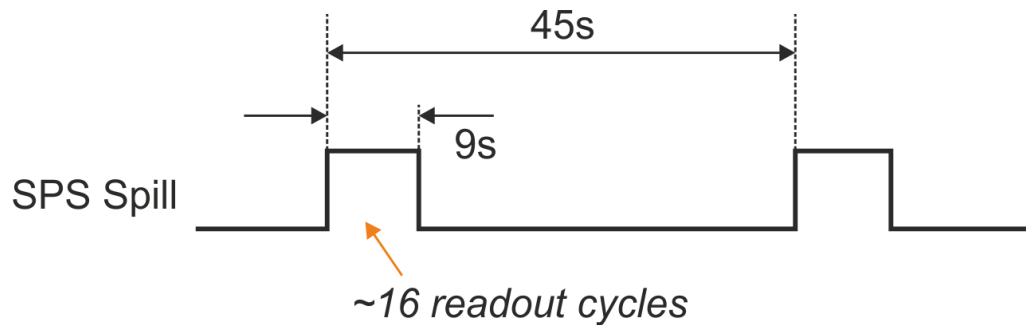
CERN testbeam

High noise on pedestal for first 1-2 readout cycles



Start-Run Problem

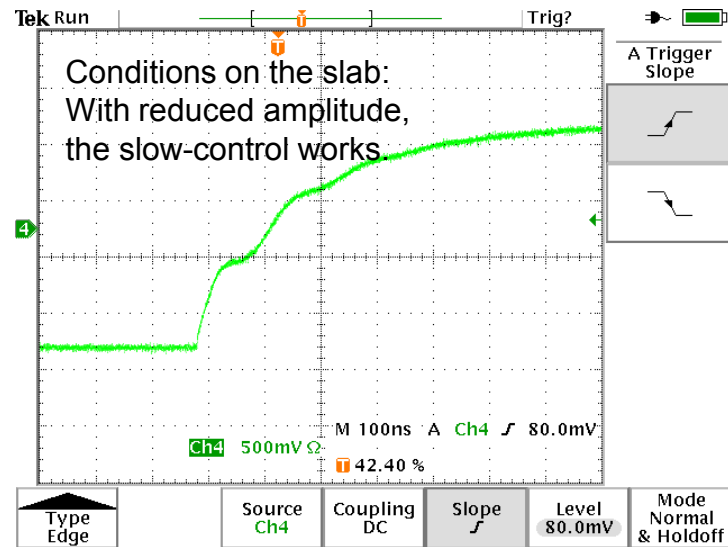
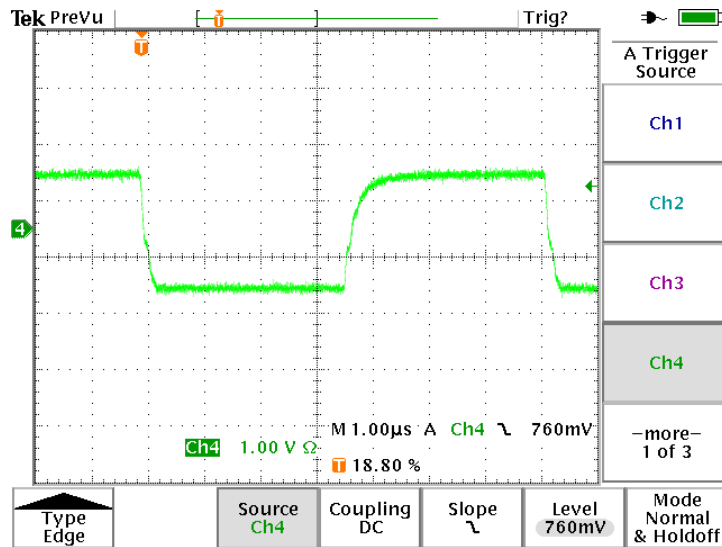
- > Data taking at CERN SPS:



- > When the data taking is interrupted for some time, the following first 1-2 readout cycles show high fluctuations of the pedestal (start-run noise). This can be observed in the lab as well, but only with the special SPILL structure at CERN, this effect impairs data quality (2 of 16 cycles with high noise).

Slow-Control Problem

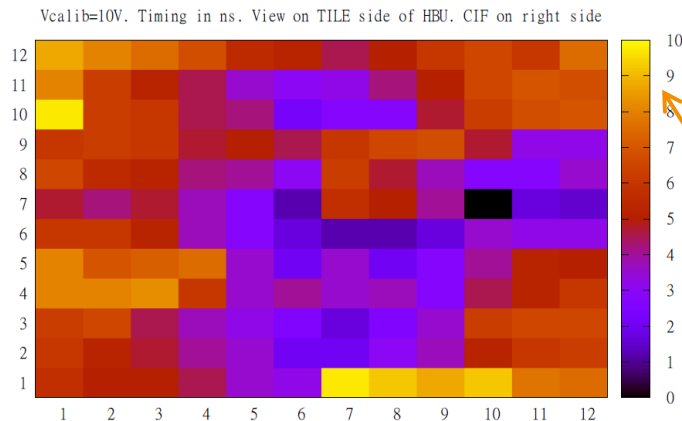
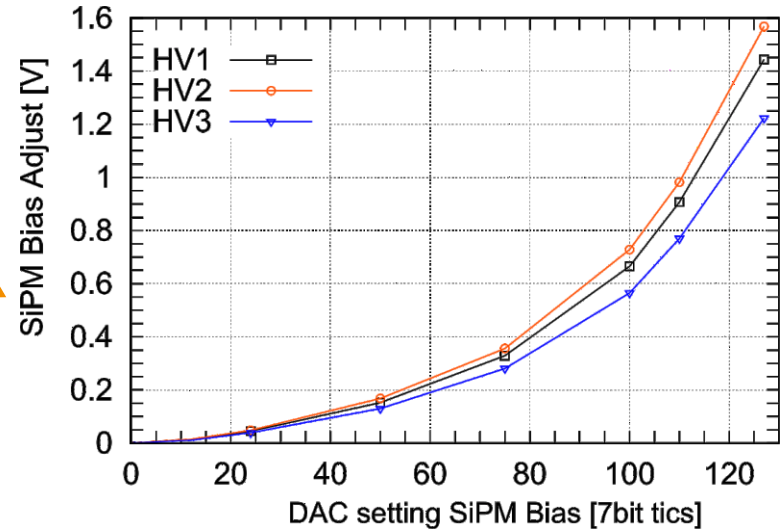
- For longer AHCAL slabs, the slow-control programming is instable. Reason: Slow-control clock, special pulse-shape needed (series R, termination R, block-C)



- Although the slow-clock looks fine, the configuration does not work.
- Analysis ongoing, I2C in SPIROC3.

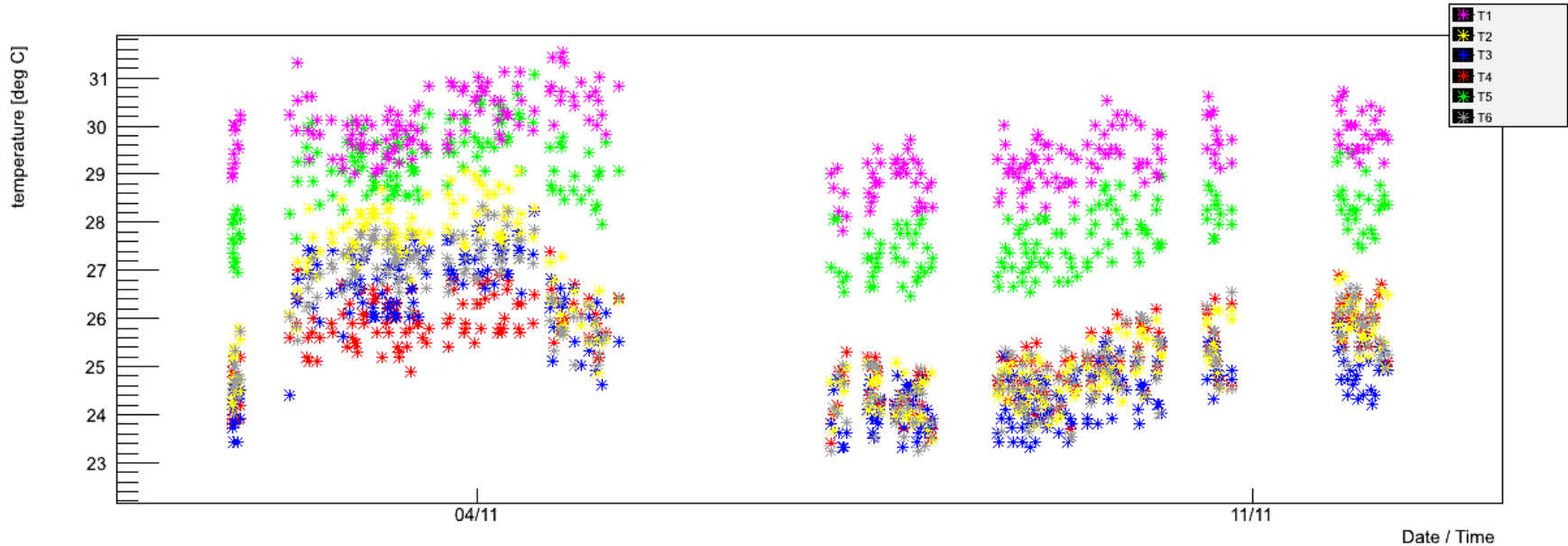
SiPM Bias Adjust, LED ch-to-ch spread, temperature ro

- > The SiPM bias can be adjusted channel-wise by the SP2b inDACs and for all channels altogether (new, 7bit resolution).



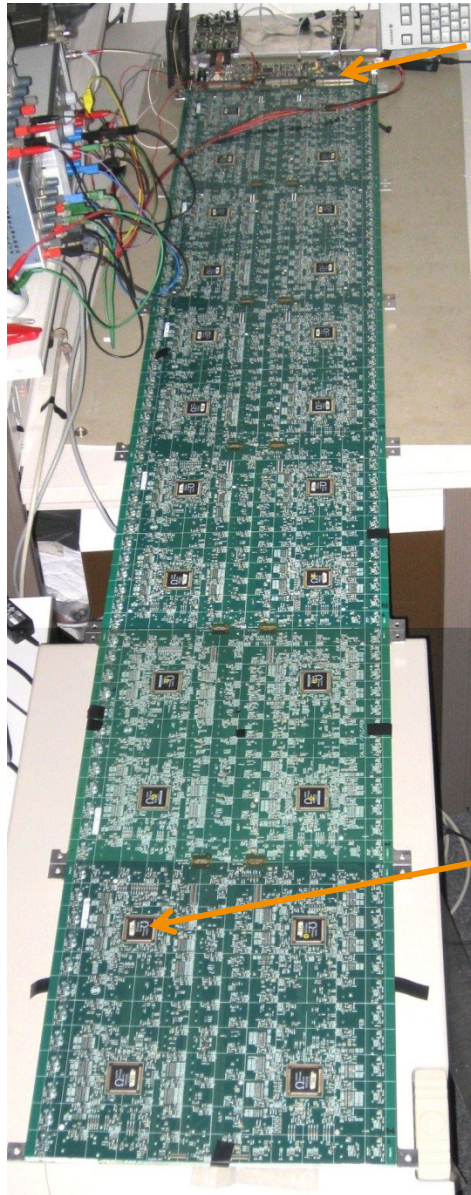
- > The LED system shows large ch-to-ch spread in the switch-on time (up to 10ns). This result has to be analyzed, although this is no problem for SiPM calibration.

Temperature Readout (CERN Module)



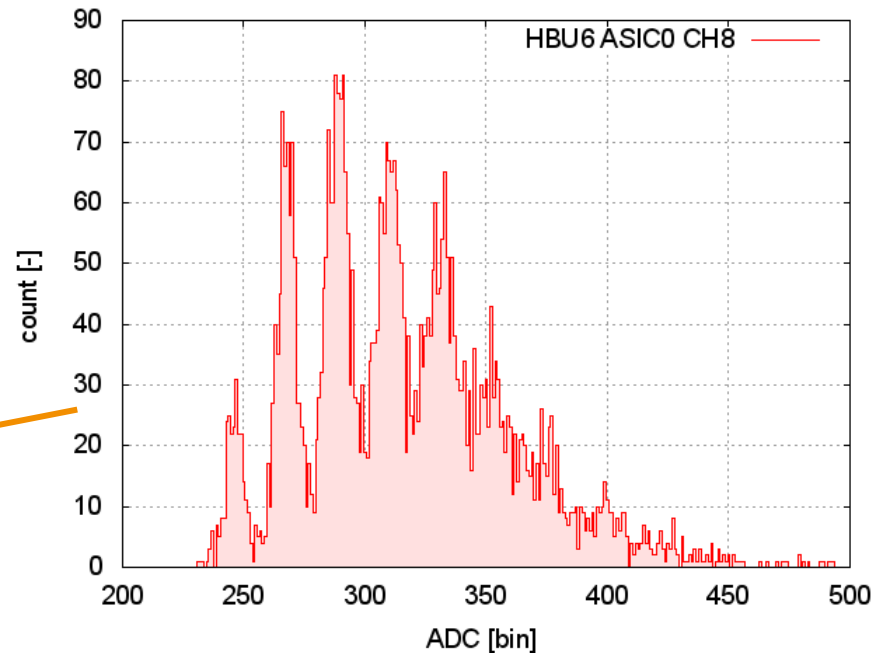
- The temperature sensors on the CERN module show large offsets and fluctuations, because there was no time for a correct commissioning.

AHCAL Full Slab



DAQ

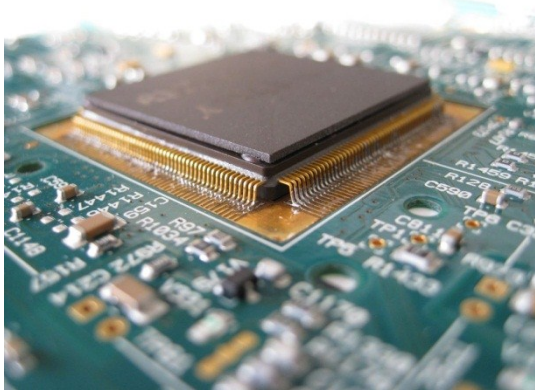
- Since a few days: First operation of a complete slab (2.20m).
- The last HBU delivers nice single-pixel spectra (Prague LED system).



Conclusions

- 2 weeks of data taking at CERN SPS without a single DAQ crash. Valuable data has been taken (see Sebastian's and Oskar's talks).
- Most of the obstacles have been identified, a lot have been corrected already, a few have to be corrected in SPIROC3 and HBU3.

Main future activities to fix SPIROC3 design:



SPIROC2c on HBU2