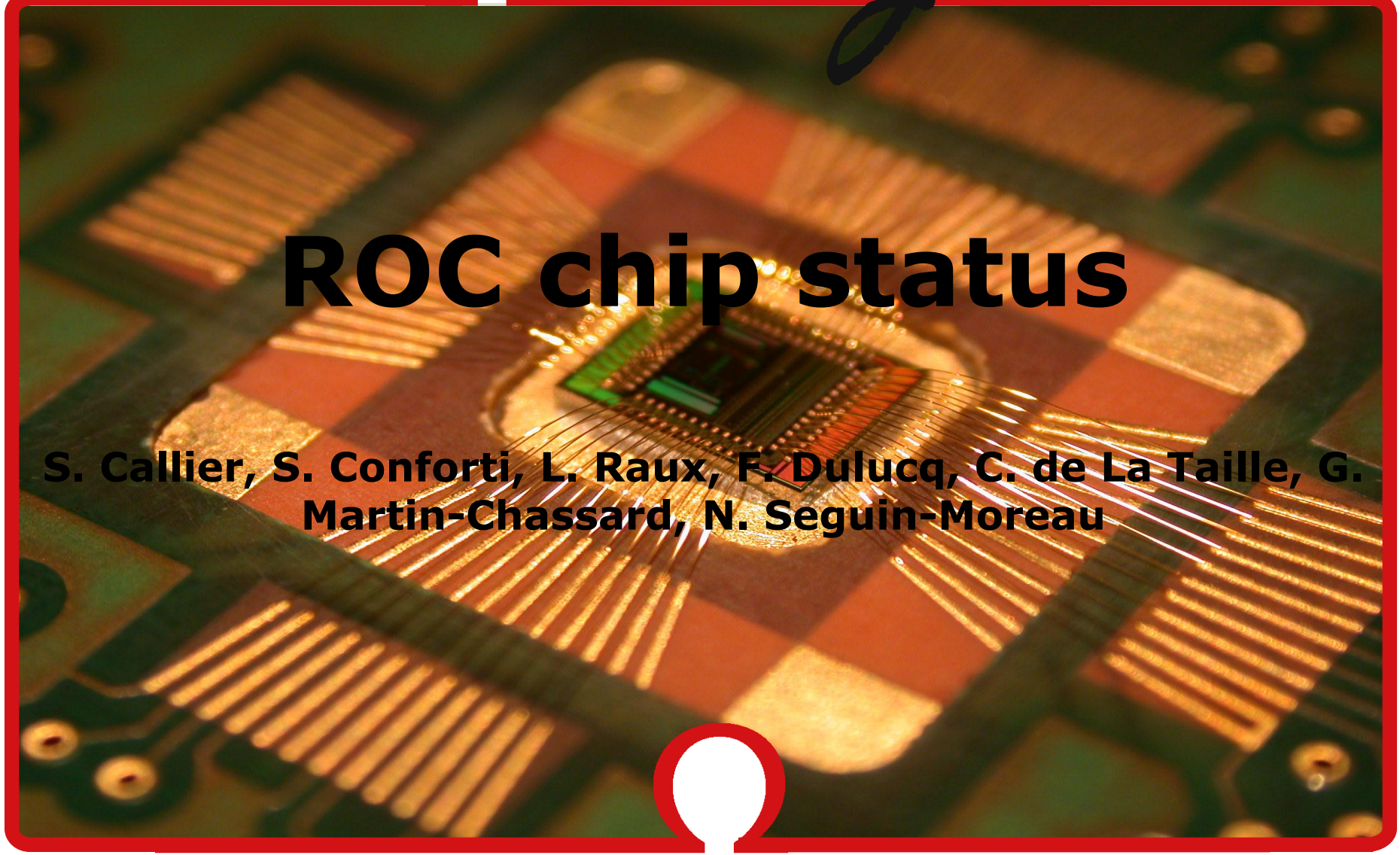


ROC chip status

S. Callier, S. Conforti, L. Raux, F. Dulucq, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau

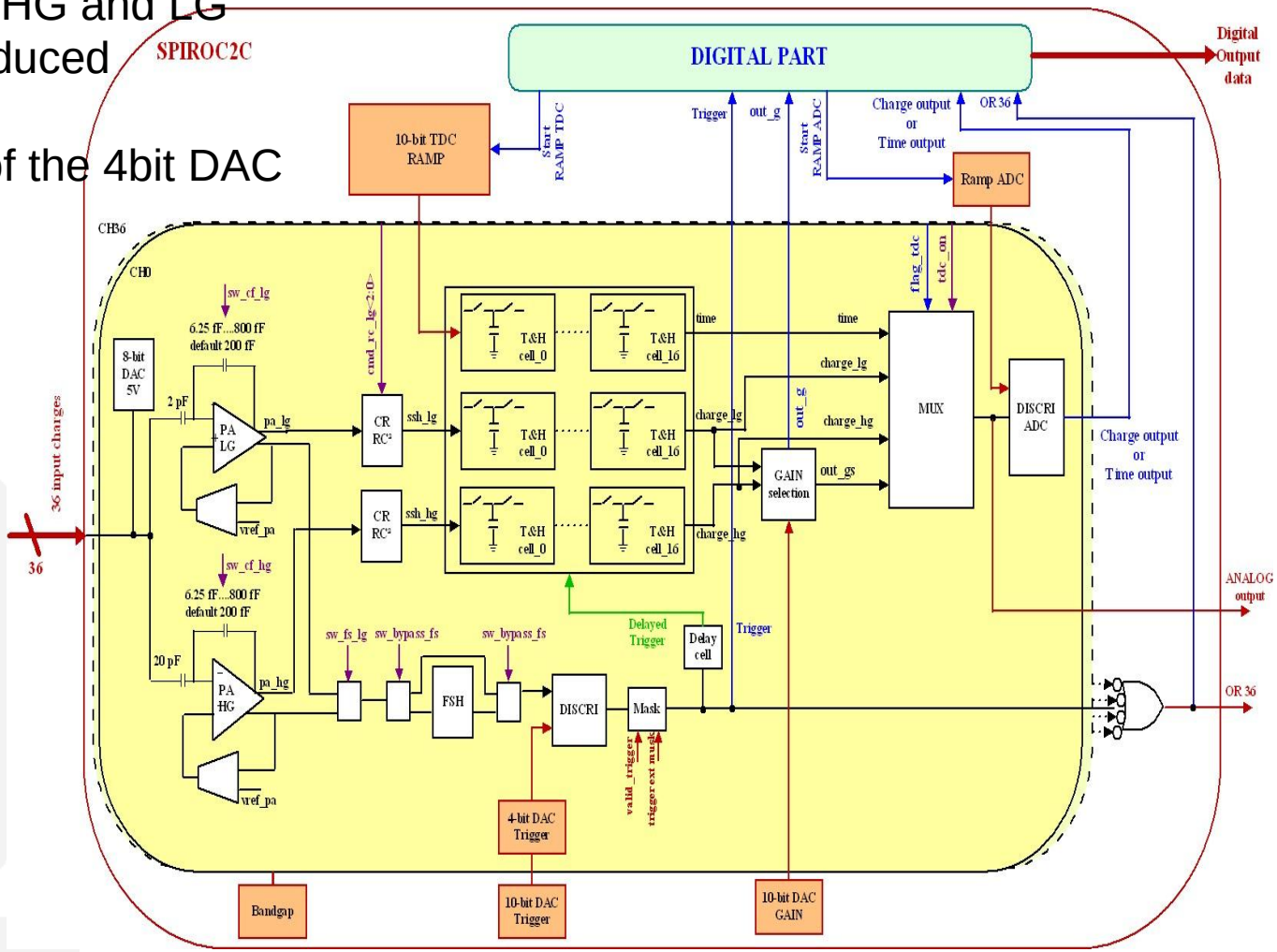
Orsay MicroElectronics Group Associated

Many measurements are still on going on test board and at system level to characterize in detail the ROC chips before submitting 3rd generation chips

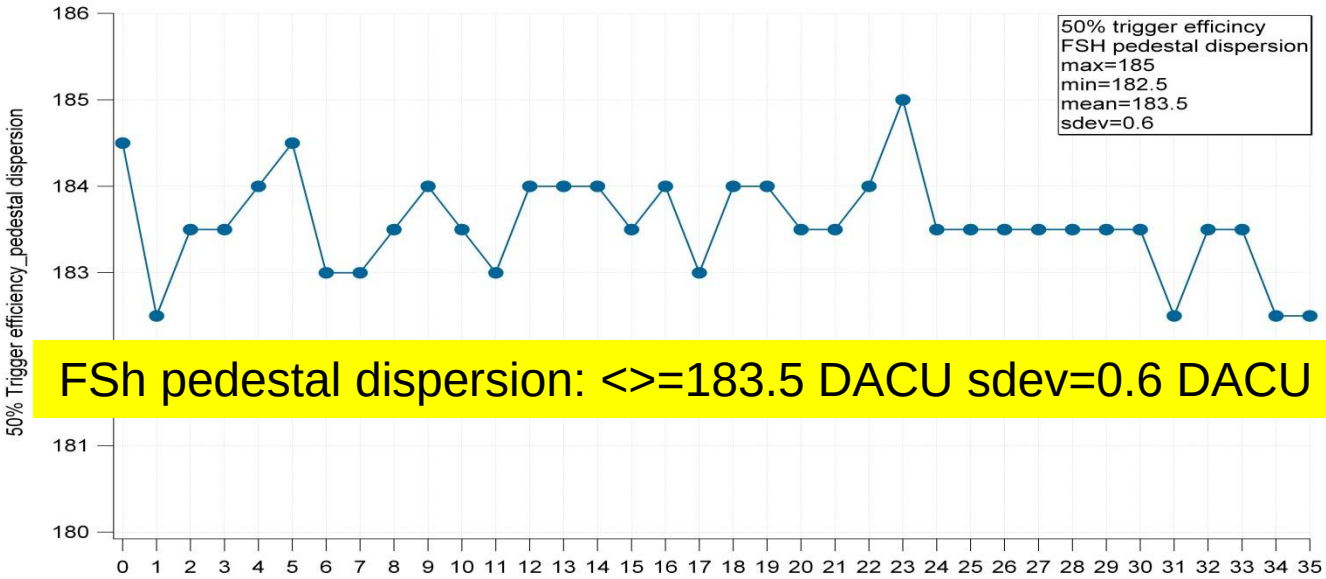
- HARDROC3: will be submitted in Feb 2013
- Many measurements performed on SKIROC2 (see Stephane's talk) and on SPIROC2B and 2C
- SKIROC2 and SPIROC2B/2C are the same except for the input preamplifier: same fast and slow channel, same digital part.

SPIROC2C

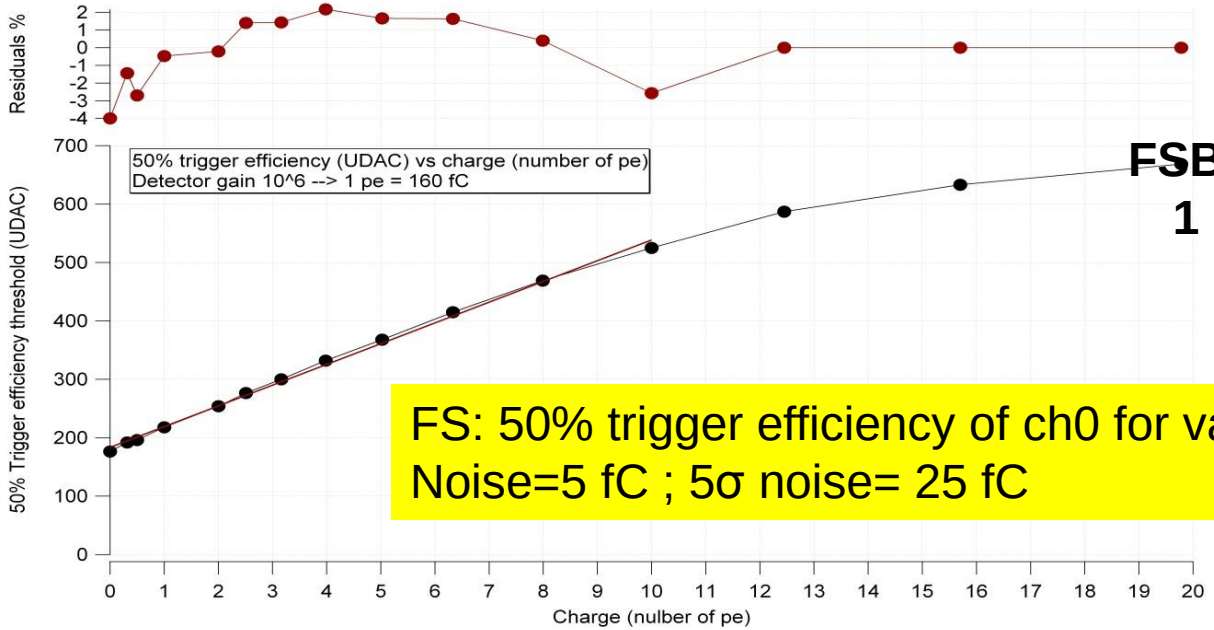
- Same pinout as Spiroc2b
- New input PA
- Independant Cf for HG and LG
- HG/LG coupling reduced
- New delay box
- Better distribution of the 4bit DAC



SPIROC2C: FS Uniformity (HG=200; LG=100)



FSh pedestal dispersion: <>=183.5 DACU sdev=0.6 DACU

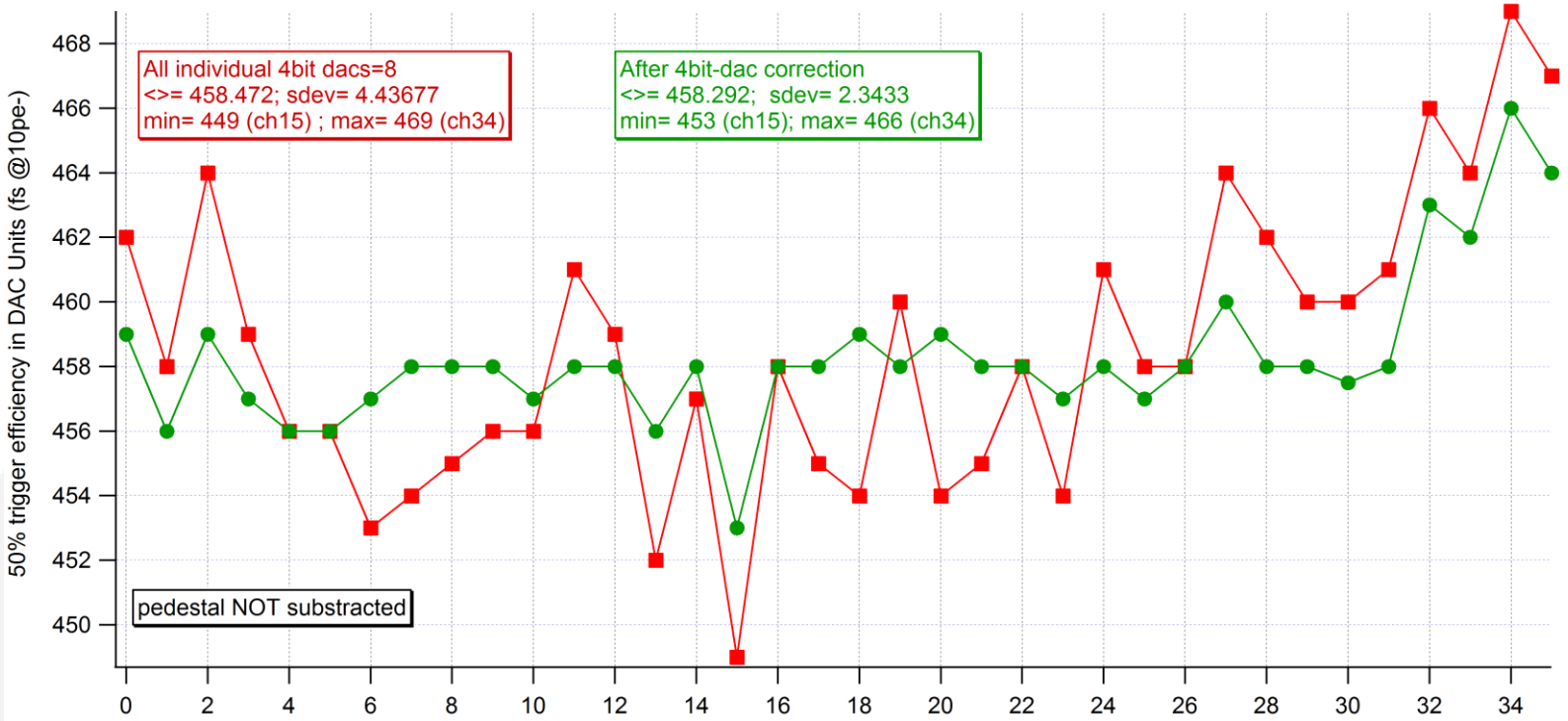


FSB = 30 DACU/pe
1 DACU ~ 2mV

FS: 50% trigger efficiency of ch0 for various injected charge.
Noise=5 fC ; 5σ noise= 25 fC

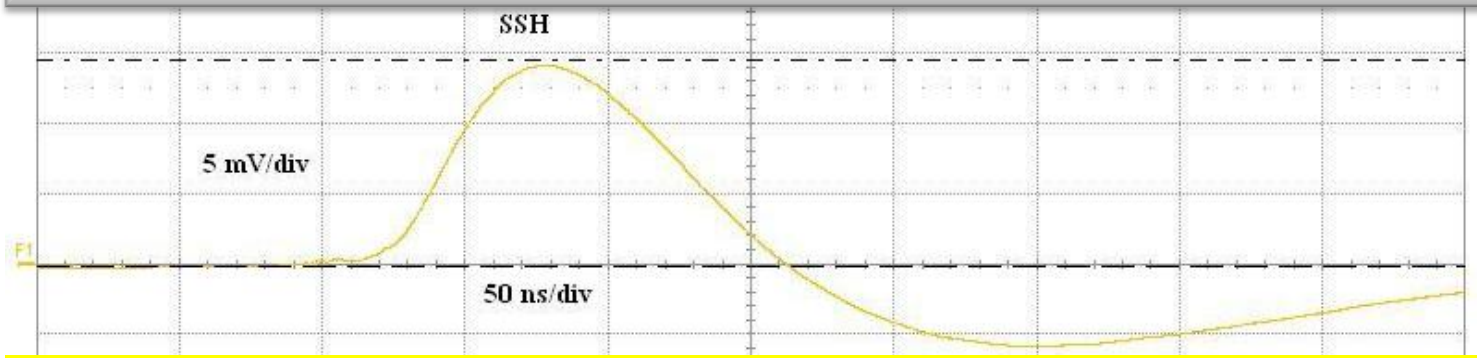
SPIROC2C: 4-bit DAC channel wise tuning

FS@ 10 pe injected

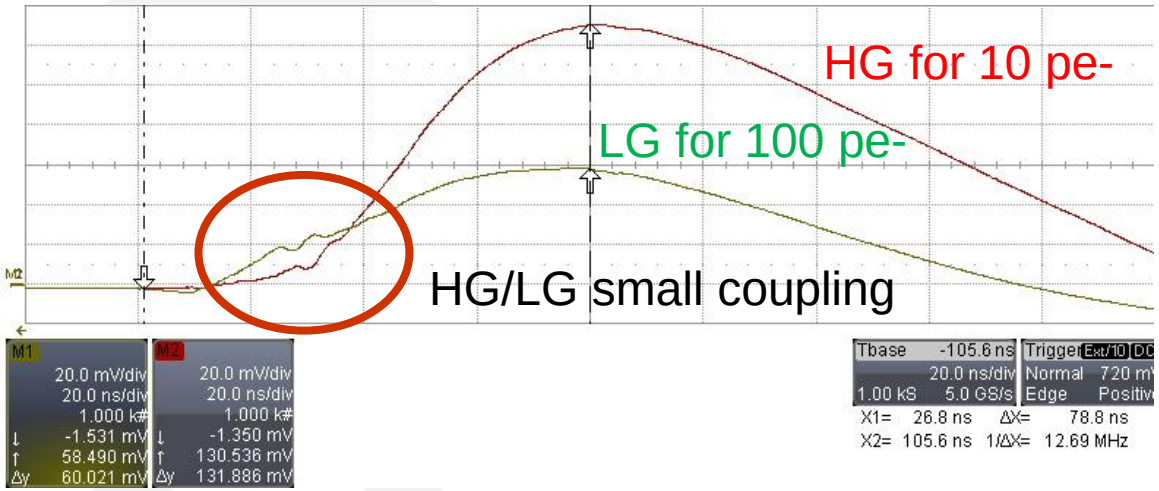


SPIROC2C: HG and LG slow shapers

PA_HG=bit100 x 6.25fF= 625fF => G=20pF/625fF= 32 => dyn range up to 100 pe-
PA_LG=bit200x6.25 fF=1.25pF => G=2pF/1.25pF= 1.6 => dyn range up to 1500 pe-

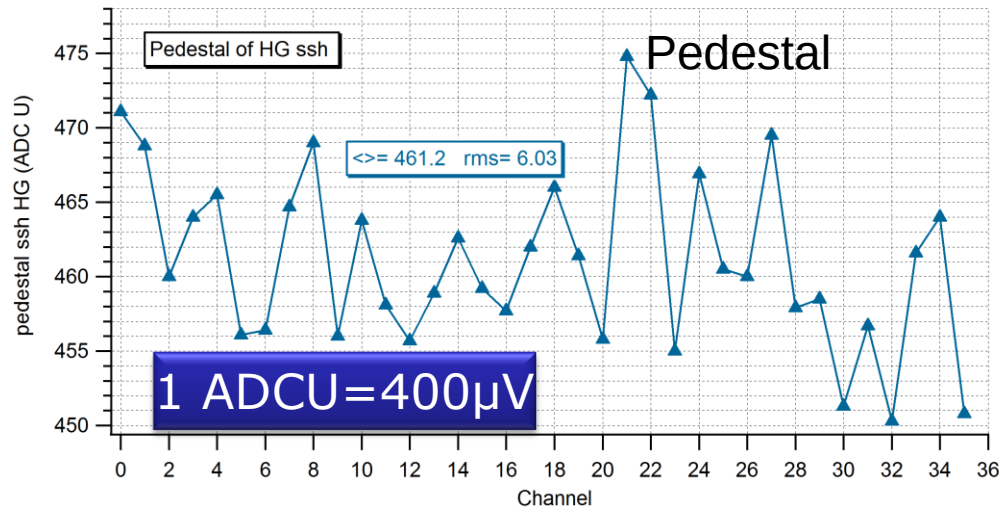


HG SSh: Vmax= 14.65 mV/pe (1pe=160 fC) RMS noise = 1.2mV = > SNR ~ 12

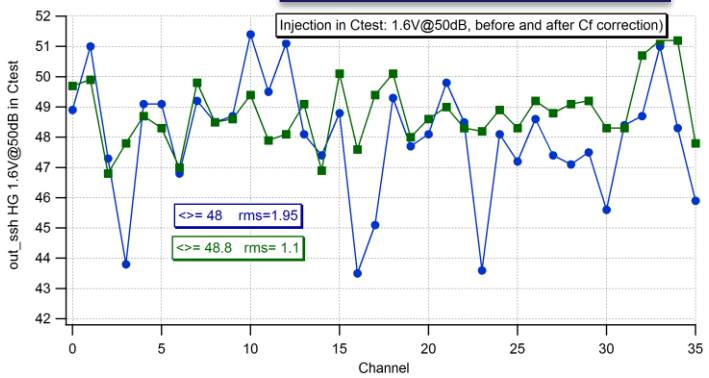


tp HG,LG ~50 ns

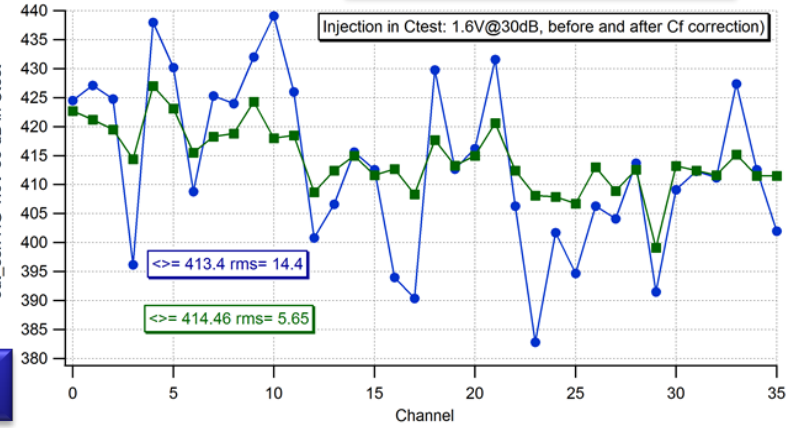
HG SSH UNIFORMITY BEF. and AFTER Cf cor.

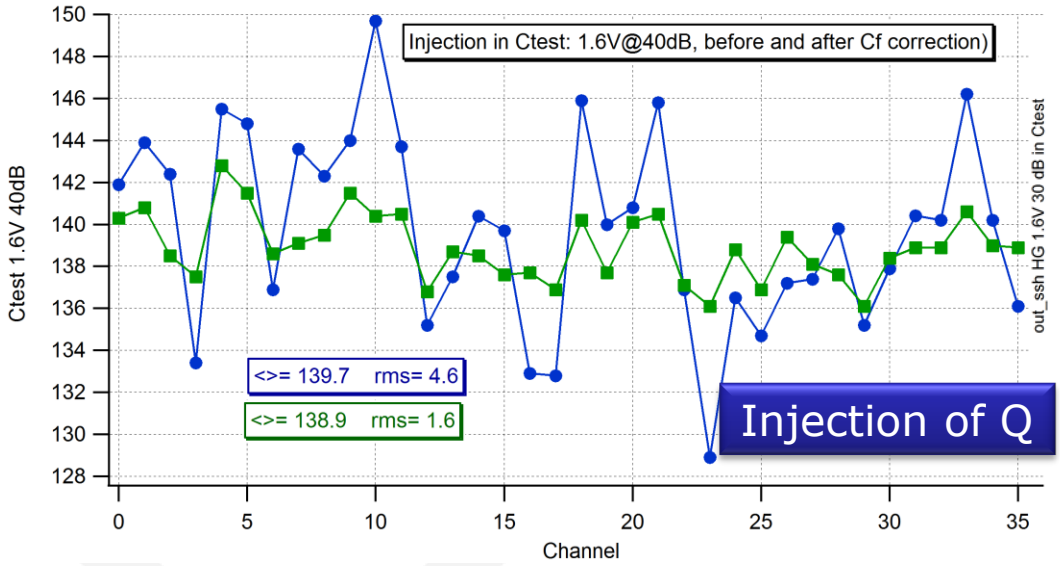


Injection of Q/3



Injection of 3xQ

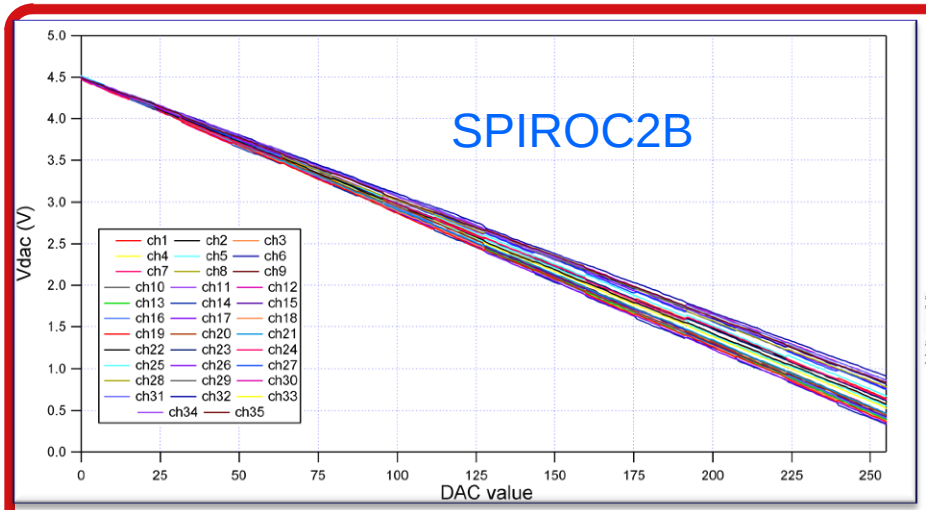


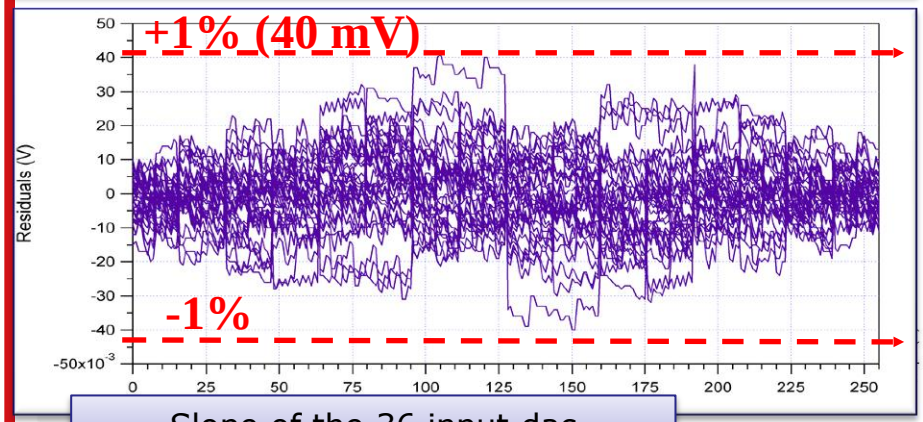


Injection of Q

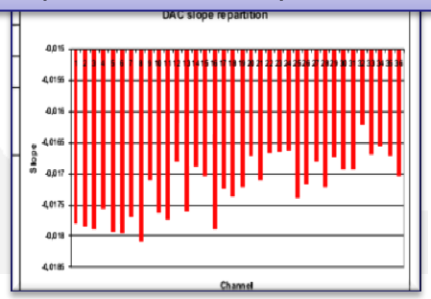
Uniformity for 3 injected charges (Q, Q/3 and 3*Q), using the same gain correction

8-bit input DAC linearity

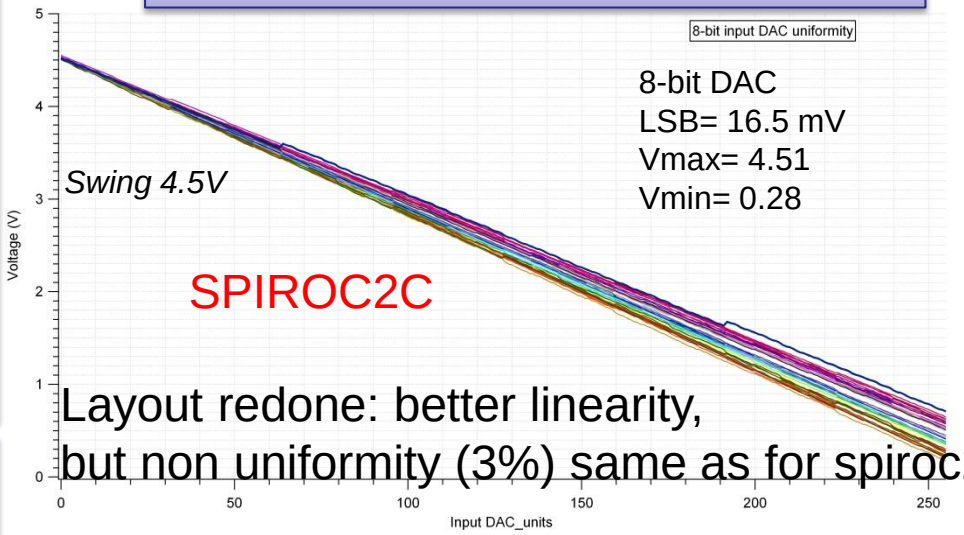




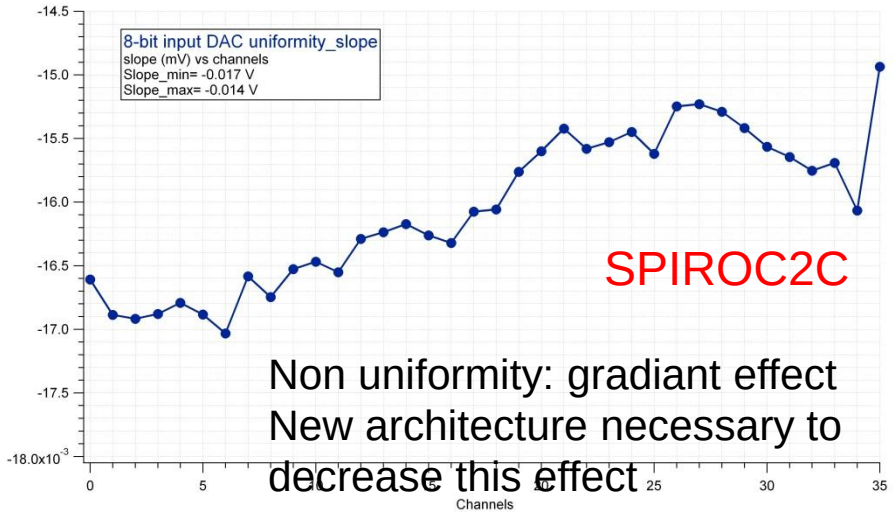
Slope of the 36 input dac



Linearity of the 36 input dac



Layout redone: better linearity,
but non uniformity (3%) same as for spiroc2b



Non uniformity: gradiant effect
New architecture necessary to decrease this effect

Slope of the 36 input dac

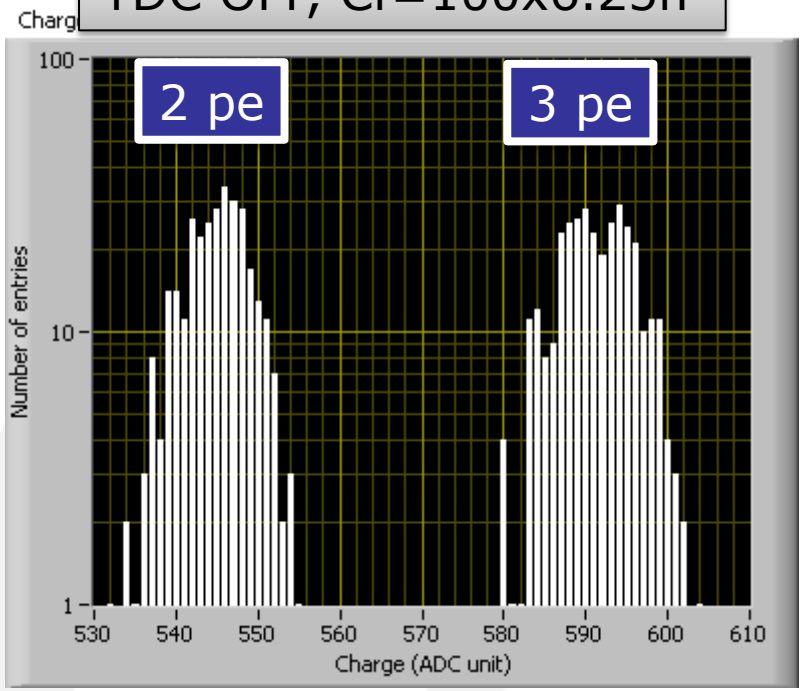
Spiroc2c: Digital coupling with G hg_ssh=100

Acquisition using the autotrigger mode

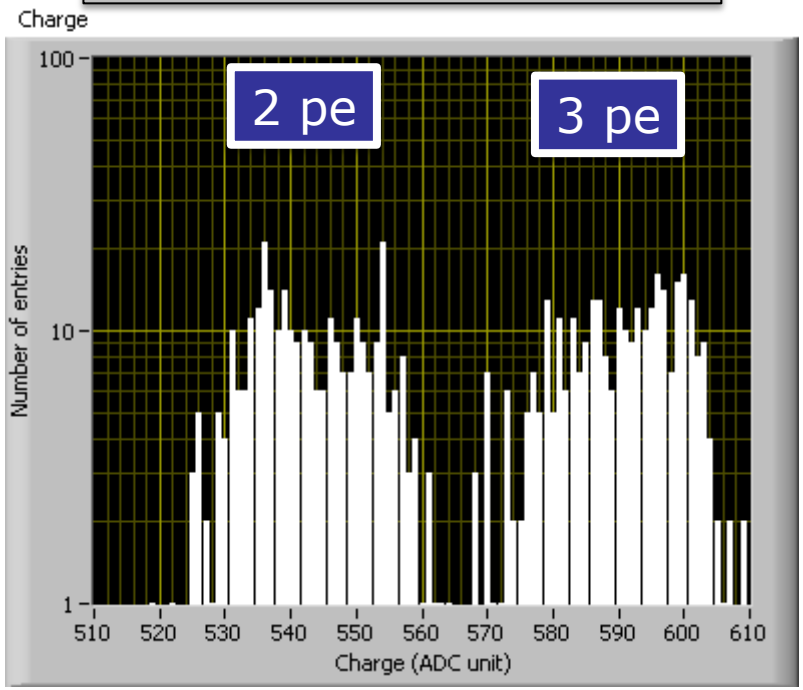
1 ADCU= 400 µV

Injection through 100pF, **2 and 3 pe- pe-** , HG Ssh @ 50ns
HG: G=100 (Cf=100x 6.25fF) for all the channels,
Vth=230 (=1.7 pe-)

TDC OFF, Cf=100x6.25fF



TDC ON, G=100x6.25 fF

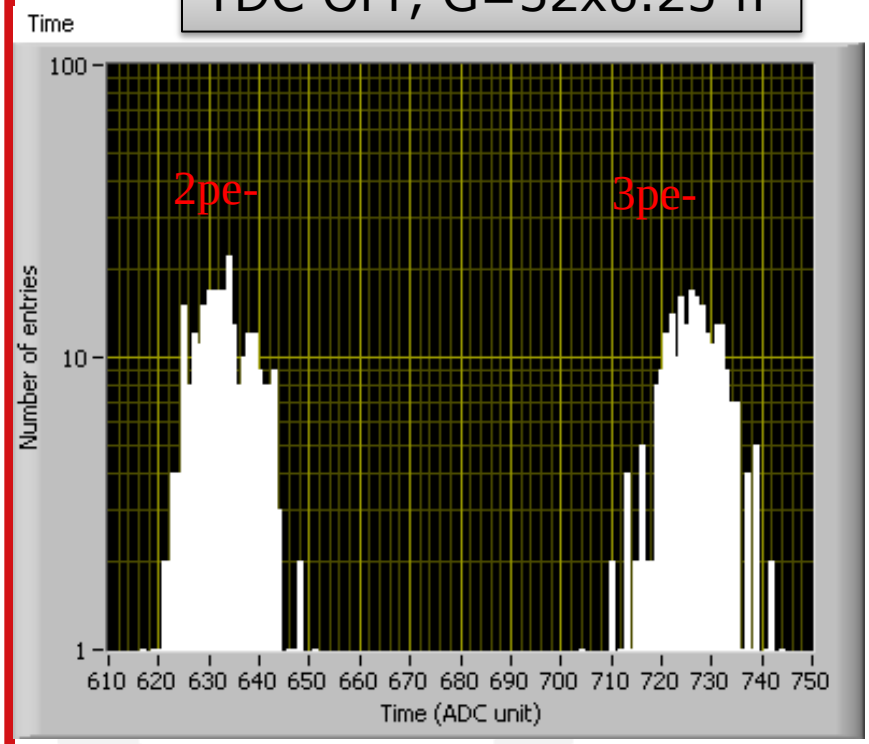


TDC => digital coupling in spiroc2c through the substrate (NMOS preamp connected to gnd)
There is no digital coupling in spiroc2b (PMOS transistor connected to vdd)

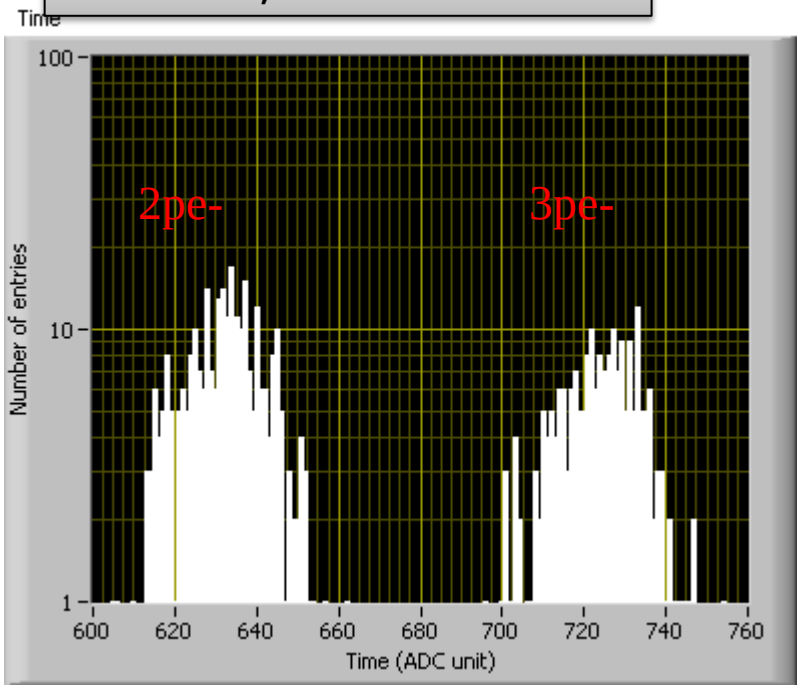
Digital coupling in Spiroc2c with G hg_ssh=32

Injection through 100pF, **2 and 3 pe- HG with G=32 (32x6.25fF)** for all the channels, ssh@50ns
Vth=260 (~1pe-)

TDC OFF, G=32x6.25 fF

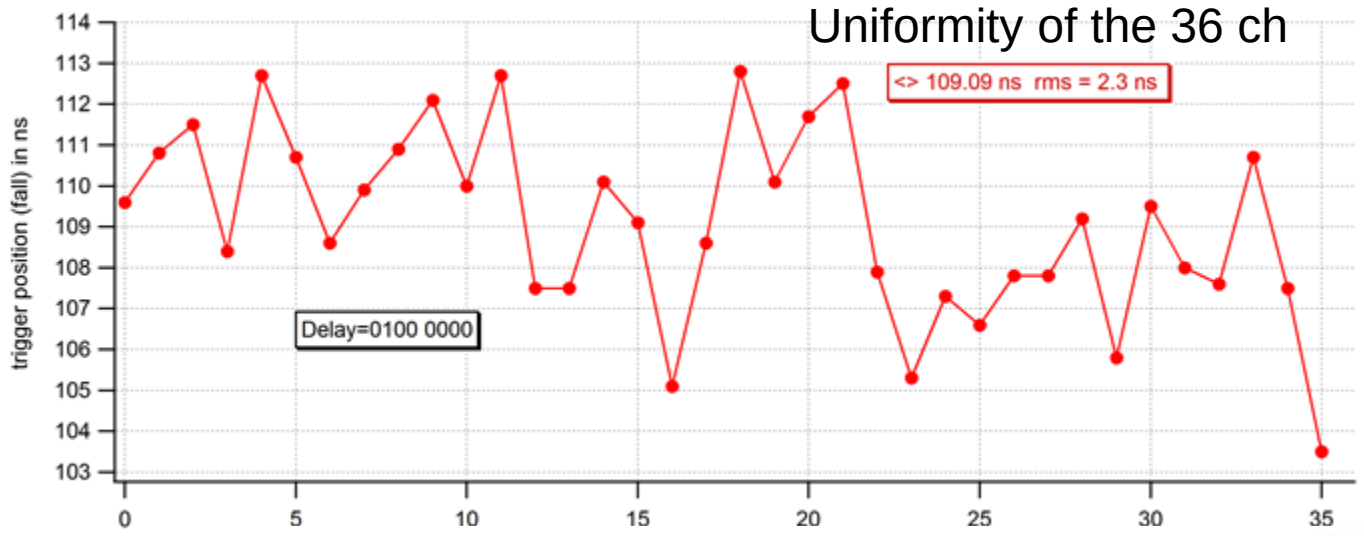


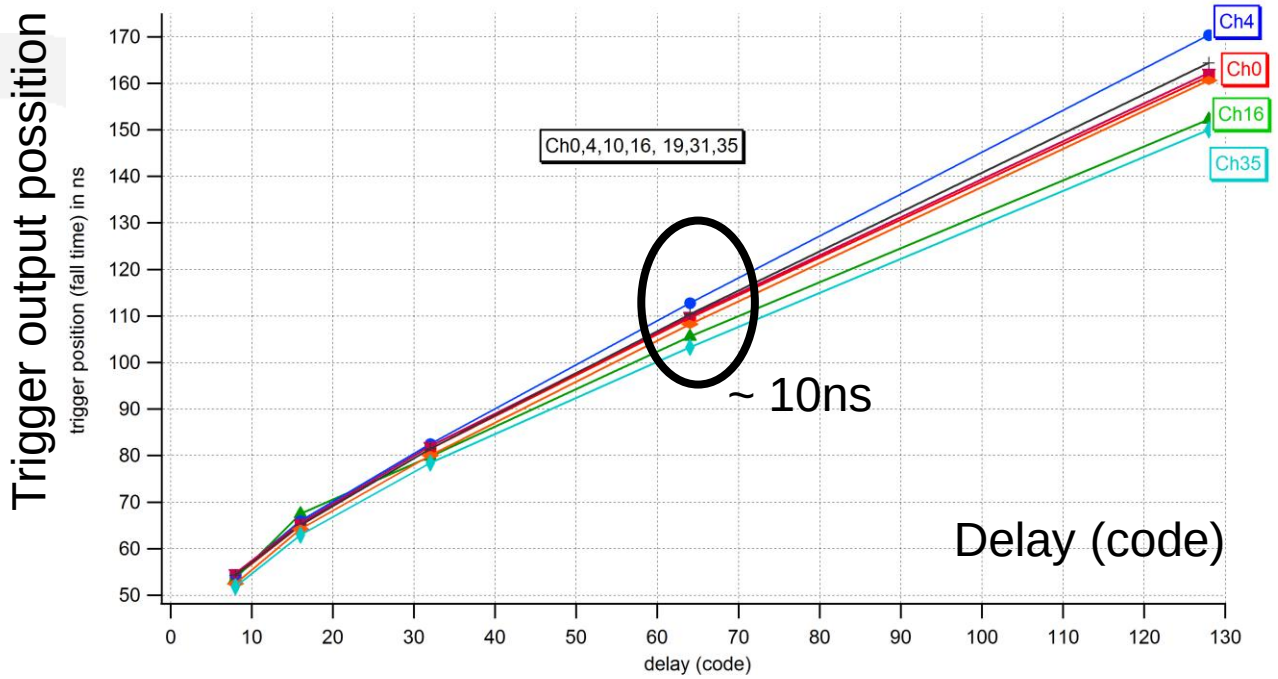
TDC ON, G=32x6.25 fF



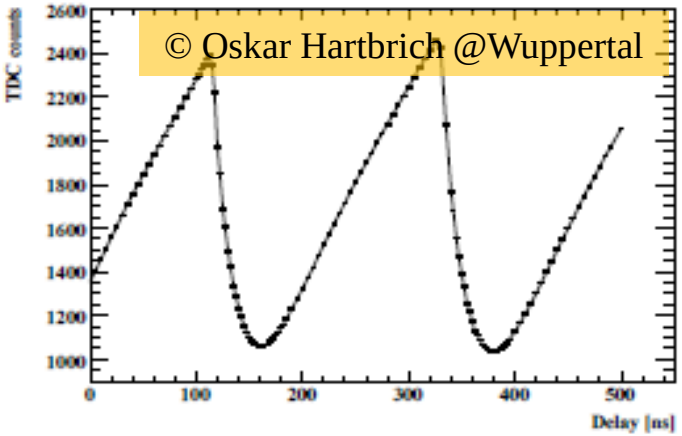
TDC coupling in Spiroc2c doesn't prevent to distinguish 2 and 3 pe-

DELAY BOX

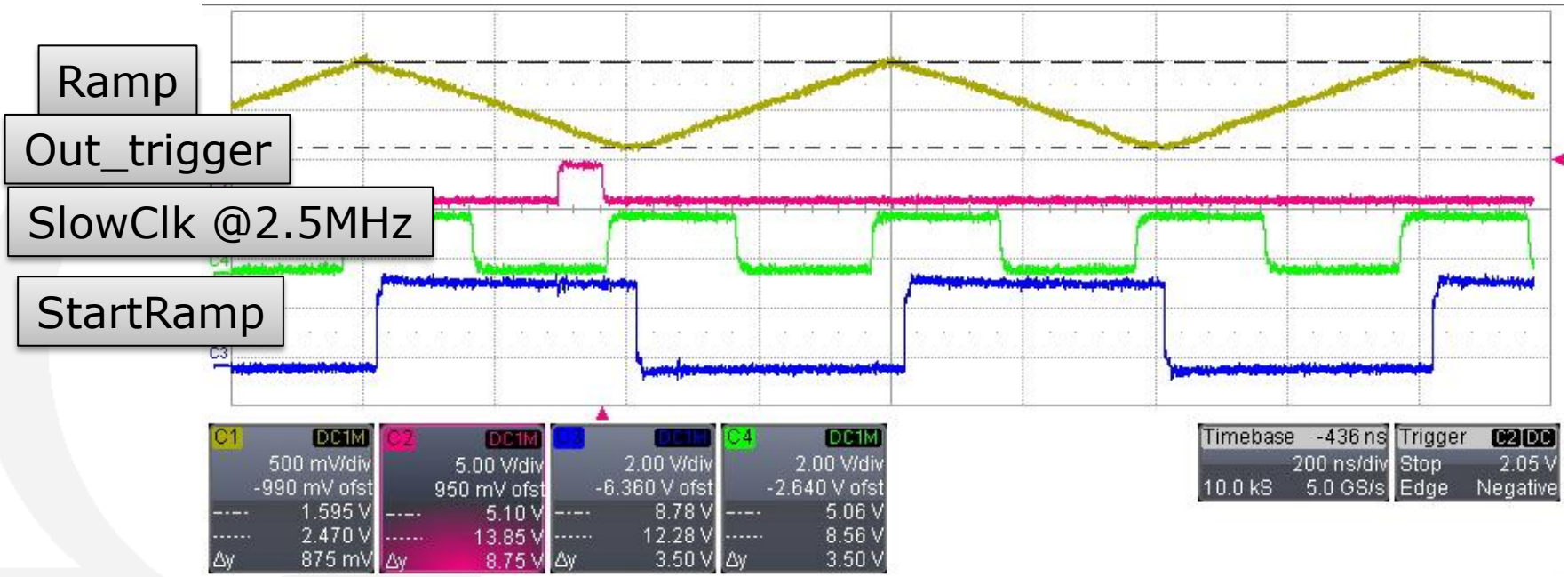

Uniformity of the 36 ch
<> 109.09 ns rms = 2.3 ns
Delay=0100 0000
trigger position (fall) in ns


Trigger output possition
trigger position (fall time) in ns
Ch0,4,10,16, 19,31,35
Ch4
Ch0
Ch16
Ch35
~ 10ns
Delay (code)
delay (code)

- SPIROC2B TDC: Dead time due to the mutiplexer

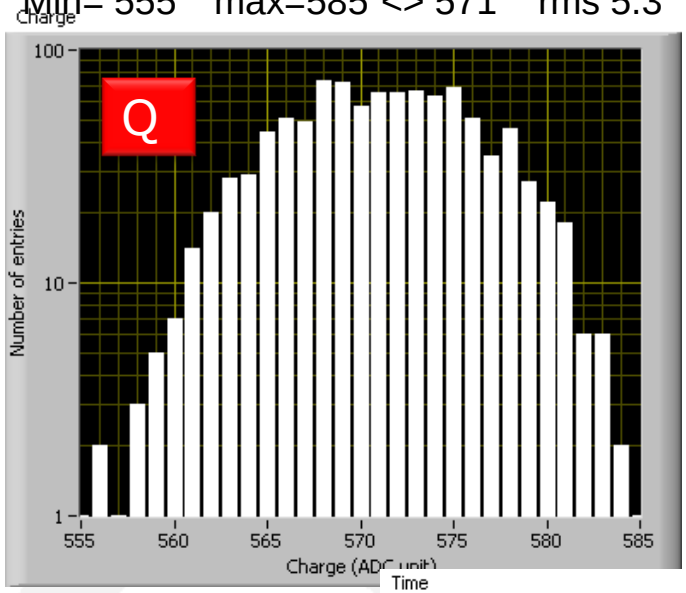


- SPIROC2C TDC
  - To decrease dead time during transition => alternation of a rising and a falling ramp implemented
  - Conservative modification

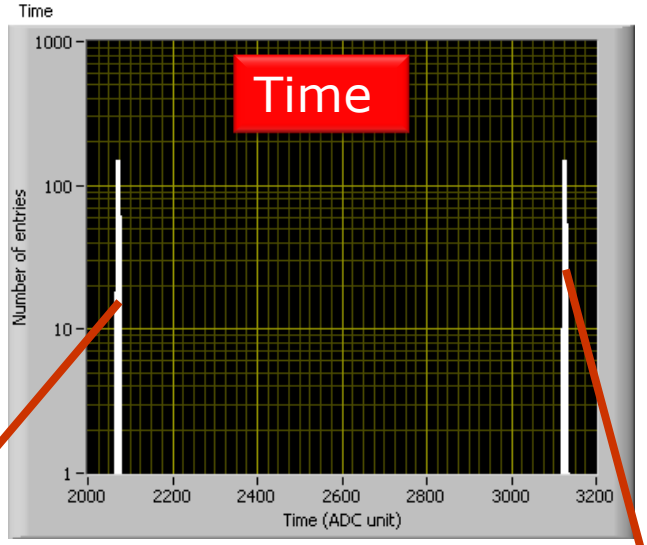


- 3 pe- injected in one channel

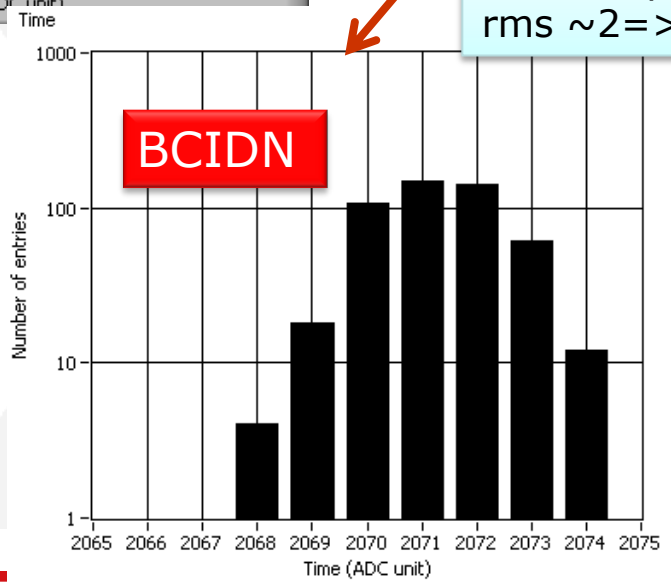
Min= 555 max=585 <> 571 rms 5.3

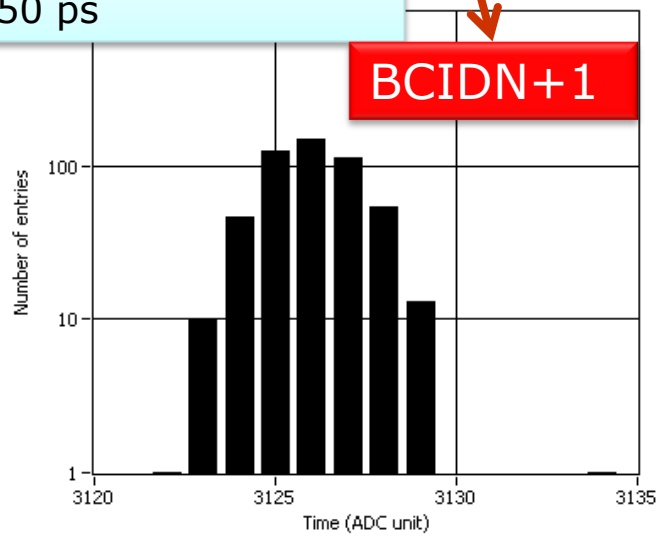


Min=2068 Max=3134

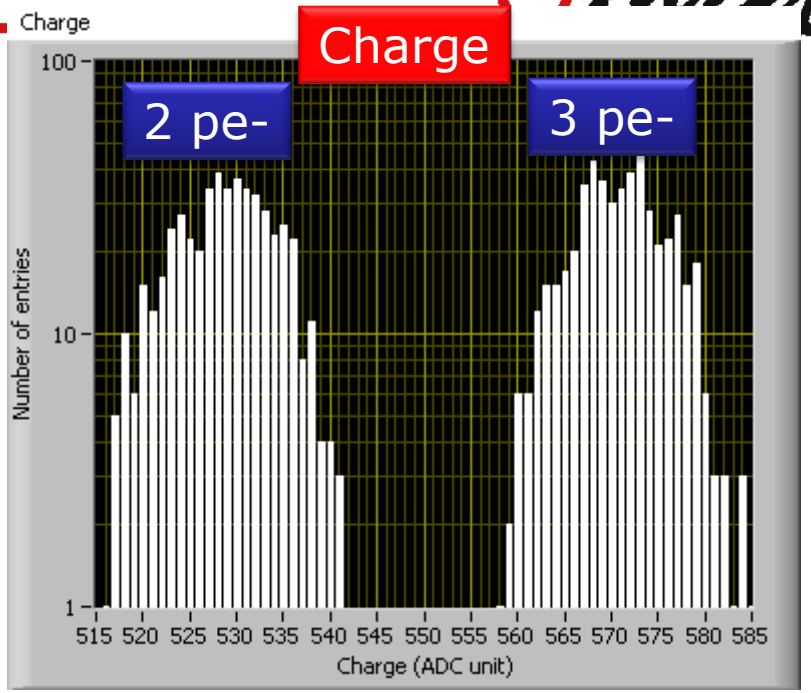


TDC ramp 400ns , 5.8 ADCU/ns
rms ~2=> 350 ps

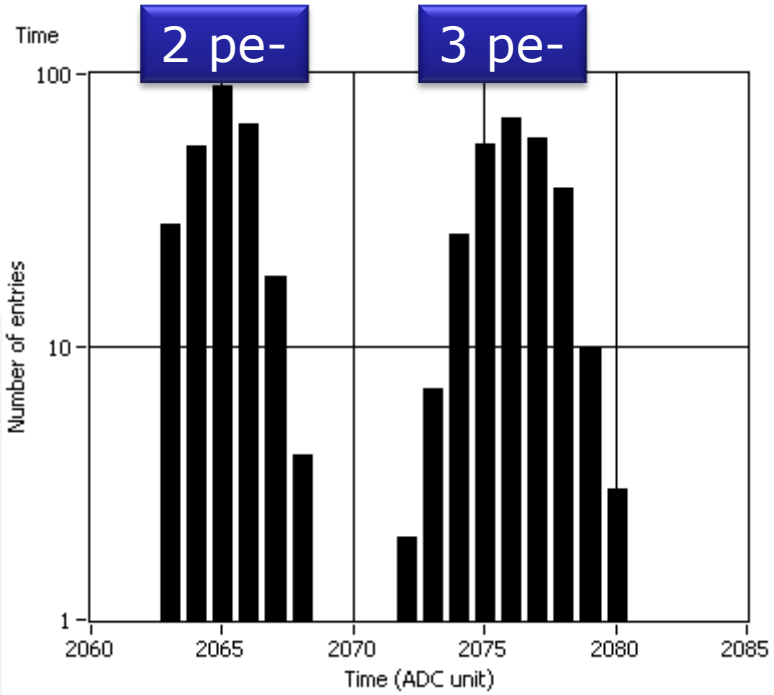




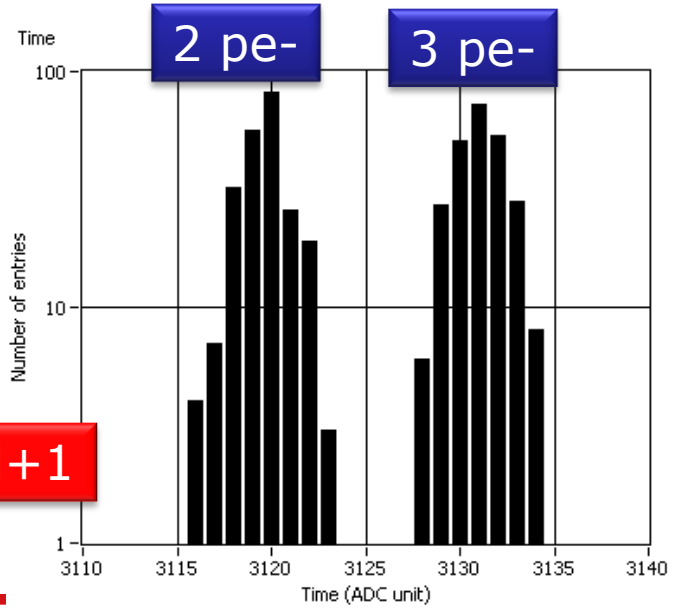
- 2 and 3 pe- injected in one channel



Time, BCID N



Time, BCID N+1



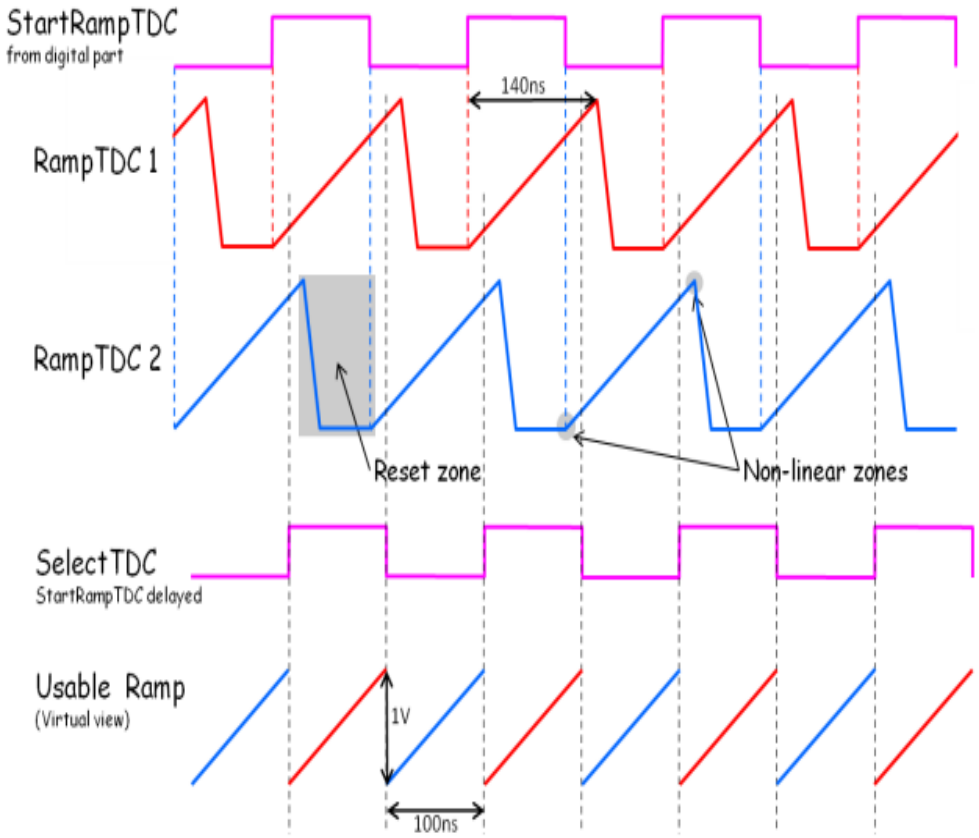
TDC for SPIROC3: PARISROC TDC ramp ?

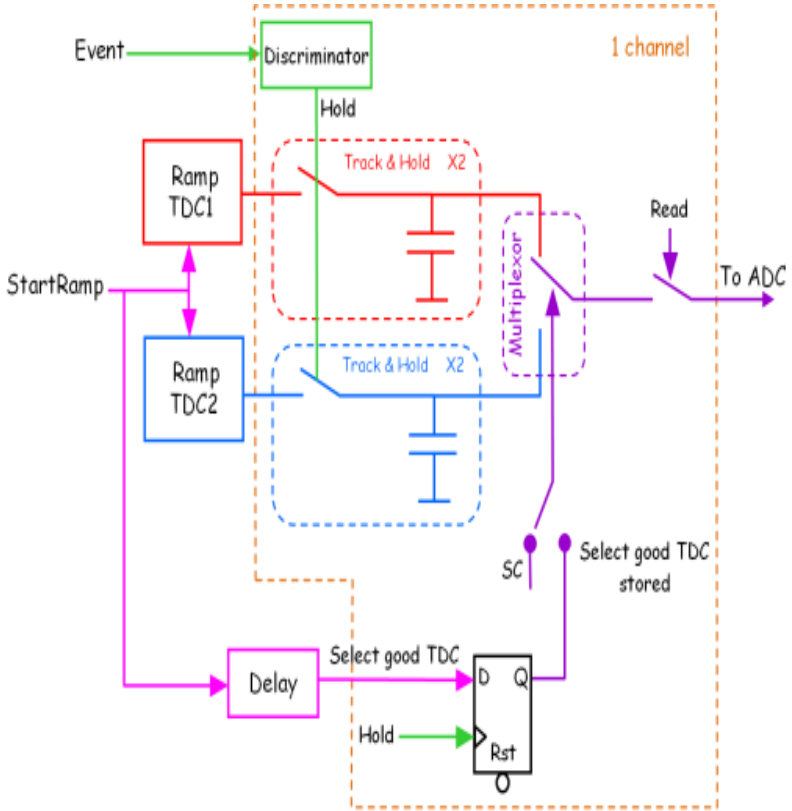
tested by IPNO team

2 independent ramps and an overlap between them to minimize dead time.
Sampled at the same time
Internal module to tag the valid ramp

1. Coarse time by 24-bit gray counter
- working at 10 MHz
- with 1.67 s of dynamic
- 100 ns steps

2. Fine time by analog TDC
- 100 ns dynamic
- 100 ps step



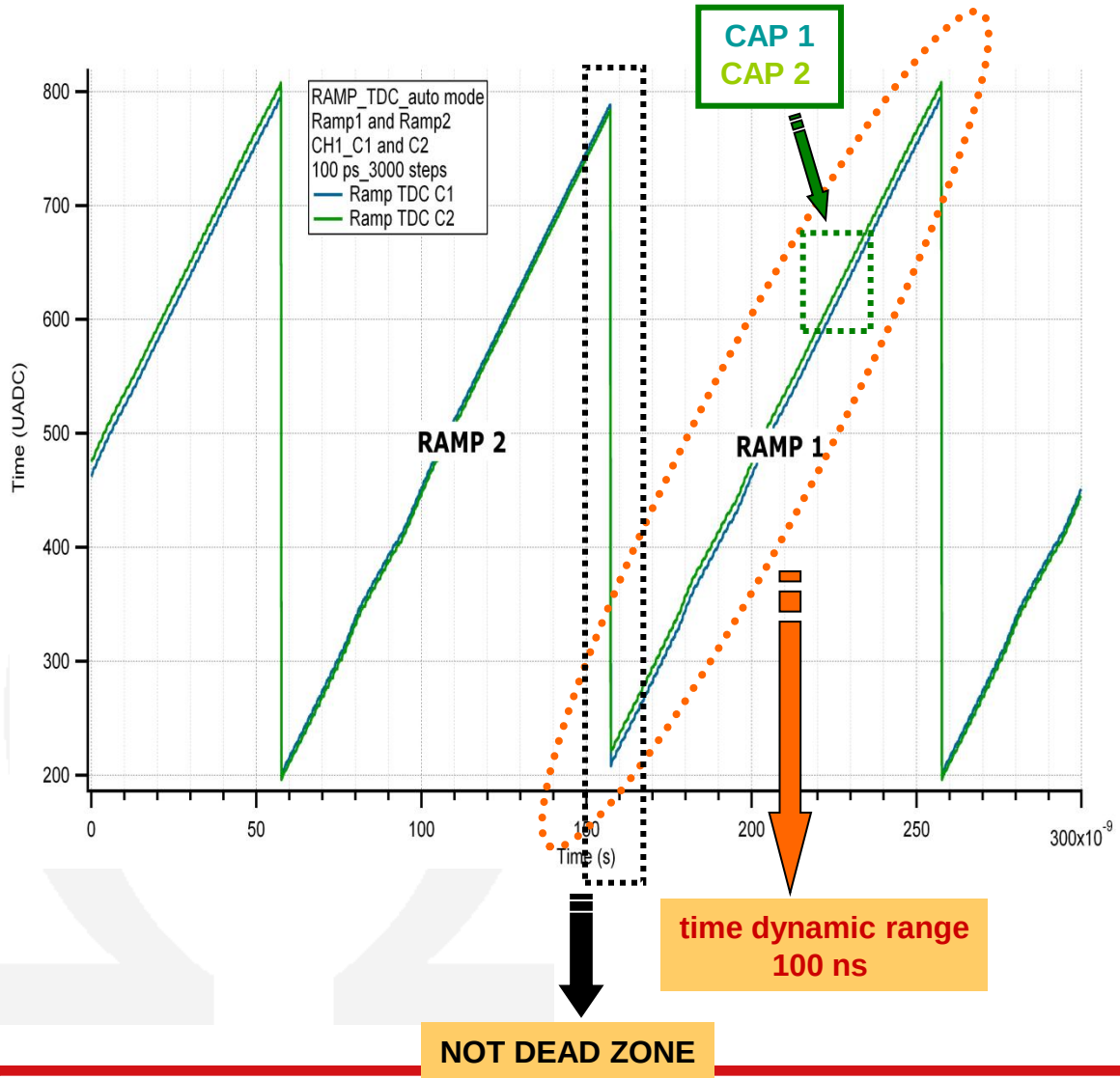


PARISROC TDC ramp

tested by IPNO team

Reconstruction of the ramp from the time values saved in the analog memory and converted by the ADC (10-bit).

The validation of the good ramp is made automatically



	Second version
Time dynamic range	100 ns
"Blind zone"	0
linear zone	100 ns
Ramp 1 linear	± 1 ns
Ramp 2 linear	± 1 ns

Complex chip (internal SCA, ADC, TDC)

- Many bugs corrected + new features in SPIROC2c:
  - HG/LG coupling
  - Independent Cf for HG and LG
  - 4-bitsDAC
  - Delay box
  - Rate dependency
  - Pedestal shift (to be checked by DESY)
  - Zero events
- Still improvements to be done:
  - 8-bit input DAC: to be improved
  - NMOS or PMOS preamp? = digital coupling vs pedestal shift
  - TDC
- HBU with spiroc2c to be tested
- I2C link: feedback from HR3 necessary

ROADMAP of 3rd generation chips

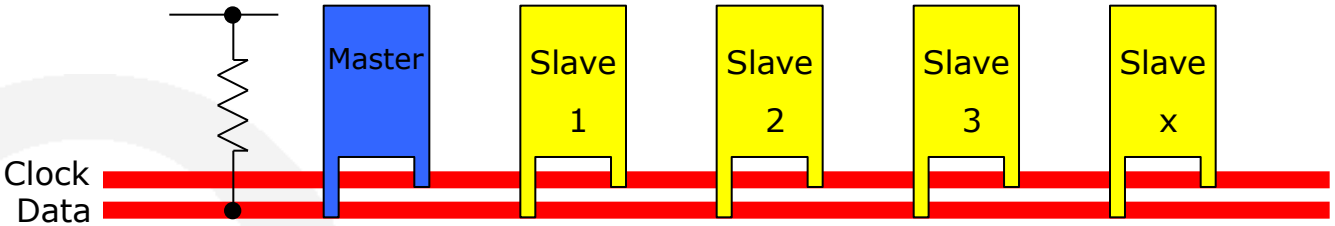
- **HARDROC3**
  - First of the "3rd generation ROC chip" to be submitted
  - **independent channels**, one register/channel, I2C link for SC parameters(@IPNL), triple voting, circular memory, temperature sensor
  - Digital part finished in July 2012
  - Analog part: No major modifications in the analog part. Extension of the dynamic range to set Vth0=100fC Vth1=5pC and Vth2 > 15 pC
  - Die size ~30 mm2
  - Submission in FEB 2013=> reception in June 2013.

- **Next: SPIROC3 or SKIROC3 ?**
  - Still many tests to be done at the system level/testbeam
  - Hardroc3 test feedback necessary before submitting Spiroc3/skiroc3
  - Spiroc3= 36 channels, 8.5 x 5 mm2 => 42.5 k€ in MPW run
  - Skiroc3= 64 channels, 8.5x9.5 mm2 => 81 k€ in a MPW run => dedicated run mandatory
  - SPIROC3 and SKIROC3 in Feb 2014 in a dedicated run (AIDA, CALICE and other partners)

BACK UP Slides

3Gen ROC chips: common features

- Slow control parameters:
  - Backward compatibility with 2Gen ROC chips slow control
    - Use of classical shift register slow control
  - Embedded I2C
    - 7-bit address + 1 general call address (127 chips can be addressed)
    - Access port doubled
    - Bidirectional data line with open collector (Driver will be the same as Dout)
  - Read back capability of SC bits (non destructive)



- Write frame:

- Read frame:

3Gen ROC chips: common features

- Extra pin needed for I2C / SC:

HARDROC 2		HARDROC 3	
ShiftReg_In	1	ShiftReg_In	1
ShiftReg_Out	1	ShiftReg_Out	1
ShiftReg_Clk	1	ShiftReg_Clk	1
ShiftReg_Rst	1	ShiftReg_Rst	1
		ShiftReg_Loadb	1
		ShiftReg_ReadBack	1
		Error_Triple_Voting	1
		7-bit I2C @	7
		2 x (SCL / SDA)	4
		Select_I2C_Port	1
		Clk_I2C_SR	1
		Rstb_I2C	1
		Select_I2C_SR	1
Total	4	Total	4+18

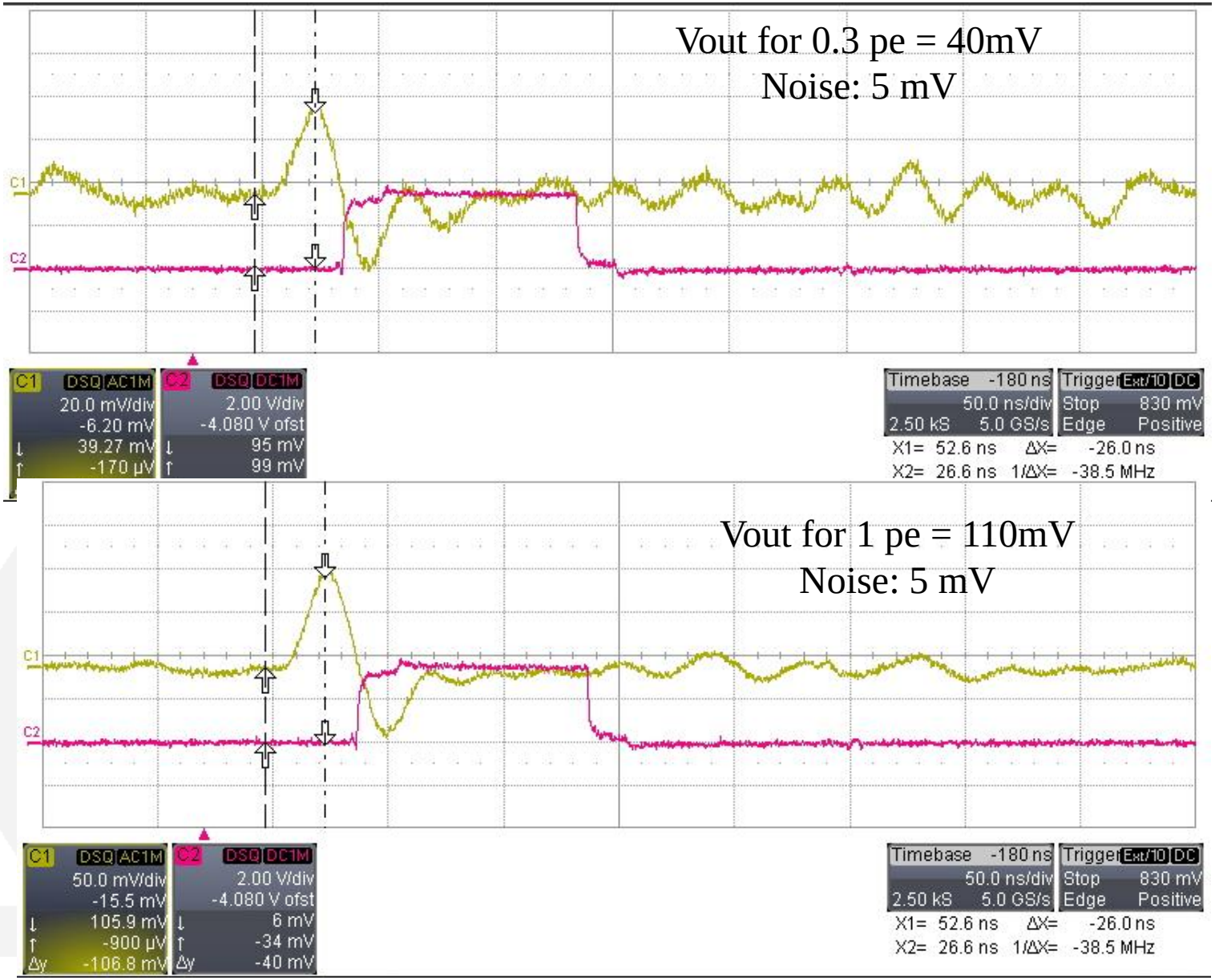
Standard SC

SC with triple voting

I2C

Selection I2C or std SC

FS @1/3 and 1pe, Cf=32x6.25fF=200fF



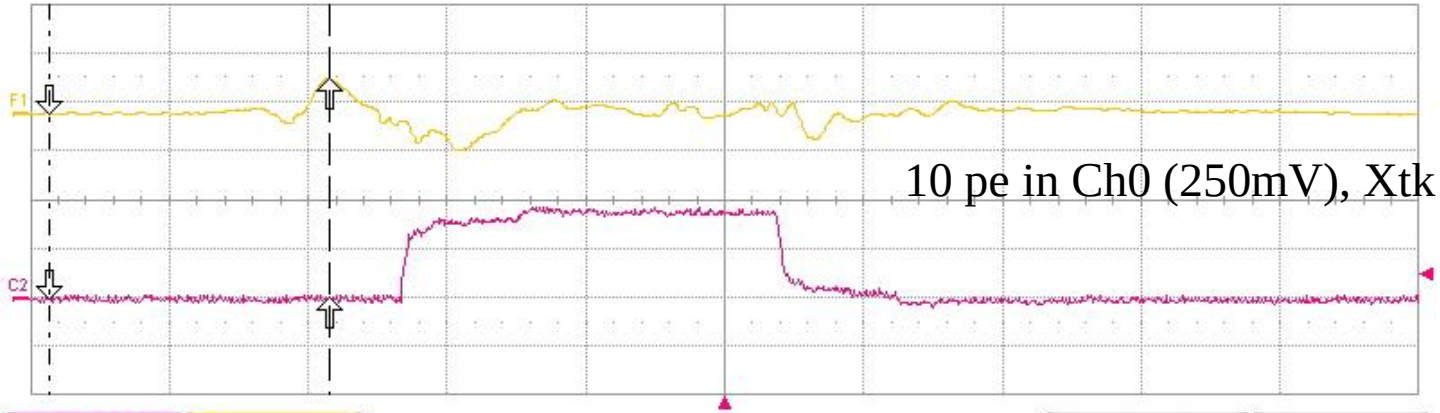
« Pedestal shift » due to coupling on Vdda_pa on spiroc2b

Spiroc2c: Injection of 10, 100, 300 and 1000pe- in ch0 and measurement of the charge (HG) seen on the neighbours (all preamp on but all discris masked except of ch<0>:

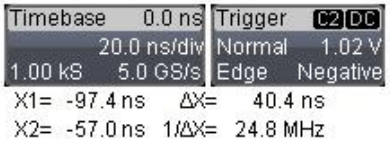
	10pe-	100pe-	300pe-	1000pe-
Ch<0>	950 UADC	3500	3500	3500
Ch<1>	470	470	450	450
Ch<2>	470	460	440	440
Ch<3>	460	463	446	446
Ch<20>	460	457	450	450
Ch<35>	455	457	455	455

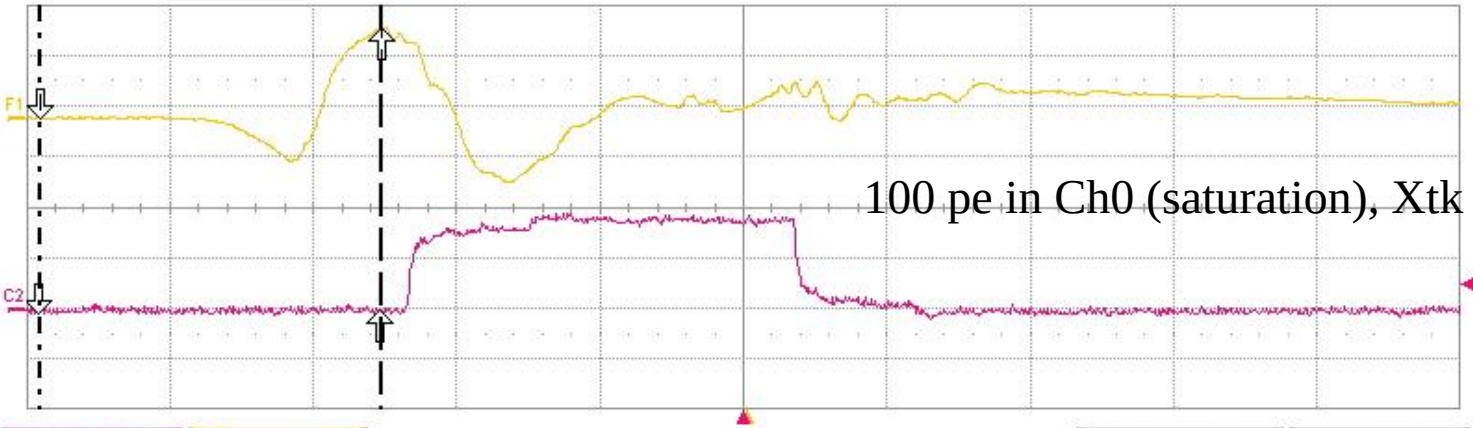
When discris of the other channels are ON => we measure Xtk in the neighbours

SPIROC2C: Xtk

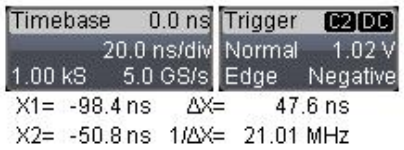


10 pe in Ch0 (250mV), Xtk in Ch1=3.5mV

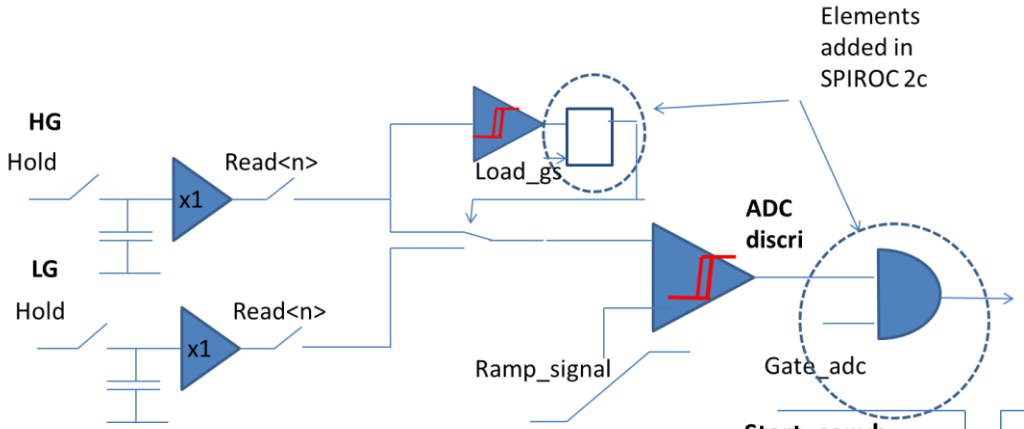


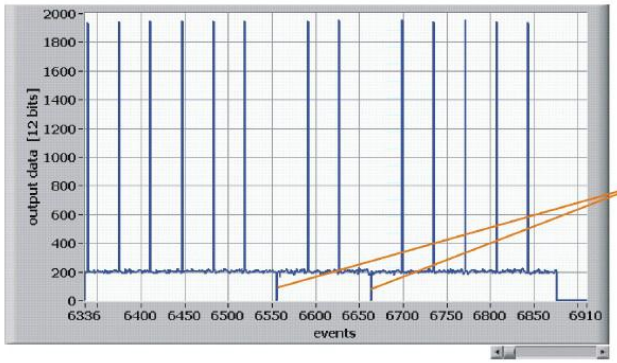


100 pe in Ch0 (saturation), Xtk in Ch1=10 mV

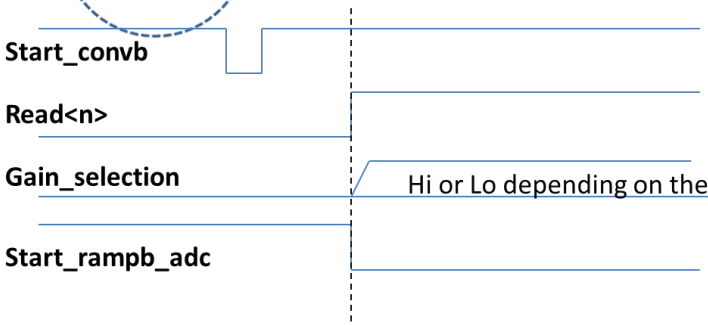


SPIROC 2c: Zero event bug

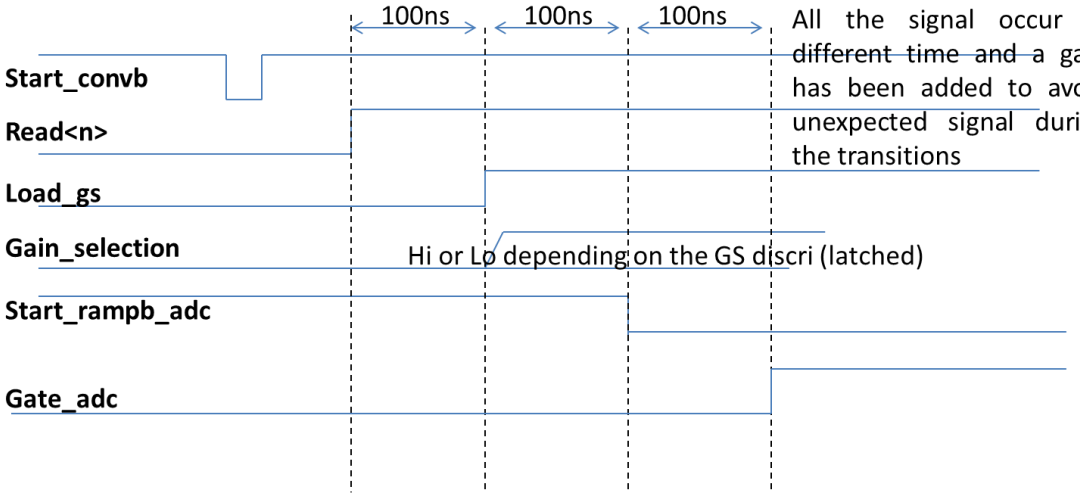




- "zero event" occurs randomly
- **Problem solved in SPIROC 2c**
- No major change in the digital part D-flip-flop, a gate on ADC discri and delays on control signals

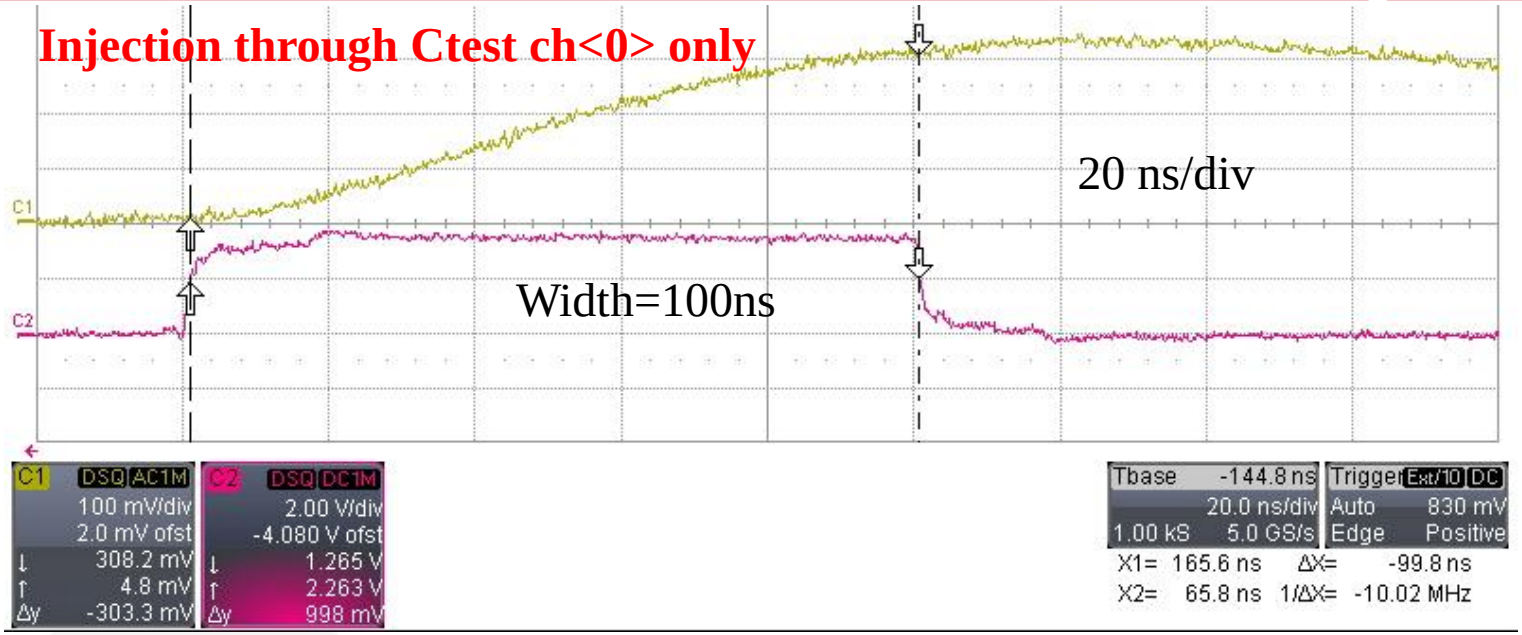


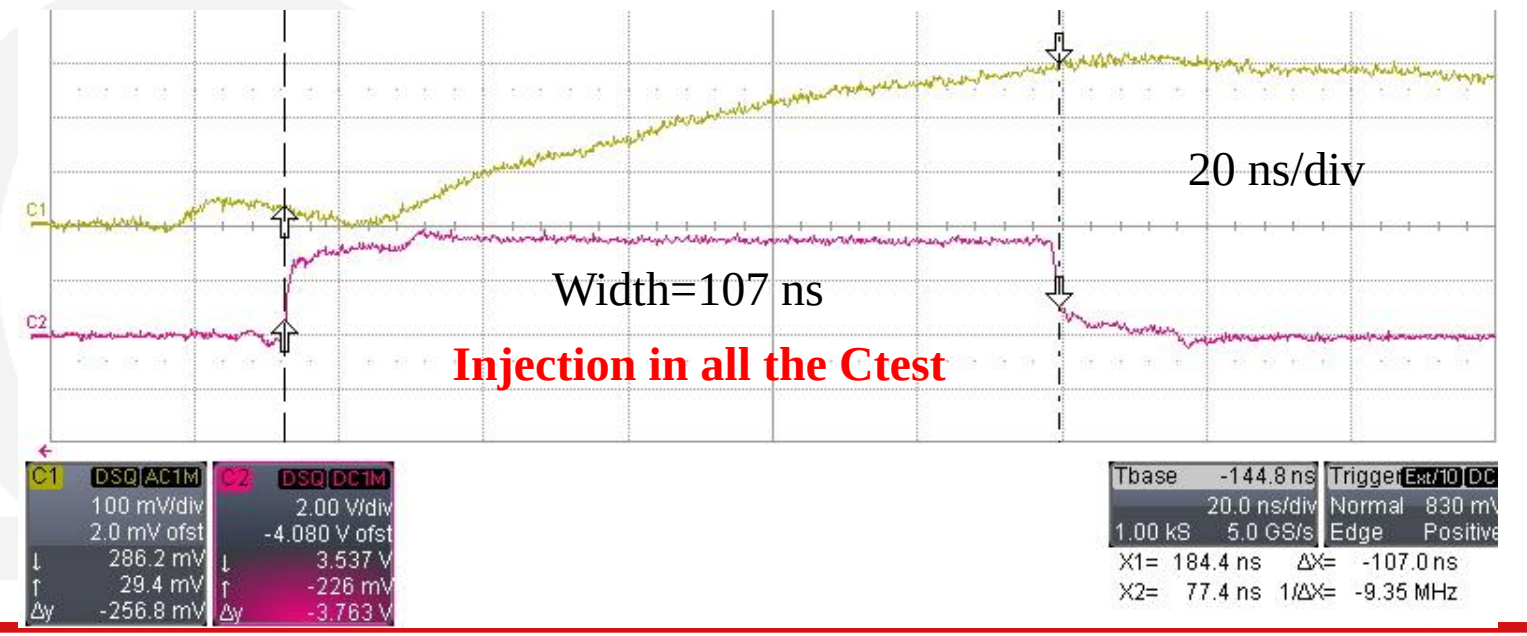
Situation in SPIROC 2b
All the signal occur at the same time



Situation in SPIROC 2c
All the signal occur at different time and a gate has been added to avoid unexpected signal during the transitions

SPIROC2C: New Delay box





SPIROC2C: HG SSh linearity using the acquisition mode