SKIROC2 FEV and testbench measurements

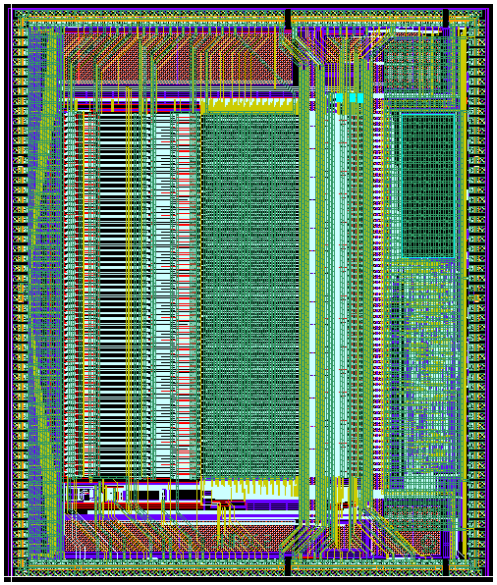
LAL, LLR and OMEGA

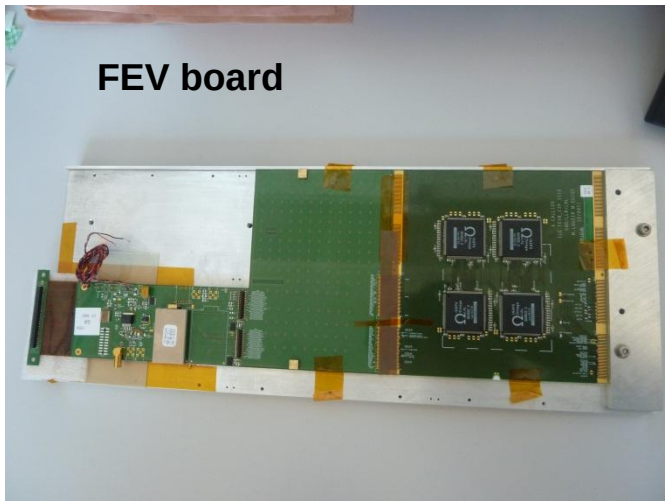
Orsay MicroElectronics Group Associated

SKIROC : Reminder

- SKIROC2 :
  - Very similar to SPIROC
  - 64 channels, 65 mm^2
  - Very large dynamic range:
    - HG for 0.5-500 MIP
    - LG for 500-3000 Mip
  - Internal 12 bit ADC/TDC
  - Autotrigger on MIP (4 fC)
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Pulsed power -> 25 µW/ch
- 1200 chips produced in March 2010 (dedicated run => 42 k€)
- TB in July 2012:
  - 6 FEV boards equipped with 4 SK2 (1536 channels)

65 mm2 => 65 k€

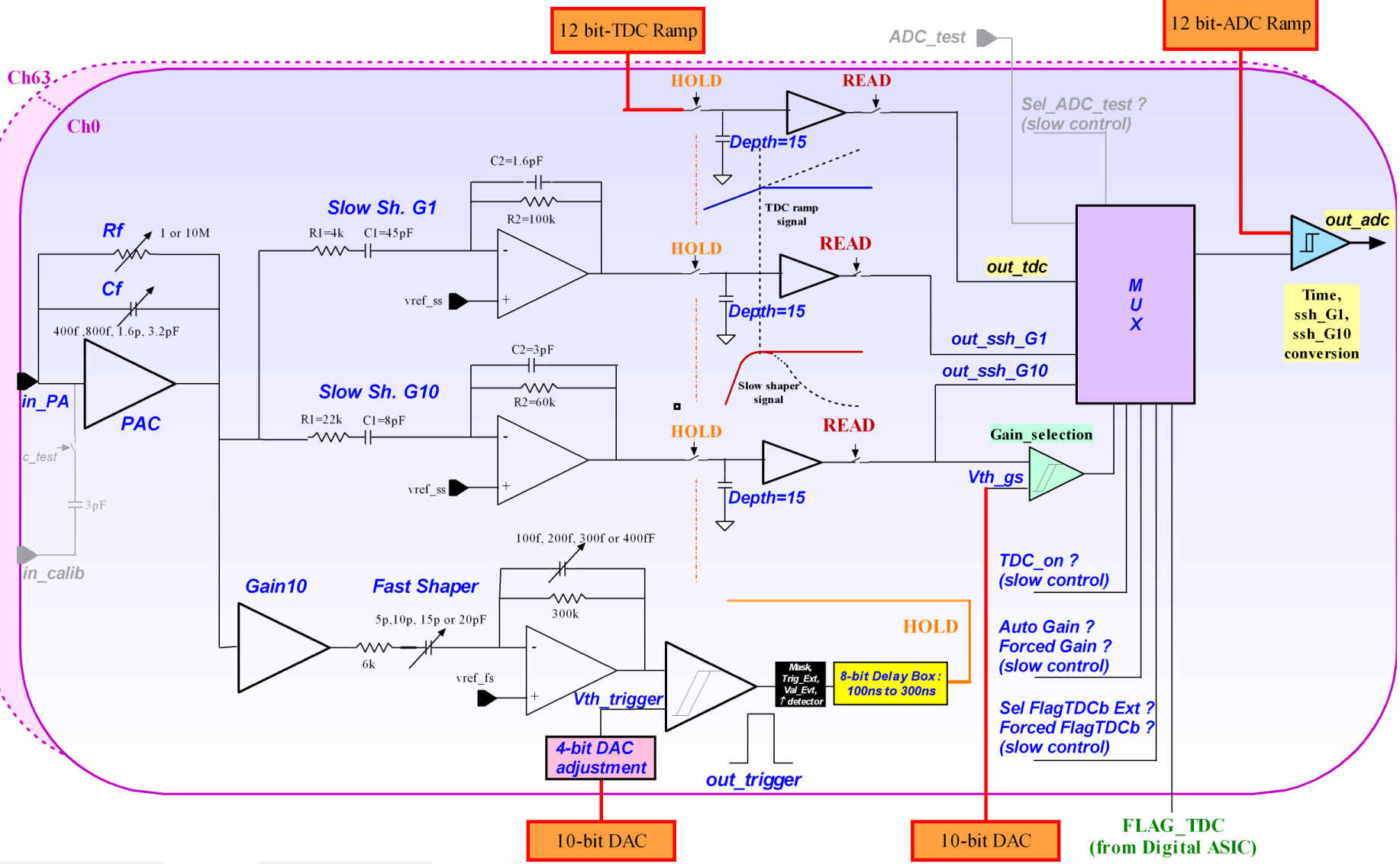




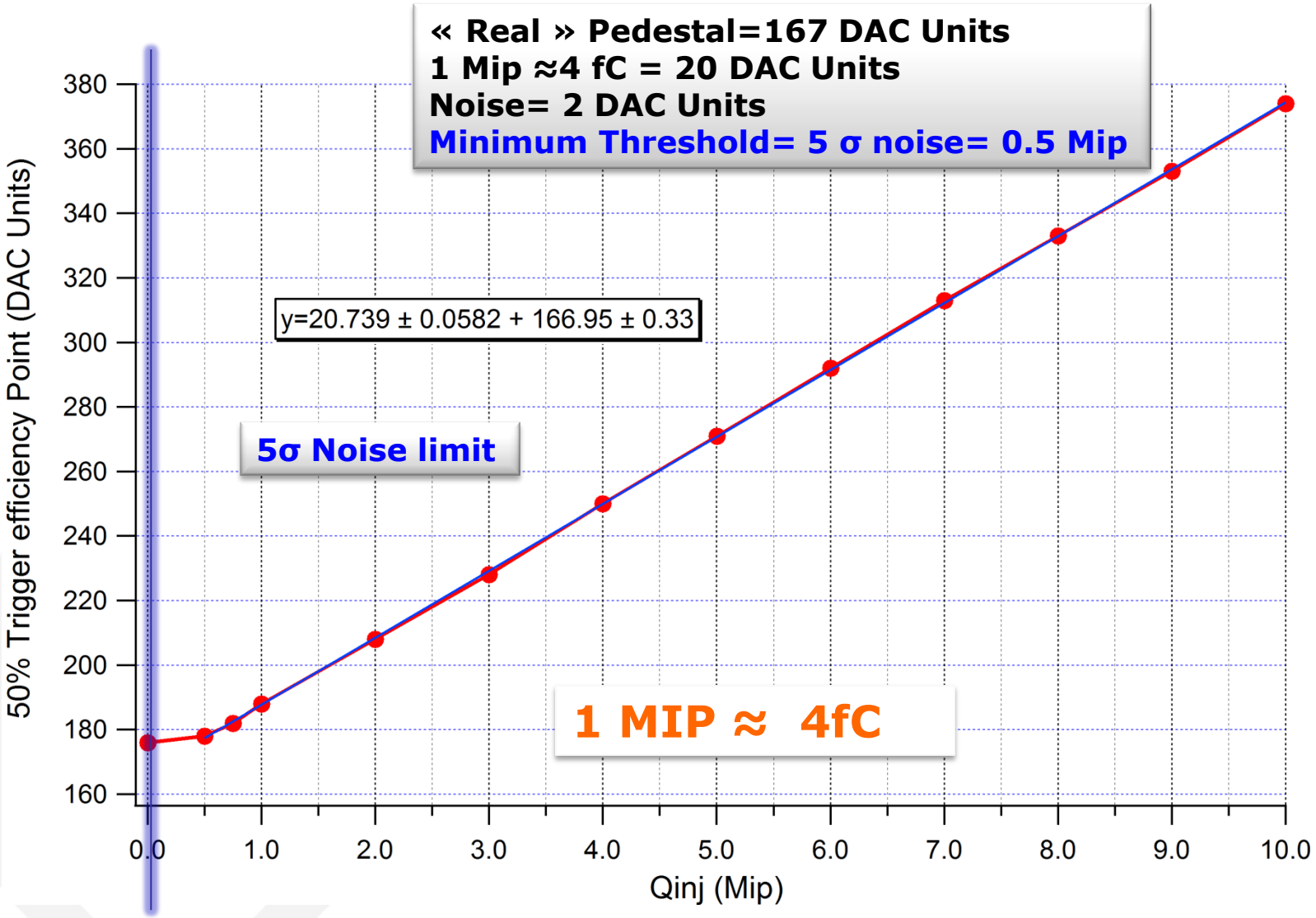
SKIROC2 features

- **VERY SIMILAR TO SPIROC, same digital part**
- Very low noise (0.4 fC = 2 500 e-) and very large dynamic range (2fC up to 10 pC) charge preamplifier
- **180ns** shaping time Slow Shapers for charge measurement
- 2-bit shaping time adjustable Fast Shaper (50 to 100ns)
- 10-bit DAC for discriminator threshold , With 4-bit adjustment on each channel
- Analogue Memory depth : up to 15 events can be stored
- Trigger Discriminator for autotrigger on ½ MIP
- 8-bit adjustable delay to position the Hold signal
- Digitization of either time and charge or of both charges

SKIROC2 Analogue core



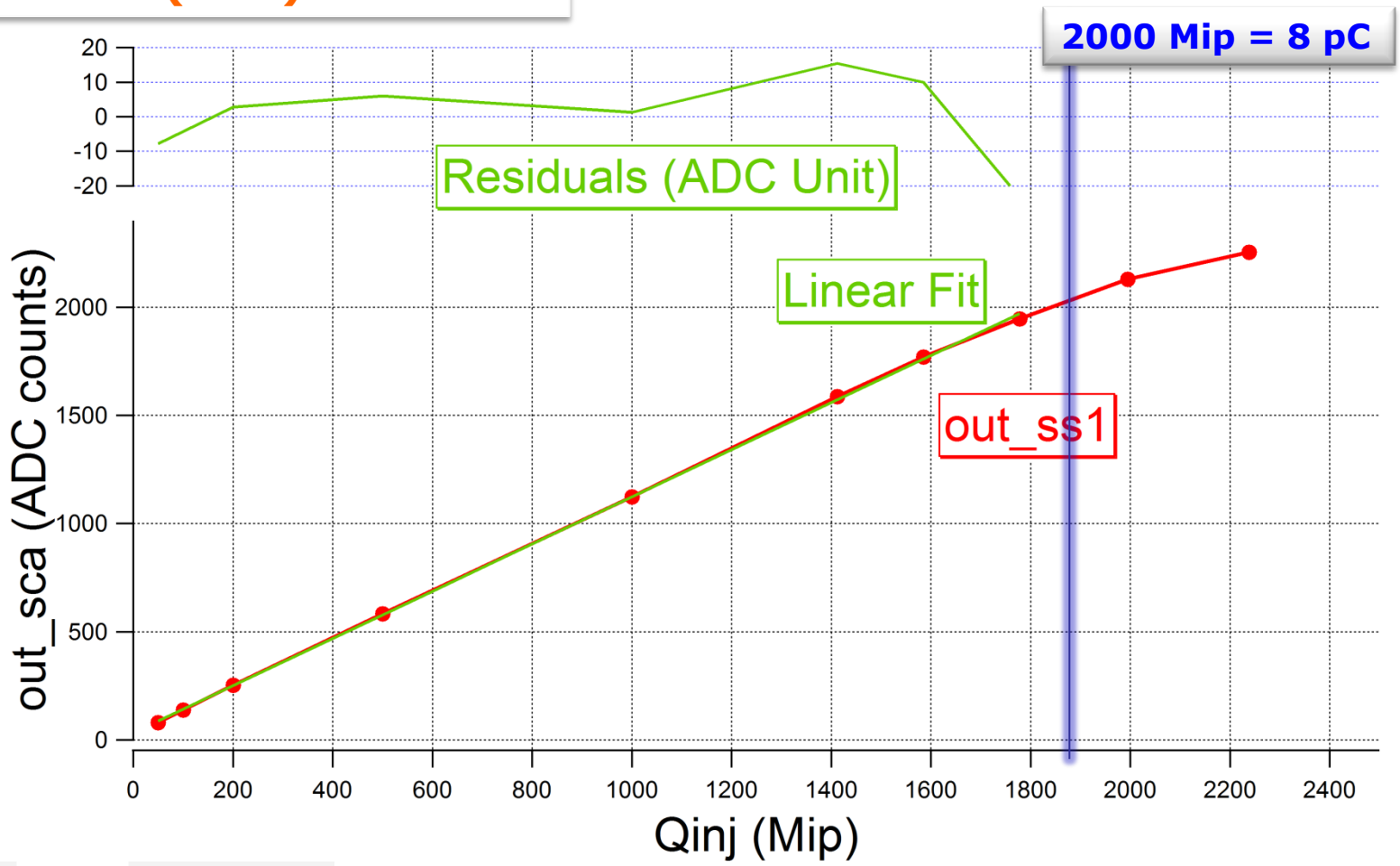
Trigger efficiency



Linearity of the Low Gain Shaper

MEASUREMENTS using SCA and internal ADC

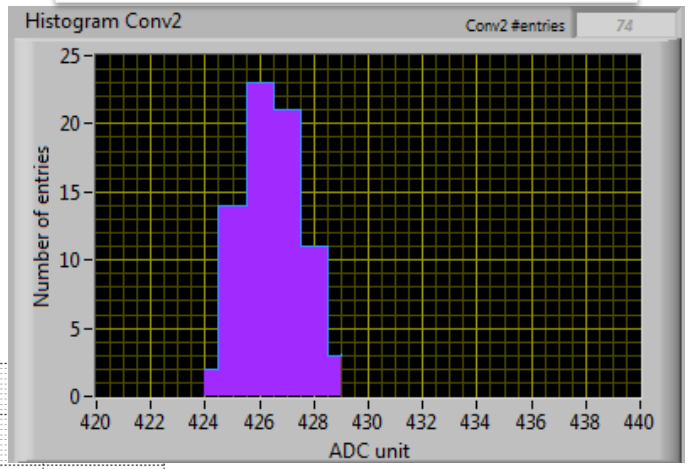
Autotrigger Mode
With 1 MIP (4 fC) threshold



Linearity of High Gain Shaper

Noise = 630 µV
1 Mip gives 5.7 mV
S/N=9

ss10@20 Mip
Rms =1.16 ADC U=600µV



MEASUREMENTS using SCA and internal ADC
Autotrigger mode
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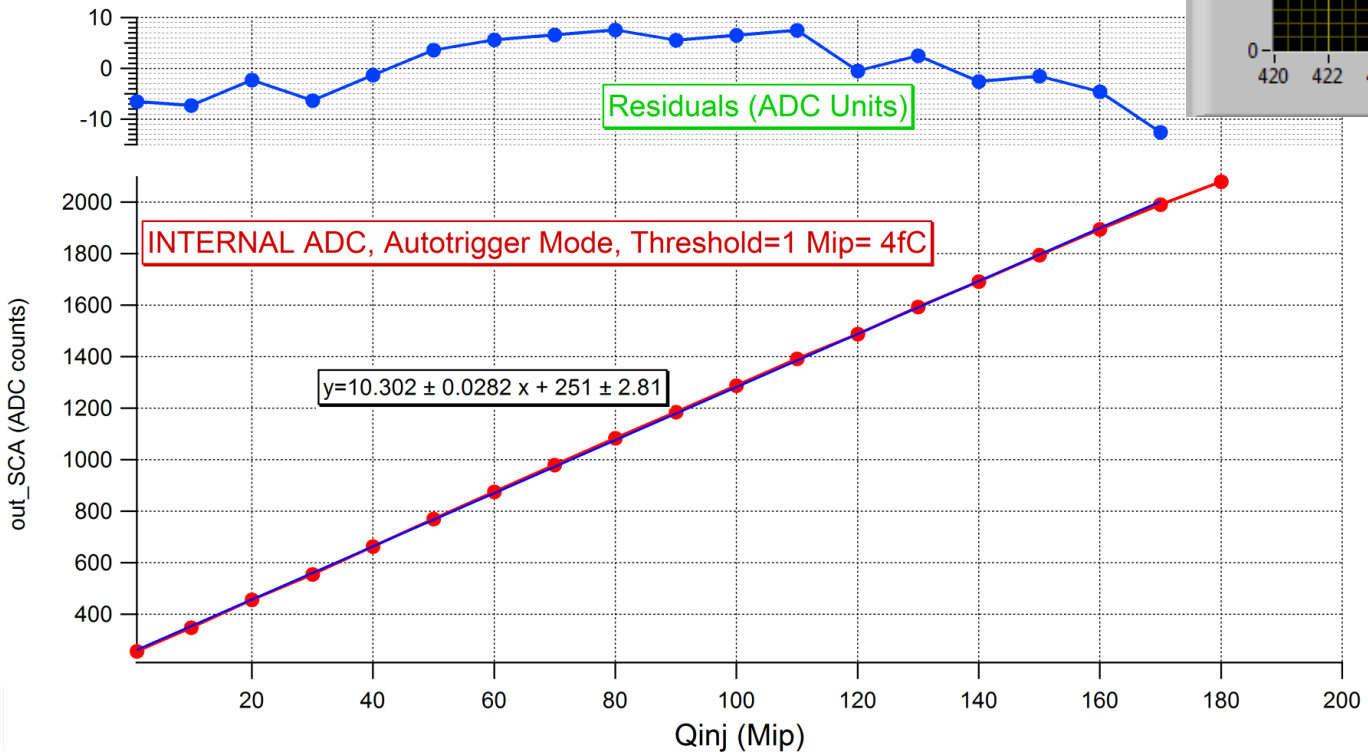


First test beam with the technological prototype

@Thibault Frisson, IEEE 2012

DESY – April and July 2012

e- (1 - 5 GeV)

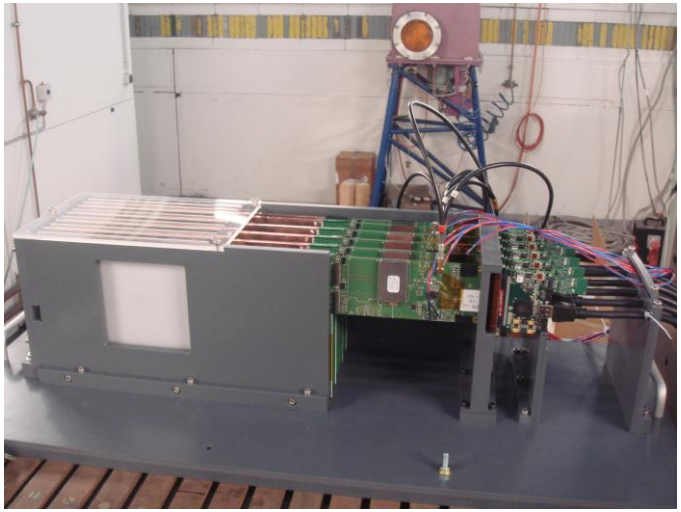
- 6 layers (FEV8)

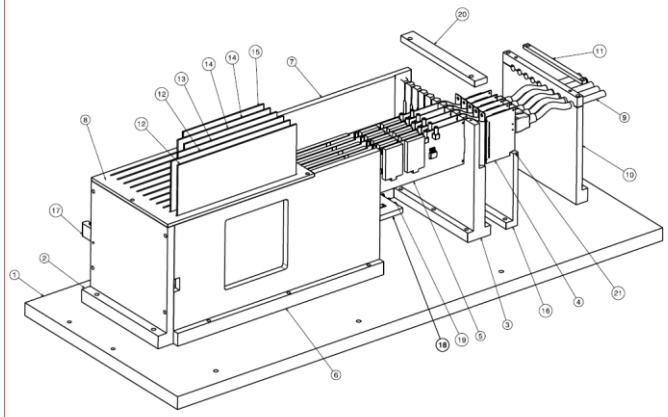
- Internal trigger

- **Total = 1536 channels**
- channels with not aligned pedestal ➡ switched off
- **total active channels = 1278**

- PVC structure

- position for tungsten plates (2.1 mm)



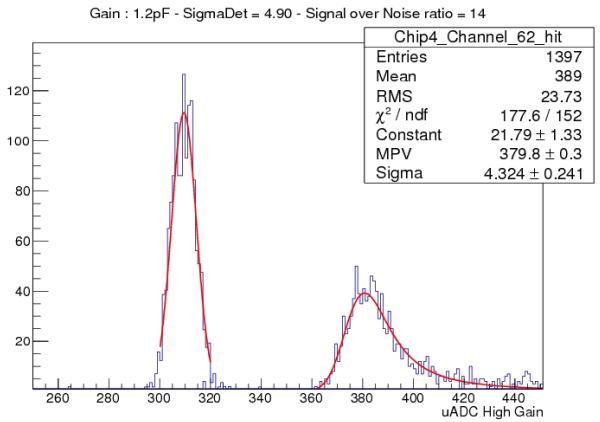


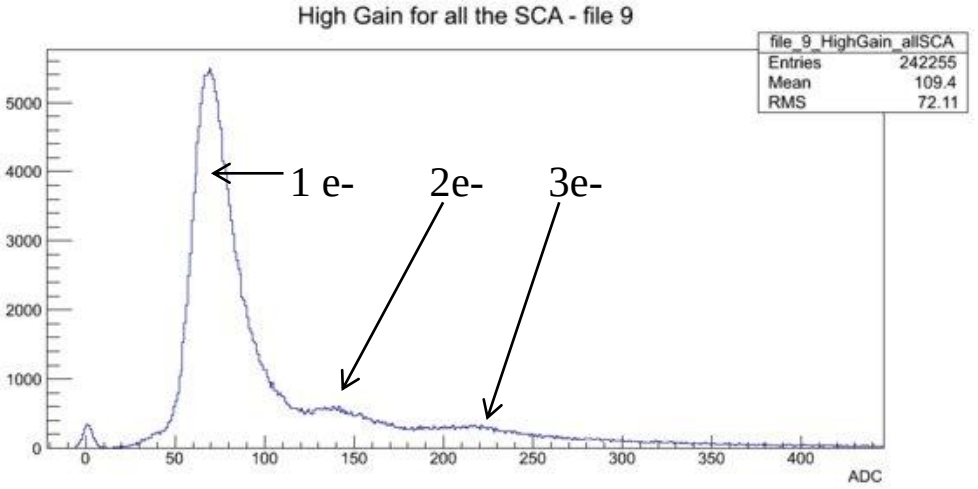
Goals:

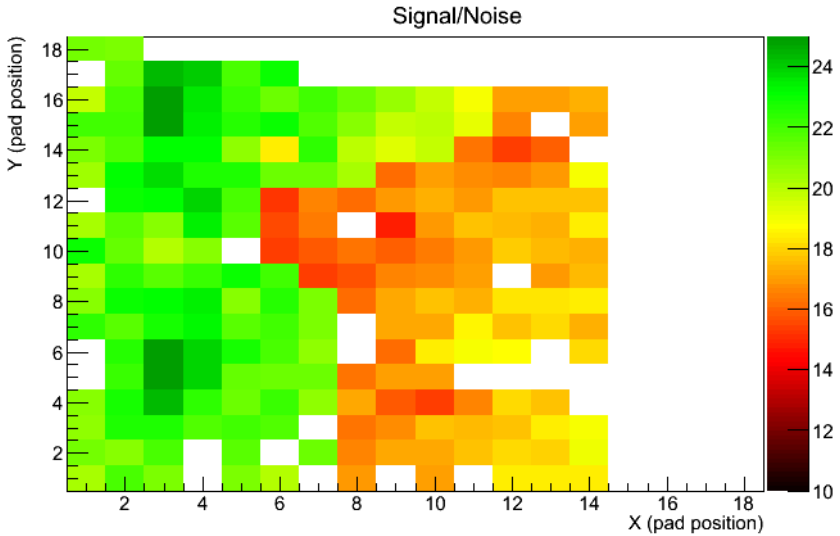
- **Determine signal over noise ratio of the detector**
- Operate first layers of the technological prototype
- Establishment of calibration procedure for a large number of cells
- Homogeneity of response (x,y scan of detector)

First results

@Thibault Frisson, IEEE 2012



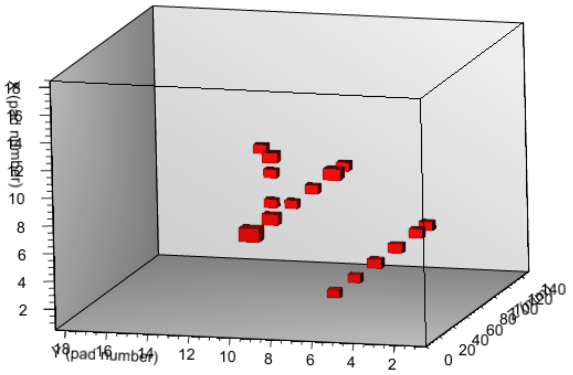




S/N > 10

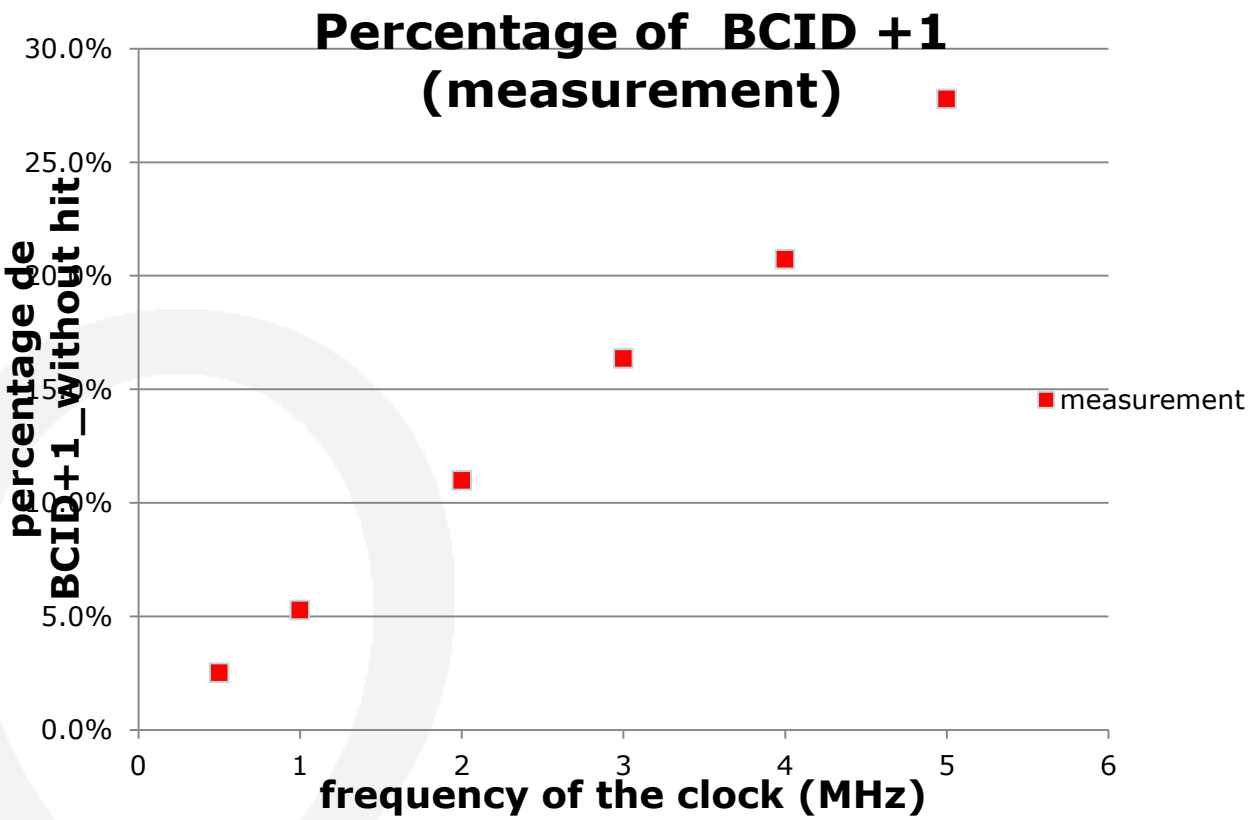
(for all gains available with SKIROC2)

2 e- (3 GeV, no tungsten)



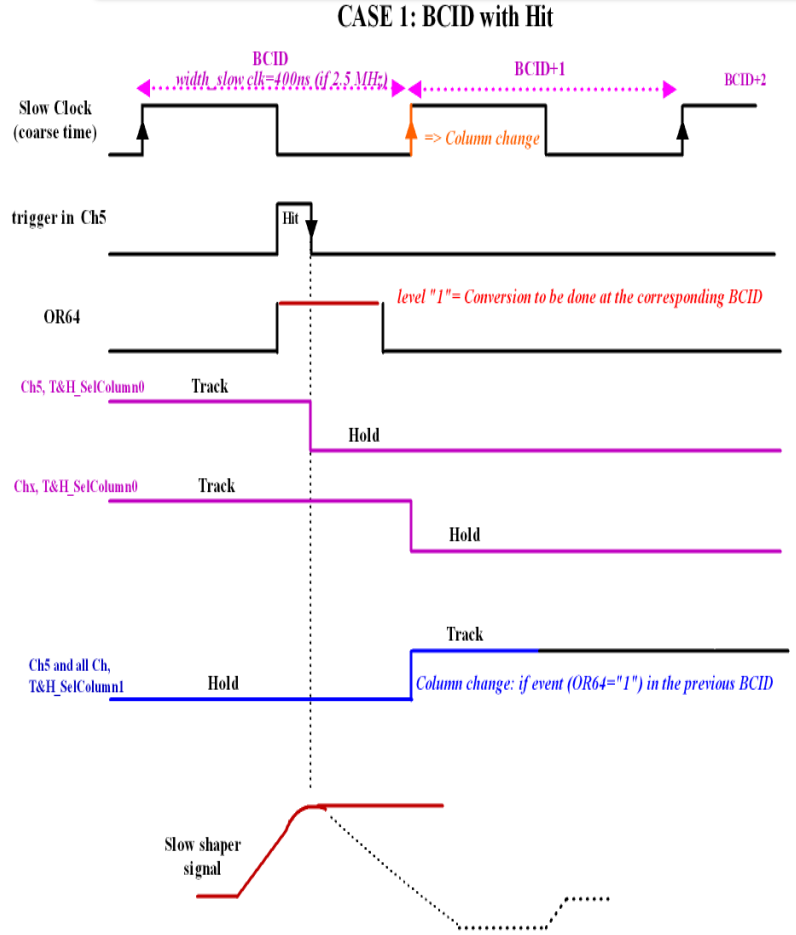
BCID+1 events

- Good test beam results but many points to be undertsood
- Number of BCID +1 events without hit effect : increases with the frequency of the clock

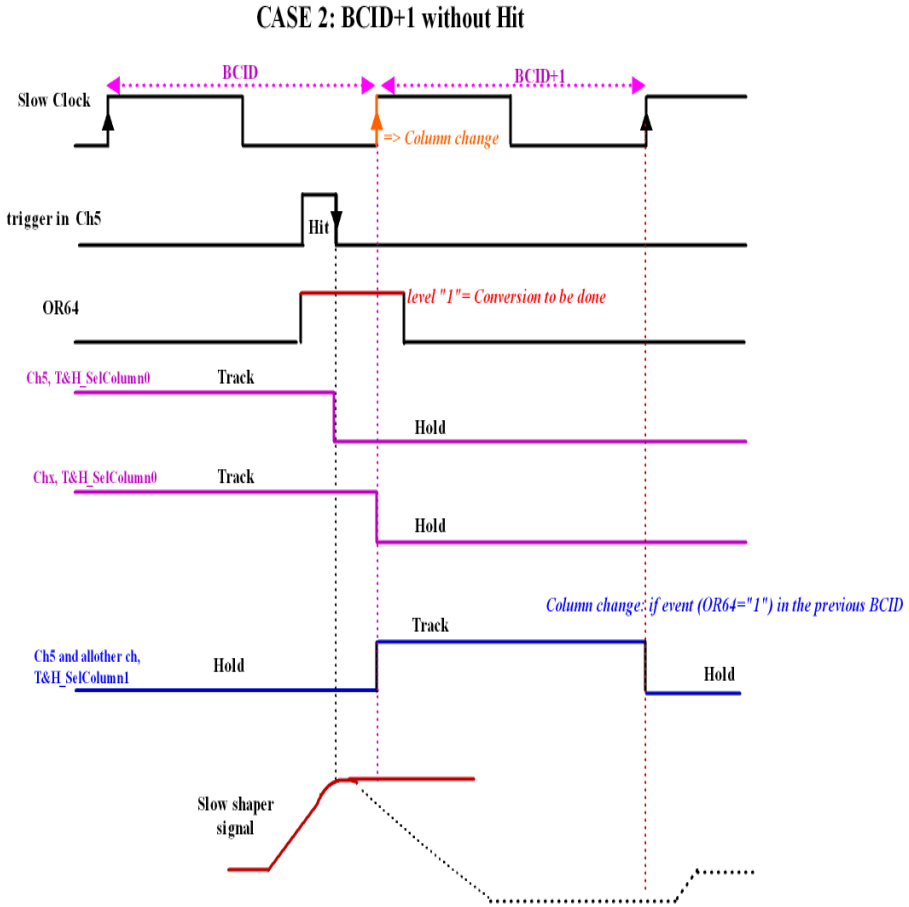


BCID + 1 wo hit explanation

Probability of such events= Width OR/width clk

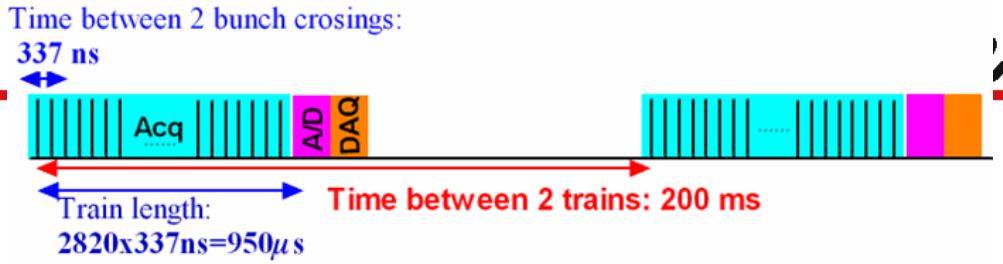


Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi= ped
BCID+1: No conversion because OR64 level=0 during this BCID+1

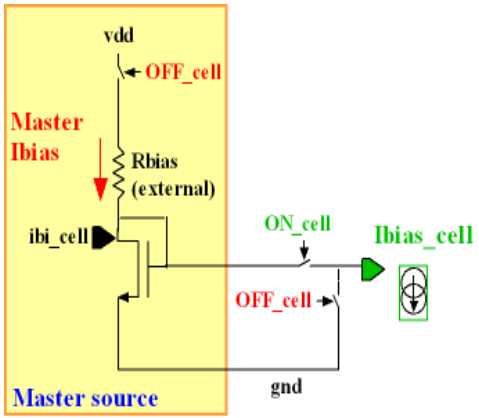


Conversion: BCID, one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal
BCID+1, no hit, SCA1 ch5 holded value=value < pedestal or pedestal, other SCA1 holded value=ped.

POWER PULSING (1)



- **Requirement:**
  - **25 μW/ch with 0.5% duty cycle**
  - **500 μA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**

- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

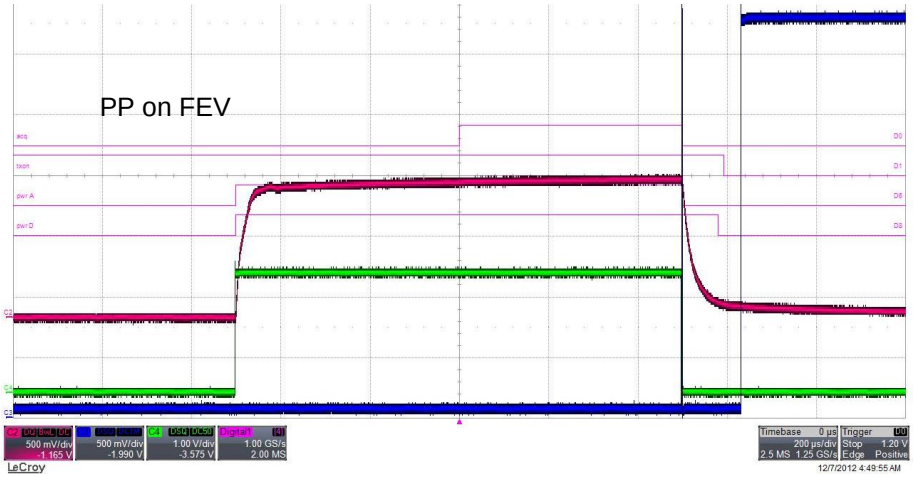
Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 μW/ch

POWER PULSING: Timing

- First measurements by LLR and LAL, performed on testbench (one ASIC) and on FEV with and wo wafers
- Power pulsing on testbench: test board wo any decoupling capacitors on bias and on reference Voltages
- Pwr on A and dac= 200µs necessary for the preamp to reach its DC level
- Power pulsing of FEV board

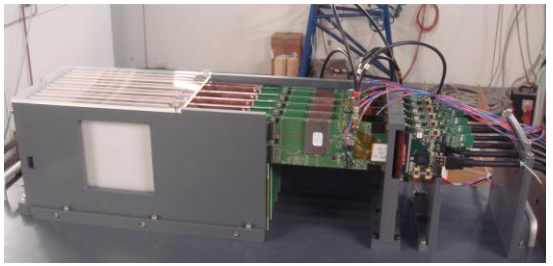
PP on testboard

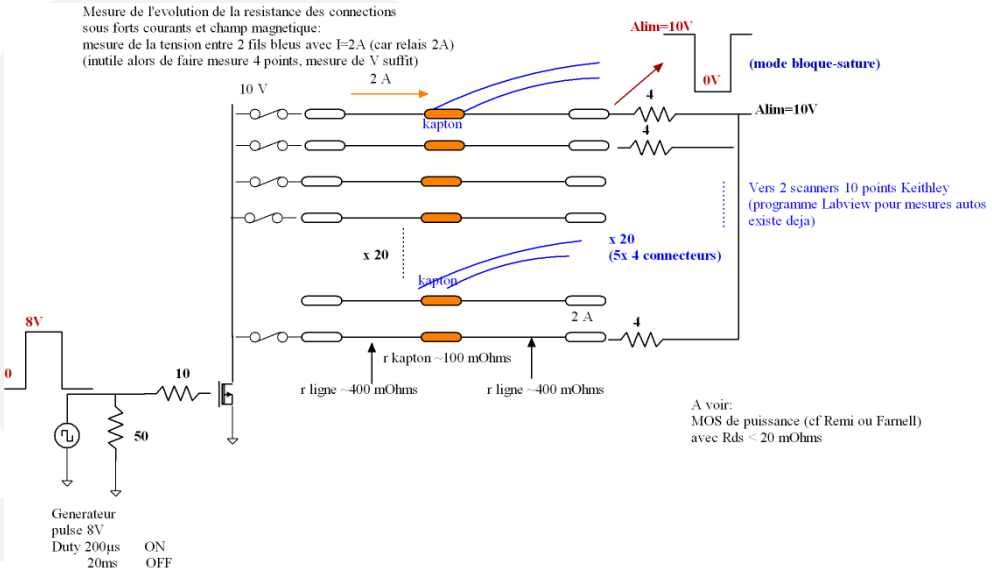


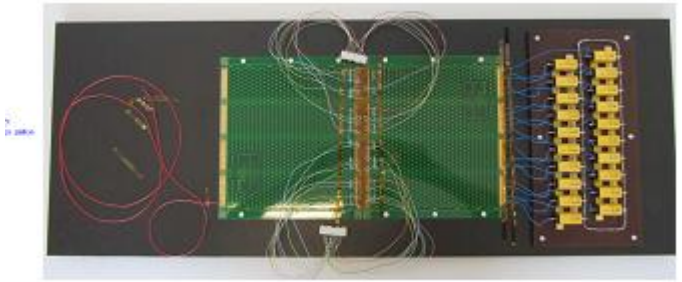
POWER PULSING: TB and B field

TB at DESY next Feb 2013

- Power pulsing in TB conditions of one of the 7 layers: layer 7 wo decoupling capacitors
- scrutinizing understanding of detector response
- Power pulsing of 2 ASUs to test the interconnections in a 2T field and with 2 amps flowing in the connections







CONCLUSIONS

- Many measurements on testbench and at system level and many analysis of the last testbeam data still on going:
  - BCID + N (N>1) events = plan events to be understood
  - To prepare next testbeam (February 2013) and power pulsing
  - To prepare SKIROC3:
    - 64 independant channels
    - Estimated area= 8.5x9.5 mm2
      - => dedicated run necessary just as it was in 2010