CCC

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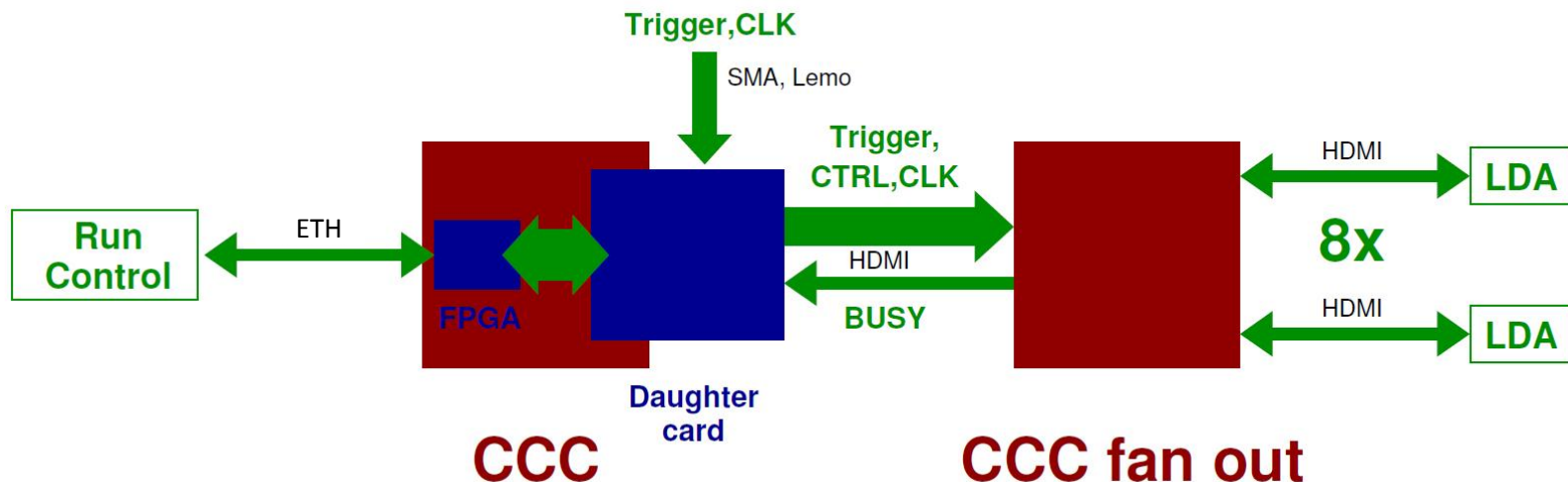CALICE electronics and DAQ Meeting
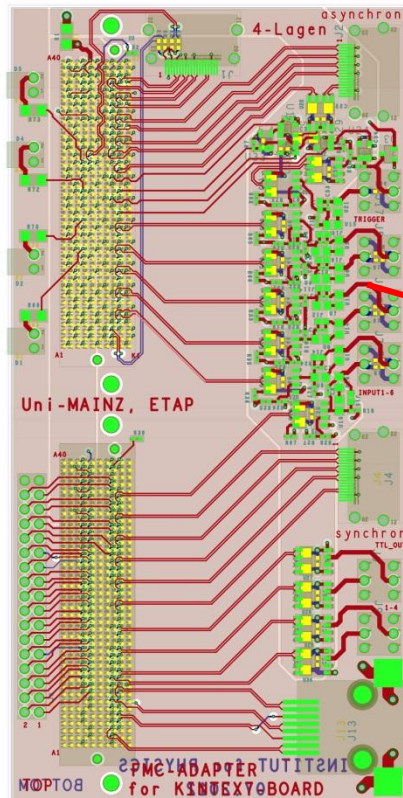DESY Hamburg, Dec. 10, 2012

New design for CCC

Aim:

1. **New configuration interface via Ethernet**
   - to set the four different running modes
2. **Improve stability**

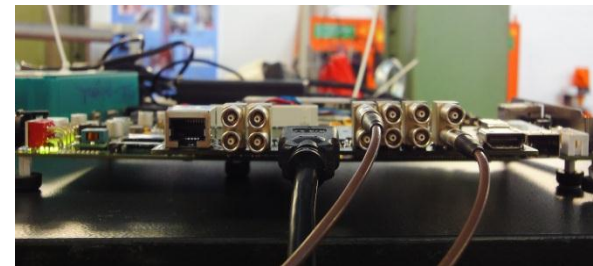3. **Additional commands and read-back of status**

Current (Mz) version of CCC
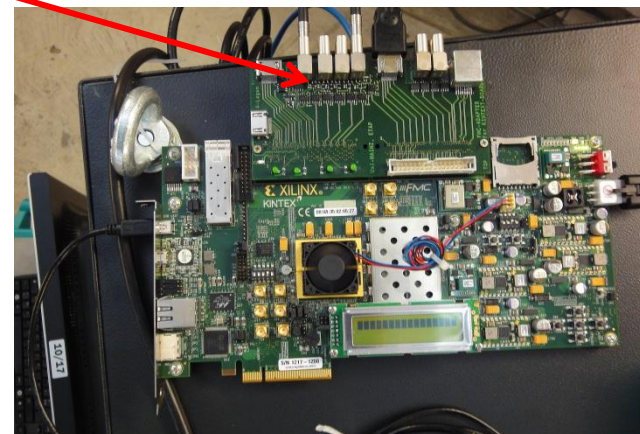
Mezzanine on an Kintex 7 Evaluation-Board:

1. **FPGA-controlled CCC board:**
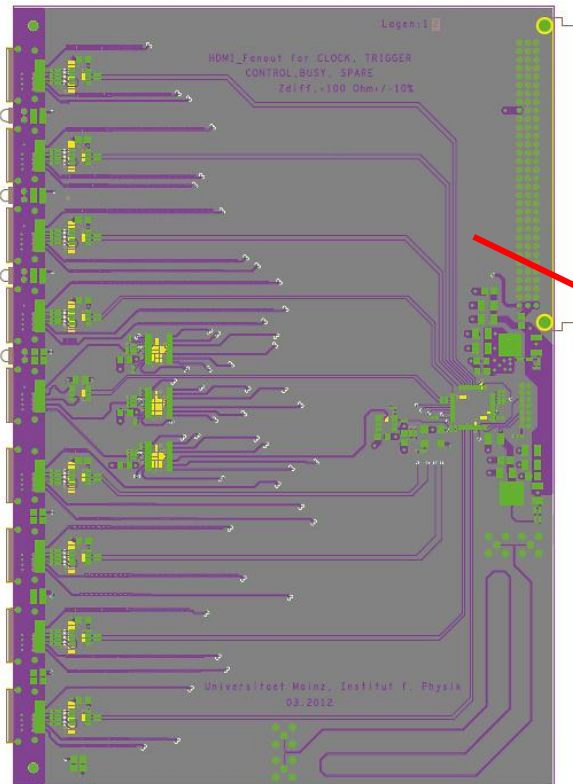
CCC at the testbeam (front):

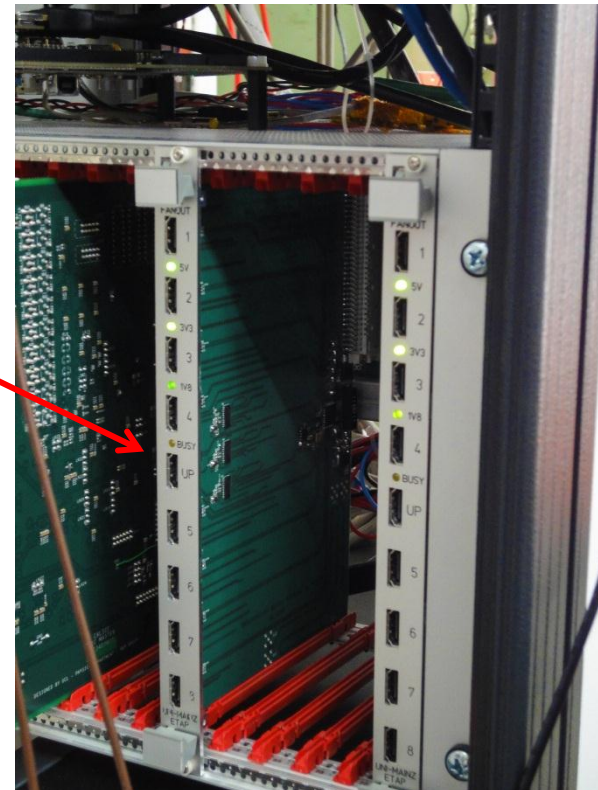**CCC at the testbeam (top):**

Fan-out

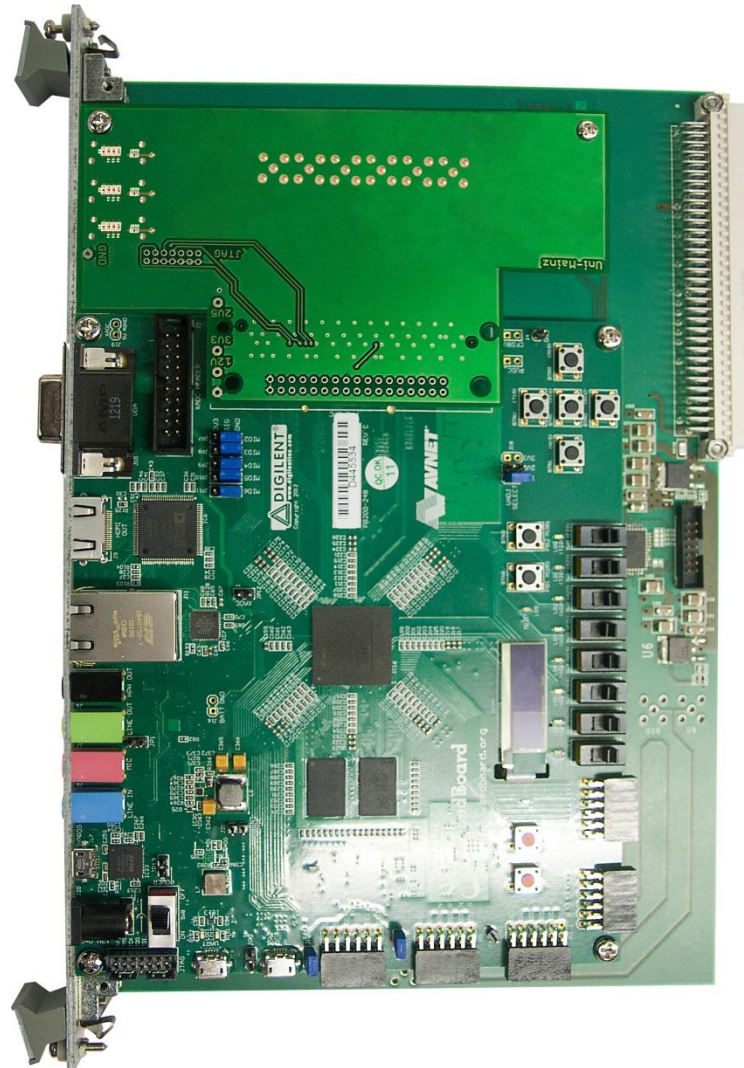**6U-VME Fan-out board:**

2. **Fan-out board layout:**

Fan-out board at the testbeam:

CCC: Current development

1. **6U-VME standard (initially double width)**

2. **3 HDMI (SYNC, ASYNC, USER/optionally into DAQ)**

3. **6 LEMO-connectors (3 TTL IN/OUT) (TRIG, SPILL, IN3; BUSY, OUT2,OUT3)**

4. **Control the CCC over the Ethernet**

New CCC

SYNC

ASYNC

USER

TTL IN

TTL OUT

ETH
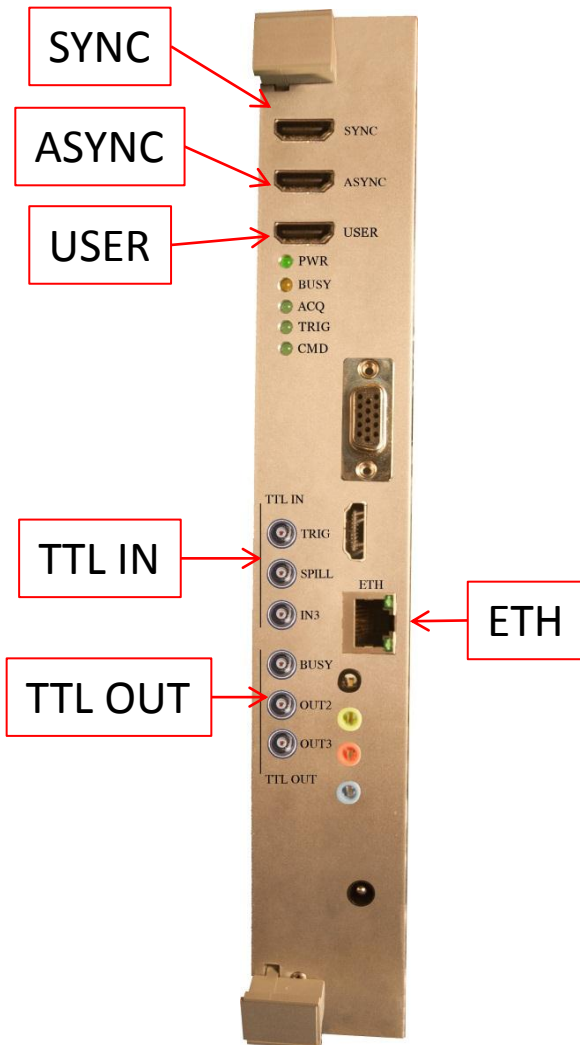
Zedboard

Modes

Four main modes and 13 configuration commands:
(e.g. status, manual trigger, hold trigger, pass trigger, rising edge, reset)

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1. **Spill only:**

U

42   62

ILC-mode(TB data ctrl)

t

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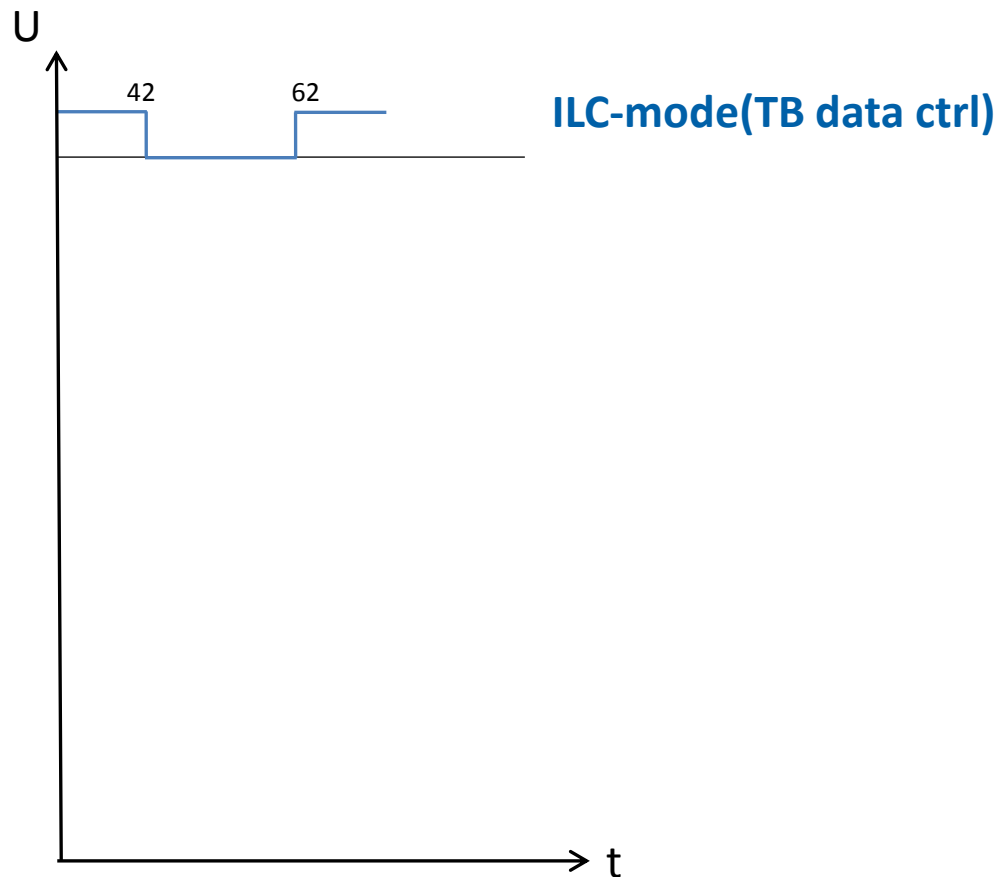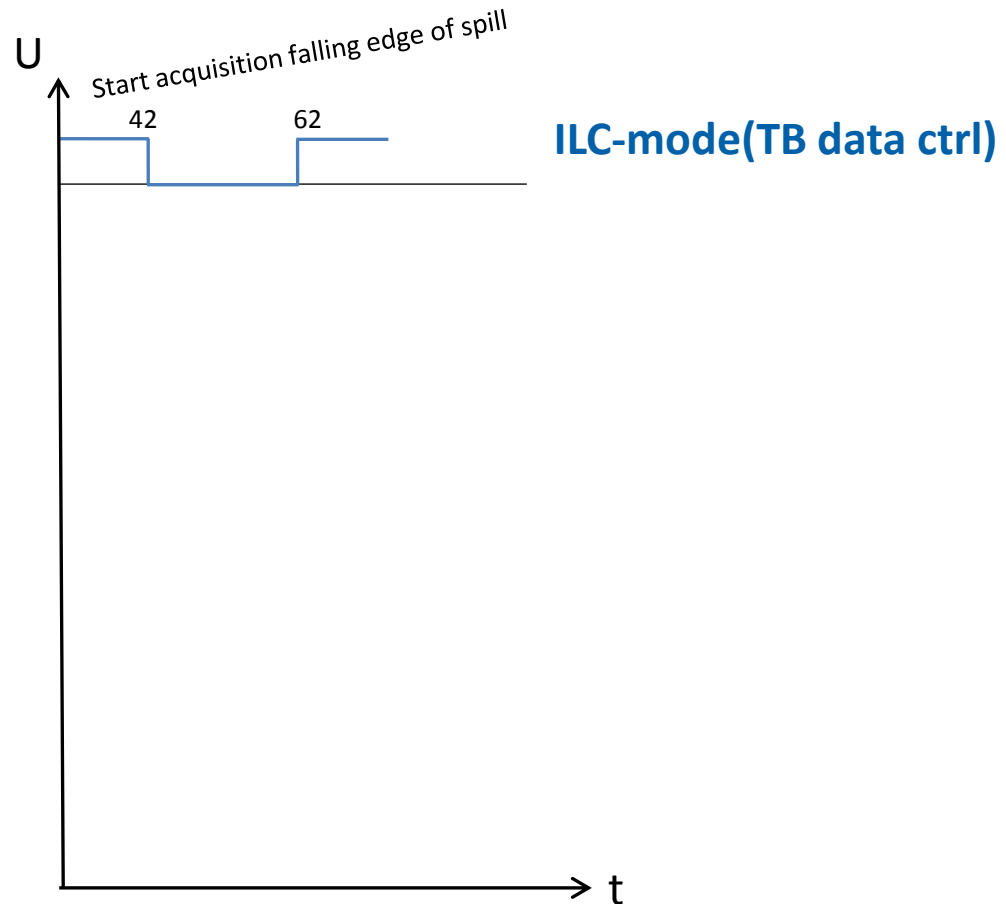
1. **Spill only:**

ILC-mode(TB data ctrl)

Modes

Four main modes and 13 configuration commands:
(e.g. status, manual trigger, hold trigger, pass trigger, rising edge, reset)

U

Start acquisition falling edge of spill

Stop acquisition rising edge of spill

1. **Spill only:**

42   62

ILC-mode(TB data ctrl)

2. **Busy only:**

62   42
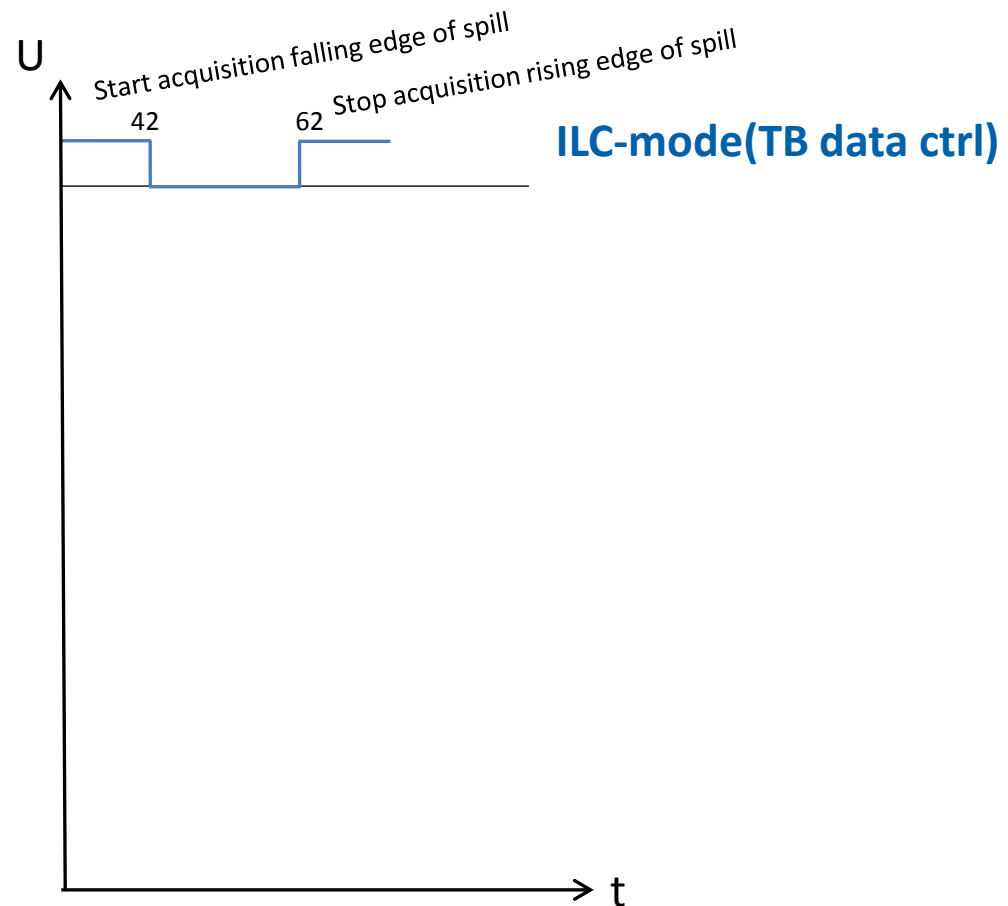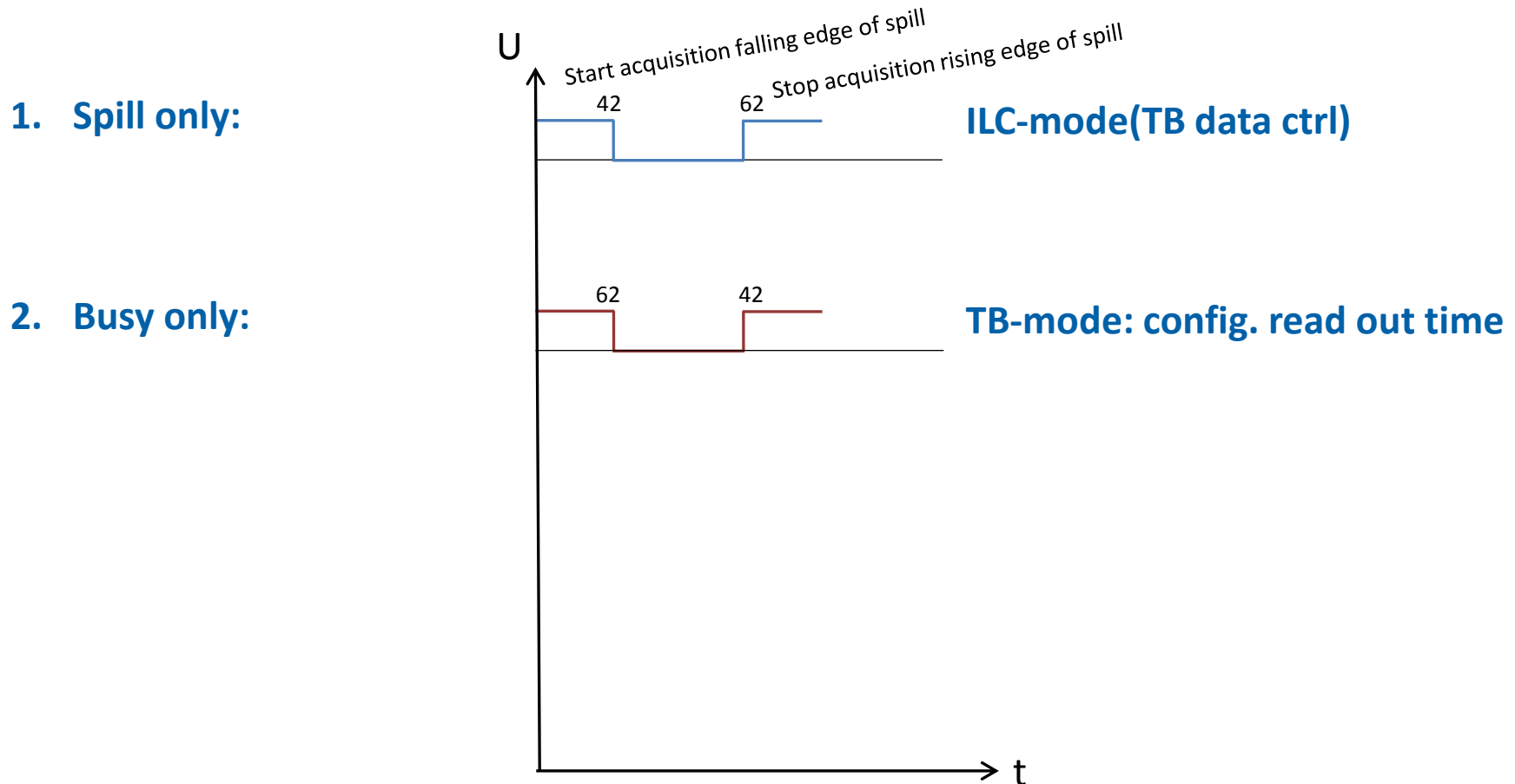
TB-mode: config. read out time

t

Modes

Four main modes and 13 configuration commands:
(e.g. status, manual trigger, hold trigger, pass trigger, rising edge, reset)

1. **Spill only:**

2. **Busy only:**

3. **Spill main busy:**

Current op modes

Four main modes and 13 configuration commands:
(e.g. status, manual trigger, hold trigger, pass trigger, rising edge, reset)
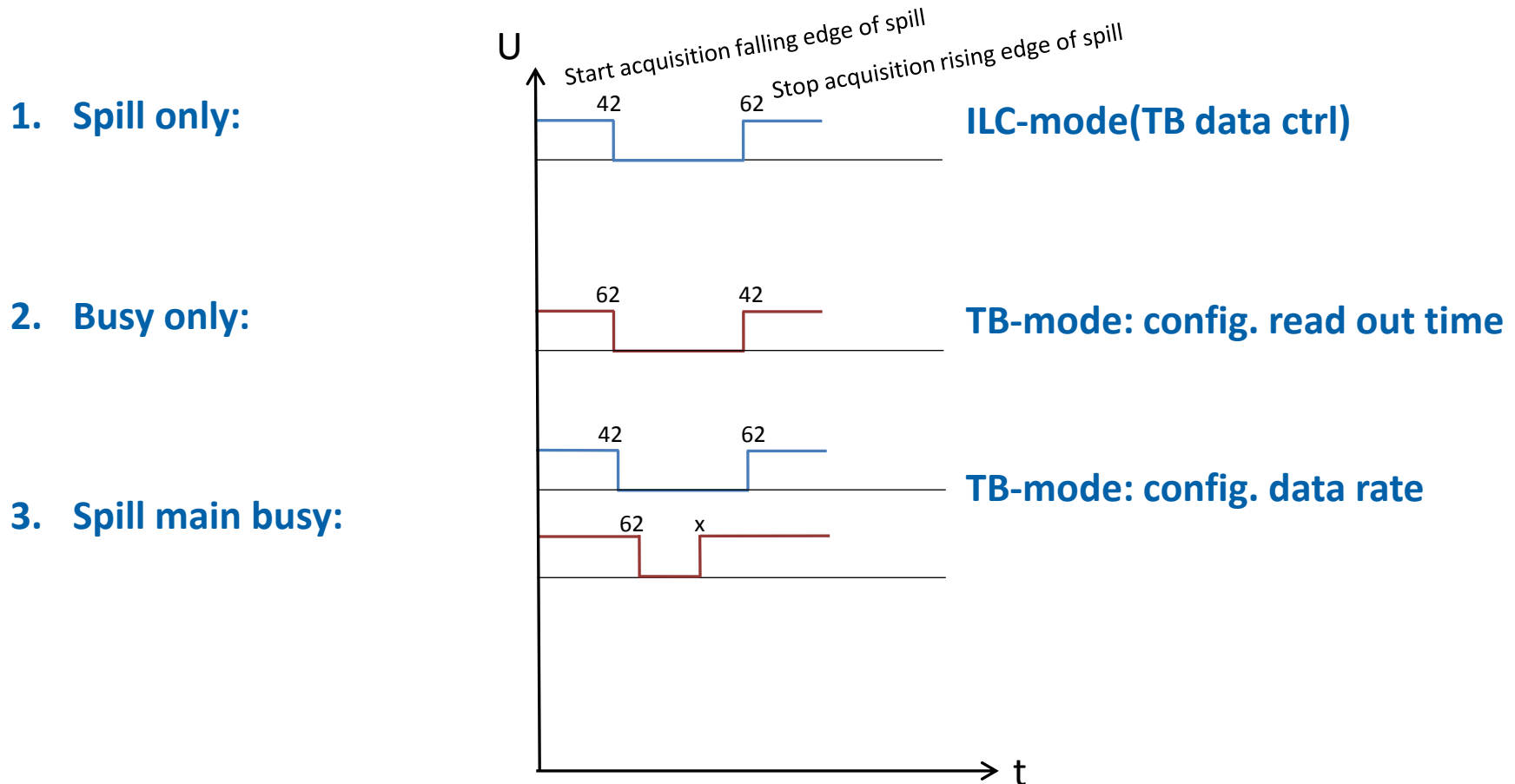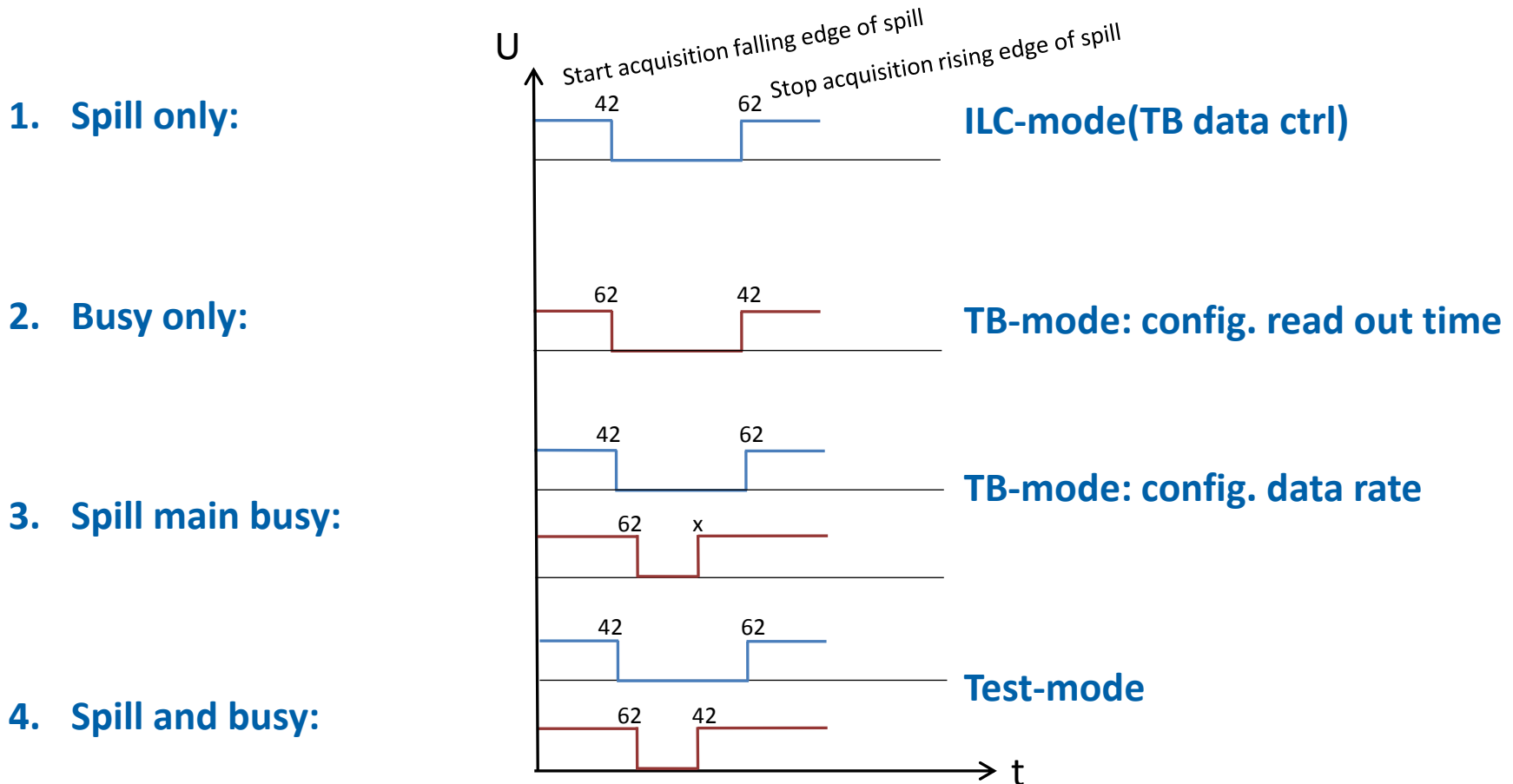

1. **Spill only:**
2. **Busy only:**
3. **Spill main busy:**
4. **Spill and busy:**

Status/next steps

1. **Mz Group is growing**

2. **Currently busy moving into the new detector lab**

3. **Zynq based CCC under development**

4. **PCB design almost finished (R.D. and A.W.)**

5. **Software and firmware development under way (S.K. and R.S.)**

6. **Further last minute input welcome**

Thank you for your attention!