# GDCC news

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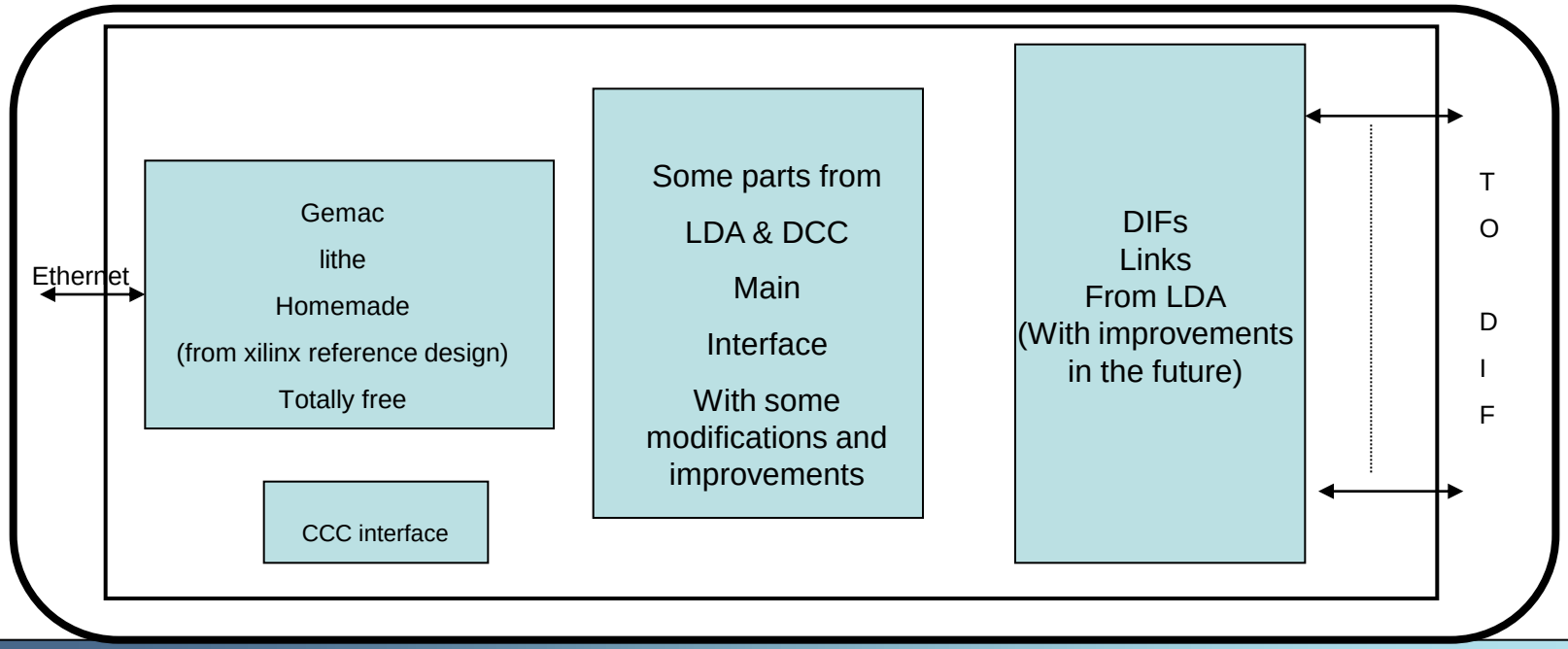
# Outline

- GDCC status in 2 main items
  - The Firmware
  - The Board
- Conclusion
  - Planning

# GDCC firmware

- All firmware is in progress.
  - A lot of parts come from the LDA and DCC with/without improvements
  - Other parts are new (homemade Gemac, Handshake with the DIF to moderate the flux,….)
- The behavior is equivalent at the LDA firmware (not modification for the software)
- Remark :

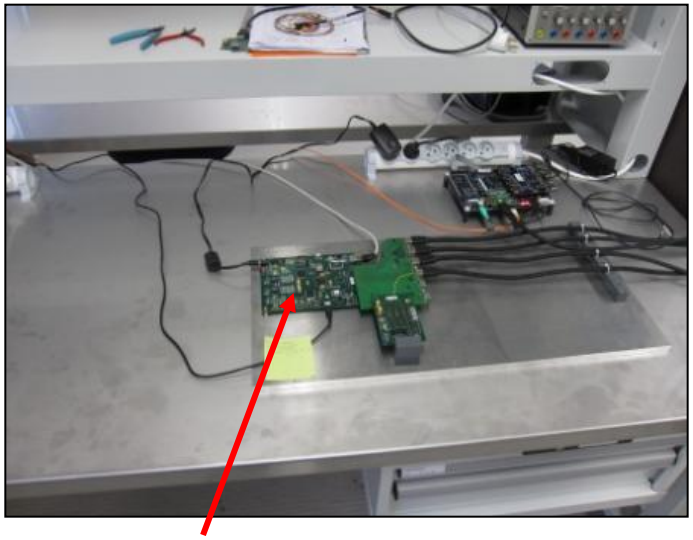
  *Some little parts of functions improved, have been implemented in the LDA for ECAL*.



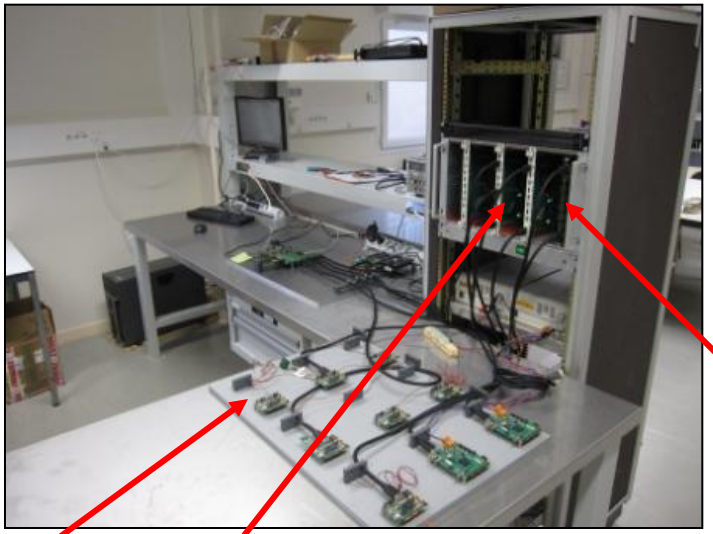
# Firmware tests

- The firmware is tested on Xilinx Spartan 6 evaluation boards.
- This board communicates with 3 DIFs or DCC and one CCC
- Currently, the software used is python (it's the same function than LDA)

*Link is locked, fast command works, random data sent by the DIFs,….*



SP601 emulates a GDCC



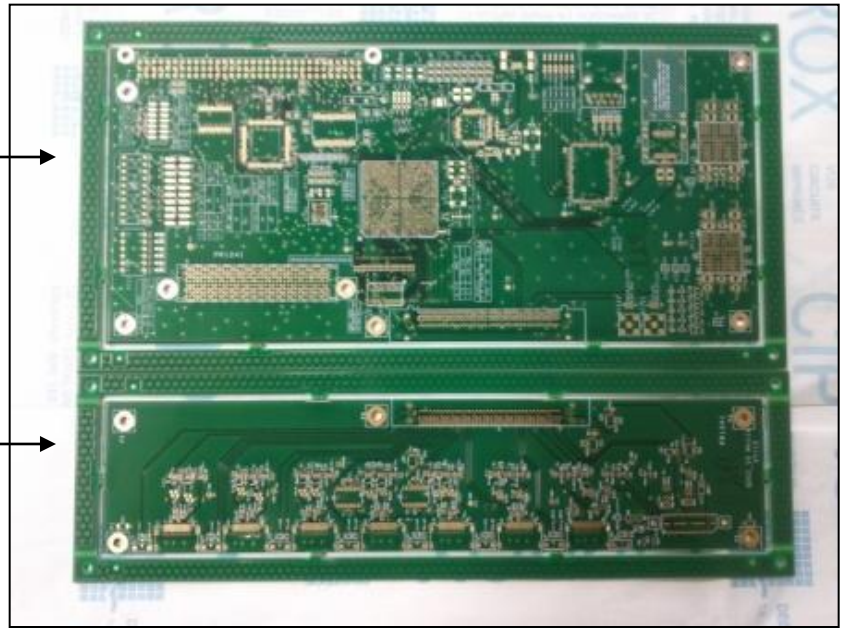

DIF and DCC connected to the SP601

# GDCC board

- We launched 3 prototype boards in manufacturing in October
- Here is a picture of the PCB before assembling components
- The PCB is shared in 2 parts : the main GDCC and the mezzanine part (HDMI connection)

Main part

Mezzanine part



GDCC

12 layers

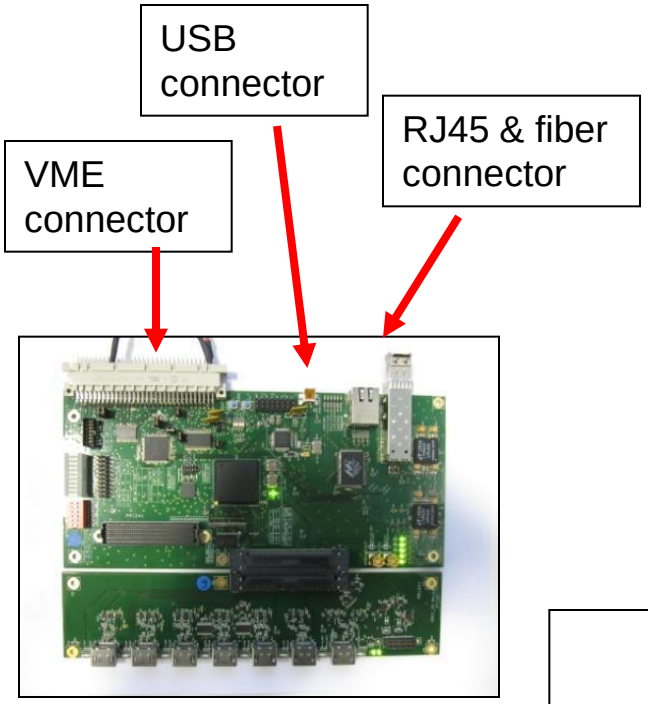
Size : 233 x 106.66 mm

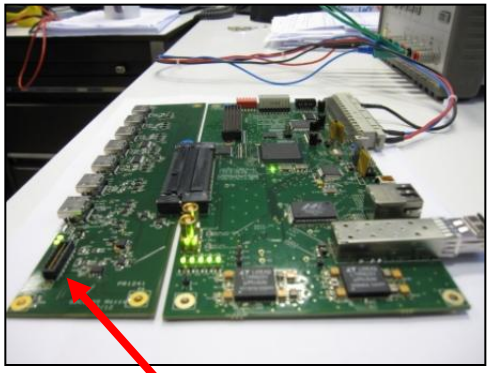
Thickness : 1.81 mm

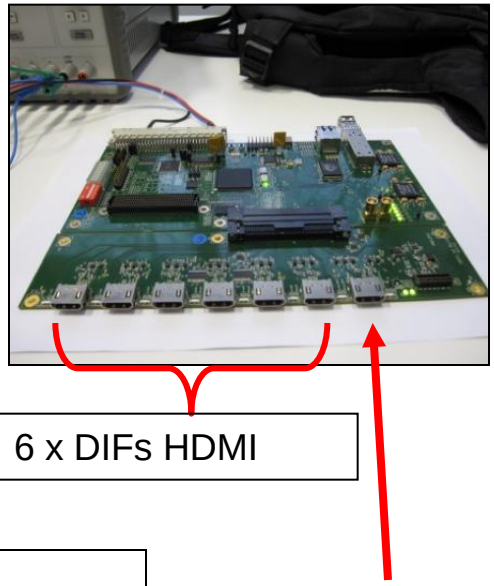
Mezzanine
12 layers
Size : 233 x 52.8 mm
Thickness : 1.81 mm

# GDCC after assembling

- We have received the GDCC last Thursday




First test

Power supply : seems to be correct !

# Conclusion

- Tests will start in the next days
  - They will be done in several steps
    - Check the hardware part : FPGA download, clock and trigger distribution, etc…
    - Firmware tests in LDA mode
      - Long term tests
  - Tests of USB, Jtag, VME, DDR2 have less priorities and will be done later (need to write few VHDL bloc)
- GDCC will not be available before April 2013
  - Cross our fingers that there is not a significant problem