### AHCAL LDA

#### André Welker

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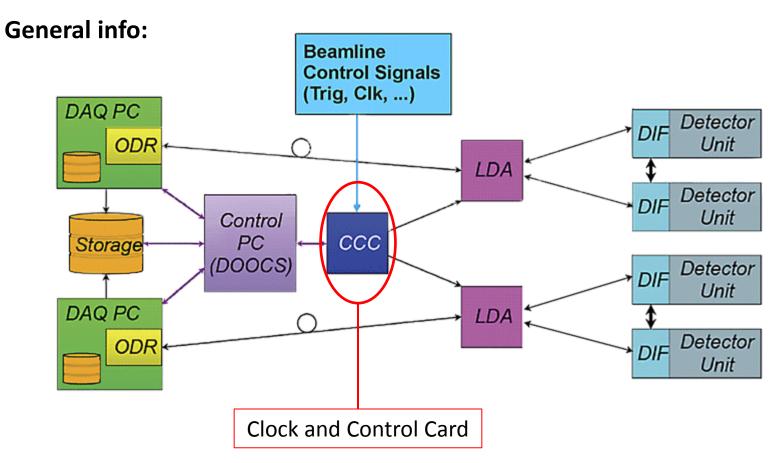
CALICE electronics and DAQ Meeting DESY Hamburg, Dec. 10, 2012





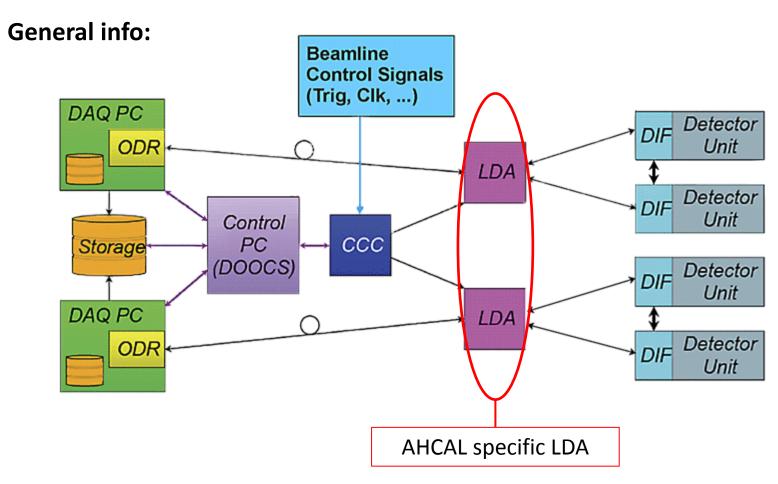
## Readout chain





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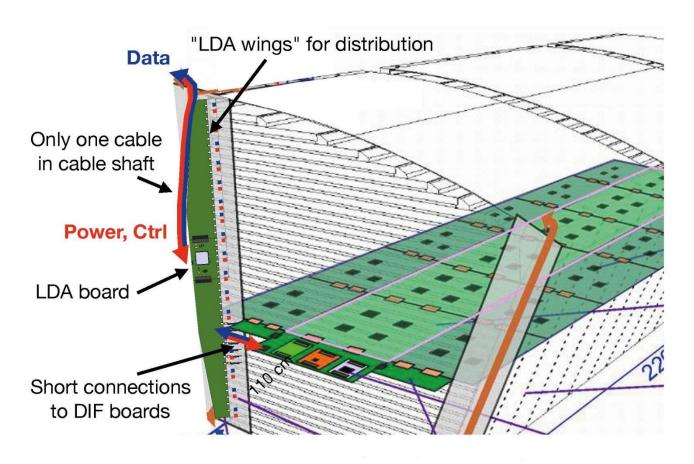




# Cambridge Meeting September 2012



Put LDA board inside cable shaft:



# Cambridge Meeting September 2012



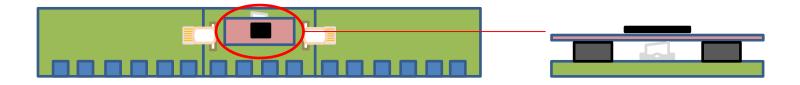
#### **Consists of four separated parts:**

- 1. Three passive PCBs:
  - the 48 HDMI-connectors are on this three PCBs.
- 2. One active PCB:

on this mezzanine we can change our FPGA/processor without problems.

#### **Solution:**

LDA with flex ribbon cable:



# Cambridge Meeting September 2012



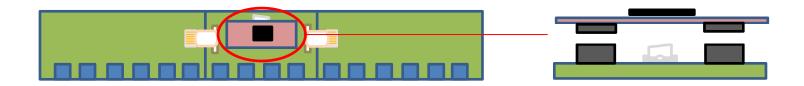
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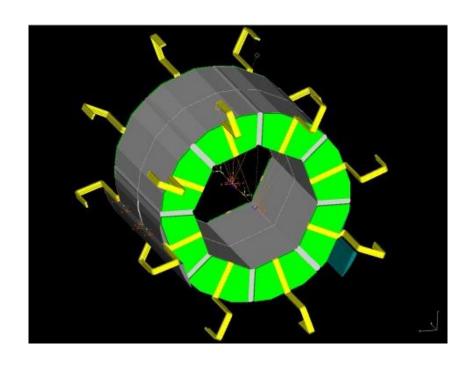
#### **Solution:**

LDA with flex ribbon cable:



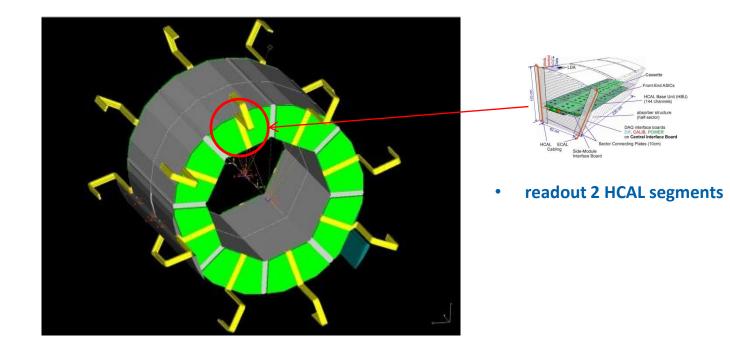


#### **ILD** barrel:





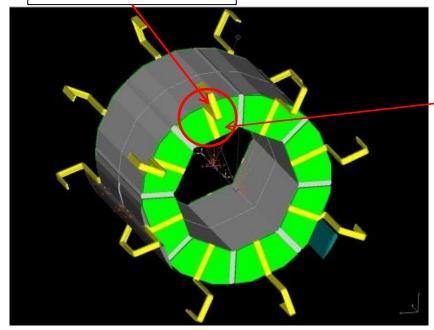
#### **ILD** barrel:

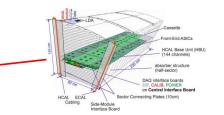




**ILD** barrel:

HCAL shaft with cooling pipes and TPC cables

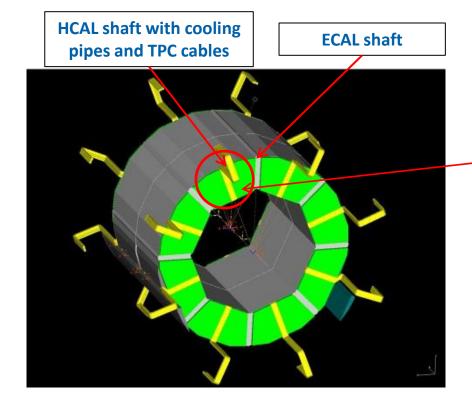




readout 2 HCAL segments



**ILD** barrel:



readout 2 HCAL segments



**ILD** barrel:

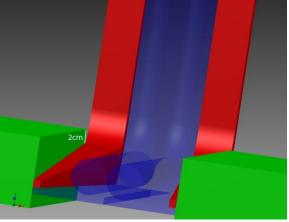
**HCAL** shaft with cooling **ECAL** shaft pipes and TPC cables

Cassette
Front-End ASICa
HCAL Base Unit (HBU)
(14d channels)
Absorber structure
(hulf-acctor)
DAO (lateface boards
DIF CALIB, POWER
HCAL ECAL
Cabing Sich-Module

readout 2 HCAL segments

#### More than anticipated:

48 96 HDMI-connectors on the PCBs.



## Specific AHCAL LDA



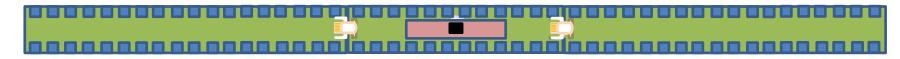
#### **Consists of four separated parts:**

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#### **Solution:**

LDA with flex ribbon cable:



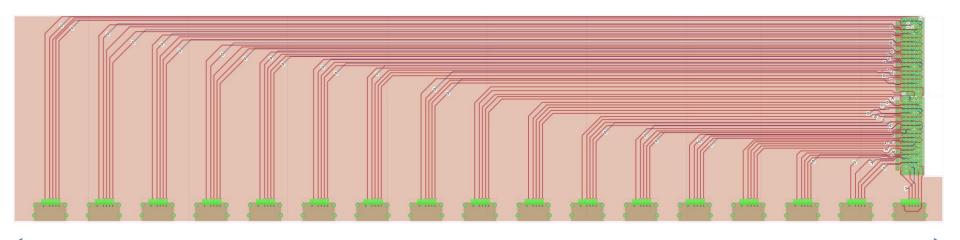
Left Wing Middle Wing Right Wing

# Wing-LDA



#### The three PCBs:

1. Wing with 18 HDMI-connectors routed (without flex ribbon cable):



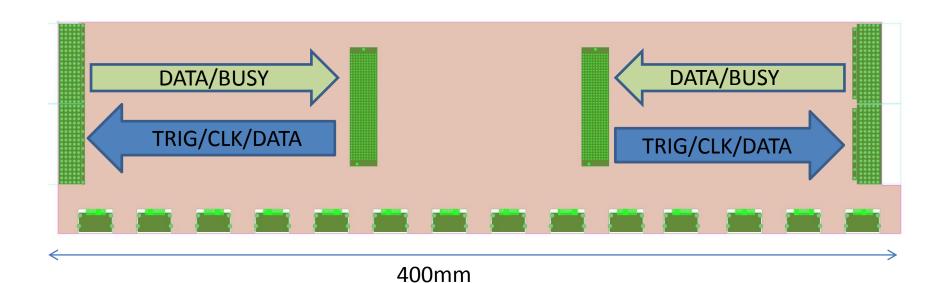
450mm

# Wing-LDA



#### The three PCBs:

2. Middle PCB with 12 HDMI-connectors (without flex ribbon cable):

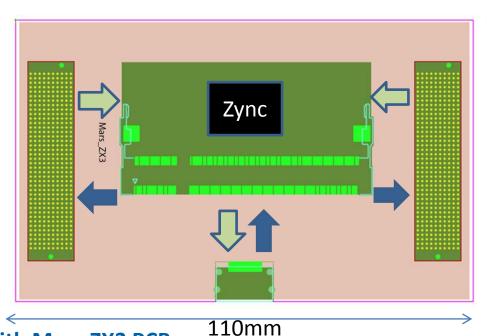


# Wing-LDA



#### The three PCBs:

#### 3. FPGA mezzanine:





- 1. First test with Mars-ZX3 PCB:
  - New Xilinx FPGA/processor (108 I/Os), needed 490
- 2. Later with a FPGA/processor who can handle more I/Os:

## Amount of data



#### Data:

1. 1 SPIROC max. 18696bits (8bits ID, 256bits time stamp, 9216bits TDC, 9216bits Data)

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- 2. Per Slab max. 24 SPIROCs

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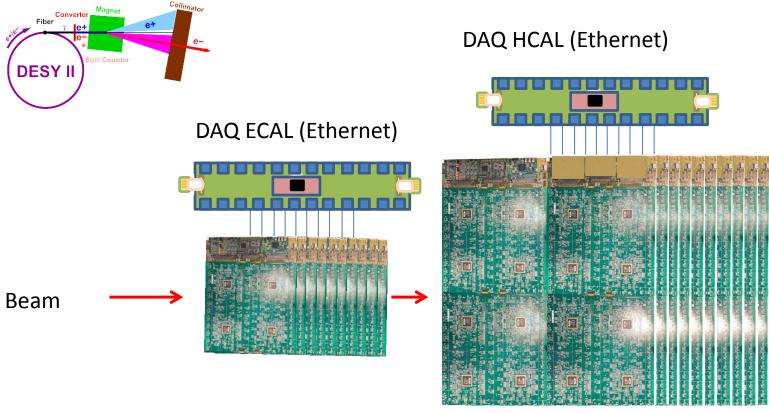


#### Data:

- 1 SPIROC max. 18696bits (8bits ID, 256bits time stamp, 9216bits TDC, 9216bits Data)
- 2. Per Slab max. 24 SPIROCs
- 3. Max. 3 Slabs  $\rightarrow$  72 SPIROCs per DIF  $\rightarrow$  1346112 bits (per 200ms)
  - → 829,9kB/s
  - → 96 x 829,9 kB/s max. 100MB/s with 1GBit Ethernet
  - → 77,03MB/s maximum amount of data

# HBU 2013 TB (DESY)





## Next steps



#### Timeline:

- 1. Finalizing layout for a full-sized functional demonstrator.
- 2. Working on the software/firmware for the LDA.
- 3. Requiring more details on the new DIF firmware.
- 4. Start tests at the Mainz PRISMA detector lab.

So that we are ready for the next TB.

## Next steps



Are there some questions?

Thank you for your attention!