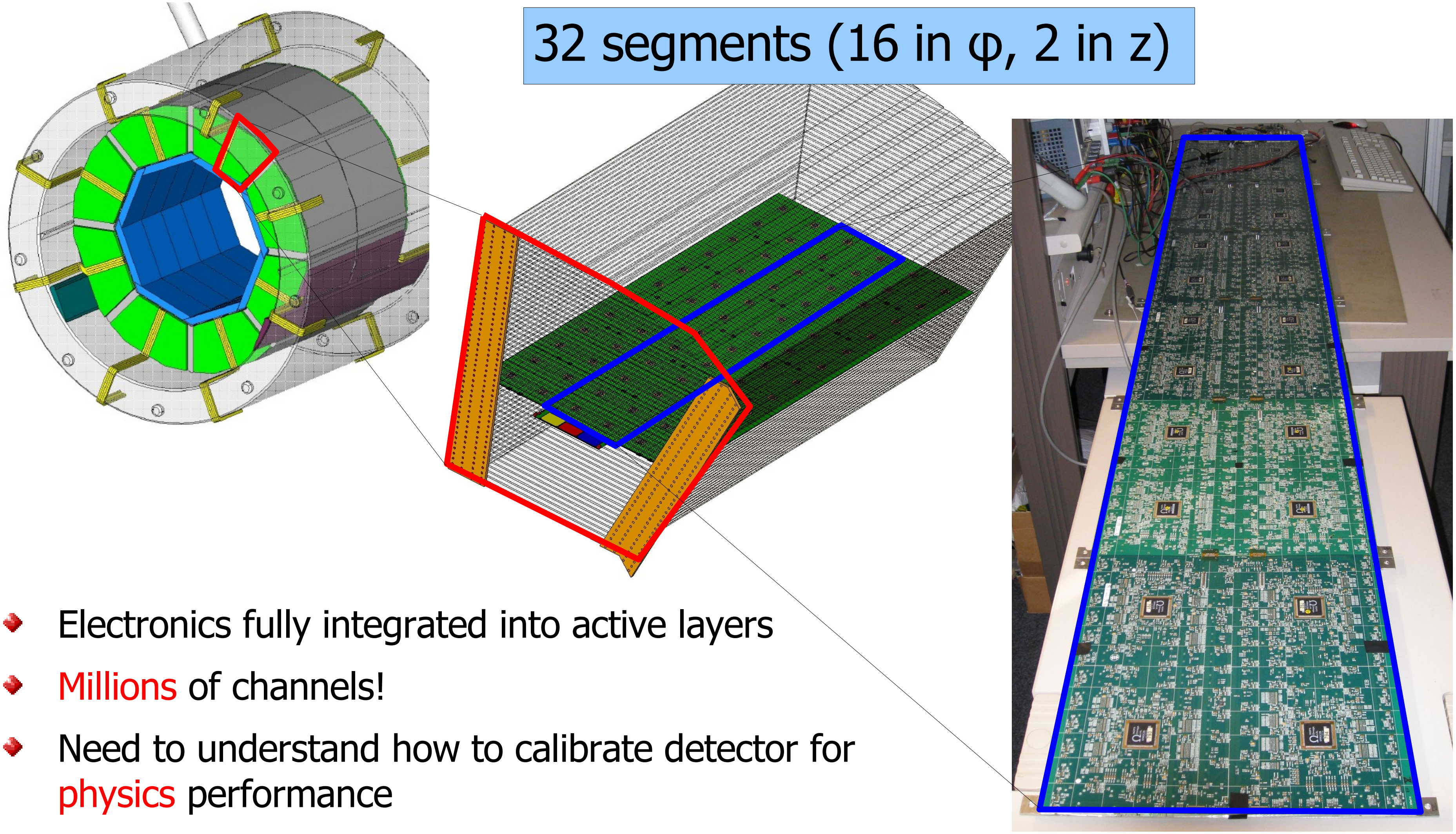
Commissioning of the new AHCAL electronics

Oskar Hartbrich

AHCAL meeting 2012,
December 11th 2012

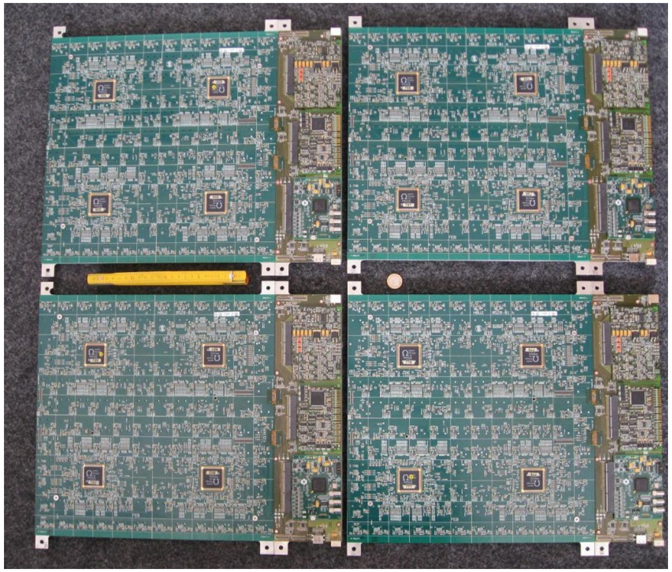
The AHCAL Engineering Prototype

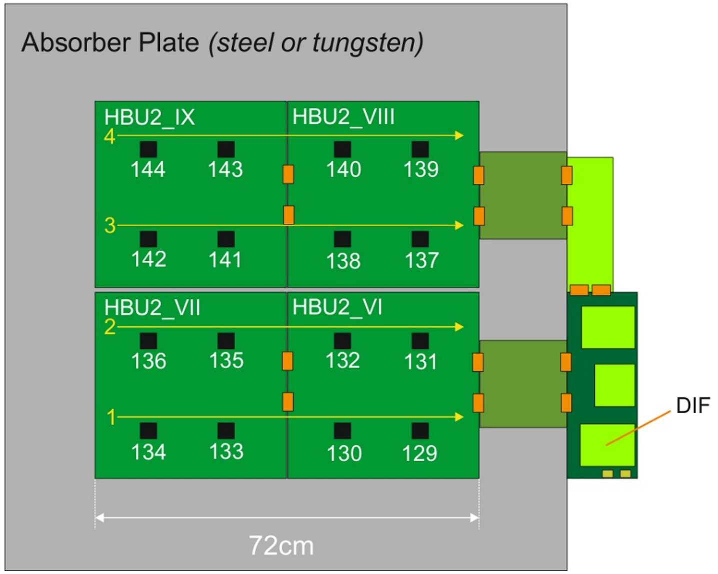


- Electronics fully integrated into active layers
- Millions of channels!
- Need to understand how to calibrate detector for physics performance
- Calibration expertise grows with size of prototypes

Cern Testbeam Layer

- Four new HBUs for an active Engineering Prototype layer for CERN hadron testbeam
  - 576 channels
- Latest revision of HBU2
  - Minor fixes from original HBU2 layout
- 16 SPIROC2b ASICs for the full layer
- Using many SPIROC features:
  - Autotrigger
  - Time stamping
  - External trigger validation
- Factor 8 in complexity compared to previous setup
  - Routines needed to configure and calibrate current (and future) setups.
  - Develop, test and improve commissioning procedures





Steps in Commissioning

- Create Tilemaps (group tiles by bias voltage)
- Configure bias voltages for each individual channel
- Adjust preamplifiers for homogenous SiPM response
- Calibrate autotrigger thresholds
- MIP calibration
- Calibrate TDC

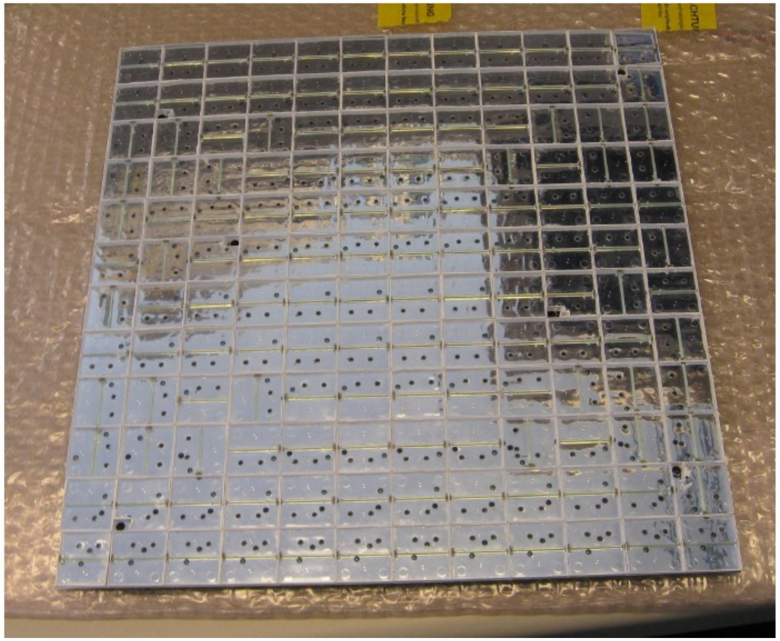
- ... Lots of parameters!
- Need to know:
  - Which parameter needs to be configured on which level?
    - Channel-/Chip-/HBU-wise?
  - What causes these differences?
  - How far do we get with clever averaging and extrapolation of measured subsets?

Tile mapping and assembly

- Physics: uniform calorimeter performance
- But tiles are not uniform! (e.g. bias voltage)

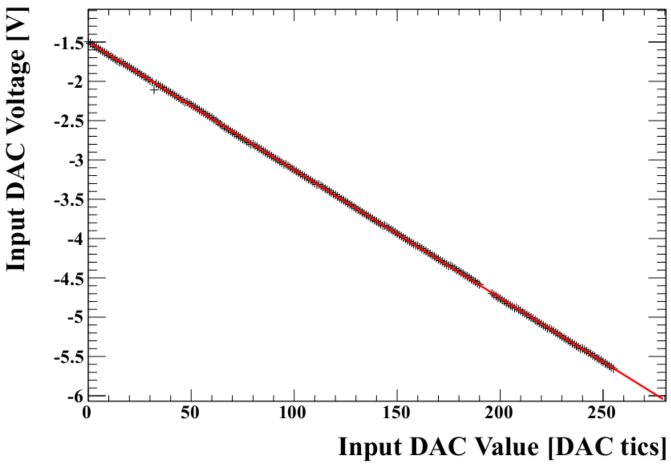
- Two different batches of ITEP tiles used
- Only enough "new" tiles for 3 HBUs
  - Better gain, better SPS
  - Bias voltage incompatible with "old" batch
- One HBU equipped with older tiles
  - Highest gain tiles equipped near beam axis for best performance near shower core
- Manual mapping and assembly
  - Mapping could be automated in software
  - Assembly still manual
- Takes ~1h per HBU (1 person)

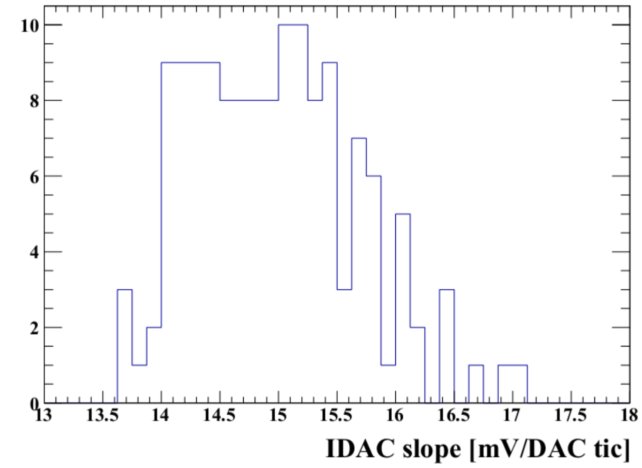
-> Manageable even for bigger prototypes



SiPM bias voltage

- Input DACs for channel-individual bias voltage adjustment
- Generates 0-5V in 8bit, working against the main HV supply of that ASIC
- Always on (no power pulsing) -> low power design
  - Causes channel to channel slope differences
  - Need to measure this for each channel individually (and manually)
    - Need efficient procedure!
- Good linearity enables fast manual procedure
  - 3 points, 45min for a full HBU
  - Would be faster if integrated on ASIC testbench before assembly onto PCB
- Achieved final bias accuracy of 20mV
  - Only slightly worse than 1 LSB
  - Would be 120mV without calibration





Checklist

Goal: uniform detector response

- Individual bias for uniform lightyield per tile ✓

Next step:

- Uniform cell gain

Preamplifier Setup

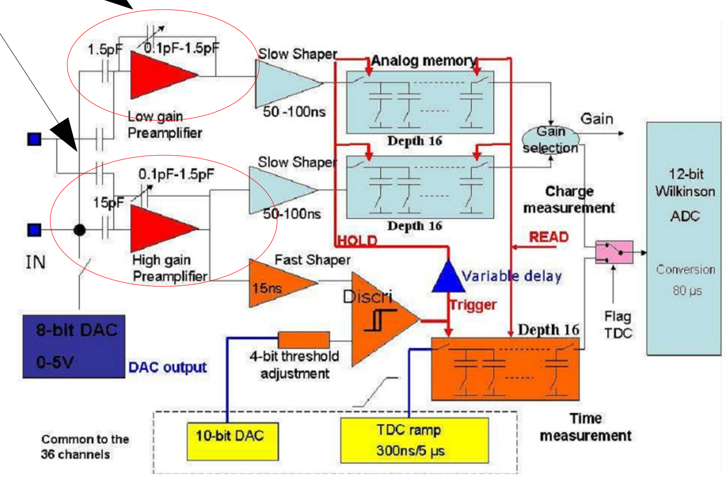
- Tile MIP response depends on tile lightyield (in pixels/MIP) and SiPM gain (in charge/pixel)

  -> Configure preamplifiers to equalise cell gain

Cell gain:
SiPM gain * Preamp gain

- Preamplifiers configurable per channel
  - Feedback capacity range 25-1575fF, 25fF steps (6bit)

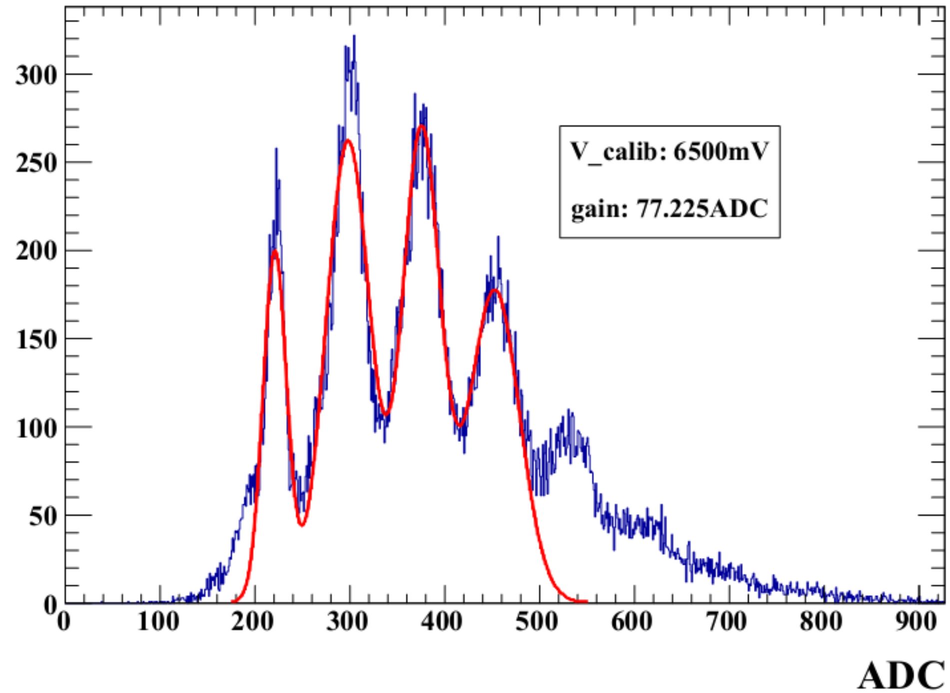
- To calculate equalised preamplifier setup:
  - Get SiPM gains from SPS fits
  - Measure precise preamplifier dependence



Gain from single photon spectra

- Measure SiPM gain at reference preamplifier setup
- Using internal LED system
  - Up to 20 different LED voltages needed
    - Very inhomogeneous LED output
    - LED trigger pulse degradation across HBU
  - Needs high statistics

    -> 4-8h for full gain calibration

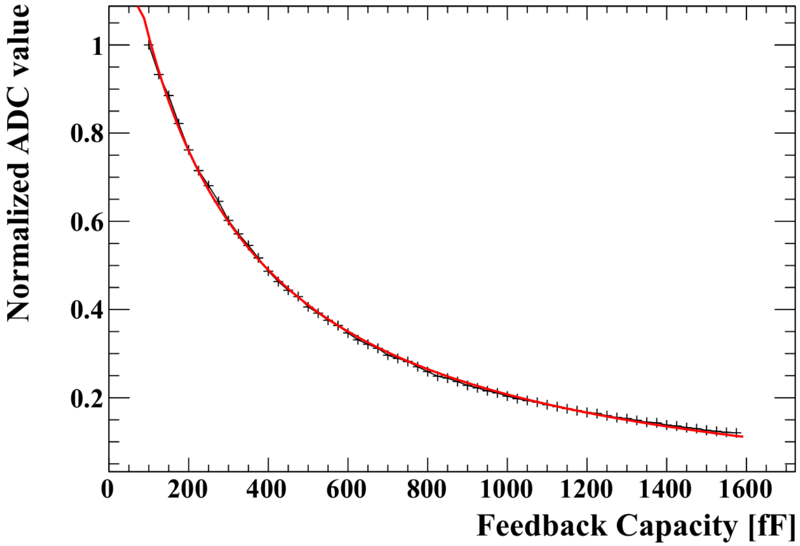


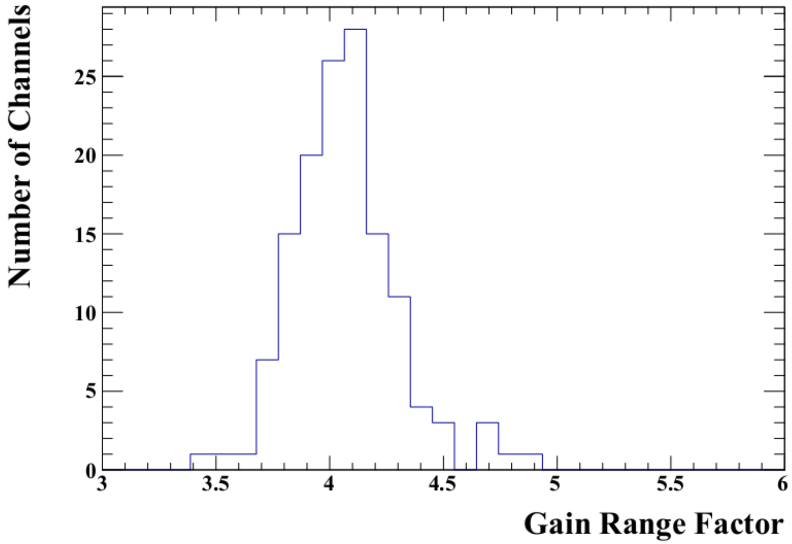
Preamplifier Setup

- Preamplifier curves scanned for each channel
  - Using LED system to generate signals
- Cannot scan full HBU at once
  - Pedestal shift (ASIC effect) warps signal
  - LED output not homogeneous across HBU
  - Needs manual setup
- 2h setup + 4h of measurement per HBU

- Is channel individual measurement necessary?
  - One measurement per chip might suffice
  - Averaging already used for non convergingt channels

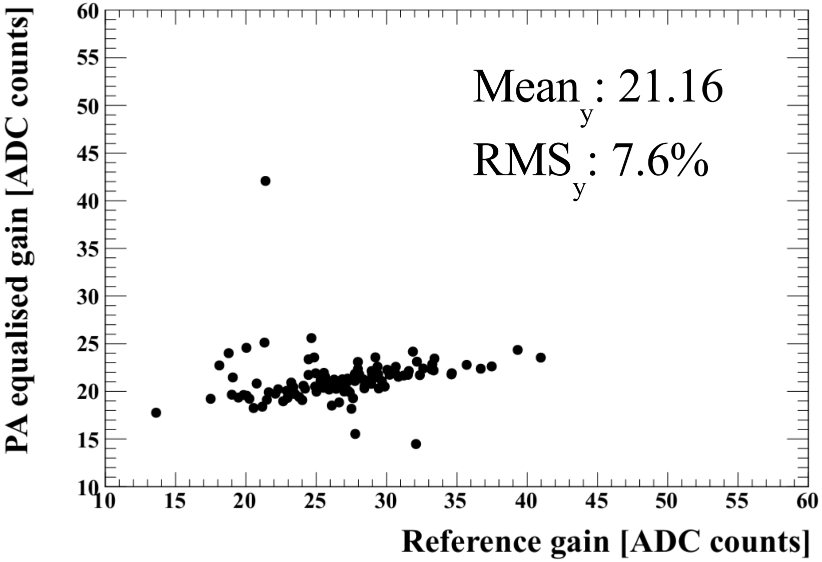
    -> results look good anyway!
  - Improvements in ASIC design?
  - ASIC testbench?





Preamplifier Setup Results

- Comparison of cell gains before/after preamplifier setups shows good improvement in gain spread
  - Results in good MIP uniformity
- Gain calibration runs take too much time
  - Manual measurement setup unfeasible for bigger detectors
- Improvements needed:
  - In ASIC: Fix pedestal shifts -> need less SPS statistics (fixed in SPIROC2c?)
  - In LED system: Improve output homogeneity -> need less LED voltages
  - In DAQ: dynamic scripting could automate procedure



Checklist

Goal: uniform detector response

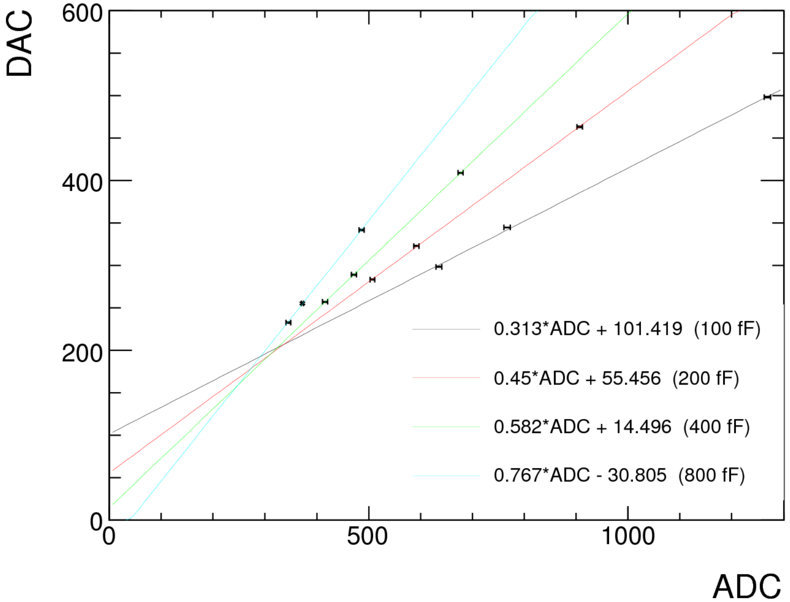
- Individual bias for uniform lightyield per tile ✓
- Uniform cell gain ✓

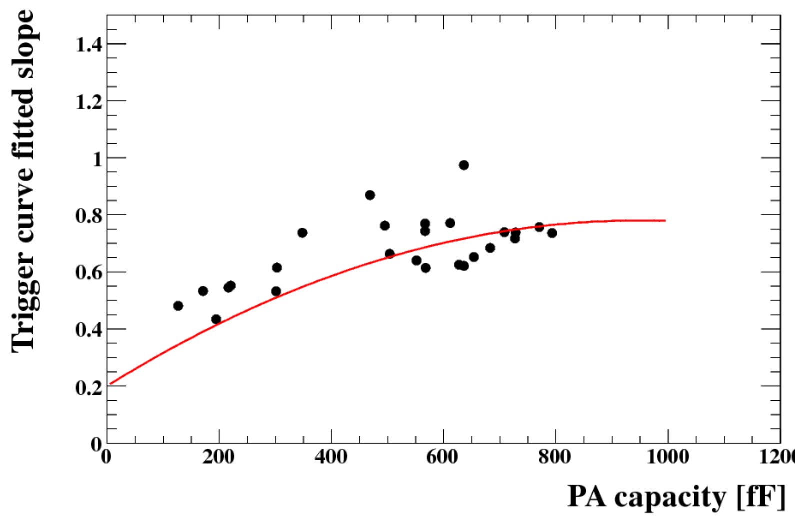
Next step:

- Check MIP uniformity

Trigger Threshold Setup

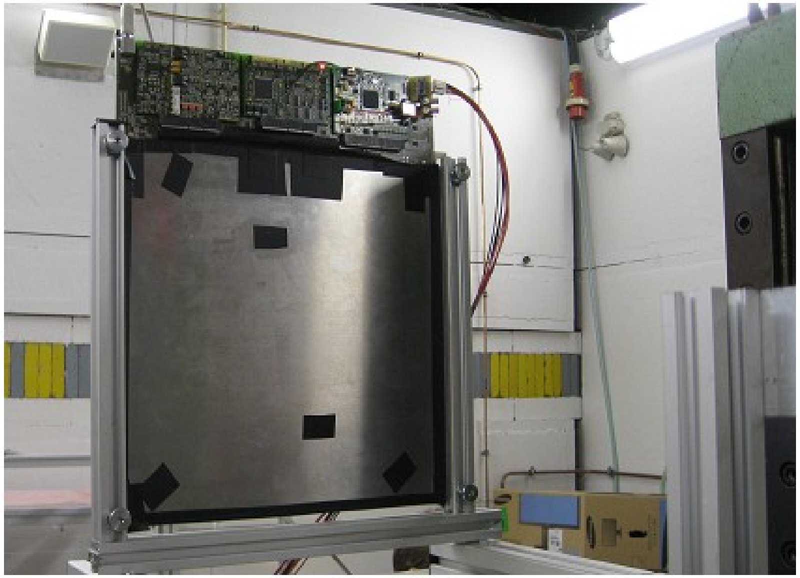
- SPIROC2b detector only reads out hits over threshold
    - Must not lose data to wrong thresholds!
- It is important to meet both MIP efficiency and noise requirements
- SPIROC2b autotrigger:
    - 10bit global threshold per chip
    - 4bit per channel adjustment (not used)
- Preamplifier gain setup alters its bandwidth
    - Channel threshold depends on preamplifier feedback capacity
- Charge injection causes different pulse shapes than real SiPM signals
    - Difficult measurement
    - Understood well enough to set thresholds at CERN testbeam

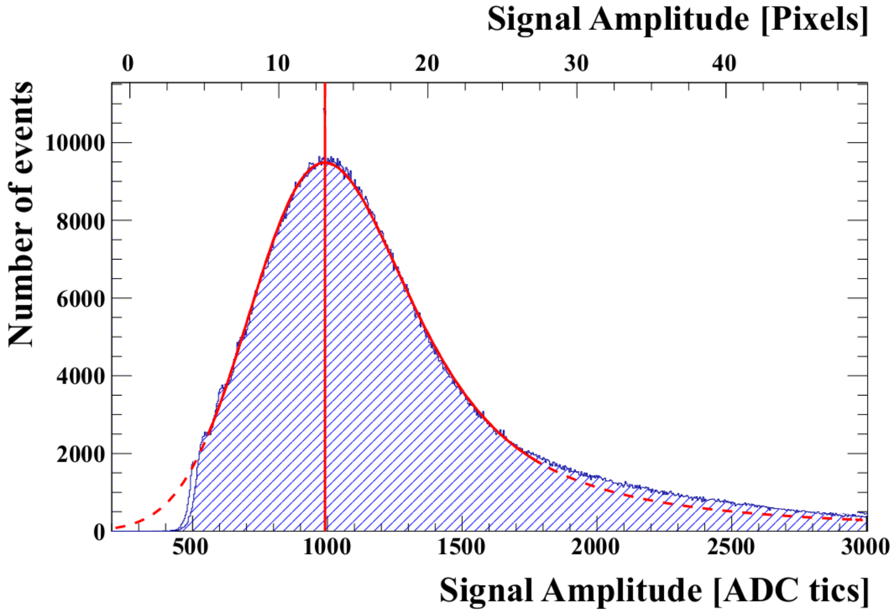




MIP Calibration

- MIP calibration in DESY-II electron testbeam
- 2-4GeV electrons
  - Response similar to MIPs
- Every channel on every HBU scanned separately
  - Huge time effort by many people!
- ADC spectrum fitted with Landau-Gaussian convolution
  - MIP value defined as most probable value from fit
- External validation confirmed to work in testbeam conditions
  - Discards auto triggered events if not coincident with external signal (e.g. scintillator)

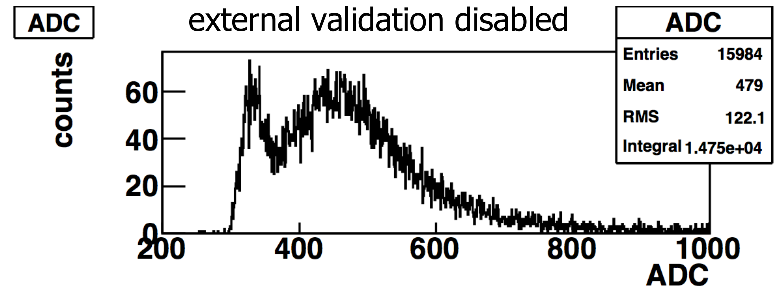


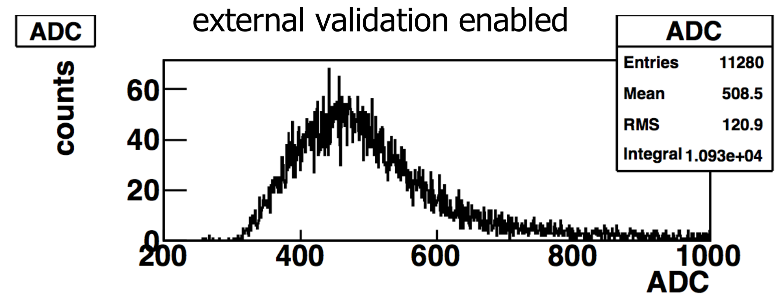


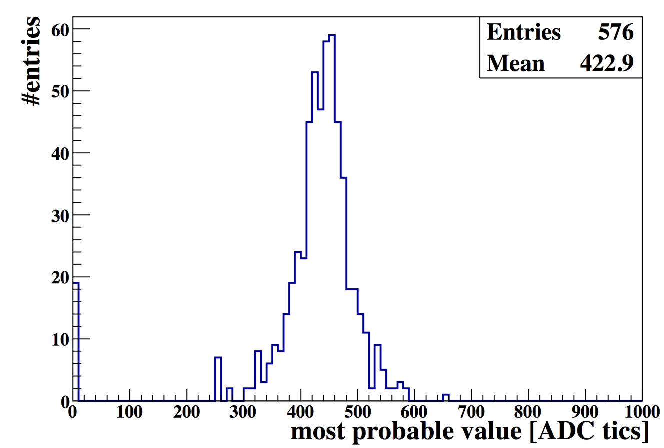
MIP Calibration Results

- External validation shows nice suppression of dark rate noise
- Fitted MIP positions show narrow distribution
  - Still a lot broader than gain distribution seen before
  - Lightyields non-uniform from temperature/bias voltages?
- Reference MIP calibration obtained for cross calibration and comparison with CERN data

- 10min/tile (~100h raw measurement time!)
- Limited by readout speed
  - Stack HBUs
  - Widen beam to hit multiple tiles?







Checklist

Goal: uniform detector response ✓

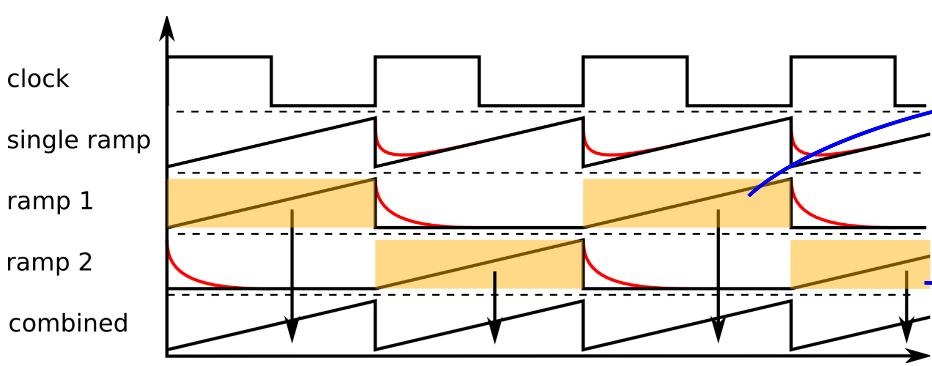
- Individual bias for uniform lightyield per tile ✓
- Uniform cell gain ✓
- MIP uniformity ✓

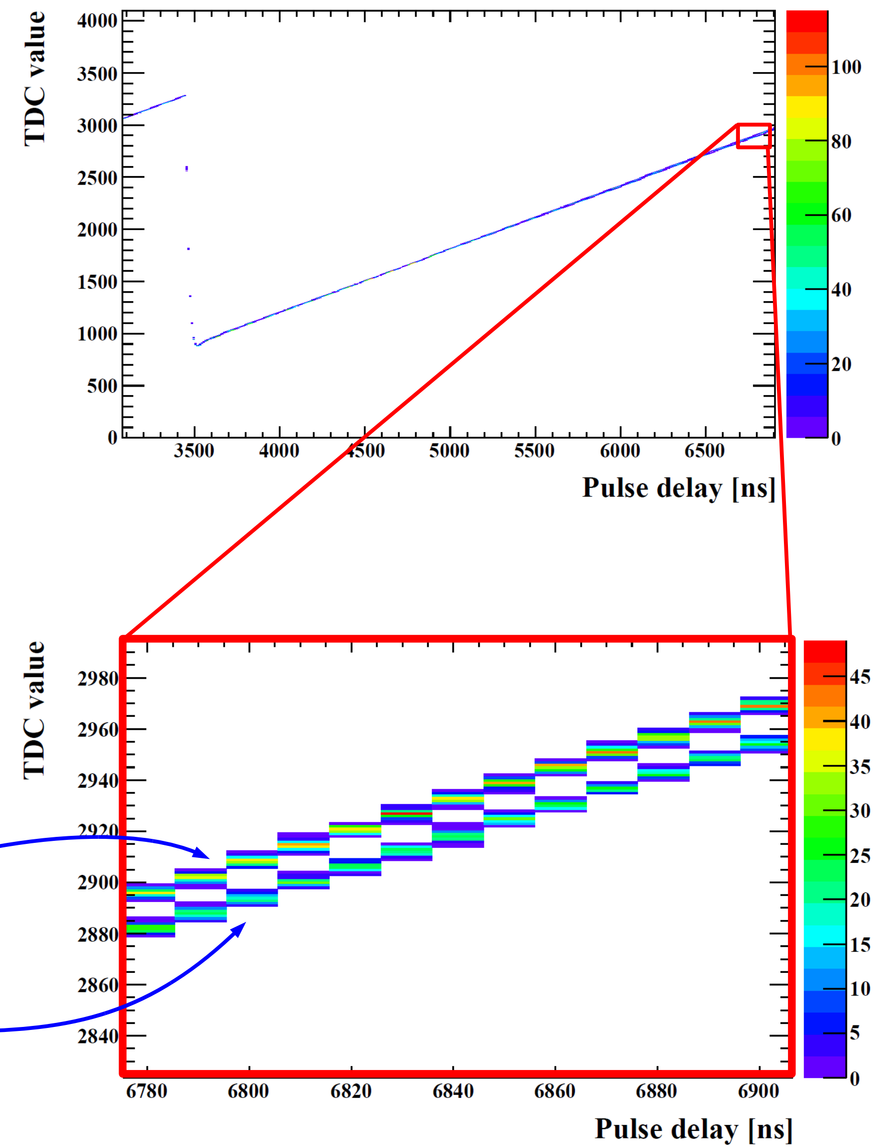
Ready for physics!

- But we also want timing: TDC calibration

TDC Calibration

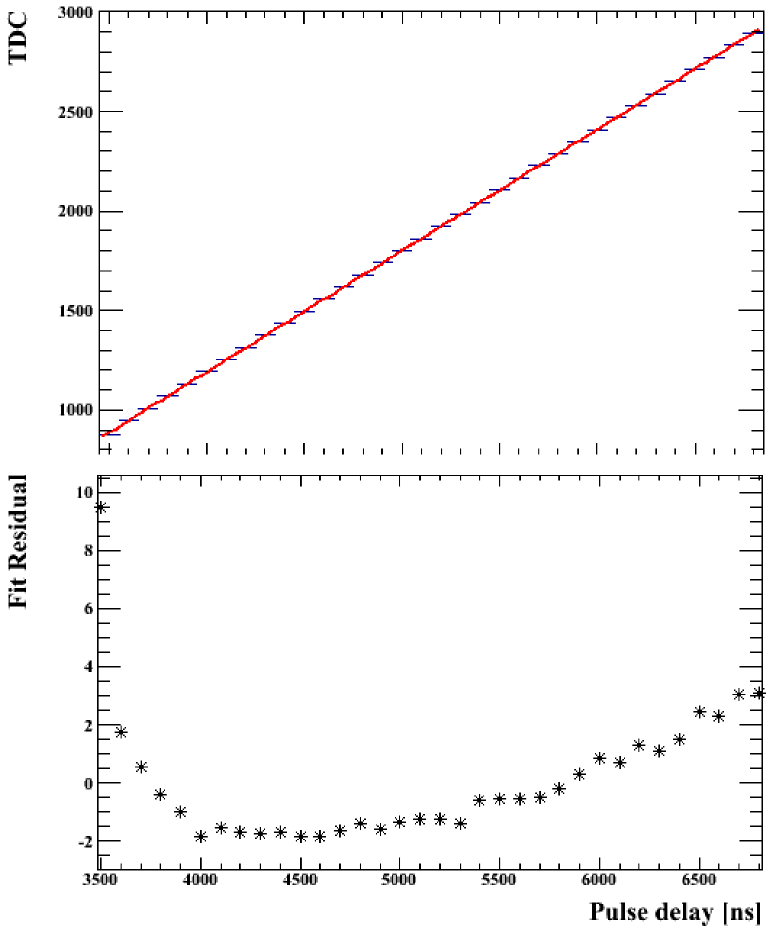
- TDC Calibration using charge injection
  - Pulse generator triggered by DIF clock
  - Adjusting delay between measurements enables ramp scanning
- Both TDC ramps measured at once
  - BCID (finally!) discriminates between ramps
- Ramps have slightly different heights/slopes
  - Need separate fits





TDC Calibration

- Physics: Hadronic shower timing
  - Need to achieve very good TDC resolution ~1ns (=1bin!)
- TDC ramps generated once in each chip
  - Working hypothesis:
  - TDC ramp shapes the same for all channels in one ship
  - Measured ramp shapes for all chips
  - Correct offsets per channel/cell
- Ramp shape parametrisation under discussion
  - Non linear fit?
  - Lookup table?
  - Details to be worked out



Checklist

Goal: uniform detector response

- Individual bias for uniform lightyield per tile
- Uniform cell gain
- MIP uniformity
- TDC calibration

Work in progress

Summary and Outlook

Summary

- Commissioning of 576 channel layer of the AHCAL engineering prototype was successful!
  - Already found and applied many shortcuts
  - Many ideas for further developments
- Essential step for taking physics data at CERN in November

Outlook

- Utilise EM showers from DESY testbeam to calibrate channel to channel TDC offsets
- Future advances in DAQ software, chip development and general understanding will improve the scalability of the commissioning procedure