CCD And Readout Electronics

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ILC Tokusui Workshop 2012

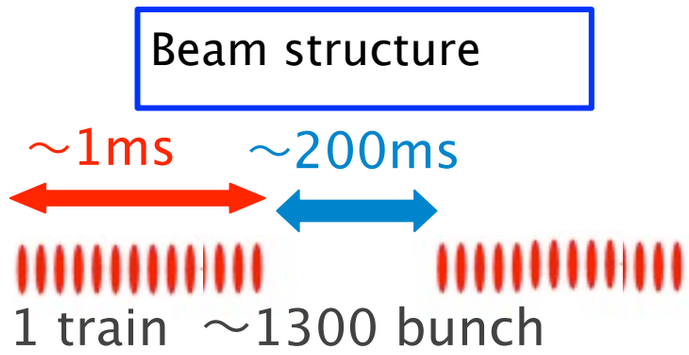
Outline

- FPCCD
- CCD and ASIC Prototypes
- Test Systems
- Results

FPCCD

- Vertex detector
  - -- high impact parameter resolution (near interaction point)
  - -- accurate tagging (pixel occupancy ~1%)

Finely segmented pixel is required.



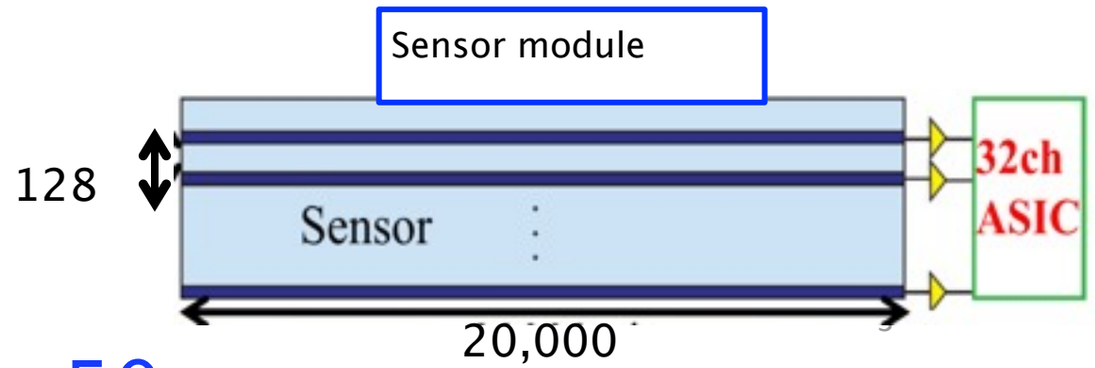
- FPCCD (Fine Pixel CCD) vertex detector.
  - -- pixel size 5x5um^2 (high position resolution)
  - -- fully depleted epi layer : 15um, Si total 50um (high two track separation)
  - -- total number of pixel : 1.6 x 10^{10} (high speed readout)
  - -- inter train readout (no beam induced RF noise)

For FPCCD we need to develop CCD and ASIC.

CCD and ASIC Prototypes

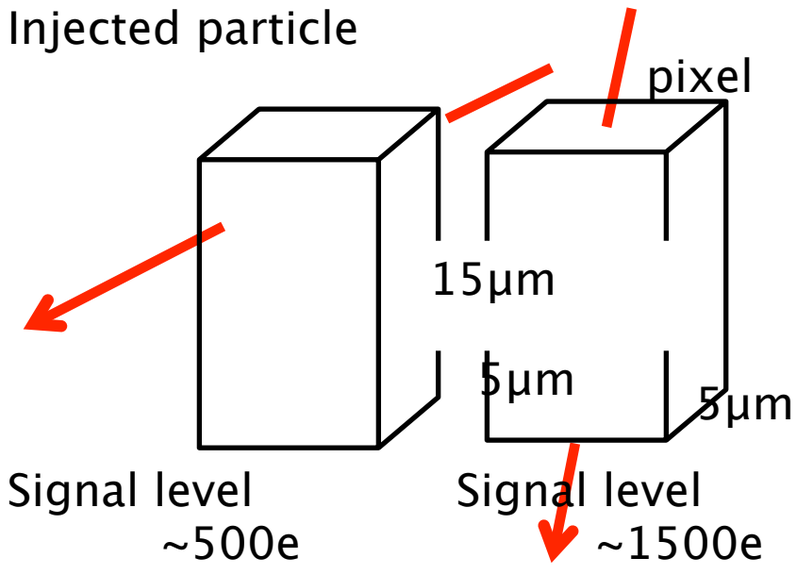
CCD and Readout ASIC Requirements

- Readout speed > 10MPix/sec
  -- using two 5MPix/sec in parallel



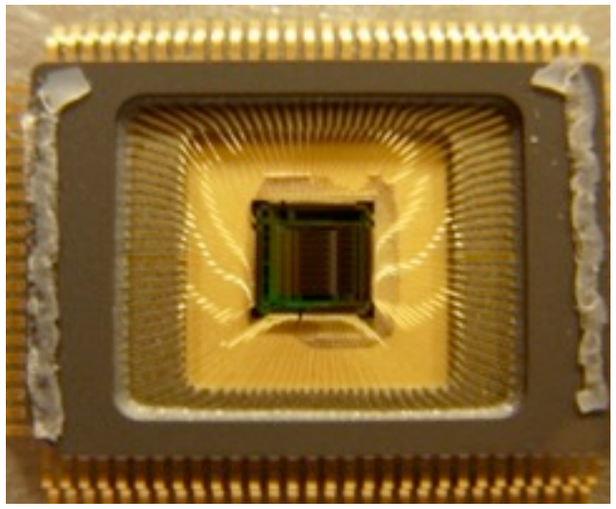
- Signal measurement accuracy < 50 e-
  -- faint signal level ~500 e-
  -- noise + analog to digital conversion accuracy < 50 e-

- Power consumption
  -- for ASIC < 6mW/ch
  -- for CCD < 10mW/ch
  -- placed in -40°C cryostat
  -- total power consumption < 100W



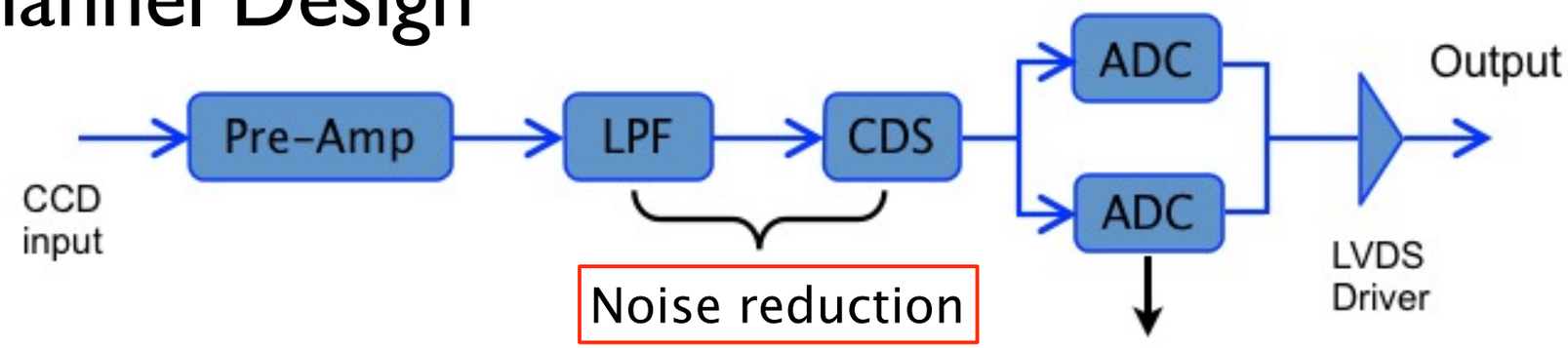
CCD and ASIC designed should have these features.

ASIC Prototype



Chip parameters	2nd prototype	3rd prototype
process	0.35um	0.25um
Chip area	4.3x4.3mm2	3.7x3.75mm2
Gain coverage(from CCD)	12.5~200 (8 steps)	32~64(2 steps)
# of channels	8ch	8ch
Input capacitance form CCD	20pF	3.2pF

Channel Design



ASIC Features And Improvements

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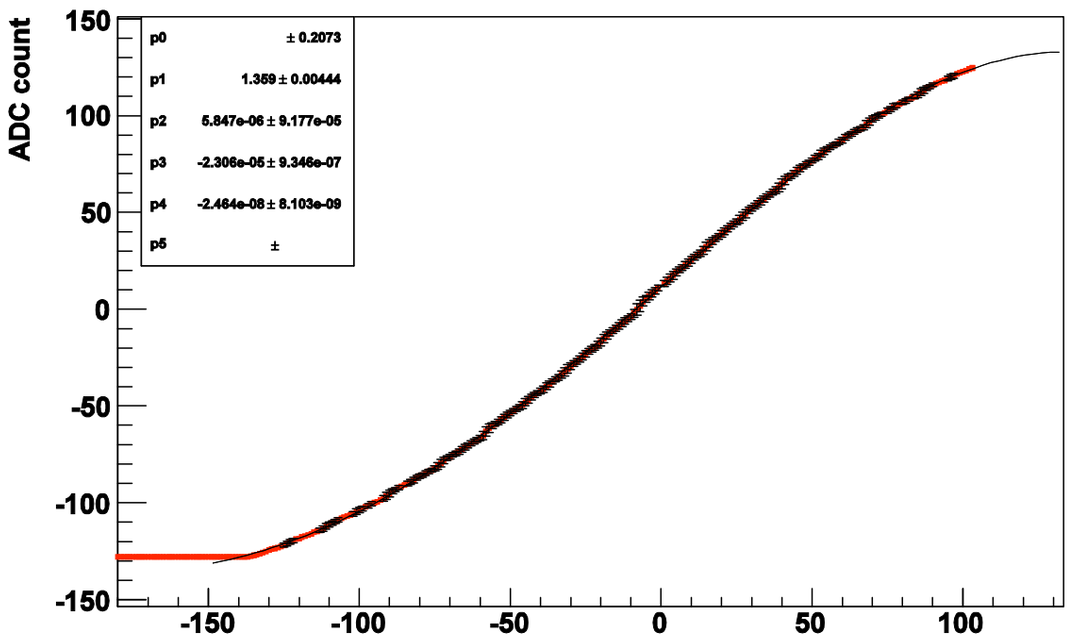
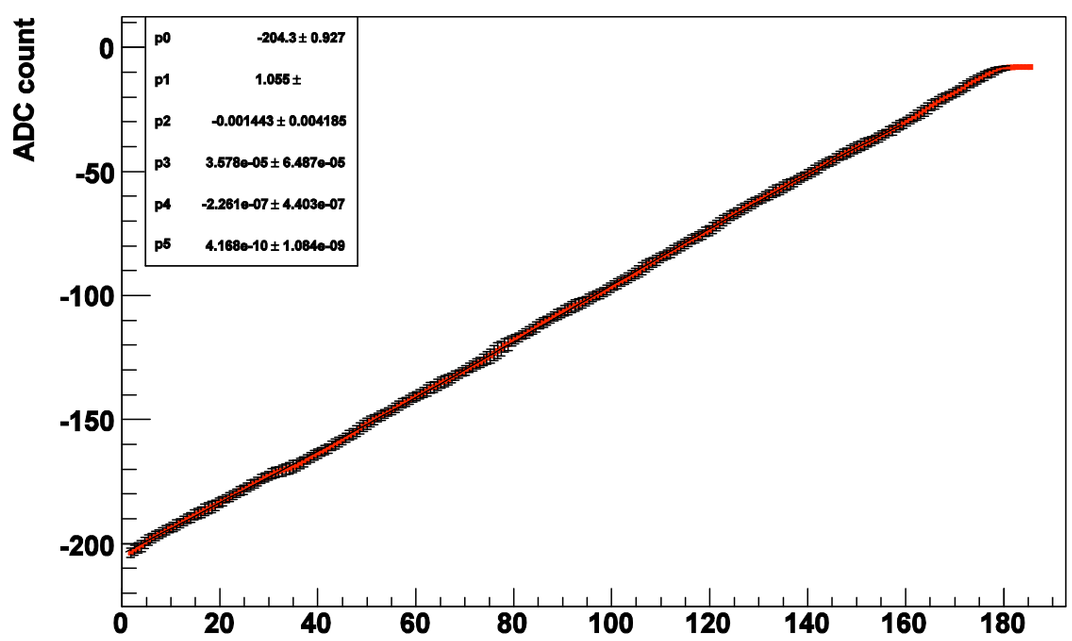
- Power consumption
  - -- improved : 30.6 mW/ch -> 5.8 mW/ch
- INL (Integral non linearity)
  - -- Showed curvatures in linearity.
  - -- Caused upstream circuits.
  - -- improved : 17% -> < 2%

2nd Prototype



3rd Prototype



ASIC Features And Improvements

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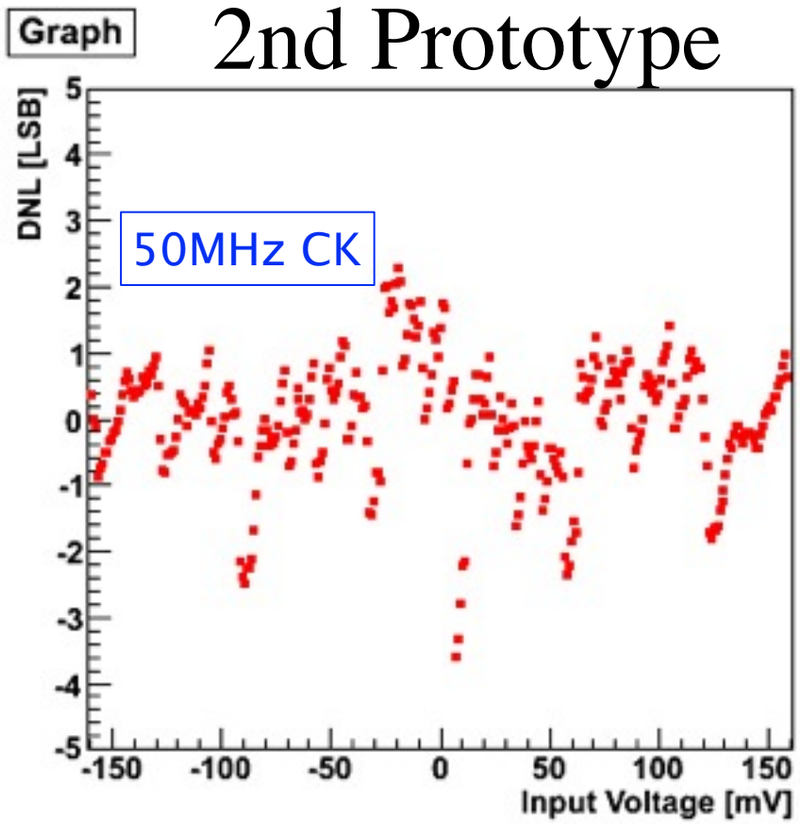
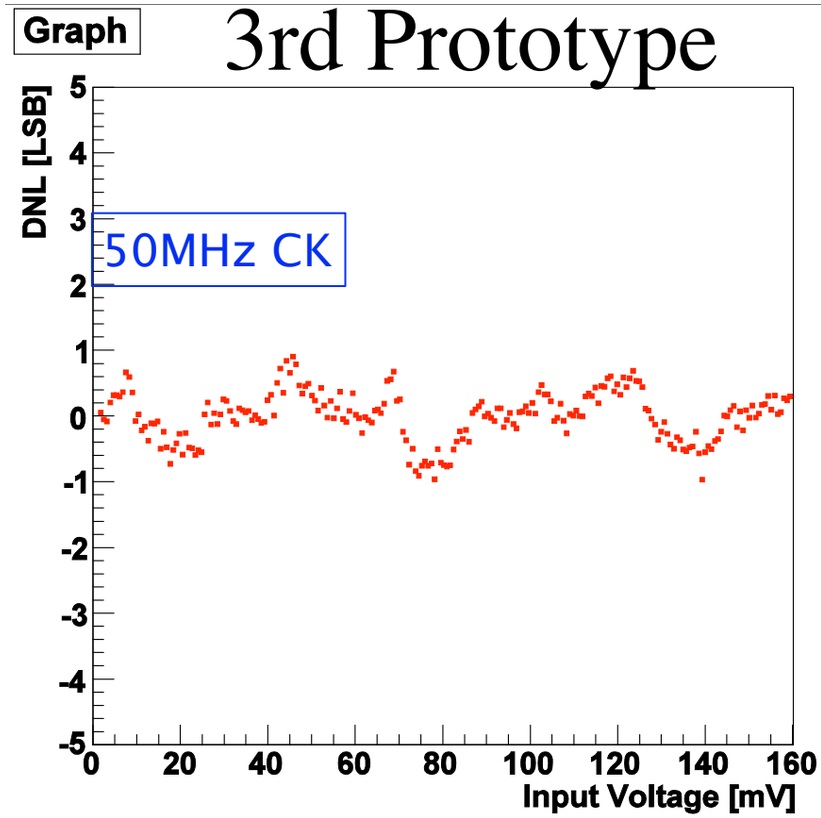
- Radiation tolerance
  -- 3rd prototype implemented DICE-FF radiation hardened by design flip-flop with high single event effect (SEE) immunity.
- DNL (Differential non linearity)
  -- due to displacement from bit weight it becomes meta-stable at bit change. Thus causes bit jump at higher frequencies.
  -- improves in 3rd prototype.

2nd Prototype



3rd Prototype



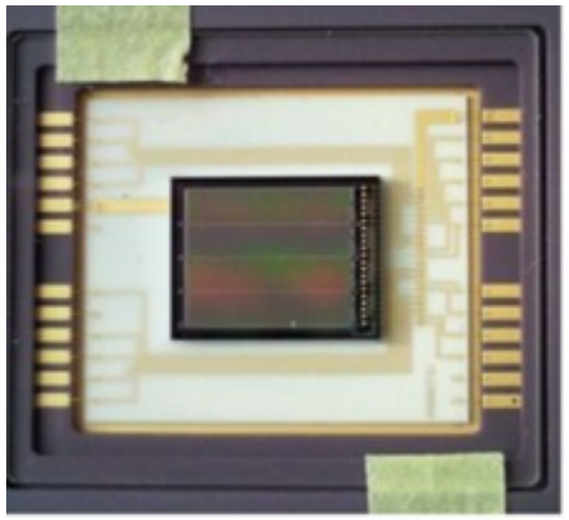
CCD Prototype

Hamamatsu Photonics two phase transfer CCD

- Pixel size 12um x 12um
  - -- chip size :8.2mm(H) x 7.5mm(V)
  - -- thickness : epi layer 15um, Si total 50um
  - -- number of channels : 4

  has been tested.

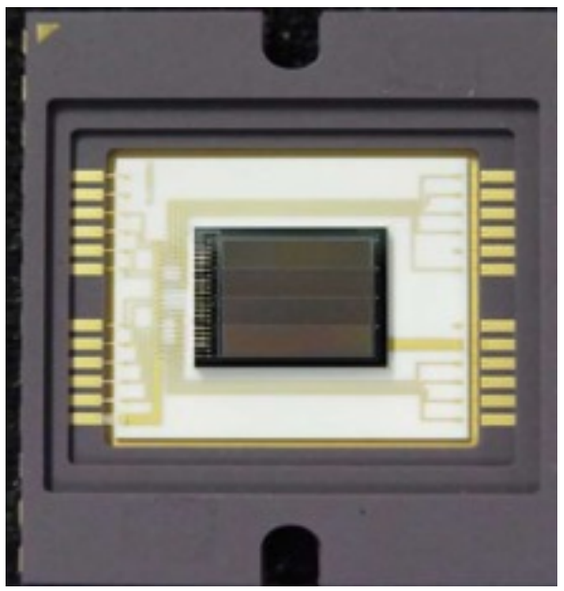
12 x 12 um



- Pixel size 6um x 6um
  - -- horizontal shift register size : 6umx12um
  - -- thickness : epi layer 15um, Si total 50um
  - -- number of channels : 4

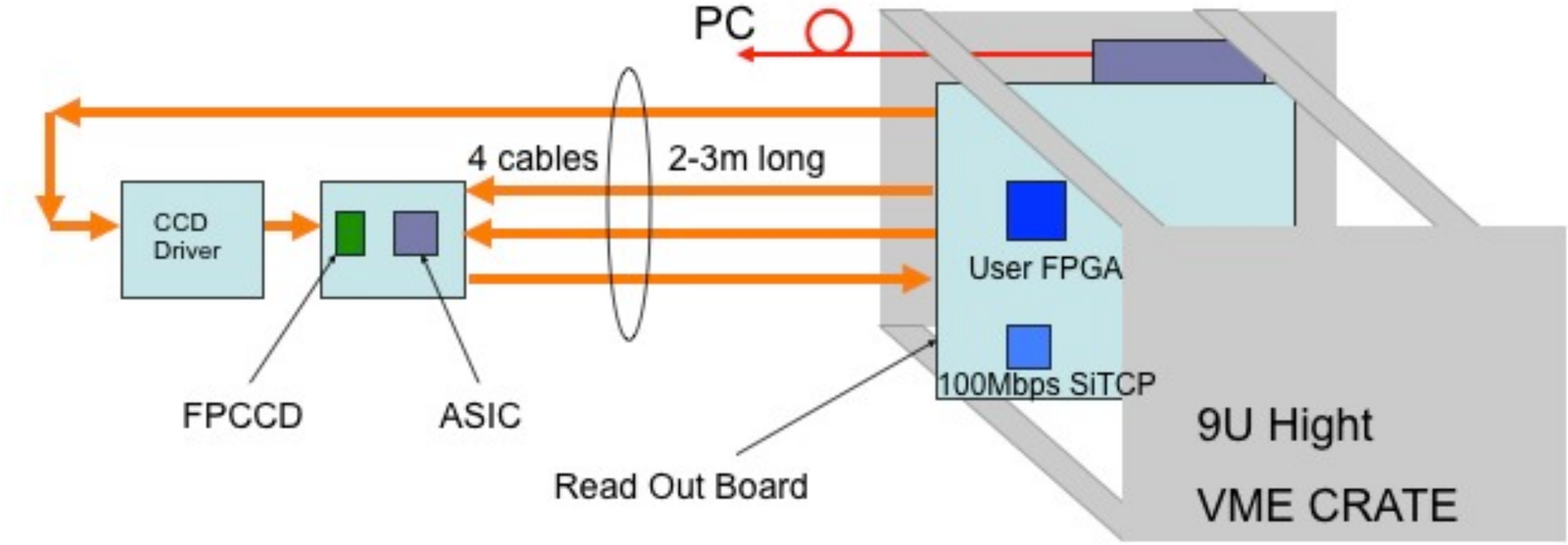
  test is going on.

6 x 6 um



Test Systems

Previous VME Based Test System



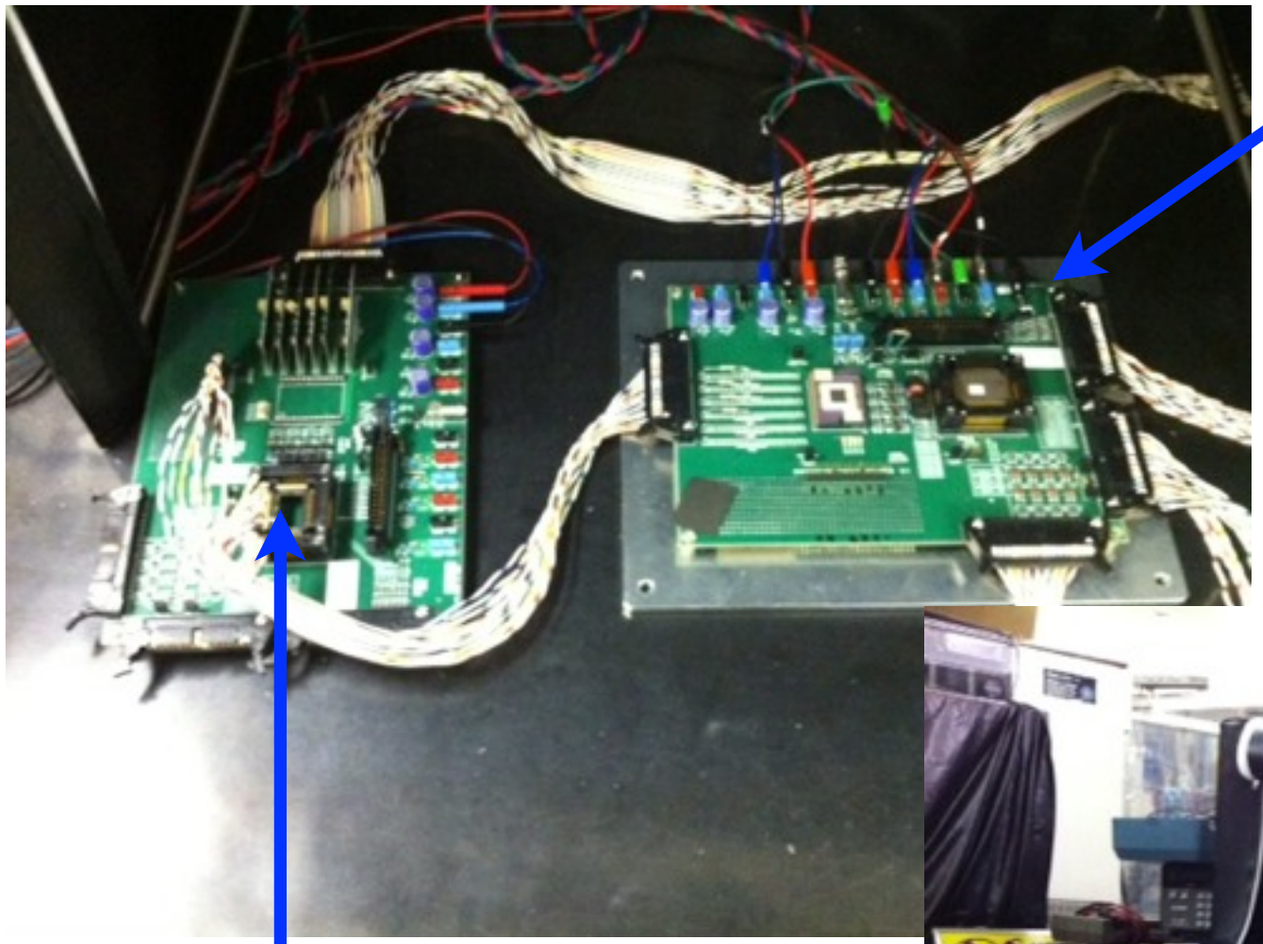
9U Read Out Board (ROB) : too large, especially for Beam Test

Long cables : not easy to detect series of 3 nsec width ADC output pulses

100Mbps SiTCP : too small data rate (planed to change to 1GbE)

Limited number of ROB and VME crate : 2 sites (Tohoku Univ., KEK)

Previous VME Based Test System

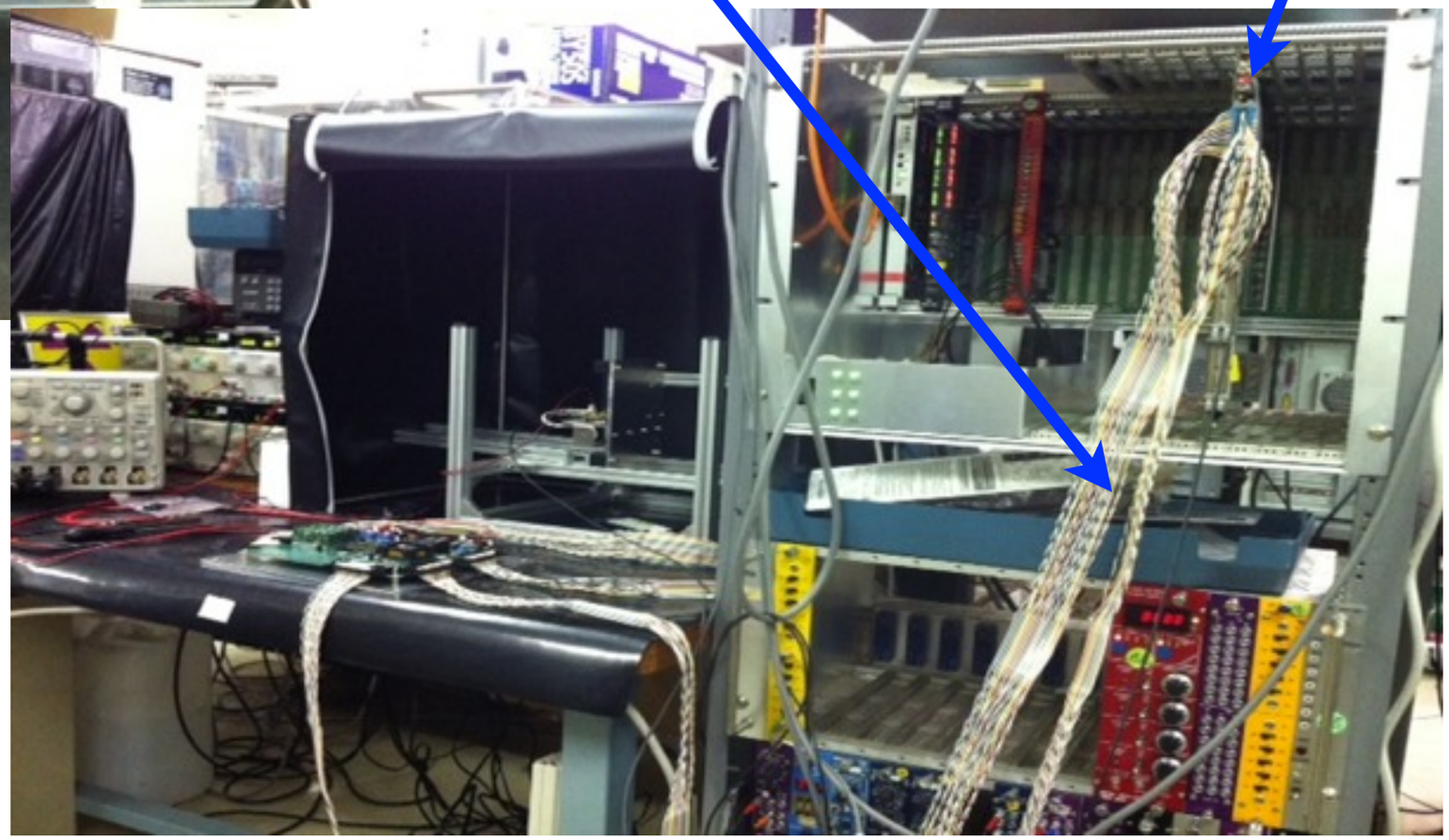


CCD, ASIC test board

Another CCD,ASIC test board dedicated for CCD drivers

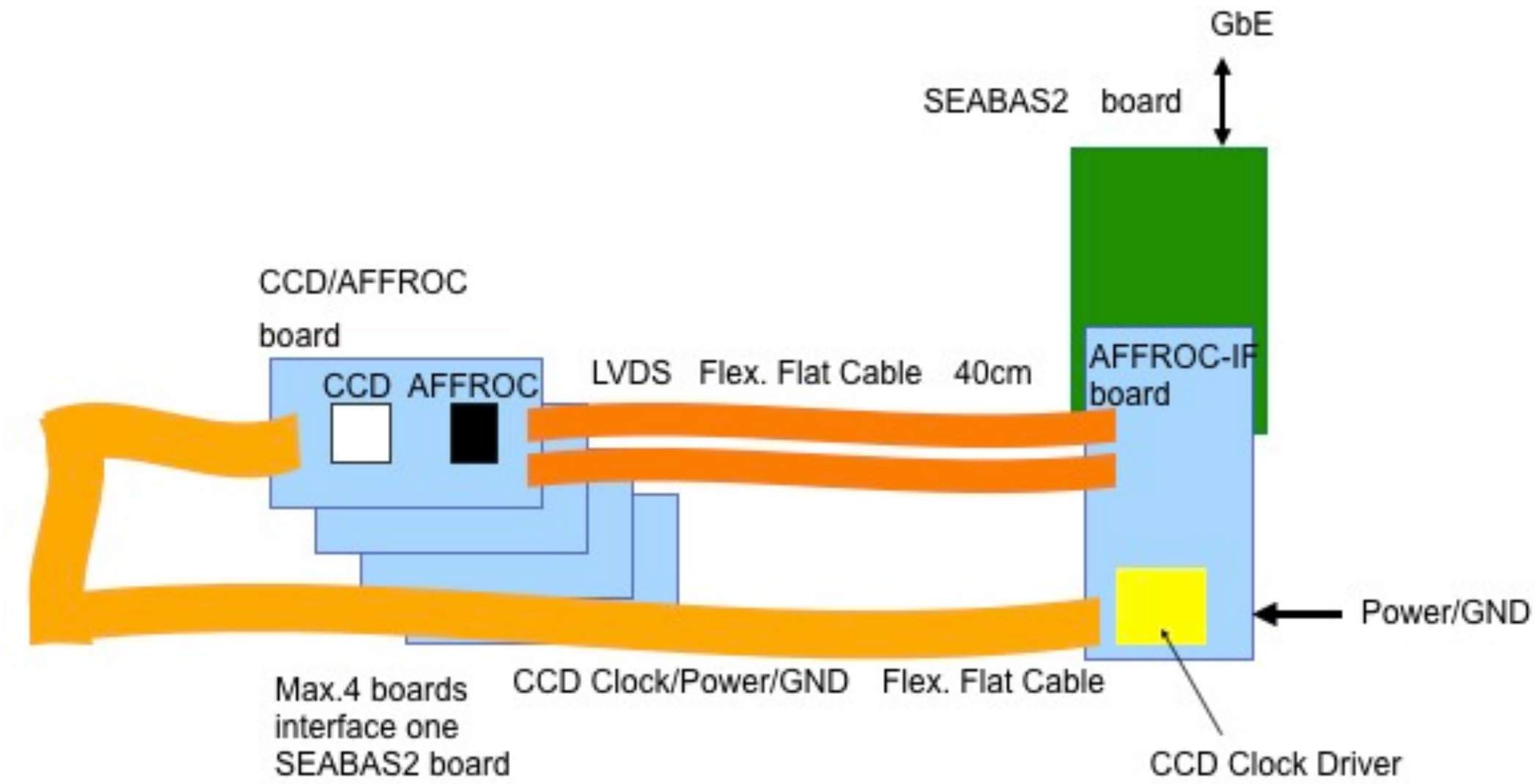
One of the long cables

ROB



SEABAS2 Based AFFROC Test System

AFFROC : Name of the 3rd ASIC



SEABAS2 Based AFFROC Test System

Features

- Employ SEABAS2 (1GbE, ADC and DAC on board, compact size)
- Shorter and less cables (FFC support LVDS spec.)
  -- Reliable operation at 100MHz or higher frequency can be expected by this LVDS cable and AFFROC new feature.
- On board DAC and ADC support automatic testing and self-diagnostics
  -- example: AFFROC linearity test will be automated by using on-board DAC and AFFROC new feature.
- SEABAS1 available for early development of test circuits and programs
- Compact to support Beam Test.
- Additional site: Shinshu University.

SEABAS2 Based AFFROC Test System

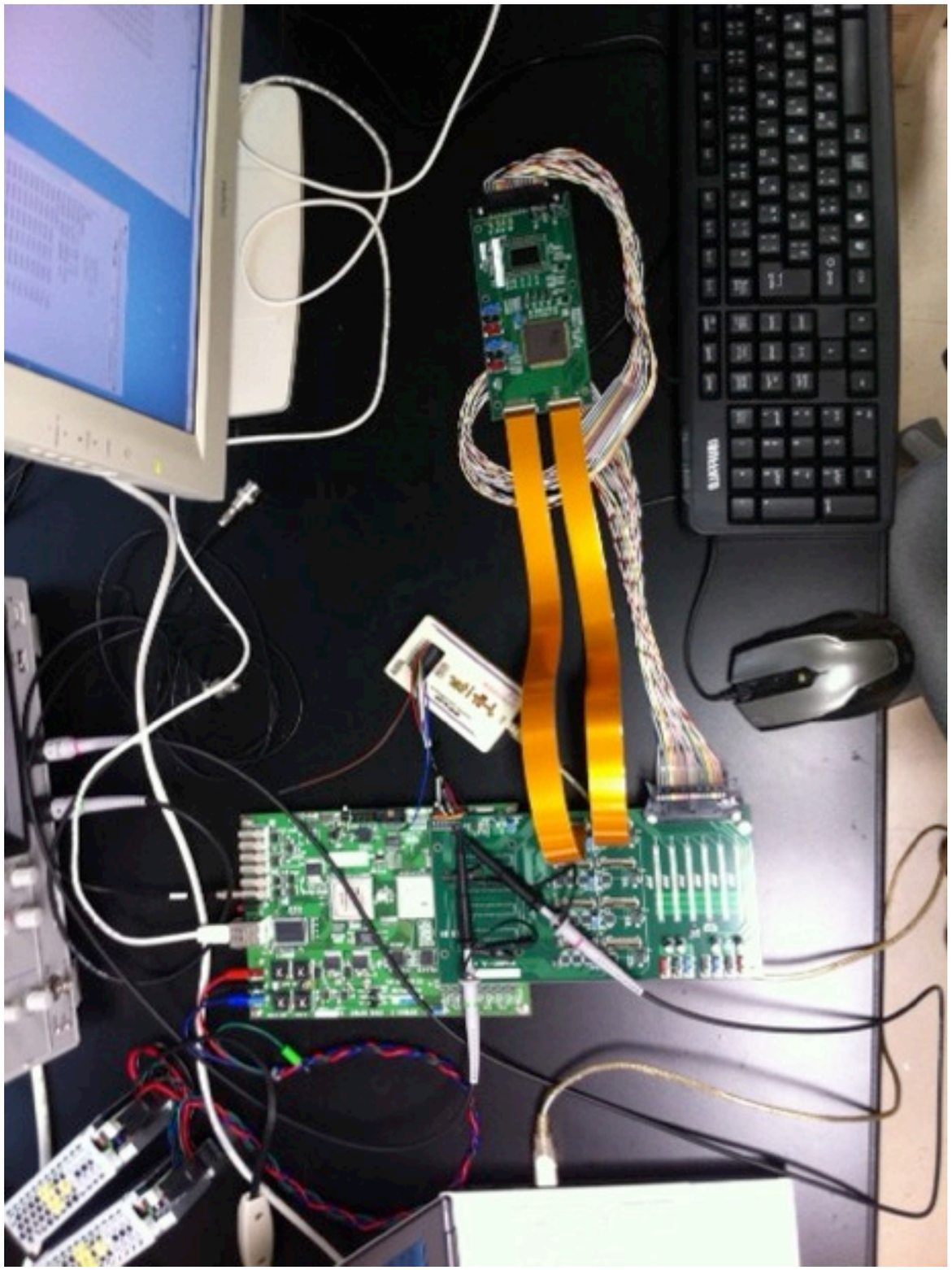
- Employing SEABAS2 saves our development man power and cost.
- User FPGA + SiTCP structure is the same as the previous VME base ROB.
- Most of the logic circuits in the previous test system can migrate to the new User FPGA of SEABAS2 board.

  -- Previous User FPGA : Xilinx Spartan 3A family “XC3S700A”
  1,472 CLB 360Kbit RAM

  -- SEABAS2 User FPGA: Xilinx Vertex 5 family “XC5VLX50”
  7,200 CLB 2,160Kbit RAM

- Logic circuits to support four AFFROC may fit in one SEABAS2 board.
- We will buy 3 SEABAS2 boards at Tohoku. One of them is for SOI but we can use them as multi-SEABAS2 system for beam test to check position resolution and efficiency.
- 1GbE is still bottle neck, to support four CCD+AFFROC, so we need some data compression technology. Or we have multi-SEABAS2 board option.

SEABAS2 Based AFFROC Test System



12 um CCD Test With ASIC Prototype 2

Fe55 X-ray Measurements

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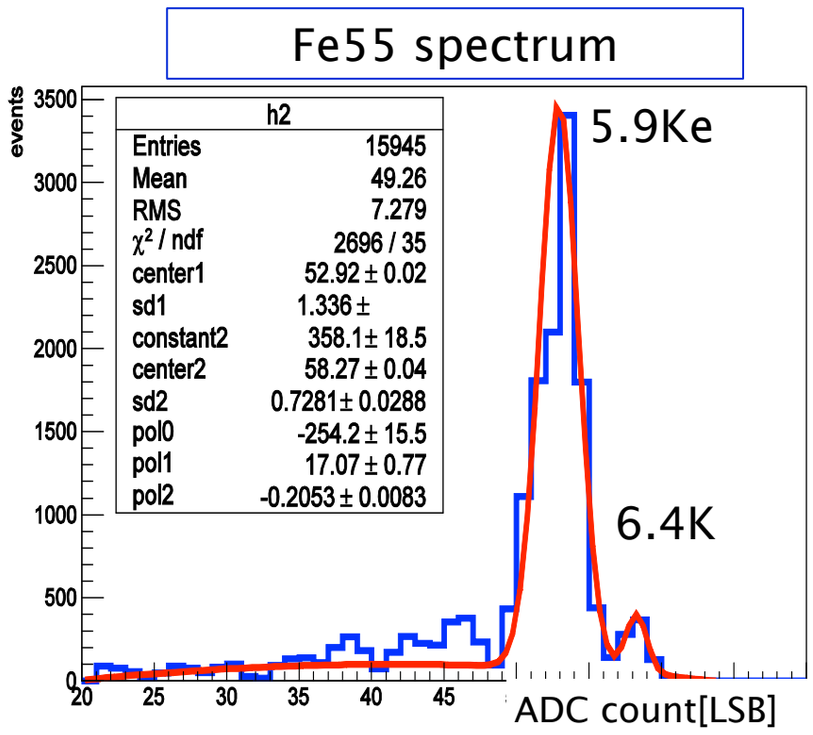
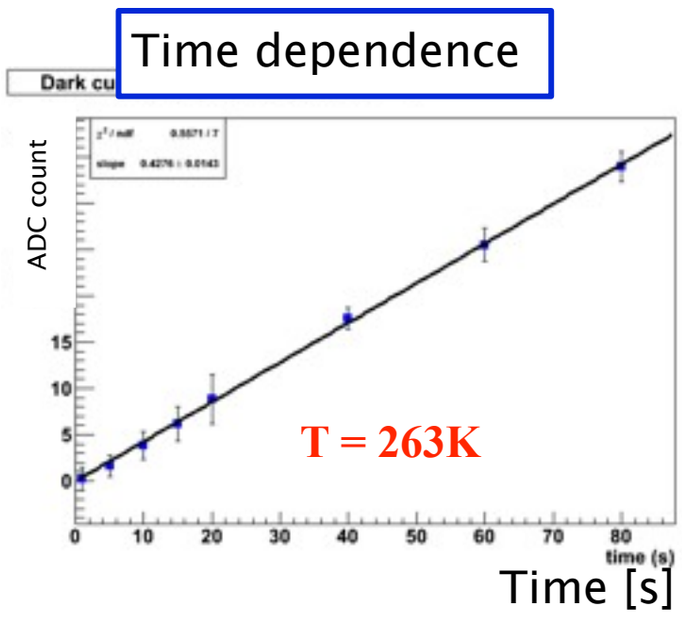
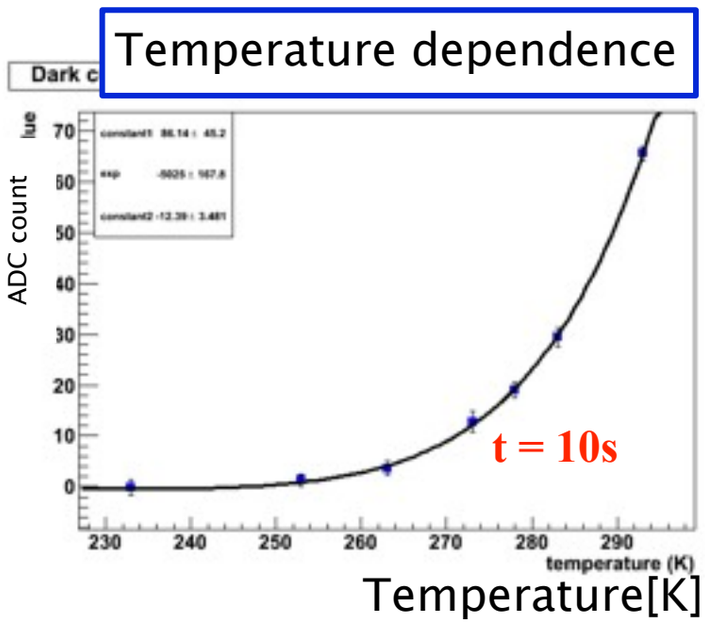
- CCD (Hamamatshu Photonics)
  - -- 12 x 12 um^2
  - -- thickness epi layer 15 um, Si total 50 um

- Setup
  - -- irradiation time 10s, -40°C
  - -- 25 MHz ASIC operation clock
  - -- S/N = 37 (single pixel hit extraction)
  - -- energy resolution 120 eV

- Pedestal
  - -- In ILC conditions (200ms and -40°C) dark current mainly suppressed.
  - -- Noise 55 e (from CCD readout)







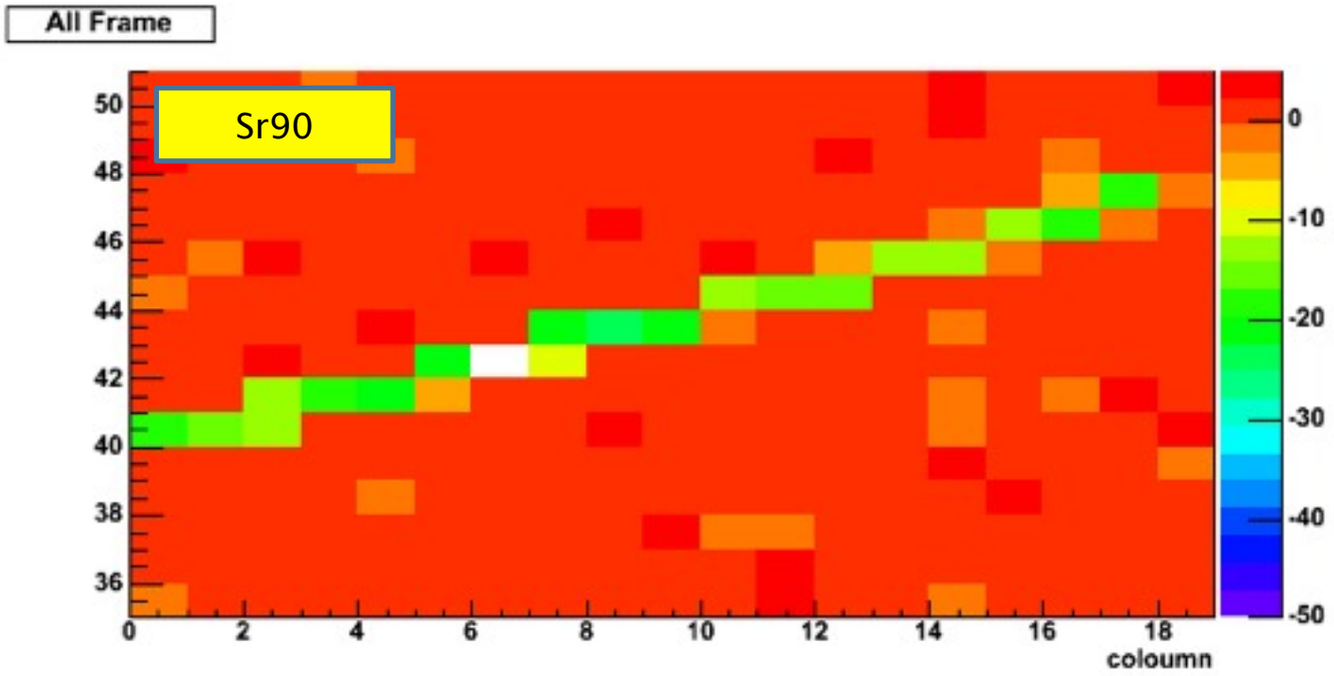
Sr90 β-ray Measurements

Eriko Kato

- CCD (Hamamatshu Photonics)
  - -- 12 x 12 um^2
  - -- thickness epi layer 15 um, Si total 50 um

- Setup
  - -- irradiation unit : 2 MeV β ray
  - -- Sr90 : ~10°C, 2.5MPix/sec

- Sr90
  - -- checked charge distribution with 2MeV β-ray.
  - -- negligible charge leakage to adjacent pixels.

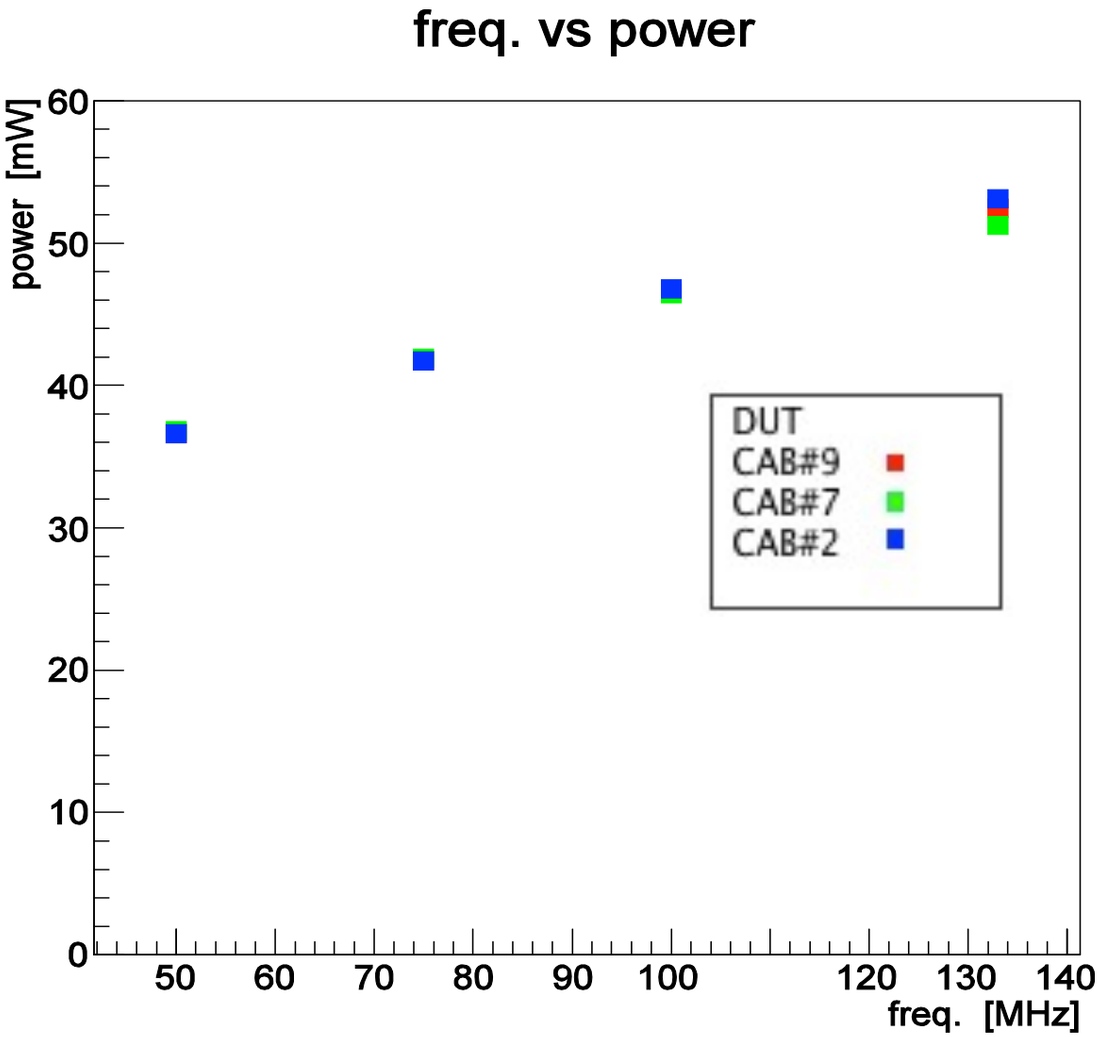


Tests with New ASIC i.e. AFFROC

Power Consumption

Hisao Sato

Power consumption at frequencies 50/75/100/133 MHz
Vdd,Vdd1 = 1.25V Vss,Vss1 = -1.25V



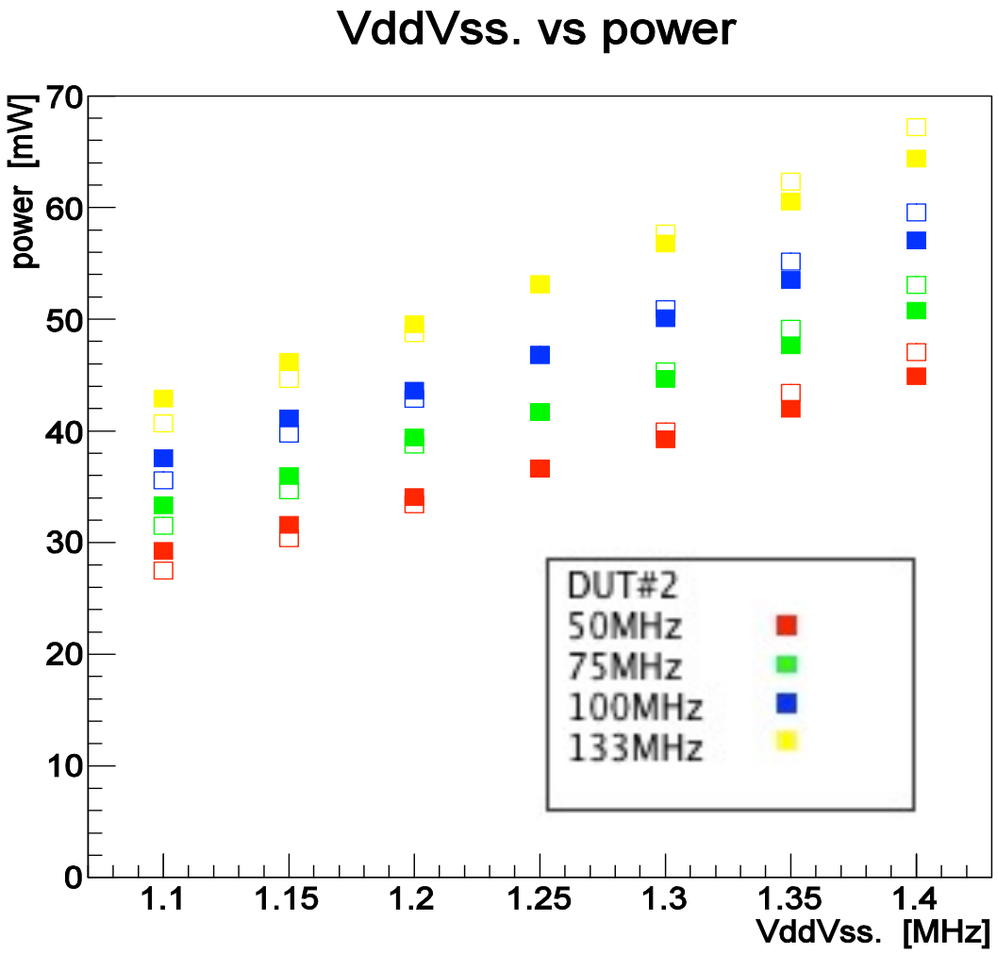
P < 6mW/ch (48mW/chip)

One of major goal of AFFROC was power consumption. Target was to achieve < 6mW/ch. Achieved.

Power Consumption

Hisao Sato

Power consumption dependency to Vdd,Vss



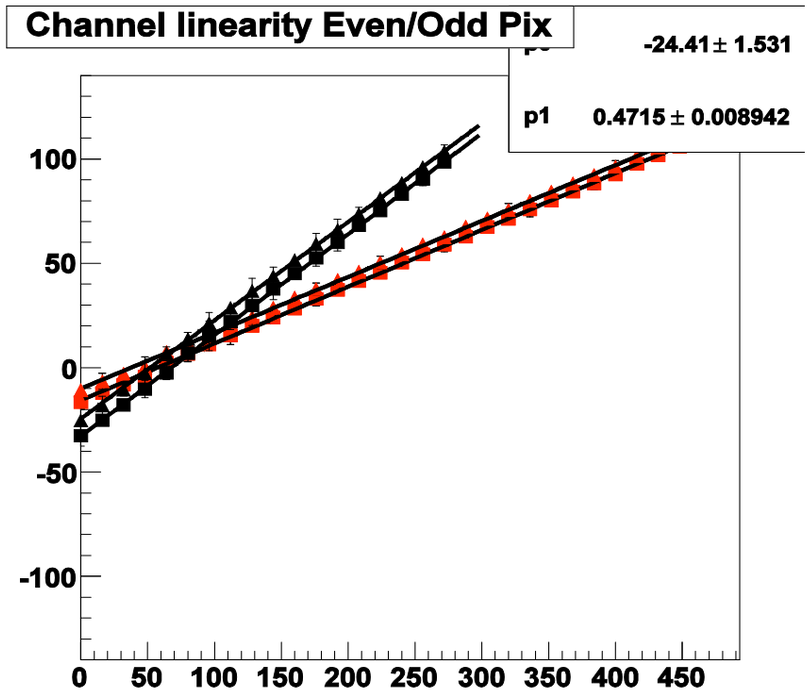
Power consumption dependency on Vdd,Vss as well on frequency looks reasonable.

Linearity

Hisao Sato

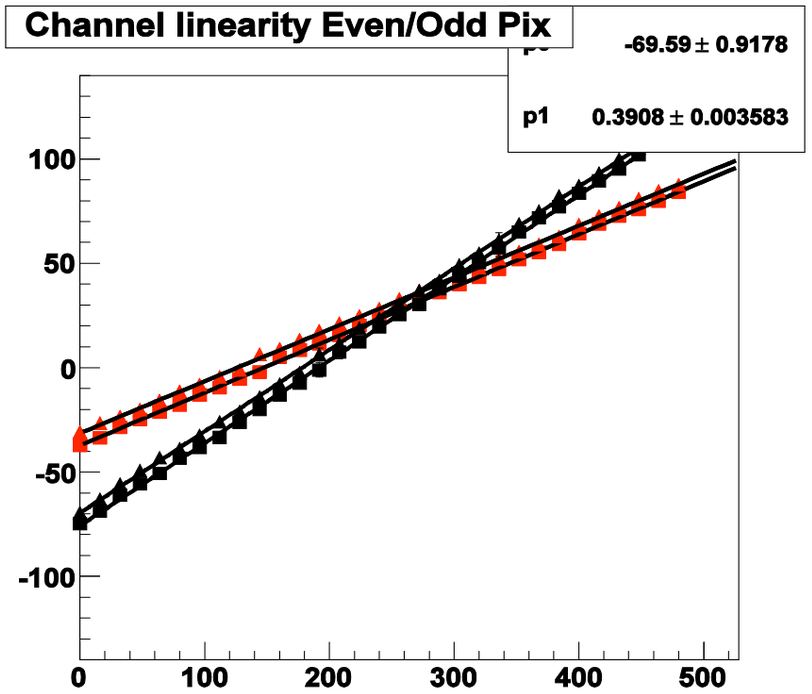
3 MHz

Gain : HIGH / LOW



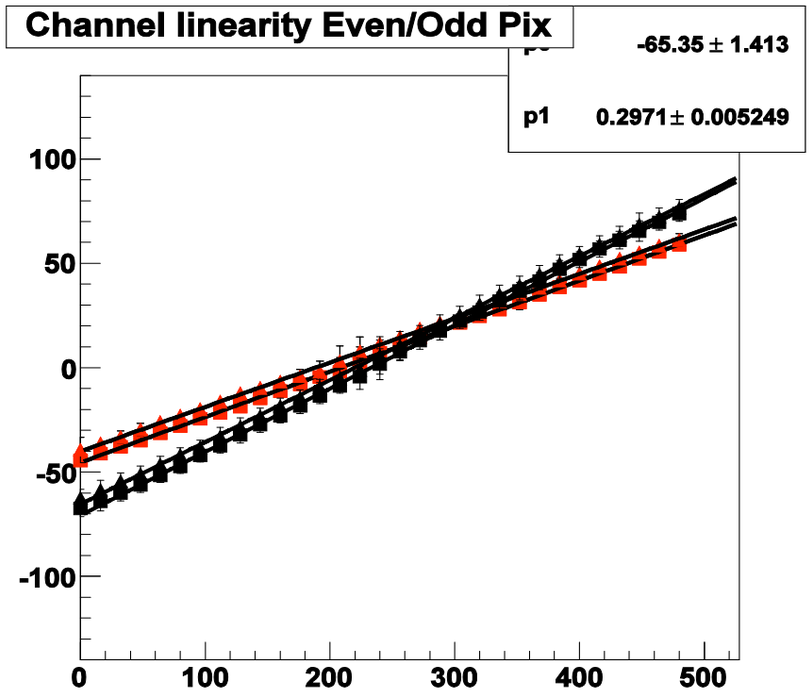
50 MHz

Gain : HIGH / LOW



100 MHz

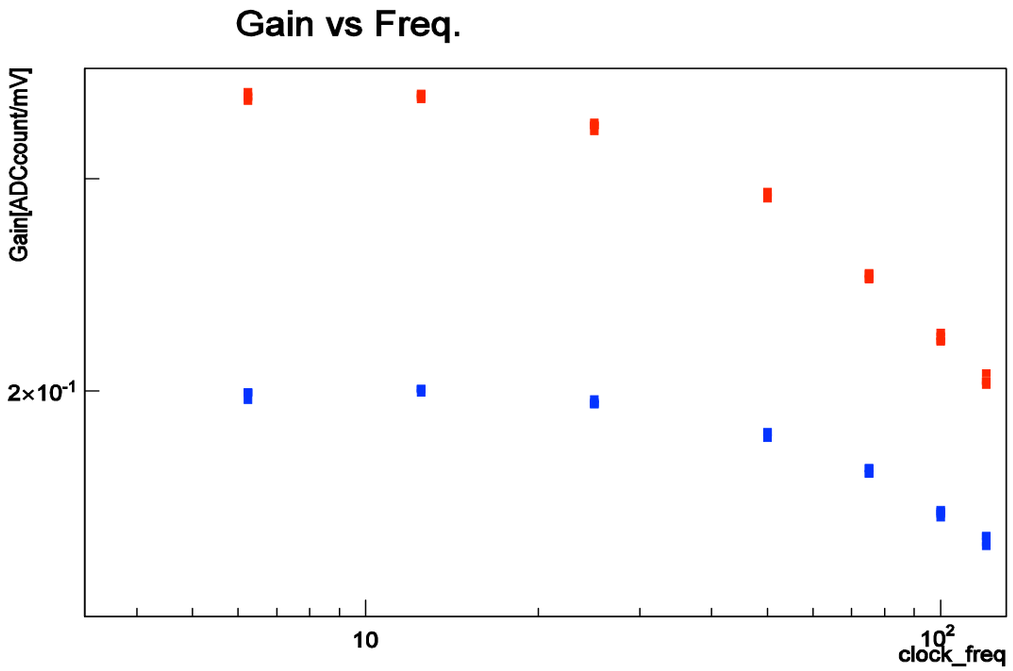
Gain : HIGH / LOW



Linearity looks reasonable, same result for all channels.

Gain/ADC Sigma vs Frequency

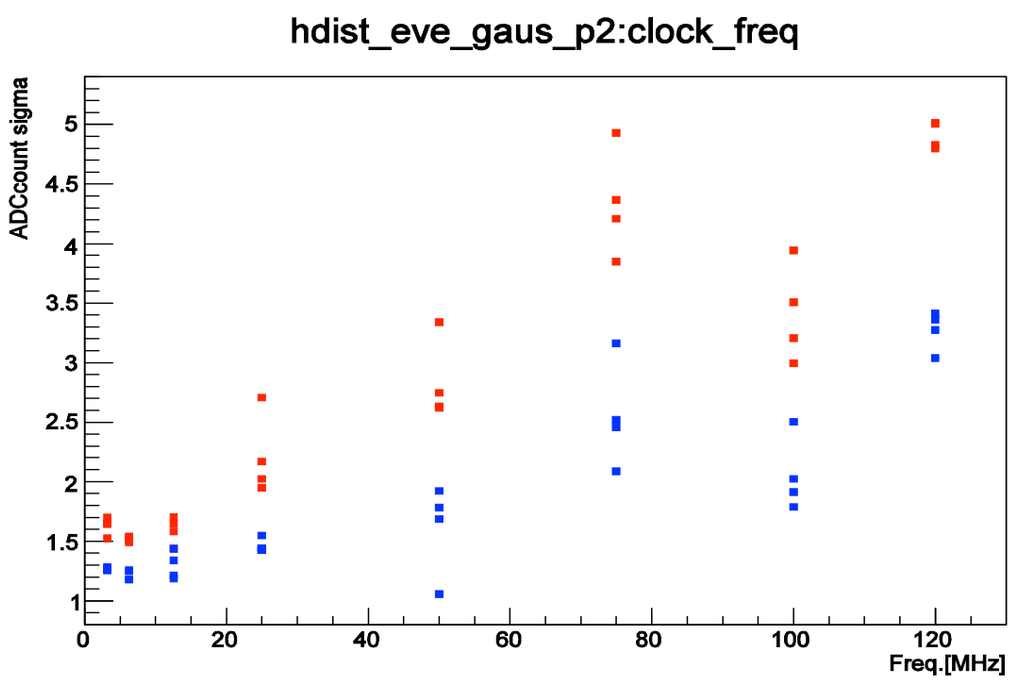
Hisao Sato



Channel 4-7

Gain [ADC count/mV] vs Freq [MHz]

Frequency dependency looks reasonable.
It may need optimization.



Channel 4-7

Sigma [ADC count] vs Freq [MHz]

Needs further study to reduce noise.

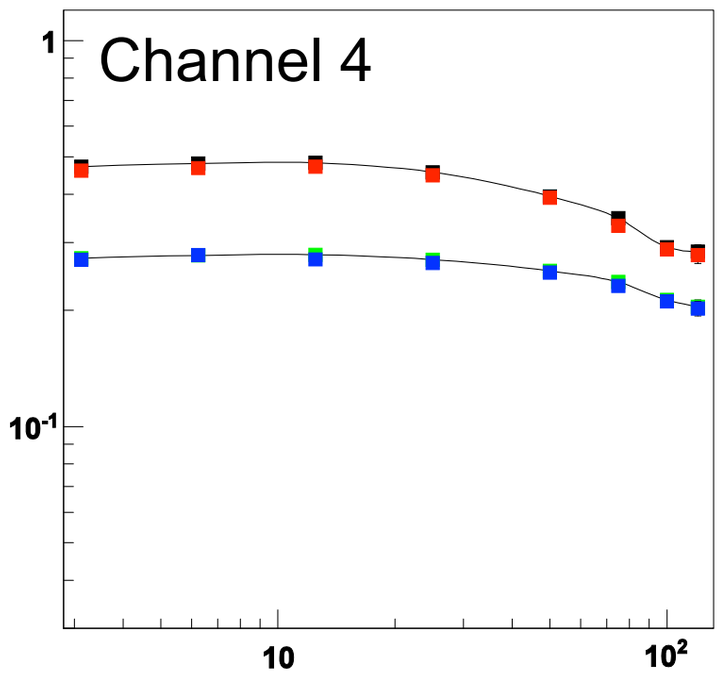
Challenges And Plans

- Presented status of CCD and ASIC tests.
- We tested successfully ASIC prototype 2 with 12um CCD.
- Successfully migrated to SEABAS2 based new test system.
- AFFROC characterization is going on.
- Power consumption goal of AFFROC is achieved.
- Frequency dependency of gain looks reasonable.
- We have just started looking into frequency dependence of noise which doesn't looks reasonable, it worsens at higher frequencies.
- Other than noise, so far no major problem has been seen in AFFROC.
- Fe55 test with 6um CCD will be done soon (before year end). all setup is ready. Just have to take data.

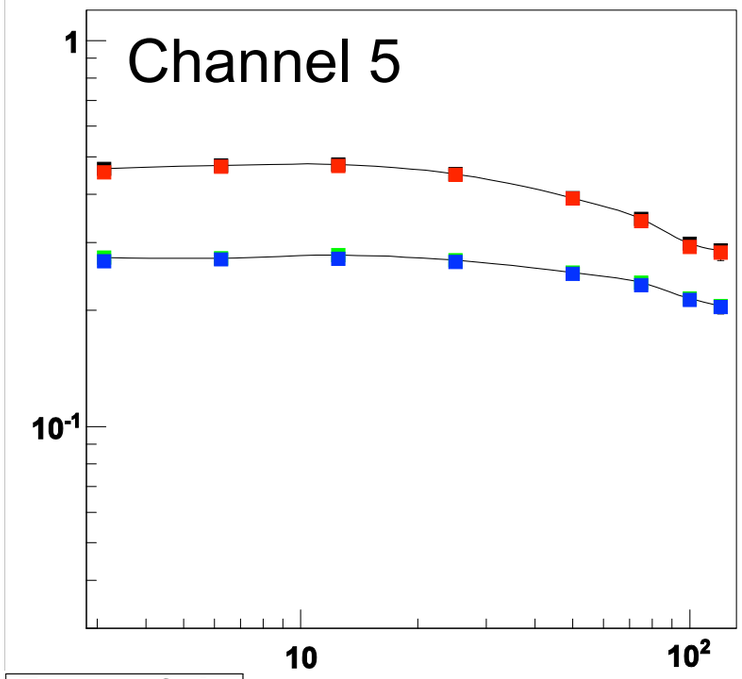
BACKUP

Gain vs Frequency

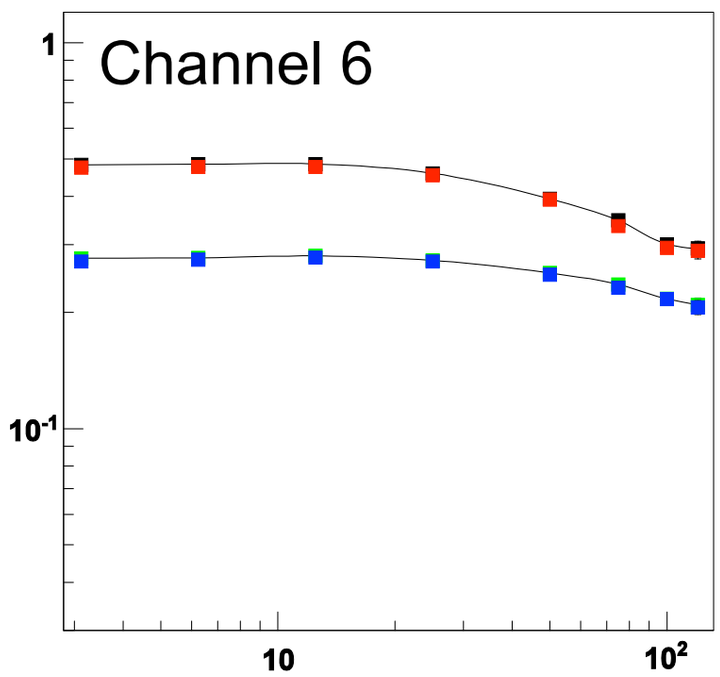
Freq vs Gain



Freq vs Gain



Freq vs Gain



Freq vs Gain