FPCCD VTX Overview

Yasuhiro Sugimoto
KEK
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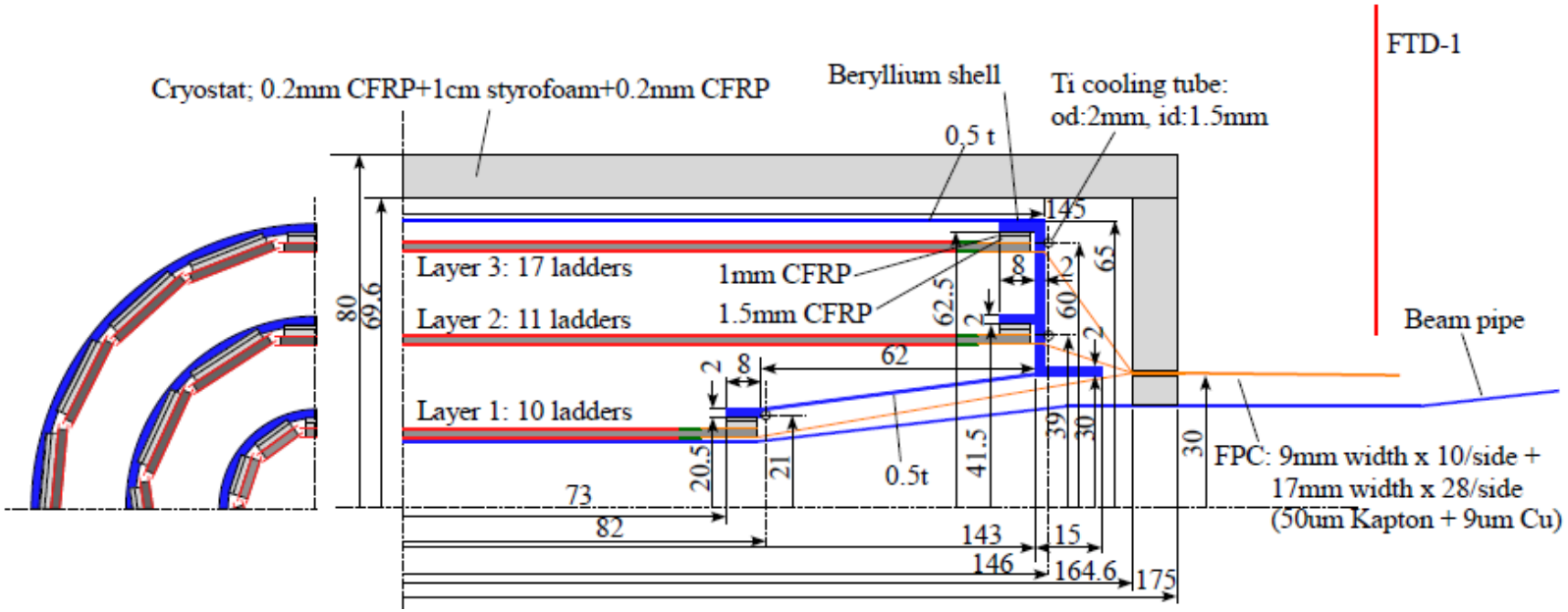
Outline

- FPCCD VTX for ILD
- FPCCD sensor R&D
- CO2 cooling for VTX
- FY2013 plan

Vertex detector for ILD

- Structure
  - Barrel part only: |z|=62.5/125 mm
  - Double-sided layer x3
  - R=16~60mm
  - |cosθ|<0.97
- Minimization of material budget of ladders is a big challenge
  - 0.3%X0/ladder = 0.15%X0/layer



FPCCD VTX for ILD

- Pixel size
  - 5um for inner two layers
  - 10um for outer four layers (previously 5um)

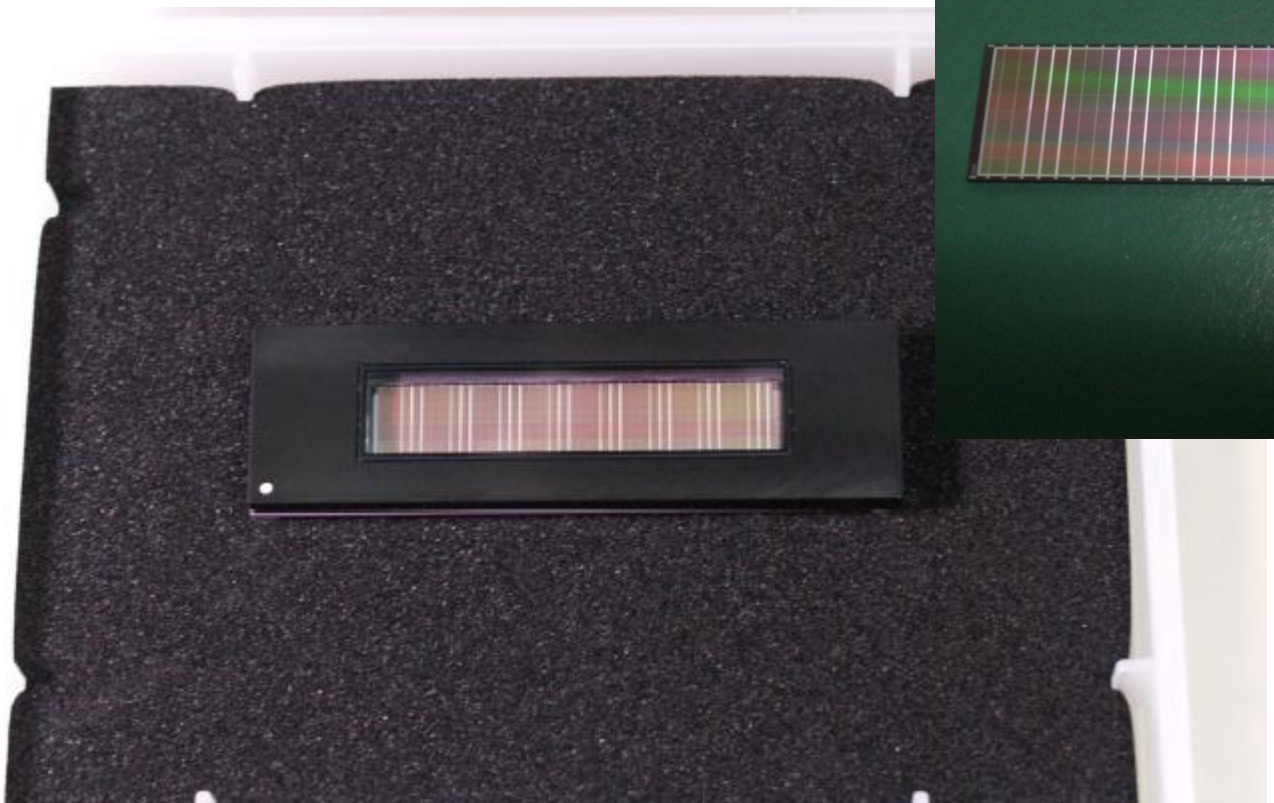
	Pixel size (in)	Pixel size (out)	# of ch /chip (in)	# of ch /chip (out)	# of ch (total)	Power consumption
Old design	5 um	5 um	28	56	7392	111 W
New design	5 um	10 um	15	15	2280	34 W

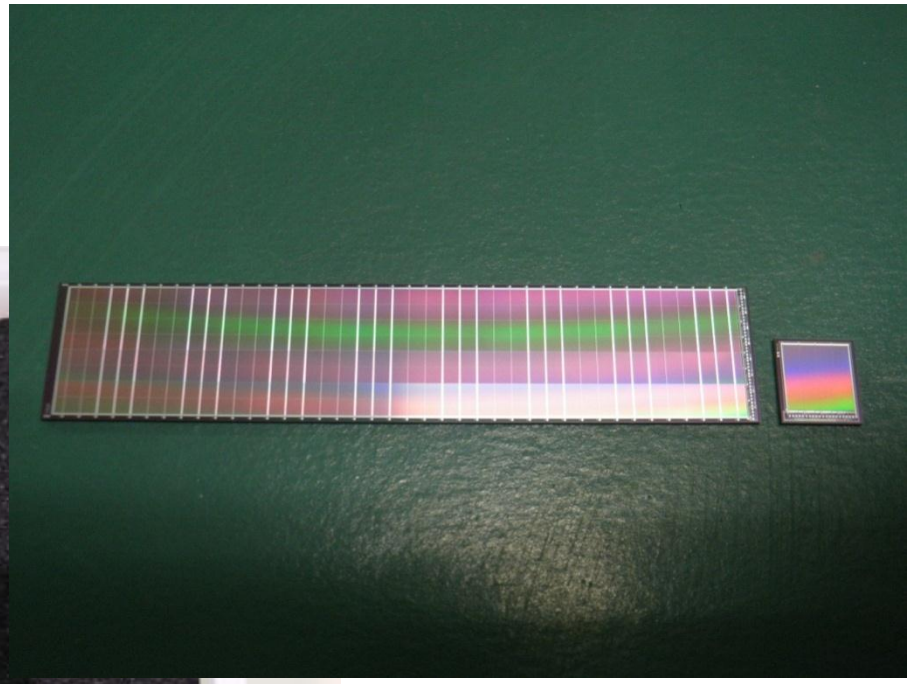
- Power consumption
  - ~40W for on-chip amp and ASICs inside cryostat
  - ~400W for clock drivers and data processing circuits outside the cryostat
  - ~?? W for the aluminum gate line on CCD

FPCCD sensor R&D

FY	Sensor
2004	Fully depleted CCD, 24um pixel
2005	Fully depleted CCD, 24um pixel
2006	Fully depleted CCD, 24um pixel
2007	1st FPCCD: small size (6mm^2),12um pixel
2008	2nd FPCCD: small size, 12um pixel (modified output amp)
2009	3rd FPCCD: small size, 12, 9.6, 8, 6um pixel
2010	4th FPCCD: small size, 12, 9.6, 8, 6um pixel (modified process) Thin wafer:50um
2011	Small size, 12, 9.6, 8, 6um pixel (modified process), thin wafer
2012	Small size, 6um pixel, 4ch, different H-register size Large size (12x64mm2), 6,8,12um pixel, 8ch Small size, 6um pixel, thin wafer (for beam test)
2013	Small size, 5um pixel ? Large size, thin wafer ?

FPCCD sensors





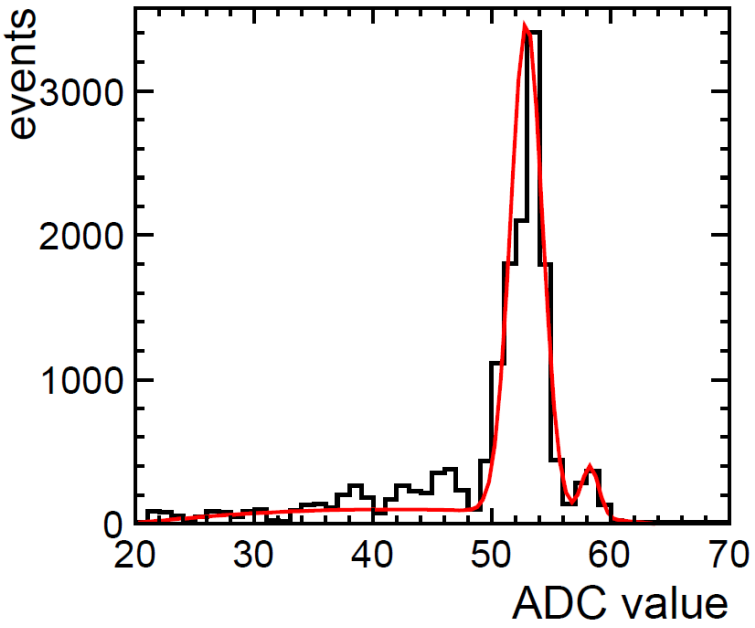
R&D goal

- FPCCD sensors
  - Pixel size; 6um → 5um (?)
  - Chip size;1cmx6.5cm
  - Speed >10Mpix/s
  - F.W.C. > 10000 e(?)
  - Power <10mW/ch
  - Rad. Tolerance >$1x10^{13}e/cm^2$ (=$1x10^{12}/cm^2/y$ x 3y x safety factor 3)
- Readout ASIC
  - Speed > 10Mpix/s
  - Power < 6mW/ch
  - Noise < 30 electrons
- Peripheral circuit
  - Clock driver
  - Data suppression
  - Etc.
- Engineering R&D
  - Over-all design
  - Low-mass ladder
  - Cooling system (~-40℃)
  - Support structure

  ➔ Engineering prototype

R&D status

- 6um pixel works if horizontal register is 6x12um^2 or larger
- Full-well capacity (~5000e) is still to be improved (>10000e)
- Large prototype works!
- Beautiful Fe55 X-ray spectrum is obtained using an FPCCD of 12um pixel at 2.5Mpix/s speed
- Test of FPCCDs of 6um pixels using new readout electronics (new CCD board with new FE ASIC (AFFROC-1)+ SEABAS2-board) on going



CO2 cooling system

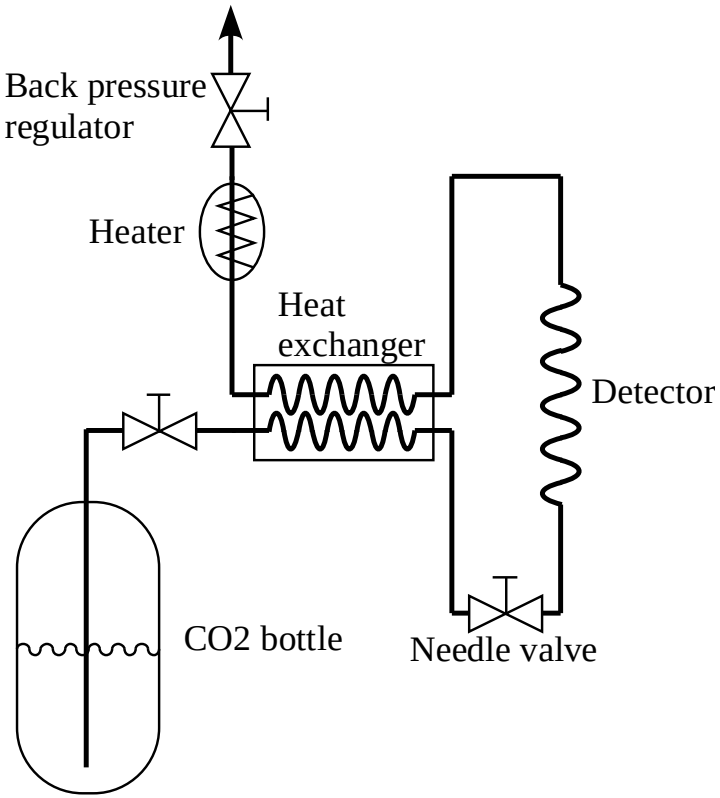
- FPCCD will be operated at low temperature (-40 degree) to minimize CTI
- Power consumption ~40W inside the cryostat
- Cooling with cold air (nitrogen) flow would not be enough
- Cooling system using 2-phase CO2 is a very attractive alternative because of its large cooling capacity (~300J/g)
- Cooling tube is attached to VTX end-plate and heat produced by CCD output amp and ASIC is removed by conduction through CFRP ladder (simulation study for thermal design is necessary)
- Material budget increase is small: 0.3%X0 for end-plate and 0.1%X0 for the cryostat
- Return line of CO2 will be used to cool the electronics outside the cryostat (~200W/side)
- Inner support tube should be air-tight and filled with dry air/nitrogen in order to prevent condensation on the CO2 tube

Common engineering design

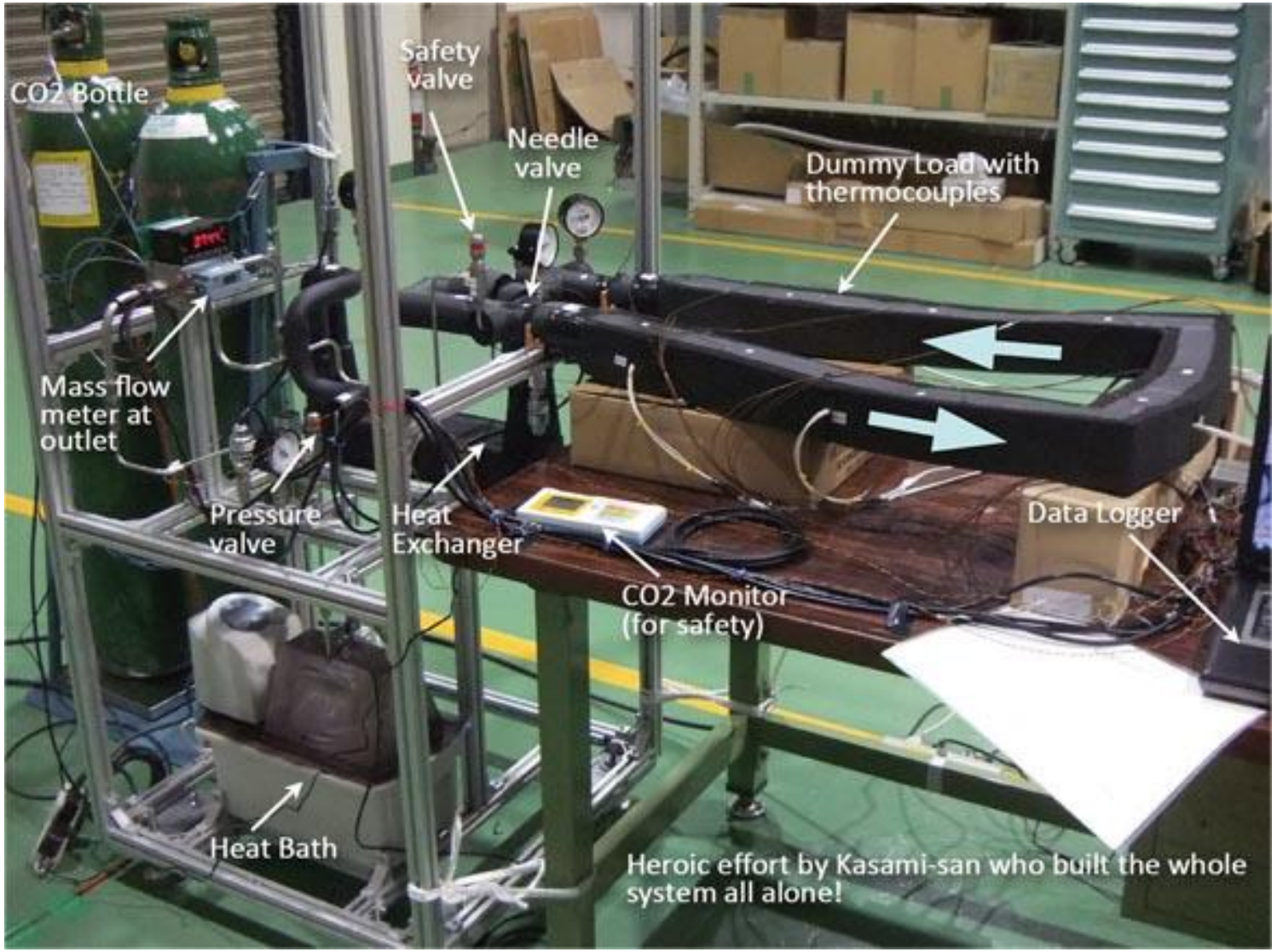
- Cooling pipe + Support shell

CO2 cooling system

- CO2 collaboration in Japan
  - ILC VTX, ILC TPC, Belle-II VTX, and KEK cryogenic group
  - We constructed “blow system” and temperature was successfully controlled between -40 and +15 degrees

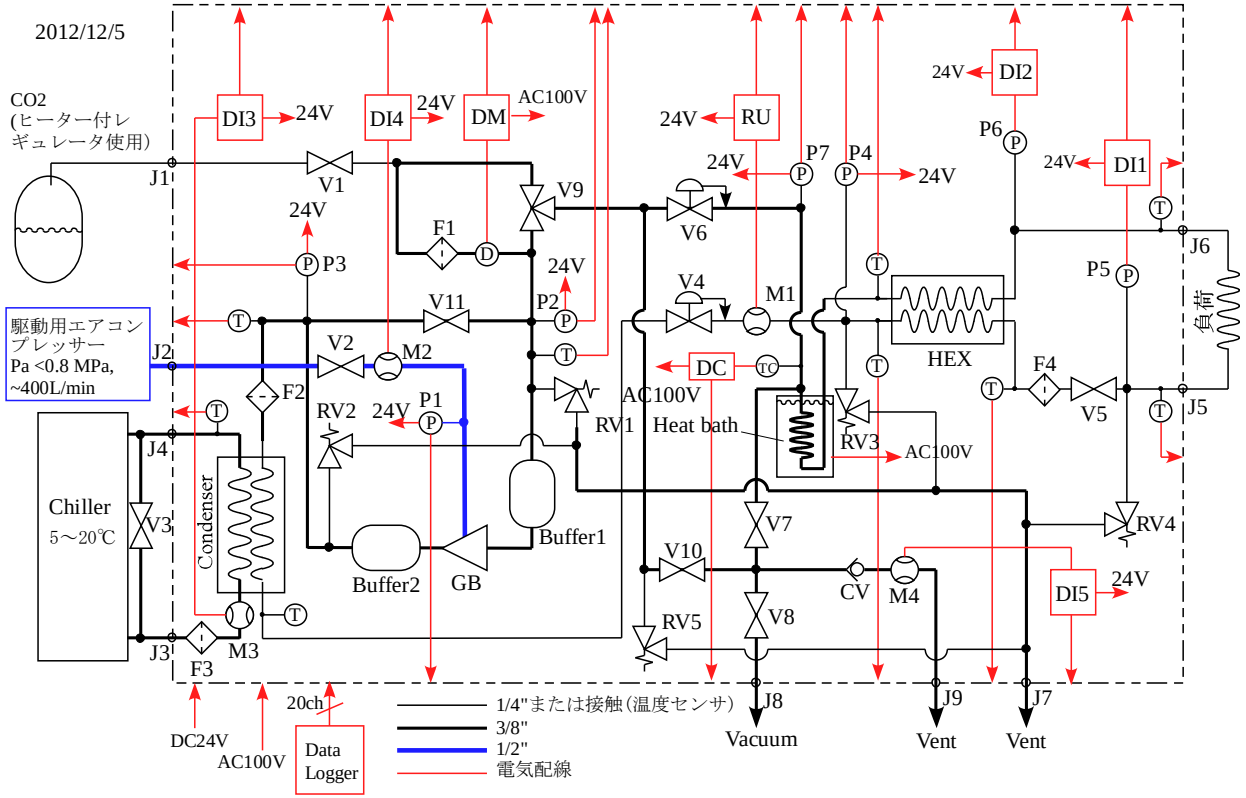


CO2 cooling system



CO2 cooling system

- R&D of circulating system using a compressor: Supported by KAKENHI(C) and KEK Detector Technology Project
  - Design completed
  - Components are ordered
  - Assembly by the end of FY2012



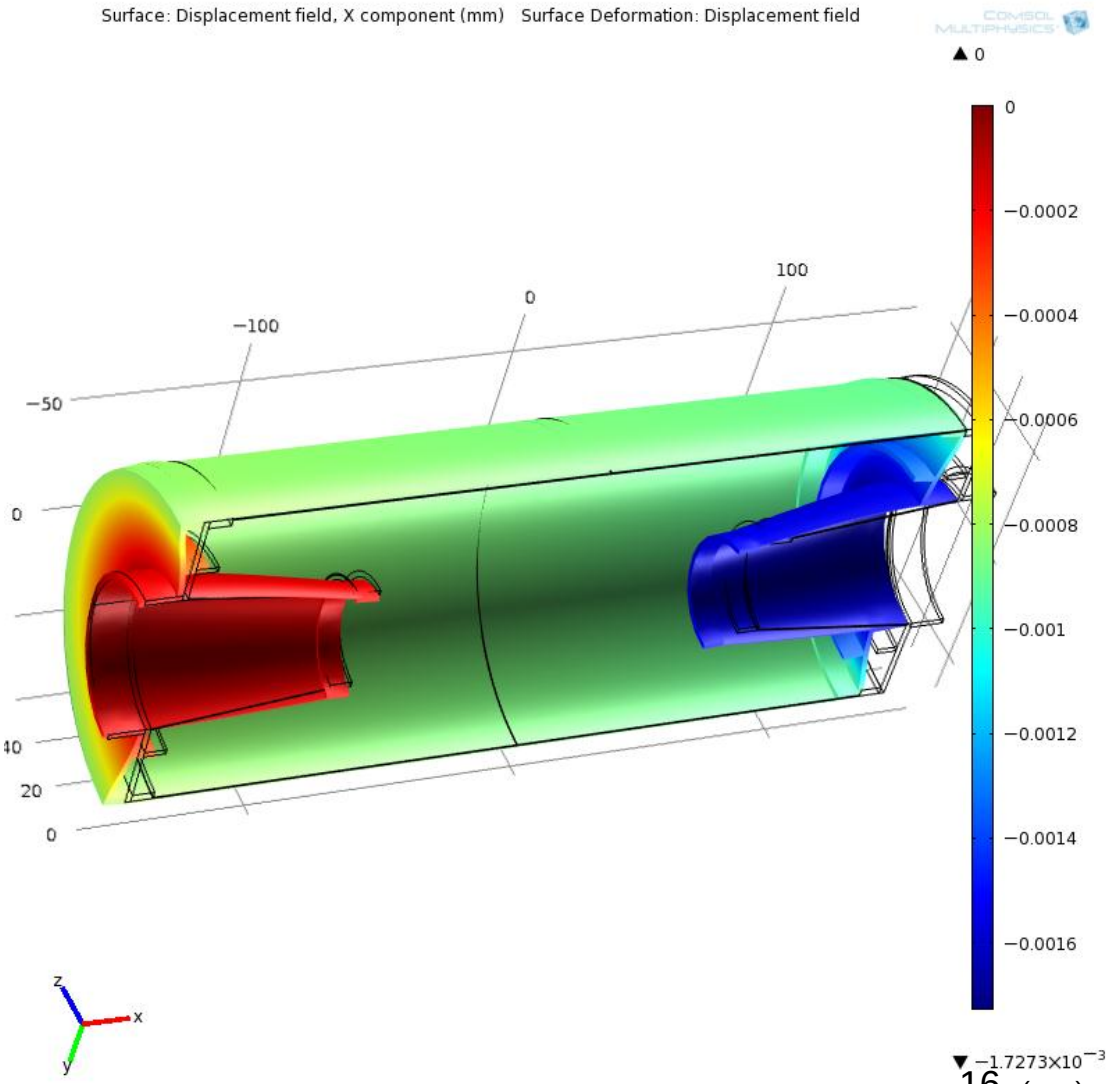
FY2013 plan

- Beam test
  - Demonstrate spatial resolution
  - Test beam at JPARC (1GeV)
- Neutron damage test
  - Few tens of MeV/c neutron beam is available at CYRIC cyclotron in Tohoku University
  - FPCCD neutron damage test in FY2013~2014
- FPCCD Prototypes
  - Large thin wafer (?)
  - Small 5um pixel chip (?)
- 2nd AFFROC prototype, if necessary
- Bare chip test
  - Fabricate a test board for bare chips before ladder R&D

Backup slides

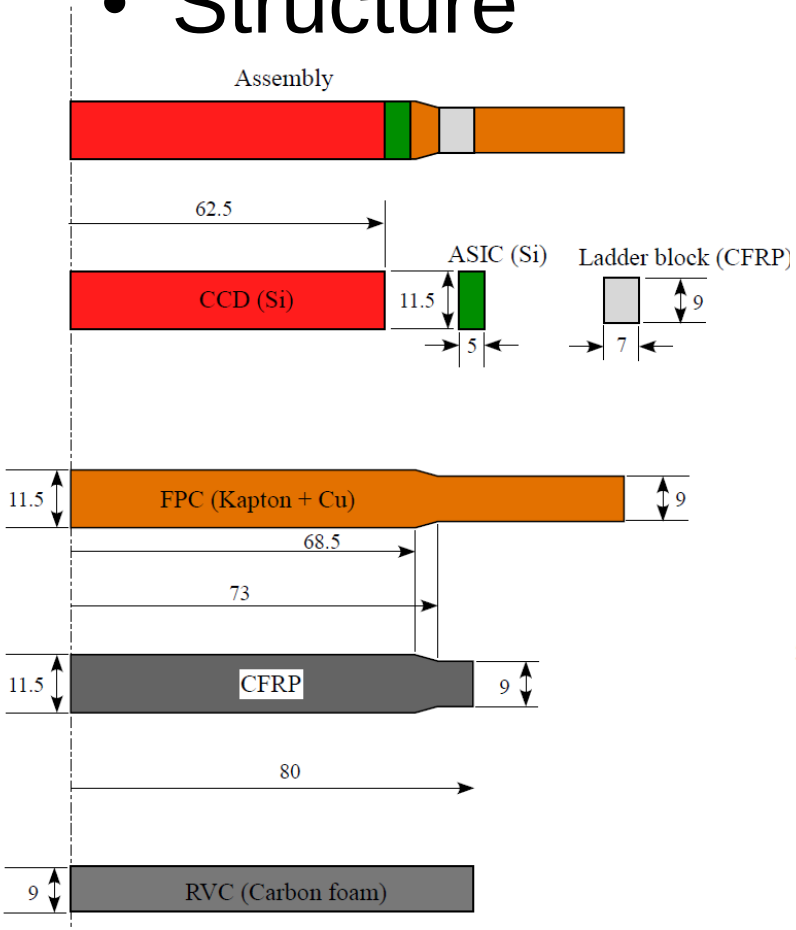
Beryllium support shell

- FEA calculation of deformation
  - 1kgf is applied in z-direction
  - Maximum deformation is less than 2μm
  - Total weight is less than 500g → max force caused by the friction at the kinematic mount would be less than 500gf

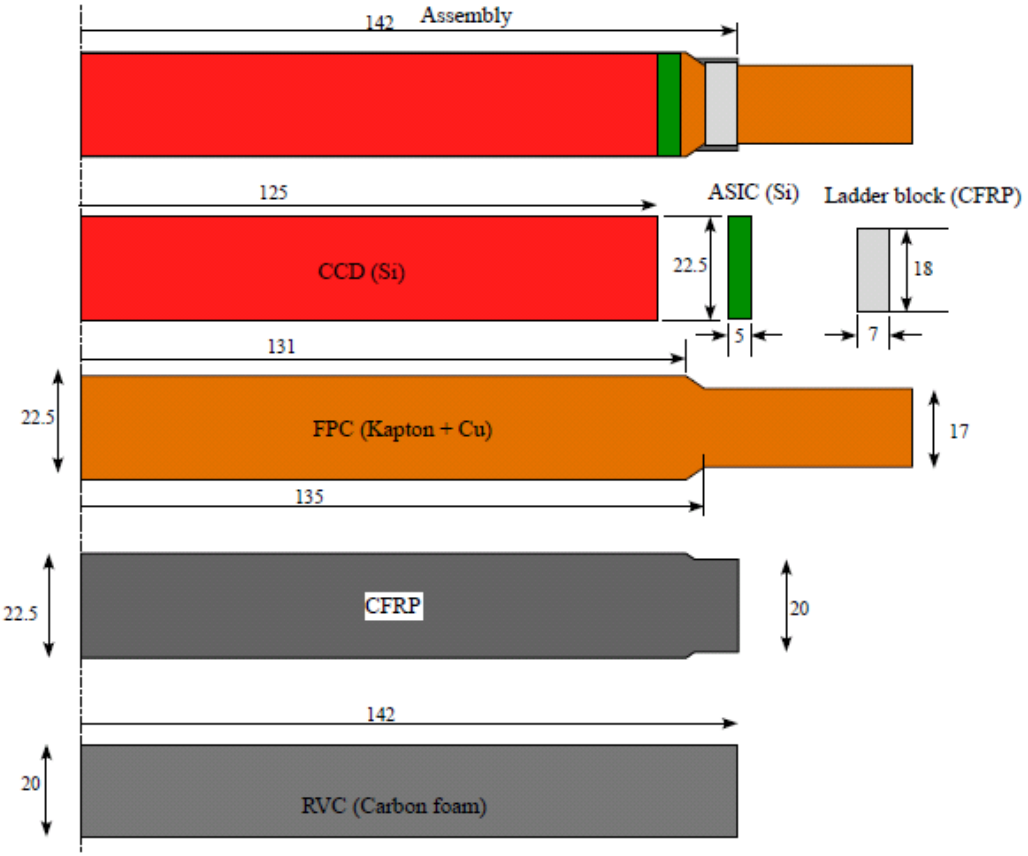


Ladder

- Structure



Layer-1



Layer-2,3

Cooling system

- Cooling tube
  - Titanium tube 2mm o.d. and 1.5mm i.d. is attached to the VTX endplate near the endplate annuli
- The return line of the cooling tube is also used for the cooling of the junction box
- 4 tubes/side run along the beam pipe between the vertex detector and the end of the inner support tube