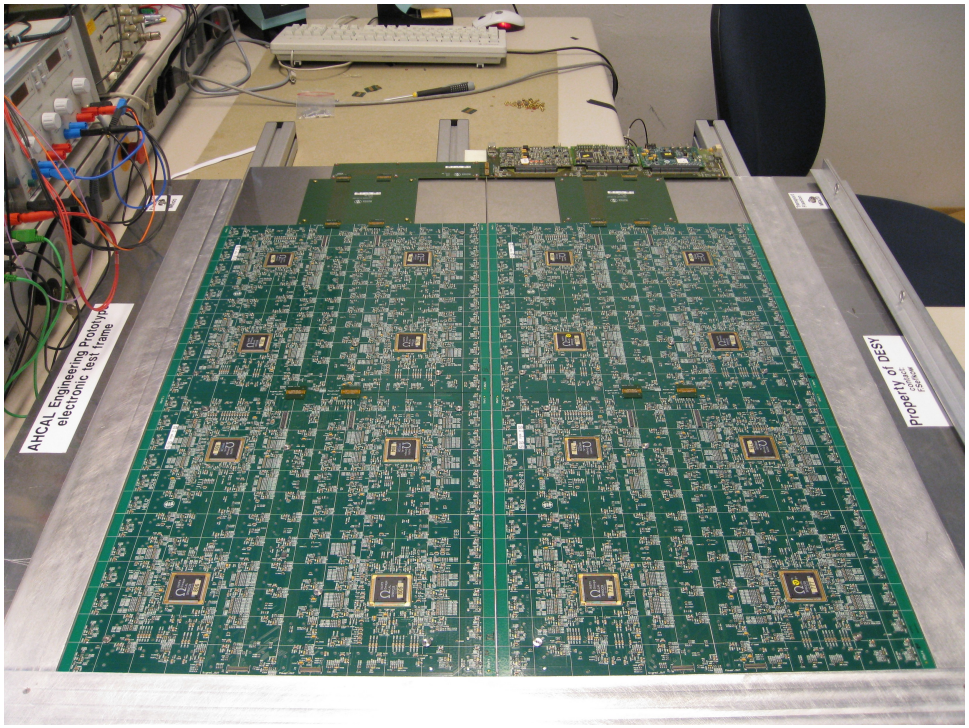
TDC calibration of a Spiroc2b driven detector (the AHCAL layer)

Overview

- Introduction
- Trigger setup
- Spiroc2b TDC calibration
  - Ramp calibration
  - Offset calibration
- Outlook



Radial Hit Time Dependency

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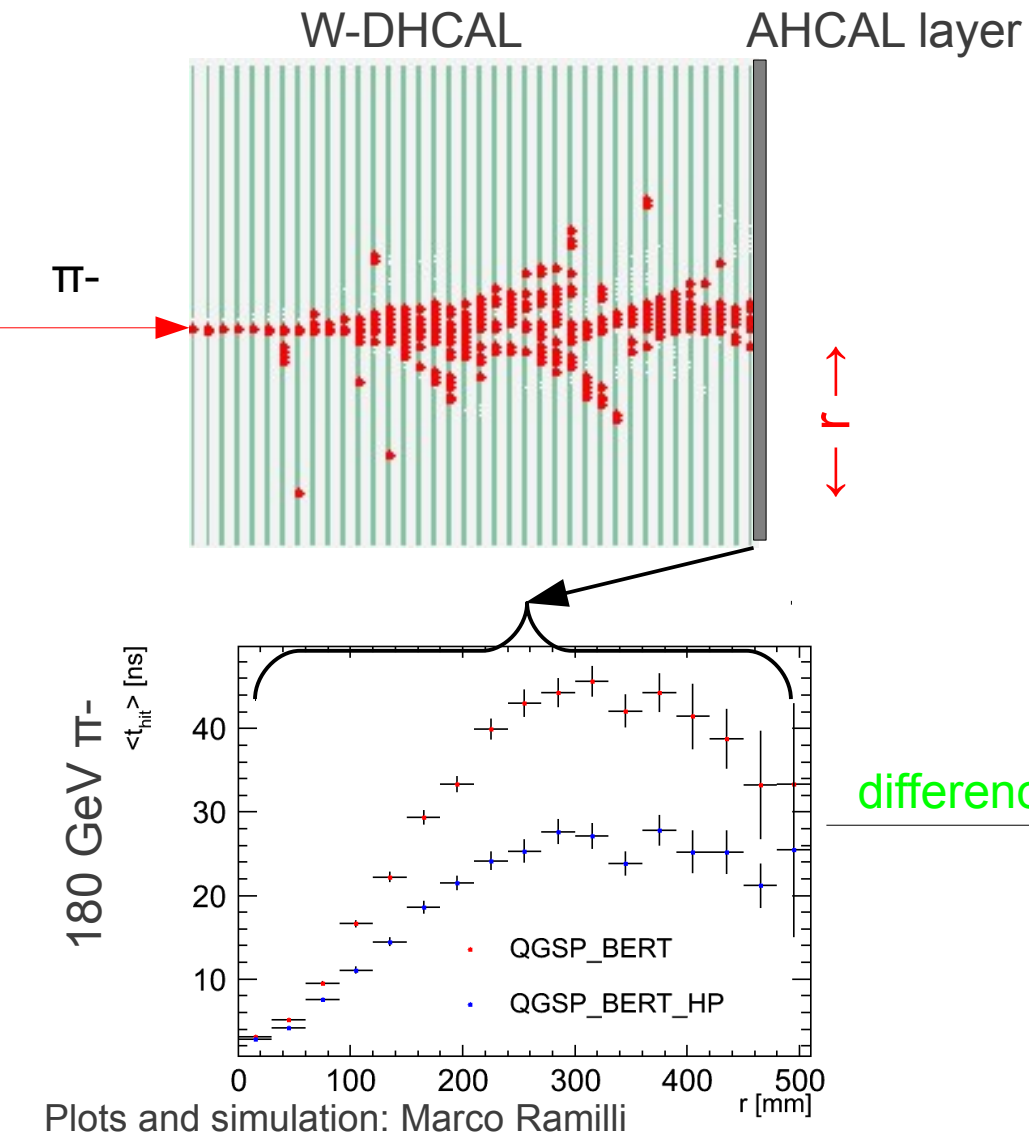
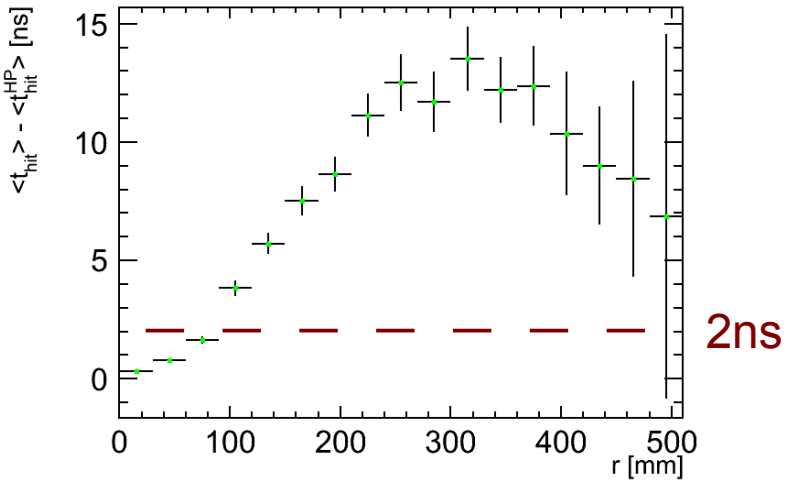


Plots and simulation: Marco Ramilli

Radial distribution of mean hit time in AHCAL layer position (> 4 λ_I)

- An increase of the mean hit time with radius is predicted
- Statistical errors allow to **distinguish between physics lists for 100 mm < r < 350 mm**
- Needed time resolution: **~2ns**

difference



Trigger T(0) Setup

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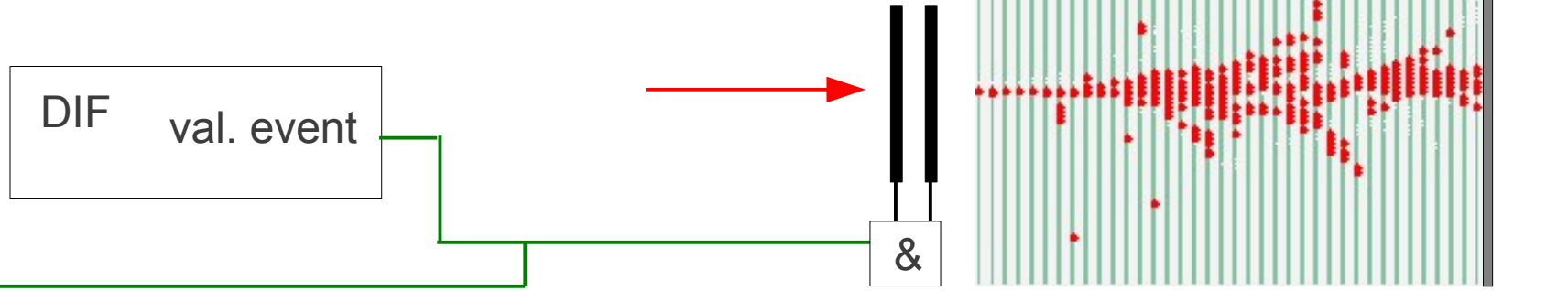
Calorimeter clock not in sync. with beam

- Time information has no correlation to incoming particles
- need to provide event by event T0 measurement
- **Validate event** signal from triggers in front of DHCAL provides T0 time signal (digital, fixed amplitude)

→ signal into two channels (instead of SiPMs)
(redundancy against failures and **crosscheck** for calibration)



Spiroc2b - TDC

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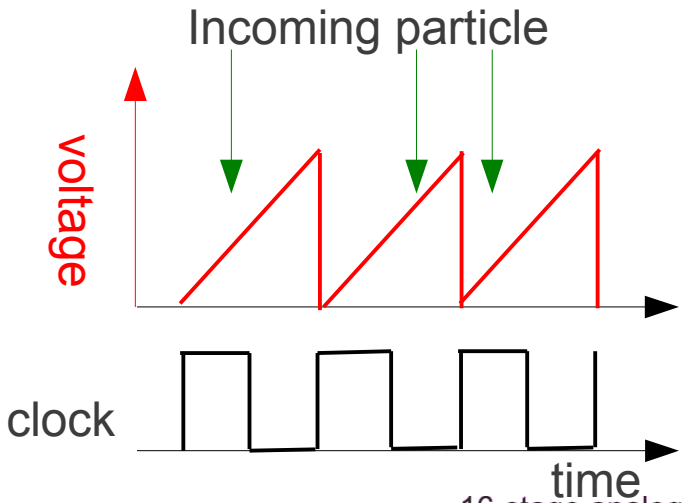
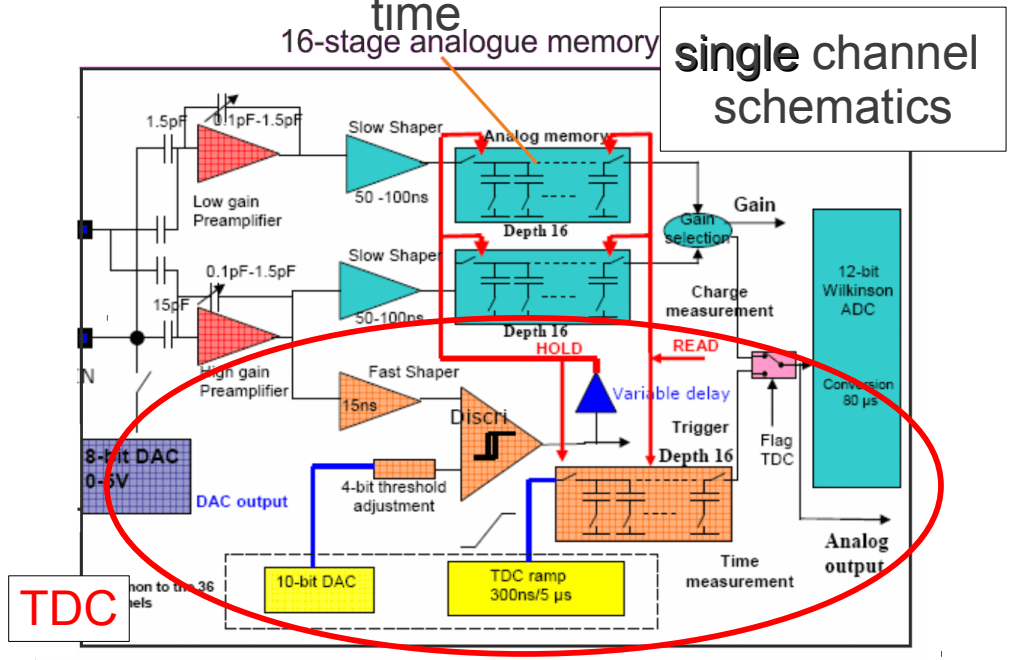
Time measurement:
- Hit → sampled voltage ramp
- Ramp produced by chip
- Analogue ADC samples voltage
- TDC is **analogue** measurement
  → needs **calibration**
- Absolute time:
  → clock cycle and TDC



Spiroc2b TDC:
- 16 **analogue** memory cells **per channel**
- 4096 TDC bins (4µs → 1ns)
- Same 12bit ADC is used for energy and time measurement
  → similar effects expected for calibration of ADC and TDC



TDC ramp calibration

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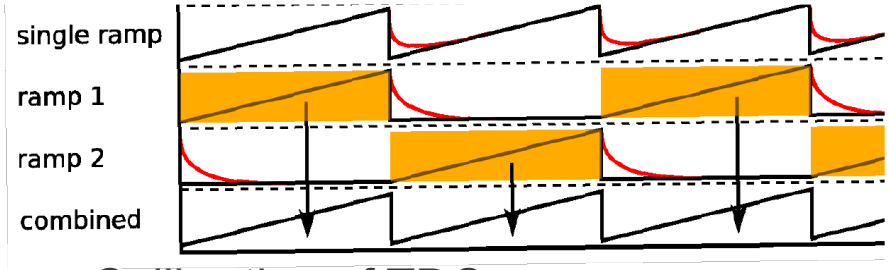
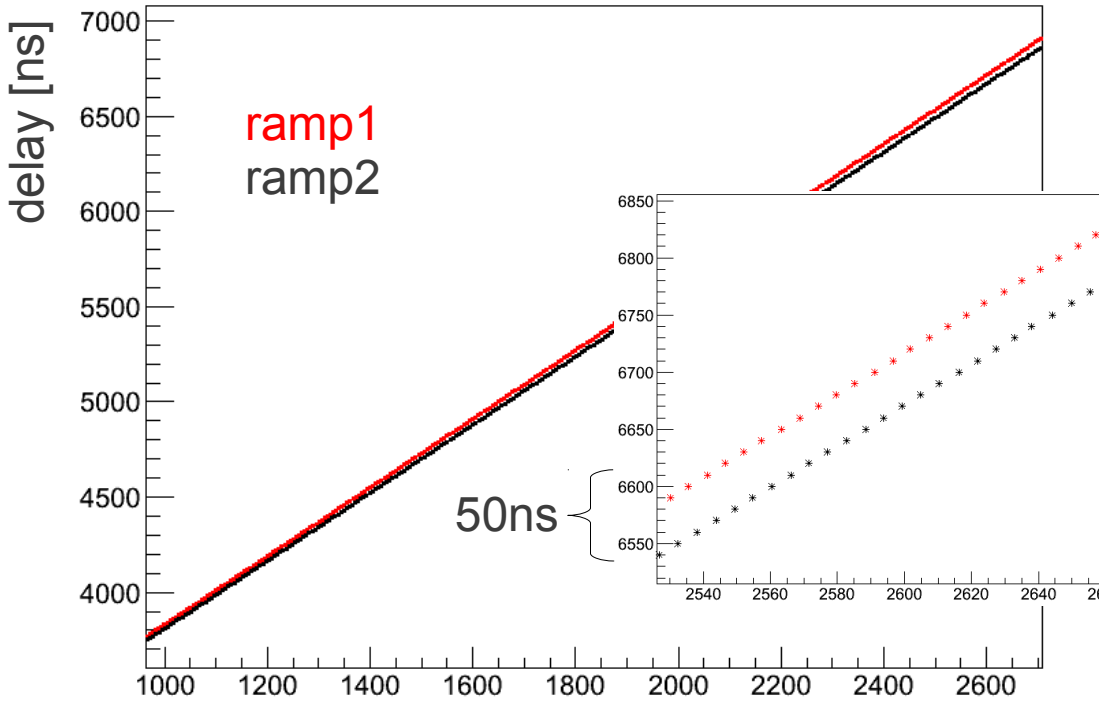
Every Spiroc2b produces **2 TDC ramp(s)**:

- Two multiplexed ramps
- Ramps are identified via clock cycle
- Ramps are **not identical**
  → different calibration
- AHCAL layer: **32** ramps (16 chips)
- Ramp calibration with **charge injection** on **one** channel





Calibration of TDC:

$$time[ns] = f_{chip,ramp}(TDC) + offset_{memory\ cell,channel}(+clock\ cycle)$$

Assumptions: linear (#32) no function of TDC (#9216)

TDC corrections assumptions

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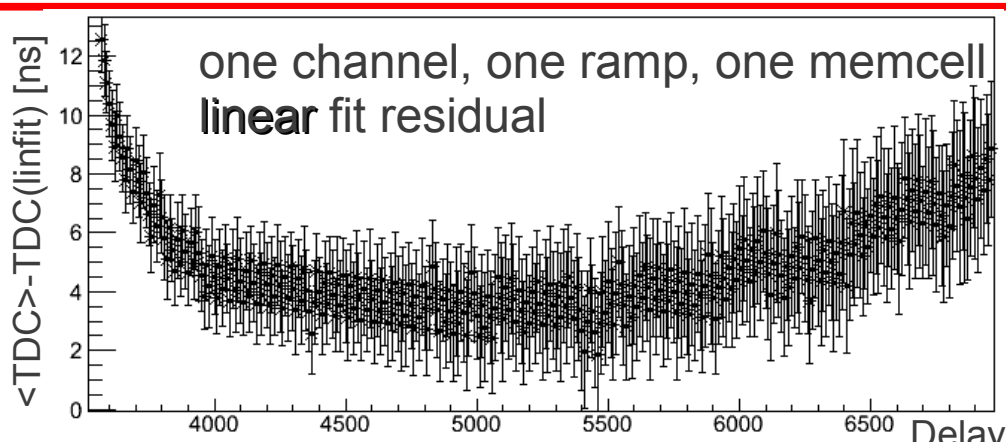
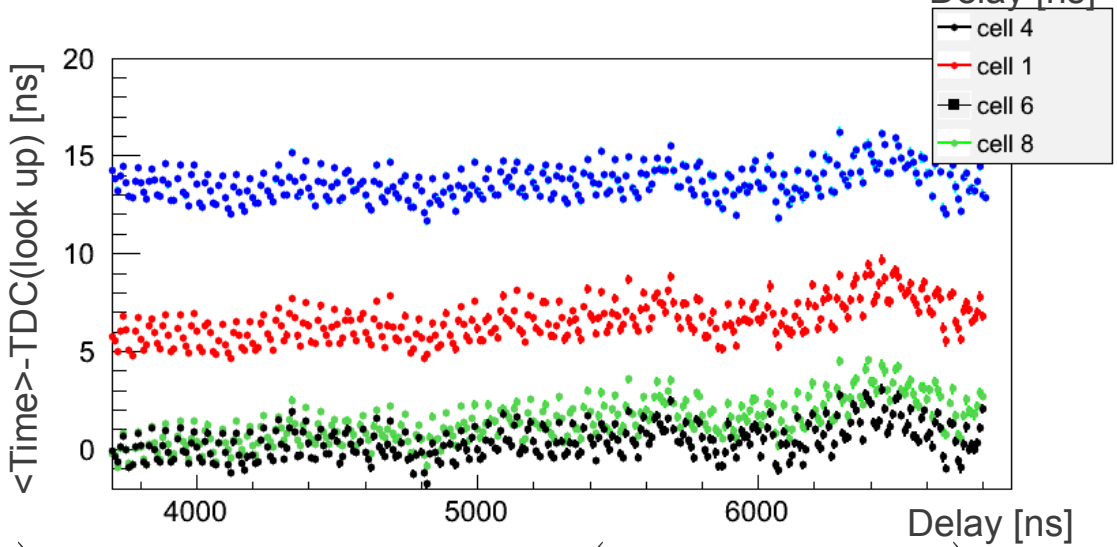
Lab measurements:
- TDC dyn. range not fully used
  → 4µs in 2500bins: **1.6ns** p. TDC bin
- Ramps are **not linear**
  → $f_{chip,ramp}(TDC)$
  must be defined for every chip
  (look up table)



Channel with 16 memory cells:
- Every memory cell has an **offset**
- Each memcell shows different TDC dependency



Offset: mean of distribution per memcell after ramp correction
→ caution if data is not evenly distributed over whole TDC range

$$time[ns] = f_{chip,ramp}(TDC) + offset_{memory\ cell,\ channel}(+clock\ cycle)$$

Assumptions: ~~linear~~ almost no function of TDC

TDC corrections

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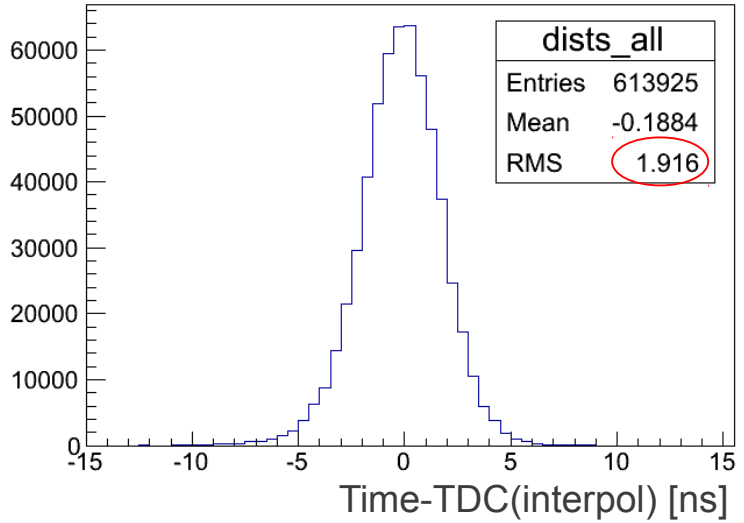
Residual distribution for **one** channel
after corrections for:
- Two different ramps
- Memory cell wise offset

→ single channel electronics resolution: **~2ns**



→ Charge injection not practicable for all 576 channels

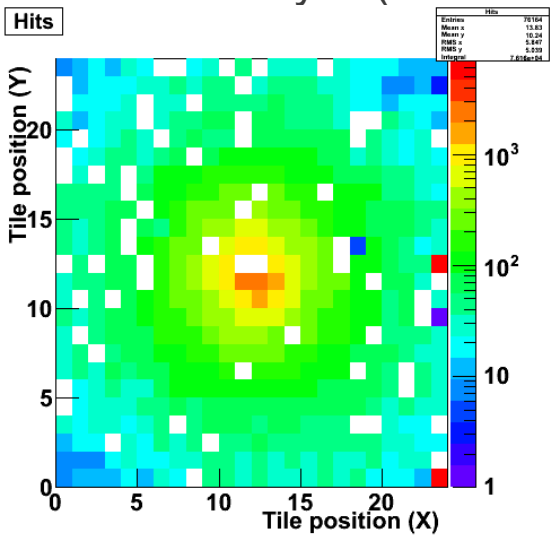
Solution to get the offsets:

Electron test beam:
- High rate (kHz)
- Instantaneous EM showers (Al target: 3.7 X_0)
- Few different beam positions to cover all chips

→ determine memory cell wise offset for
All 576 channels and 16 memcells

→ **9216** offsets

EM shower in AHCAL layer (one run)



TDC calibration DESY test beam

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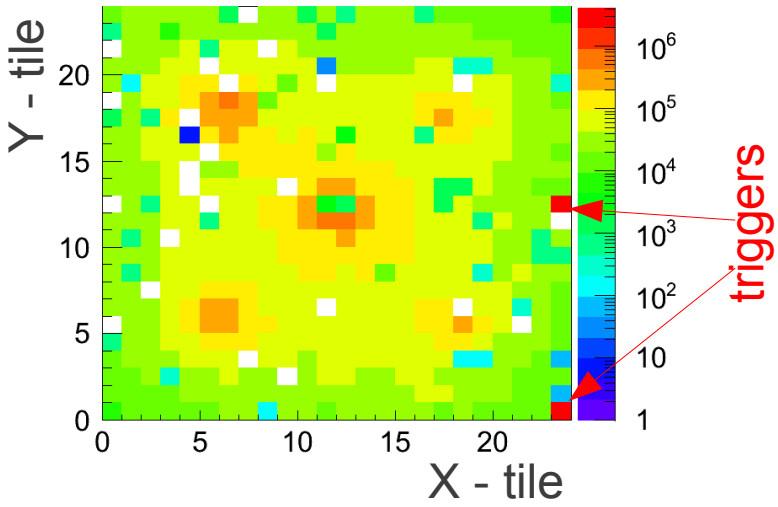
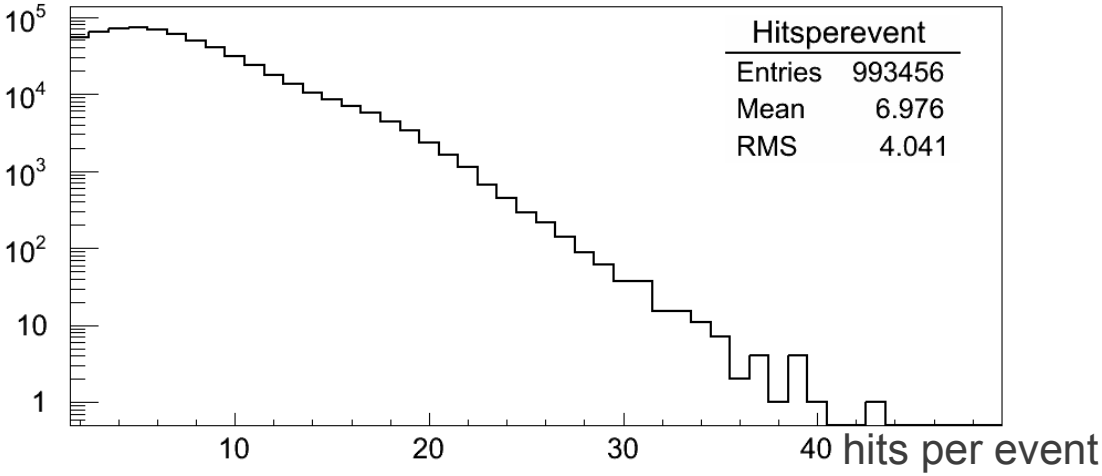
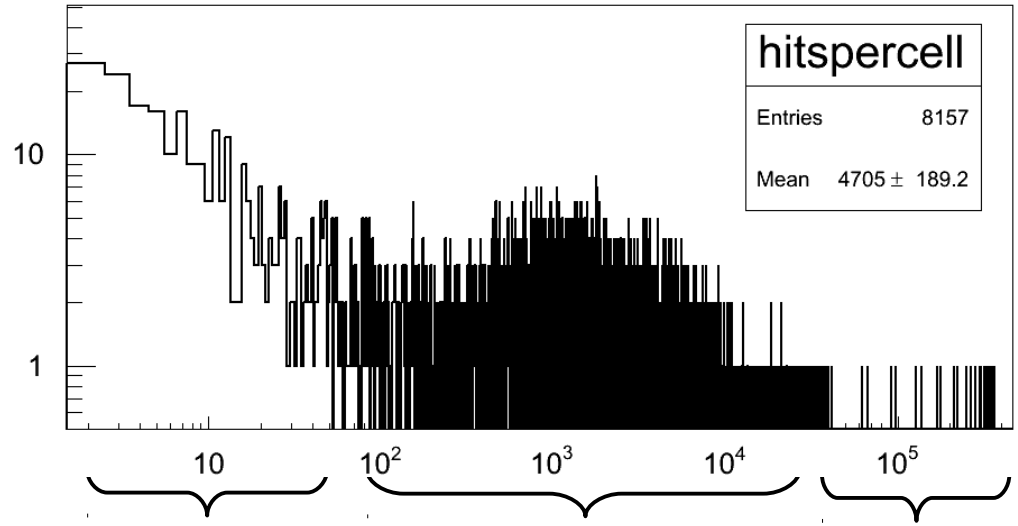
combined hit map from all runs:







1M events at different Beam positions:

- Mean: 7 hits per event
- 89% of memory cells have more than 100 hits

→ enough data for offset calibration

few hits in last memory cells

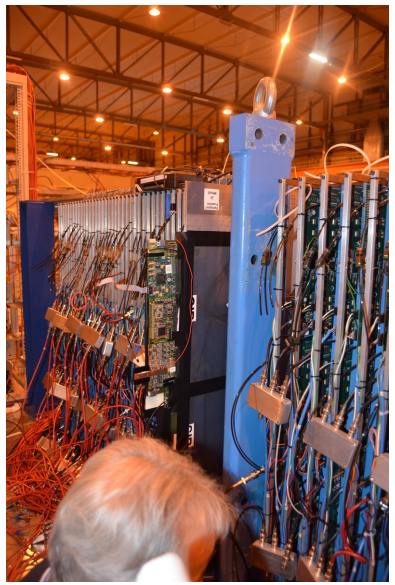
89% at least 100 hits

trigger channels

Outlook

AHCAL layer (and future prototypes)

- Detailed investigation of hadronic showers and simulations in 4D



TDC calibration of the AHCAL layer:

- Need chip wise (2) ramp correction and memory cell and channel wise offsets corrections
- Electron test beam for calibration
- Promising results for charge injection
  → electronics resolution ~2ns
- Procedure is not final
  → more effects to be taken into account