# KLauS readout ASIC
# Status and integration

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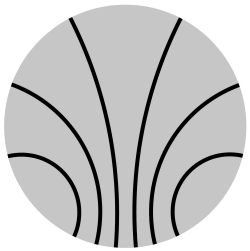
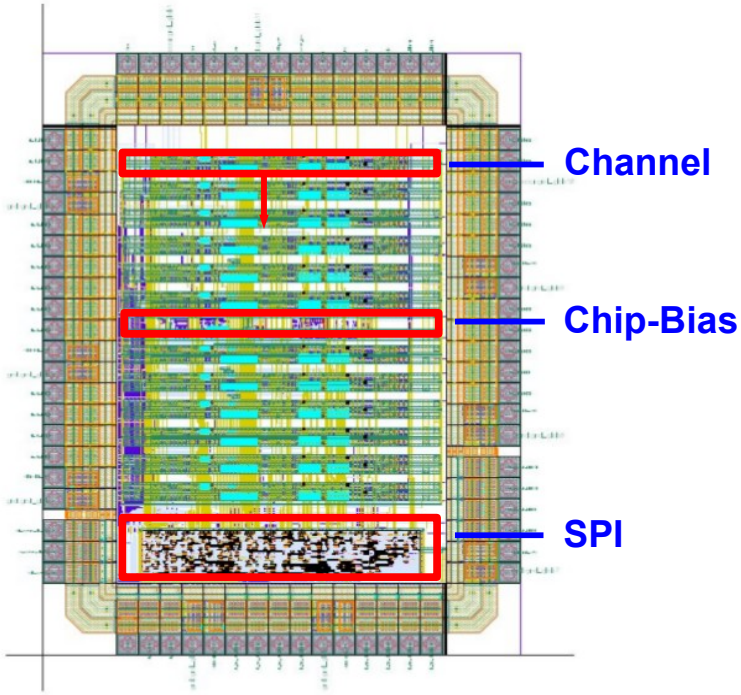


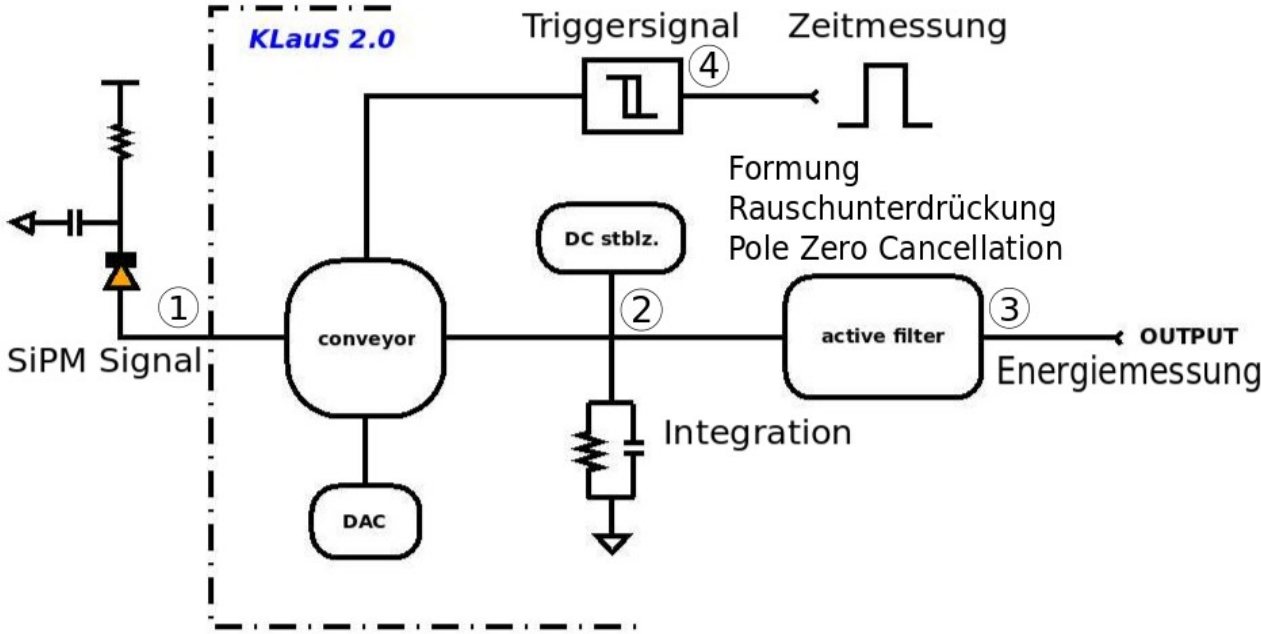

# Overview

- KlauS2 channel blocks
  - Chip characterisation Summary
  - Uniformity
- ADC & Chip integration
  - Structure
  - Basic blocks for full chip
- Conclusions



# KLauS2 – Current chip




- 12 Channels
- SiPM bias tuning with a 8bit DAC
- Trigger with low time-jtter

- Analog output for charge measurement
- SPI configuration
- Powergating Capability



# KLauS2 – Characterisation summary

**SiPM bias DAC**

- Tuning range > 2V for all channels
- Resolution 8.8 mV/LSB

**Trigger**

- Time resolution <60ps for 1MIP signal
- Charge noise ≈10fC
- Common threshold for all channels

**Charge Conversion**

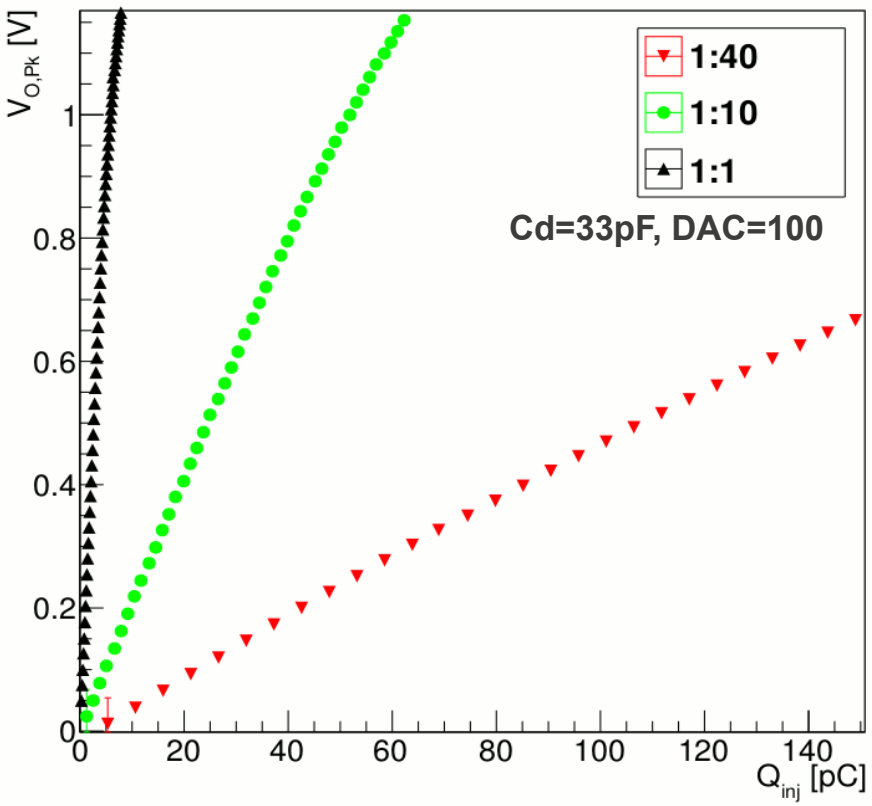
- Three signal scaling settings (1:1, 1:10, 1:40) SiPM gain Calibration and Physical events
- Linear range up to 220pC for Cd=440pF, 140pC for Cd= 33pF
- Single Pixel SNR >8 for a 50µm pitch MPPC

**Powergating**

- Power consumption decreased to ≈25µW/chan for 1% duty Cycle
- Stable spectra 100µs after switching on



# Charge measurement – signal scaling



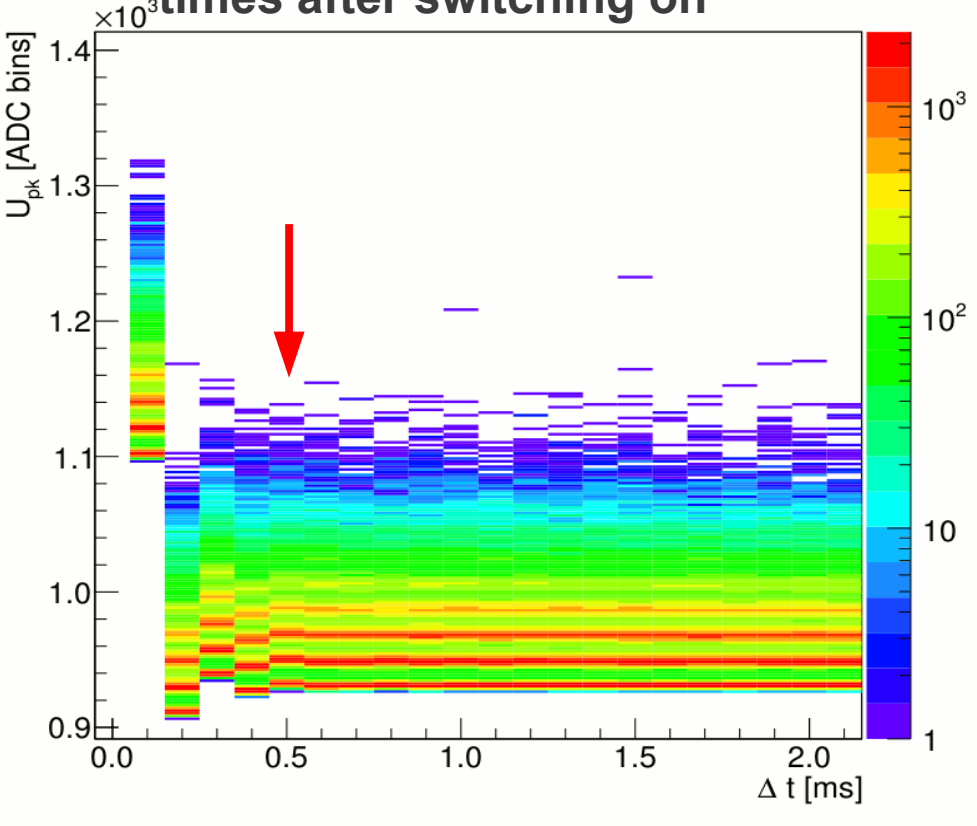

- Input signal scalable in discrete steps (1:1, 1:10,1:40)
- Dynamic range depending on detector capacitance, 220pC @ Cd = 440pF
- For Cd = 33pC

| Scaling | Conversion factor | FSR |
|---|---|---|
| 1:1 | 187 mV/pC | 4.4pC |
| 1:10 | 19.6 mV/pC | 49.2pC |
| 1:40 | 4.4 mV/pC | 138.4pC |

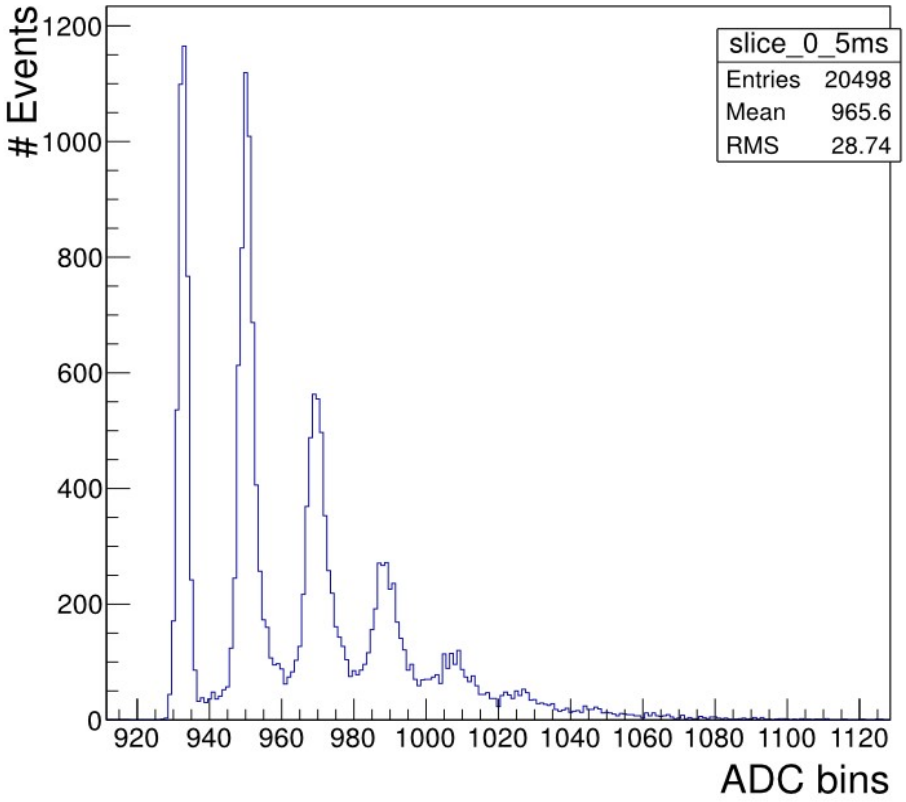


# Powergating

**Pulse height spectra for different times after switching on**



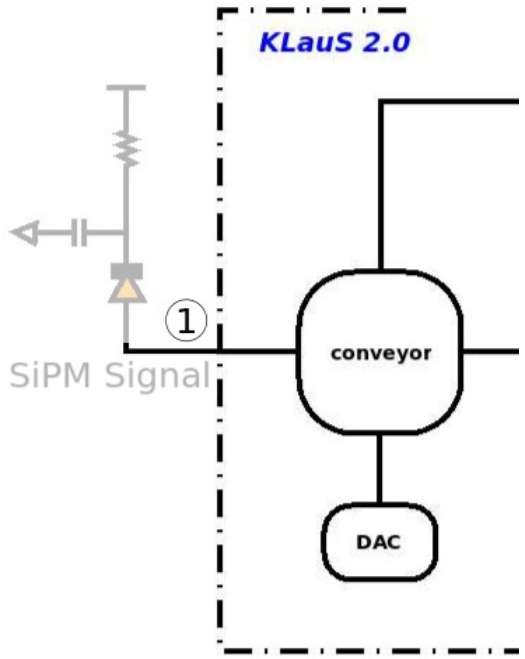

**Spectrum, 500us after clock**

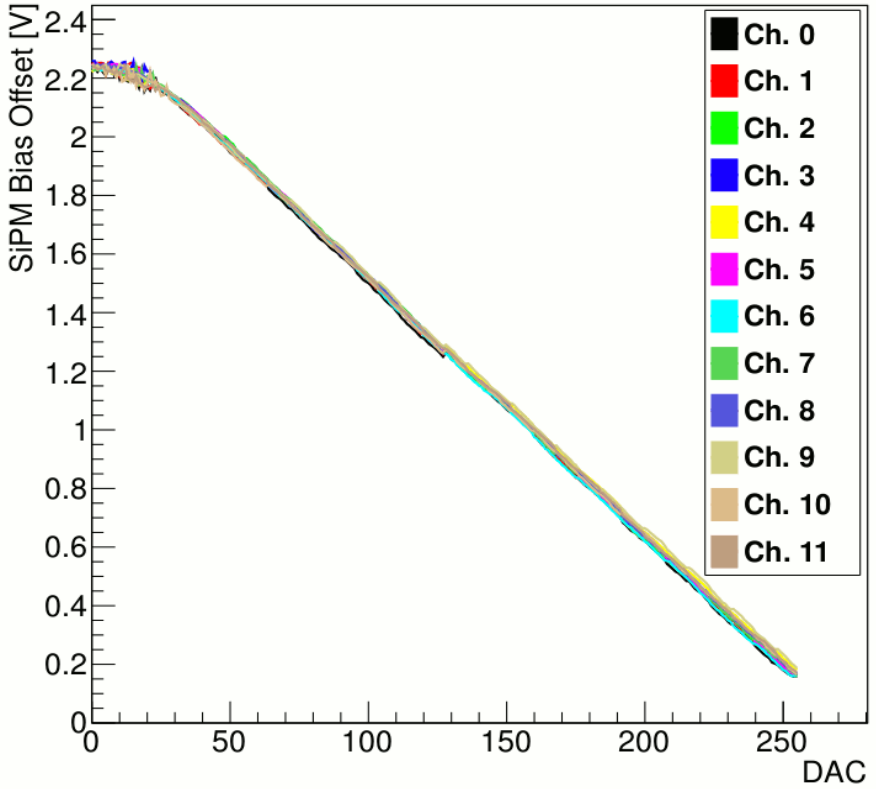



- Power consumption decreased to ≈25µW per Channel for 1% duty Cycle
- Stable spectra 100µs after switch on time
- Pedestal stabilized within 500us (time can be decreased by optimizing bias settings)



# SiPM-Bias tuning uniformity



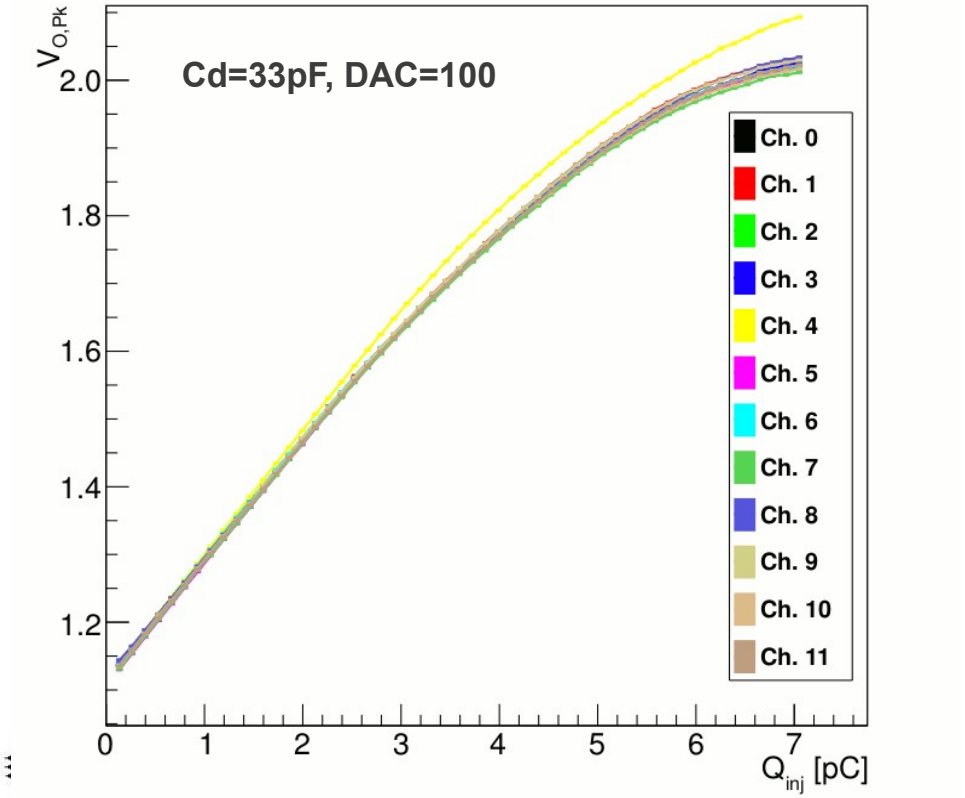



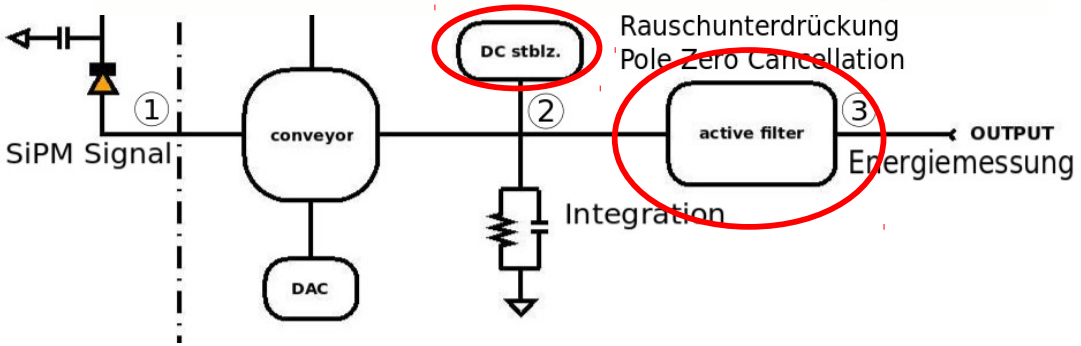

- Linear region >2V
  for Integrated nonlinearity < 2.5%
- Resolution 8.8 mV/LSB

- Spread of DAC slope from linear fit
  RMS: ≈ 64µV/LSB (0.7%)
  Peak to Peak: ≈ 2.5%



# Gain & Pedestal uniformity




**Spread of slope** in high Gain
RMS: ≈ 1.3%
Peak to Peak: ≈ 5%

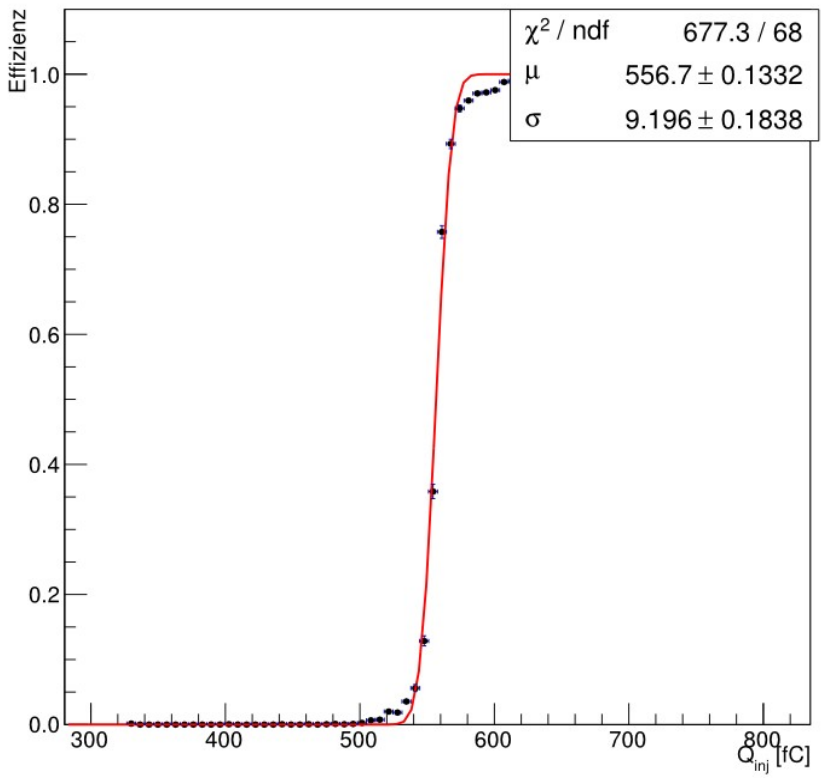
**Pedestal spread**:
RMS : ≈ 3.5mV (<> = 1.1V)

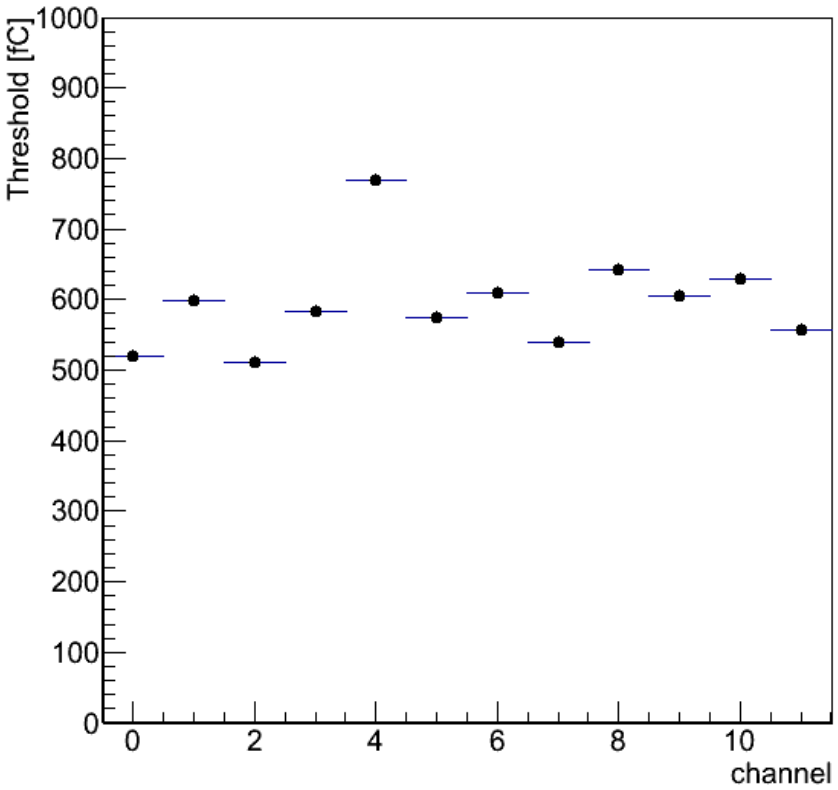
**Sources of Pedestal spread**:
Mismatch of
- Pedestal Holder Amplifier
- Shaping Stage Amplifier

**Possible solutions:**
- AC coupling for Shaper
- DAC for finetuning



# Trigger threshold uniformity




- Trigger with common threshold for all channels
- Time Jitter <60ps for MIP signals
- Charge noise ≈10fC

- Thresholds spread over chip due to mismatch
- A 4Bit DAC per channel for threshold fine tuning is sufficient to make thresholds uniform (within 10fC at ½MIP)



# ADC requirements

**3 different operation modes**

- SiPM Gain Calibration 12bit < 1mV
  - High resolution needed
- Physical Events
  - High Uncertainties 8bit 3.7mV
- Time measurements 10bit 100ps

**Requirements**

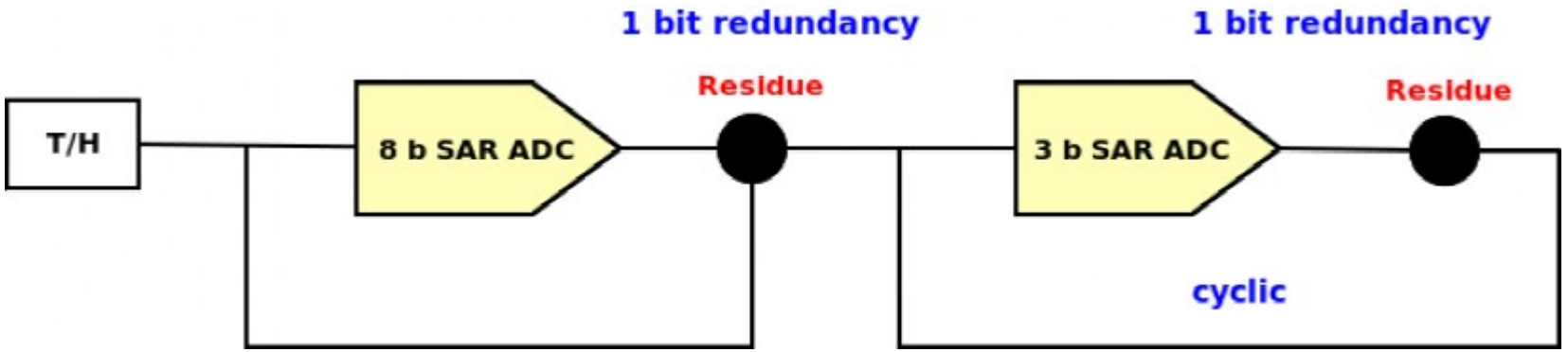
- Pipelining of the conversion, ADC for each channel
- Low area & power consumption, medium speed
- SAR ADC with up to 12bit will be used



# ADC design

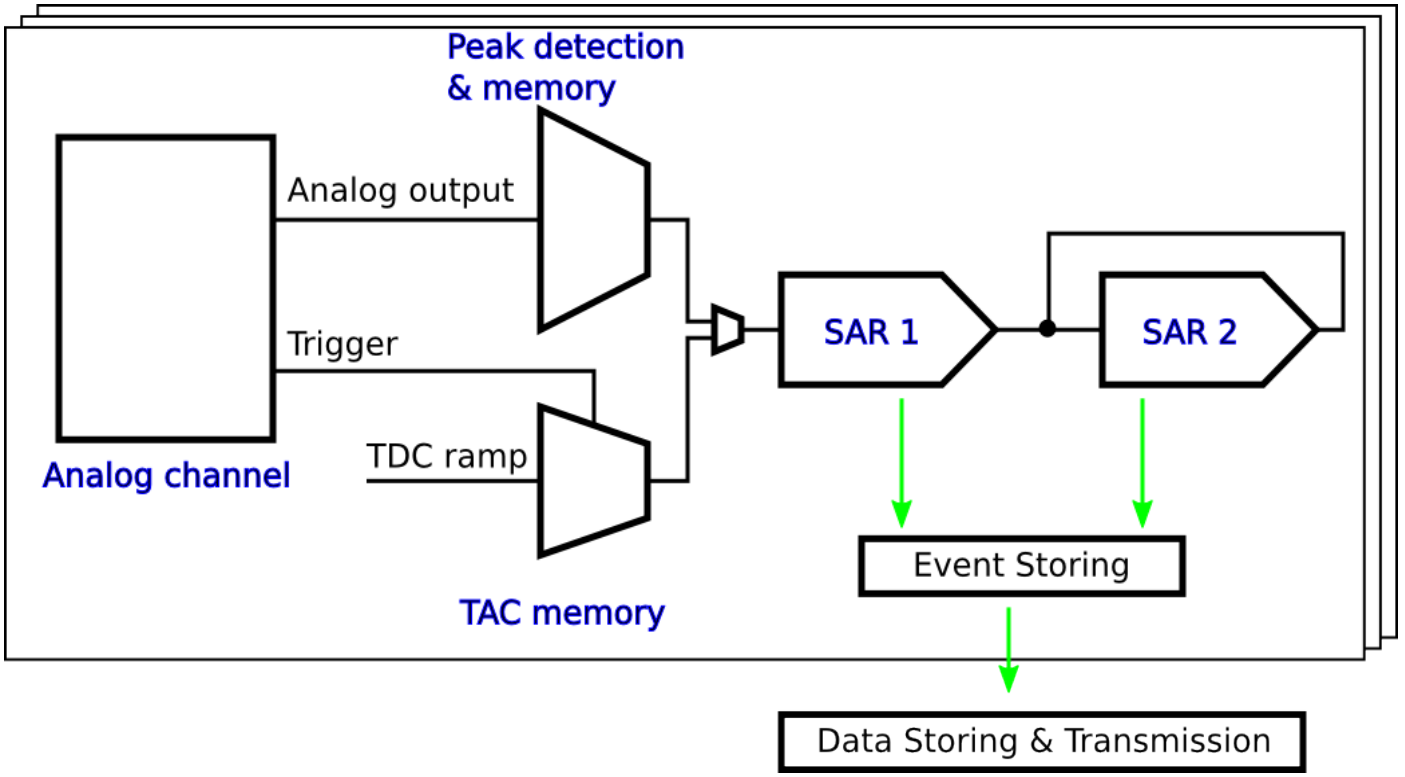
**Pipelined ADC structure chosen**

- 8bit SAR ADC for higher bits
- Second stage with a 2+1bit cyclic SAR ADC
- Pipelining of the two conversion stages with time and energy data
- Allows sampling rates of MHz for full event (T + E)
- Low storage time in analog memory cells, lower storage distortions
- One or few analog memory pairs needed






# ADC integration




Use Pipelined Structure for Time and Energy Conversion, increasing conversion speed

Compatible with different operation modes (ILC, testbeam)



# Conclusion

**KLauS2:**
- Analog Stage well understood
- Dynamic range 220pC for $C_d$ = 440pF
- SiPM bias Voltage tuneable within 2V
- Powergating tested
- Some issues found, will be corrected in following versions

**Needs for larger Chip w. ADC:**
- Trigger DAC for threshold finetuning
- Pedestal uniformity needs to be increased
- Pipelined SAR ADC structure will be used for every channel
- Small conversion time, only one pair of analog memory cells needed.

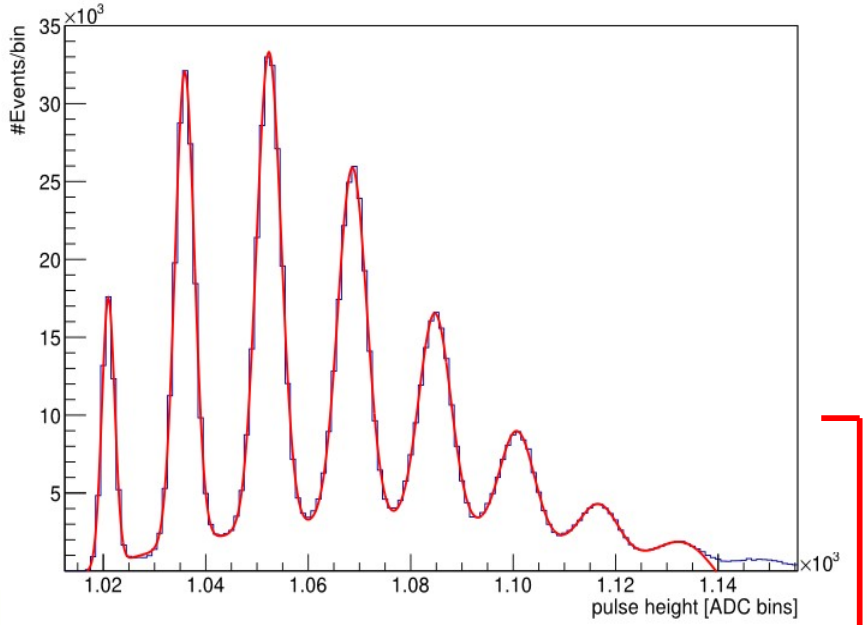
**Plan for Submission of ADC and some test blocks:**
**Autumn 2013**

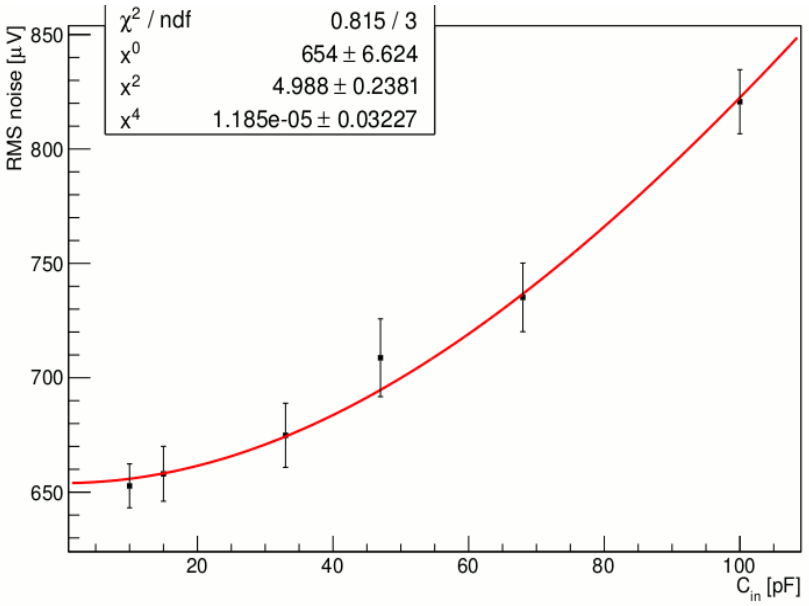


# Backup



# Noise sources for high gain mode



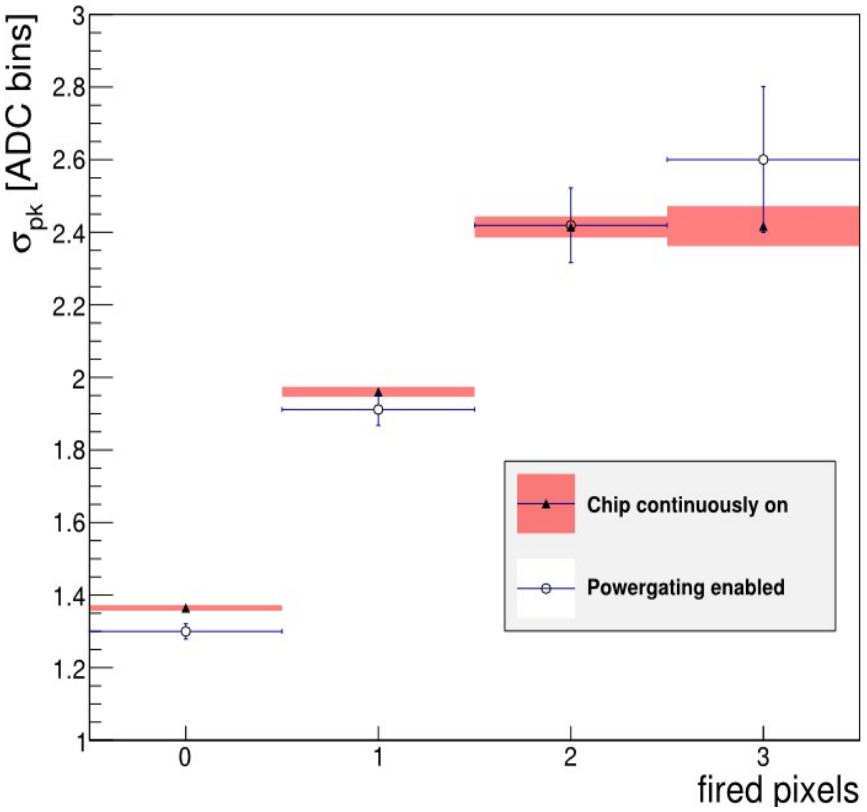




**Typical contributions to peak widths for a 1mm², 50µm-Pitch SiPM (Hamamatsu)**

| Source | Value (Abs.) | (Rel.) 1P.E. |
|---|---|---|
| SiPM-Leakage Current | 50µV | $<10^{-3}$ |
| Dark rate (Pileup) | ≈ 1mV@500kHz | ≈ 25% |
| Pixel gain uniformity | 1.04mV@ 1P.E. | 27.7% |
| Quenching fluctuations | 1.14mV@ 1P.E. | 33.3% |
| Electronic noise | 700µV@50pF | 12.5% |
| ADC (1mV/LSB) | 290µV | 2.2% |

**Signal to noise ratio for 1P.E. > 8**

# Noise using Powergating

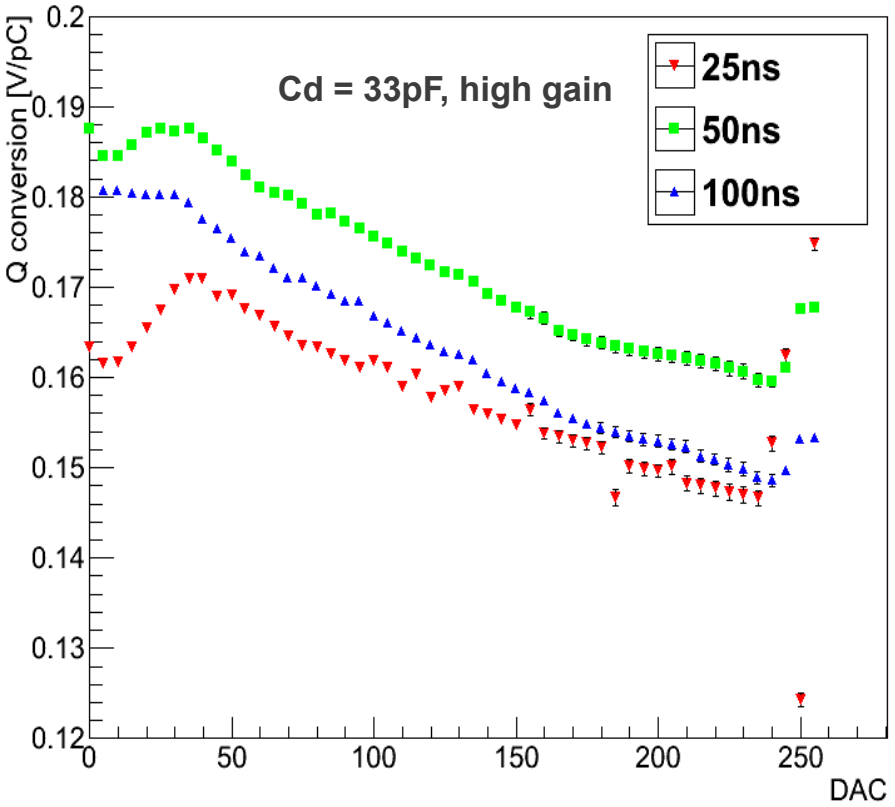



- Electronic noise decreased due to constraint on noise frequency spectrum
- Electronic noise reduced by about 20% for a charge injection measurement
- Not significant due to dominating SiPM noise sources (see slide 14)



# Charge measurement

## DAC-Dependency issue

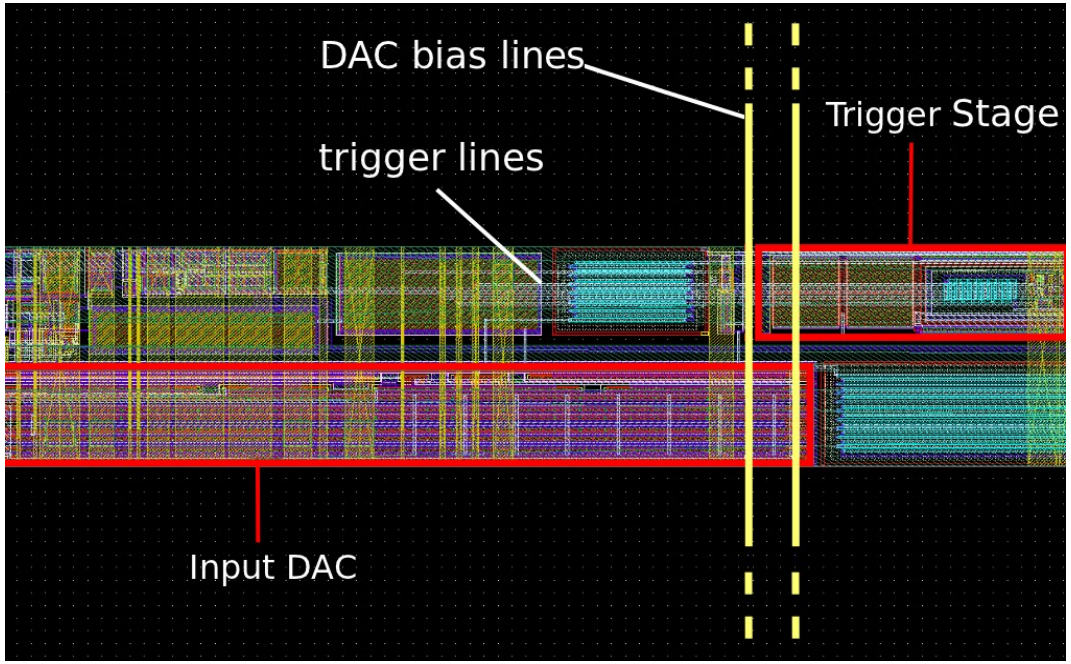


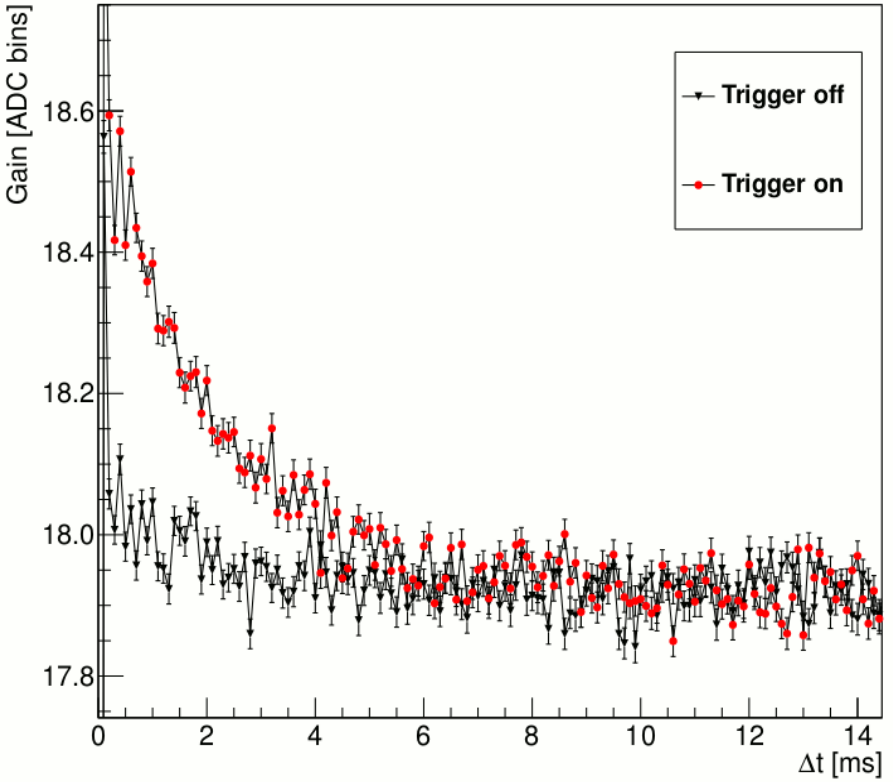

- Charge conversion is dependent on configured DAC value due to change in input impedance (“Ballistic deficit”)
- Different solutions possible, under investigation



# Powergating

## Crosstalk issue

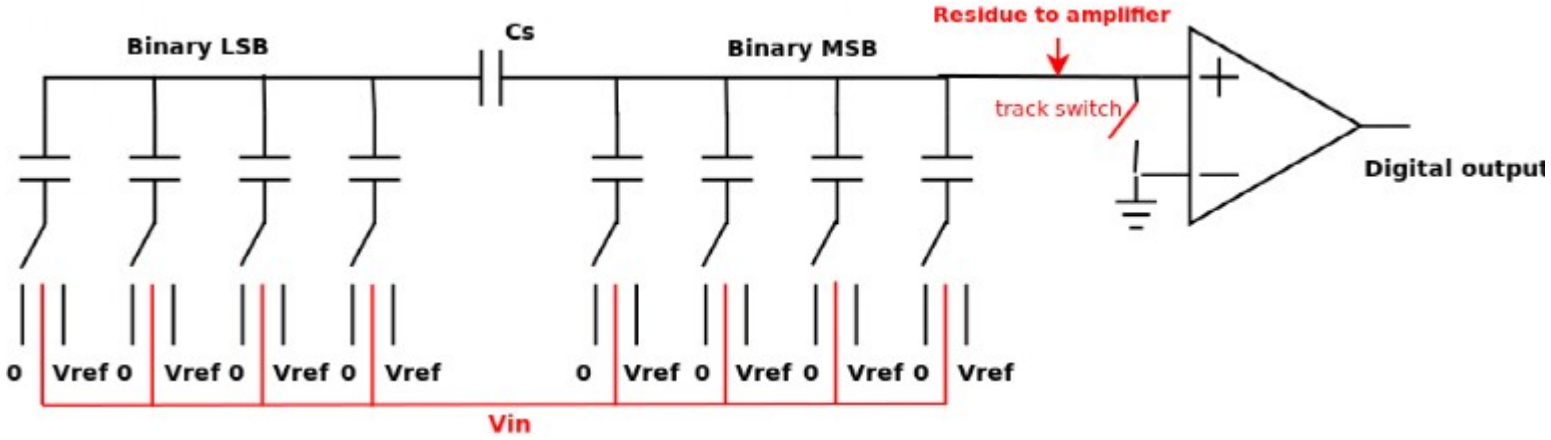



- Layout problem found for Powergating mode
- Digital clock lines cause capacitive crosstalk to the input DAC, leading to a voltage pulse at the input voltage.
- Referred increase in SiPM gain in the order of %



# ADC design details




- DNL < 0.7%, Capacitor unit size 10·10µm
- Total size approximation 32·100µm
- KT/C noise ≈200µV